CML Microcircuits

COMMUNICATION SEMICONDUCTORS

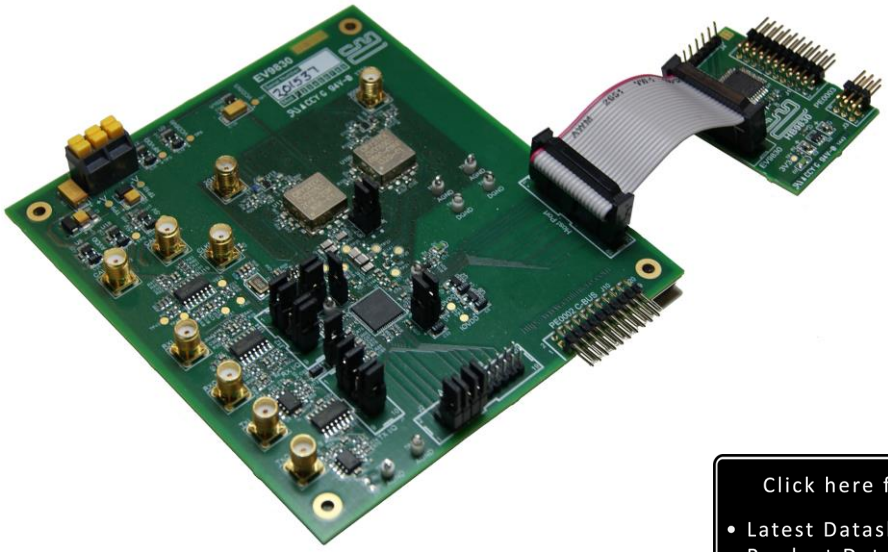
EV9830
Evaluation Kit User Manual

UM9830/3 November 2014

Advance Information

Features

- **External VCO connection option to both fractional-N synthesisers**
- **900MHz and 2.1GHz VCOs fitted**
- **Access to RF, control and baseband signals via connectors and test points**
- **On-board supply regulators operate from a dual +/-6V supply**
- **Includes HB9830 header board, allowing full PC data access and control via the PE0003 Interface Card**
- **19.2MHz oscillator or external clock input to CMX983**
- **Differential to single-ended instrumentation interfaces**
- **On-board access to all CMX983 signals, commands and data**



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1 Brief Description

The EV9830 Evaluation Kit allows evaluation of the CMX983 Baseband Interface for Digital Radio.

For evaluation of the Fractional-N synthesisers, a 900MHz VCO is fitted with connections to synthesiser1 and a 2.1GHz VCO is fitted with connections to synthesiser2. Test pads are also provided for connection to an external VCO.

An instrumentation interface with single-ended signal connections to differential baseband I/Q connections on the CMX983 is provided to allow easy connection of proprietary test equipment.

The board also incorporates all of the necessary power supply regulation facilities for operation from a dual +/-6V supply.

The 'host' header is provided with both C-BUS and fast serial port connections. When connected via the HB9830 header board to the host port of a PE0003, full data access and control is possible using the associated PC GUI software. The C-BUS is also available on a separated header for command and control only.

CONTENTS

History

Version	Changes	Date
3	Extensive update following evaluation of HB9830 header card and its incorporation into the EV9830 Evaluation Kit.	19th November 2014
2	Changes following evaluation of board and GUI updates, plus minor typographical and editorial changes.	7th May 2014
1	First Approved	1st October 2012

This is Advance Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document. Information in this advance document should not be relied upon for final product design.

It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

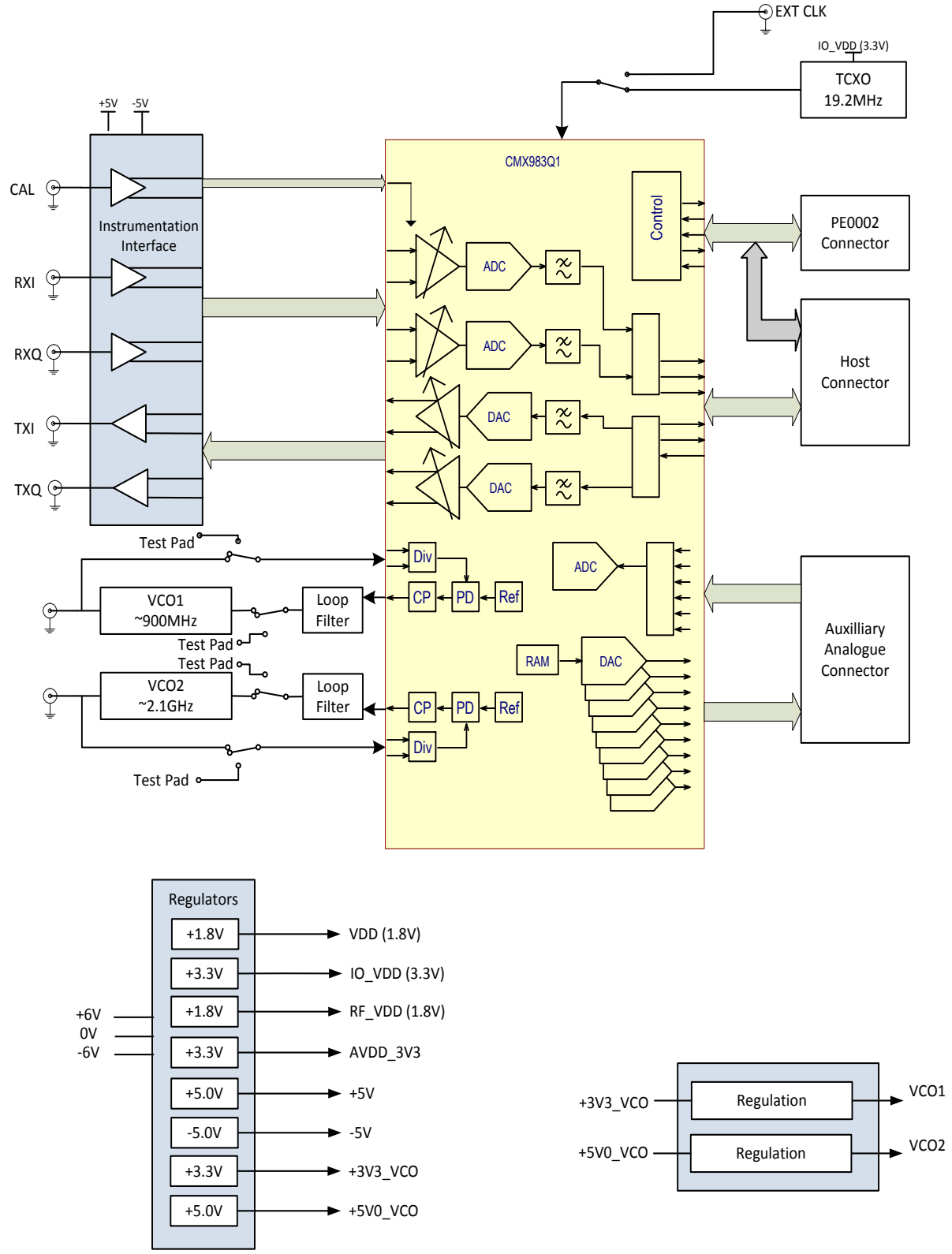


Figure 1 Block Diagram

2 Preliminary Information

2.1 Laboratory Equipment

The following laboratory equipment is needed to use this evaluation kit:

- Dual +/-6V dc power supply

If the EV9830 is being used with the PE0003 Interface Card, the following items will also be required:

IBM-compatible PC with the following requirements:

- One of the following Windows operating systems installed: XP, Vista, Windows 7 or Windows 8.
- USB port
- Minimum screen resolution 800 x 600. Recommended screen resolution 1024 x 768

USB type A male-to-mini USB type B male cable

Micro SD Card, class 10

PC application **`ES983030.exe`**, or later version, installed on the PC

2.1.1 Power Supply

The supply input voltage to the PCB is nominally +/-6V (input voltage range is 5.5 to 6.5V). On-board regulators are provided to generate all voltage rails used on the PCB (1.8V, 3.3V and +/-5V).

NOTE: When using the EV9830 with a PE0003 Interface Card, power is not supplied via the PE0003. The PE0003 must be connected directly to the +6V side of the dc power supply.

2.2 Handling Precautions

Like most evaluation kits, this product is designed for use in office and laboratory environments. The following practices will help ensure its proper operation.

2.2.1 Static Protection

This product uses low-power CMOS circuits that can be damaged by electrostatic discharge. Partially-damaged circuits can function erroneously, leading to misleading results. Observe ESD precautions at all times when handling this product.

2.2.2 Contents - Unpacking

Please ensure that you have received all of the items on the separate information sheet (EK9830) and notify CML within seven working days if the delivery is incomplete.

2.3 Approvals

This product is not approved to any EMC or other regulatory standard. Users are advised to observe local statutory requirements, which may apply to this product.

3 Quick Start

This section is divided into two sub-sections. The first is for those users who are using the EV9830 with a PE0003 controller card and its Windows PC GUI software. The second is for users who are using the EV9830 by itself, without a PE0003.

3.1 With PE0003

Check the revision and mod state of the EV9830 board. For boards up to revision D, mod 2, users are advised to change C11 to a 470nF, 0603 capacitor. This will ensure that a power on reset pulse of sufficient length for the CMX983 is generated. For correct identification of mod state (modification state) see Section 6.4.1. C11 is located just below the power indicator, D4, see below.

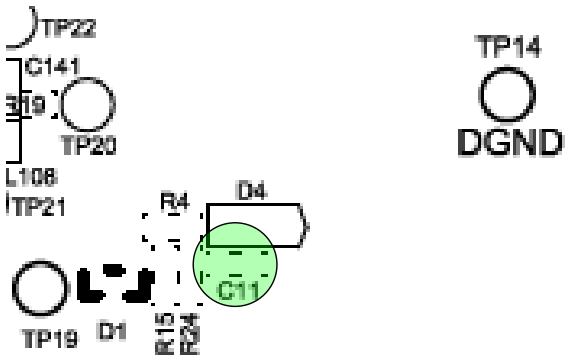


Figure 2 Location of C11

Insert the SD card into the socket on the underside of the PE0003. Connect the ribbon cable provided between connector, J4 (Host Port), of the EV9830 and connector, J2, of the HB9830. The HB9830, then plugs directly into the PE0003, with connectors, J1 and J3, of the HB9830, mating directly to connectors, J6 and J5, of the PE0003 respectively.

3.1.1 Setting-Up

The basic arrangement, when used with the PE0003, is shown in Figure 3.

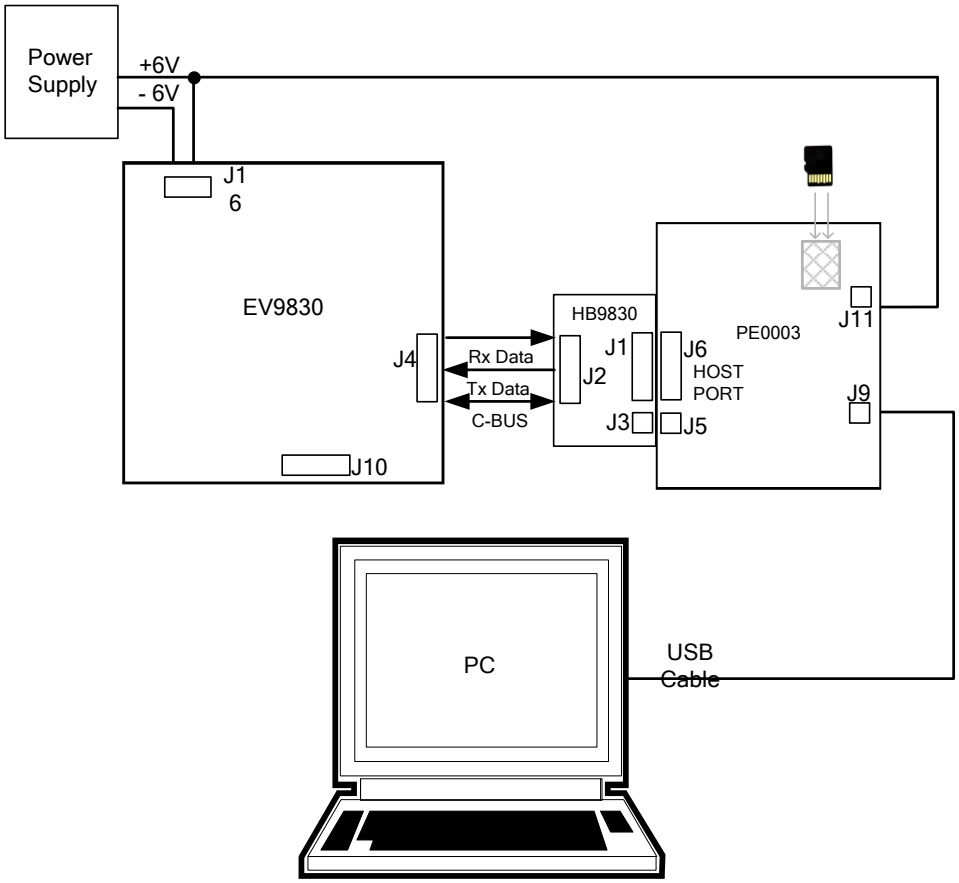


Figure 3 EV9830 used with PE0003

3.1.1.1 Software Installation

- Copy the file '**ES9830xx.zip**', which is downloaded from the CML website following registration, to the hard drive of the host PC.
- Extract the files to the hard drive of the host PC.
- Connect a +/-6V dc supply to the EV9830 and the +6V side to the PE0003
- Attach a USB cable from connector J2 of the PE0003 Interface Card to the PC USB port.
- Turn on the power supplies to both boards. The following power indicators will light:
  - EV9830; D4
  - HB9830; D2
  - PE0003; D6
- Install the USB driver when requested. Refer to the PE0003 User Manual for instructions on driver installation.

3.1.2 Operation

CMX983 device set-up, monitoring and data transfer is via the Host Port connection and can be achieved with the ES9830 GUI application.

Note: from power up, or after reset, the internal system clock of the CMX983 is disabled. From the 'C-BUS Control' tab, see Figure 7, the 'Init. Board' button **MUST** be clicked, which will issue a C-BUS general reset and configure the internal system clock to the settings entered in the 'System Clock Generator area of this tab.

3.2 Without PE0003

As an alternative to using the PE0003 Interface Kit, users may control the EV9830 with a user-supplied host controller card. C-BUS connections are made via connector J10 or connector J4 alongside the transmit and receive data ports.

4 EV9830 Signal Lists

Table 1 Signal List

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J2	1	AUXADC0	I/P	Auxiliary ADC Input 0
	2	AUXDAC0	O/P	Auxiliary DAC Output 0
	3	AUXADC1	I/P	Auxiliary ADC Input 1
	4	AUXDAC1	O/P	Auxiliary DAC Output 1
	5	AUXADC2	I/P	Auxiliary ADC Input 2
	6	AUXDAC2	O/P	Auxiliary DAC Output 2
	7	AUXADC3	I/P	Auxiliary ADC Input 3
	8	AUXDAC3	O/P	Auxiliary DAC Output 3
	9, 10	GNDA	PWR	Analogue Ground
	11	AUXADC4	I/P	Auxiliary ADC Input 4
	12	AUXDAC4	O/P	Auxiliary DAC Output 4
	13	AUXADC5	I/P	Auxiliary ADC Input 5
	14	AUXDAC5	O/P	Auxiliary DAC Output 5
	16	AUXDAC6	O/P	Auxiliary DAC Output 6
	18	AUXDAC7	I/O	Auxiliary DAC Output 7 / Auxiliary ADC Input 6
	20	AUXDAC8	I/O	Auxiliary DAC Output 8 / Auxiliary ADC Input 7
	15, 17, 19	N/C		
J4	1	IRQN	O/P	Interrupt request output. Connects to host microcontroller
	2	RDATA	O/P	C-BUS reply data. Connects to host microcontroller
	3	CDATA	I/P	C-BUS command data. Connects to host microcontroller
	4	CSN	I/P	C-BUS chip select. Connects to host microcontroller
	5	SCLK	I/P	C-BUS Clock. Connects to host microcontroller
	6	N/C		
	7, 8	GNDD	PWR	Digital ground
	9 ->12	N/C		
	13	RXCLK	O/P	Serial port receive clock

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J4 cont'd	14	TXCLK	O/P	Serial port transmit clock
	15	RXFS	O/P	Serial port receive frame sync
	16	TXFS	O/P	Serial port transmit frame sync
	17	RXD	O/P	Serial port receive data
	18	TXD	I/P	Serial port transmit data
	19, 20	GNDD	PWR	Digital ground
J5	1	CLKEXT	I/P	External master clock input.
J6	1	2100MHz	O/P	Output from 2.1GHz VCO
J7	1	ITXP_I	I/P	Transmit I channel positive, instrumentation input
	2	ITXP	O/P	Transmit I channel output positive
	3	ITXN_I	I/P	Transmit I channel negative, instrumentation input
	4	ITXN	O/P	Transmit I channel output negative
	5, 6	GNDA	PWR	Analogue ground
	7	QTXP_I	I/P	Transmit Q channel positive, instrumentation input
	8	QTXP	O/P	Transmit Q channel output positive
	9	QTXN_I	I/P	Transmit Q channel negative, instrumentation input
	10	QTXN	O/P	Transmit Q channel output negative
J8	1	TXI	O/P	Transmit I channel instrumentation output, single ended
J9	1	TXQ	O/P	Transmit Q channel instrumentation output, single ended
J10	1	RESETN	I/P	CMX983 Reset control
	2	CSN	I/P	C-BUS chip select. connects to host microcontroller

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J10 cont'd	4	CDATA	I/P	C-BUS command data. Connects to host microcontroller
	6	SCLK	I/P	C-BUS Clock. Connects to host microcontroller
	8	RDATA	O/P	C-BUS reply data. Connects to host microcontroller.
	10	IRQN	O/P	Interrupt request output. Connects to host microcontroller
	11, 12	GNDD	PWR	Digital ground
	3, 5, 7, 9, 13 to 20	N/C	-	
J11	1	CALI	I/P	Receive I channel calibration Input – single ended
J13	1	CALQ	I/P	Receive Q channel calibration input – single ended
J12	1	IRXP_I	O/P	Receive I channel positive, instrumentation output
	2	IRXP	I/P	Receive I channel input positive
	3	IRXN_I	O/P	Receive I channel negative, instrumentation output
	4	IRXN	I/P	Receive I channel input negative
	5, 6	GNDA	PWR	Analogue ground
	7	QRXN_I	O/P	Receive Q channel negative, instrumentation output
	8	QRXN	I/P	Receive Q channel input negative
	9	QRXP_I	O/P	Receive Q channel positive, instrumentation output
	10	QRXP	I/P	Receive Q channel input positive
J16	1	+V	PWR	External supply voltage, nominally +6V
	2	0V	PWR	External supply ground
	3	-V	PWR	Optional external negative supply voltage, nominally -6V

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J17	1	RXI	I/P	Single-ended input for receive I channel
J18	1	RXQ	I/P	Single-ended input for receive Q channel
J101	1	900MHz	O/P	Output from 900MHz VCO

Notes:
I/P = Input
N/C = Not connected
O/P = Output
PWR = Power supply connection
TP = Test Point

Table 2 Test Points

TEST POINTS		
Test Point Ref.	**Default Measurement**	**Description**
TP1	+1.8V	Pad – Output from on-board regulator. DC supply voltage for digital rail
TP2	+3.3V	Pad – Output from on-board regulator. DC supply voltage for digital rail
TP3	+1.8V	Pad – Output from on-board regulator. DC supply voltage for RF rail
TP4	+3.3V	Pad – Output from on-board regulator. DC supply voltage for analogue rail
TP5	+5.0V	Pad – Output from on-board regulator. Positive supply voltage for instrumentation interface, +5.0V
TP6	+5.0V	Pad – Output from on-board regulator. +5.0V supply for VCO and charge pumps
TP7	+3.3V	Pad – Output from on-board regulator. +3.3V supply for VCO and charge pumps
TP8	-5.0V	Pad – Output from on-board regulator. Negative supply voltage for instrumentation interface, -5.0V
TP9	+6V	Pad – External positive supply voltage
TP10	-6V	Pad – External negative supply voltage
TP11, TP12, TP15, TP16	0V	Loop – Analogue ground
TP13, TP14	0V	Loop – Digital ground
TP19	+3.3V	Loop – Interrupt request
TP20	-	Pad – RF1 single ended (or negative input) from external VCO
TP21	-	Pad – RF1 positive input from external VCO
TP22	-	Pad – CP1 output from charge pump 1 – input to external VCO
TP23	-	Pad – RF2 single ended (or negative input) from external VCO
TP24	-	Pad – RF2 positive input from external VCO
TP25	-	Pad – CP2 output from charge pump 2 – input to external VCO
TP26	1.65V	Loop - Buffered V_{BIAS}
TP40	-	Spare operational amplifier circuit input
TP41	-	Spare operational amplifier circuit input
TP42	0V	Spare operational amplifier circuit output
TP43	-	Spare operational amplifier circuit input
TP44	-	Spare operational amplifier circuit input
TP45	0V	Spare operational amplifier circuit output

Table 3 Jumpers

JUMPERS			
Link Ref.	**Positions**	**Default Position**	**Description**
JP1	1-2	Short	Isolates digital supply rail from the CMX983 if removed
JP6	1-2	Open	Select 5.0V dc supply for charge pump 1 if shorted
	2-3	Short	Select 3.3V dc supply for charge pump 1 if shorted
JP7	1-2	Open	Select 5.0V dc supply for charge pump 2 if shorted
	2-3	Short	Select 3.3V dc supply for charge pump 2 if shorted
JP11	1-2	Short	Isolates analogue supply rail from the test chip if removed
JP13	1-2	Short	Isolates I/O supply rail from the test chip if removed
JP14	1-2	Short	Isolates RF supply rail from the test chip if removed
J1	-	-	See Table 5 Clock Select Jumper Positions
J7	1-2	Short	Isolates Transmit I channel +ve from instrumentation interface if removed
	3-4	Short	Isolates Transmit I channel -ve from instrumentation interface if removed
	7-8	Short	Isolates Transmit Q channel +ve from instrumentation interface if removed
	9-10	Short	Isolates Transmit Q channel -ve from instrumentation interface if removed
J12	1-2	Short	Isolates Receive I channel +ve from instrumentation interface if removed
	3-4	Short	Isolates Receive I channel -ve from instrumentation interface if removed
	7-8	Short	Isolates Receive Q channel -ve from instrumentation interface if removed
	9-10	Short	Isolates Receive Q channel +ve from instrumentation interface if removed

Table 4 LEDs

LEDs	
LED Ref.	**Description**
D4	Indicates that the digital supply voltage is present.

5 Circuit Schematics and Board Layouts

For clarity, circuit schematics are available as separate high-resolution files. These can be obtained via the CML website.

5.1 EV9830

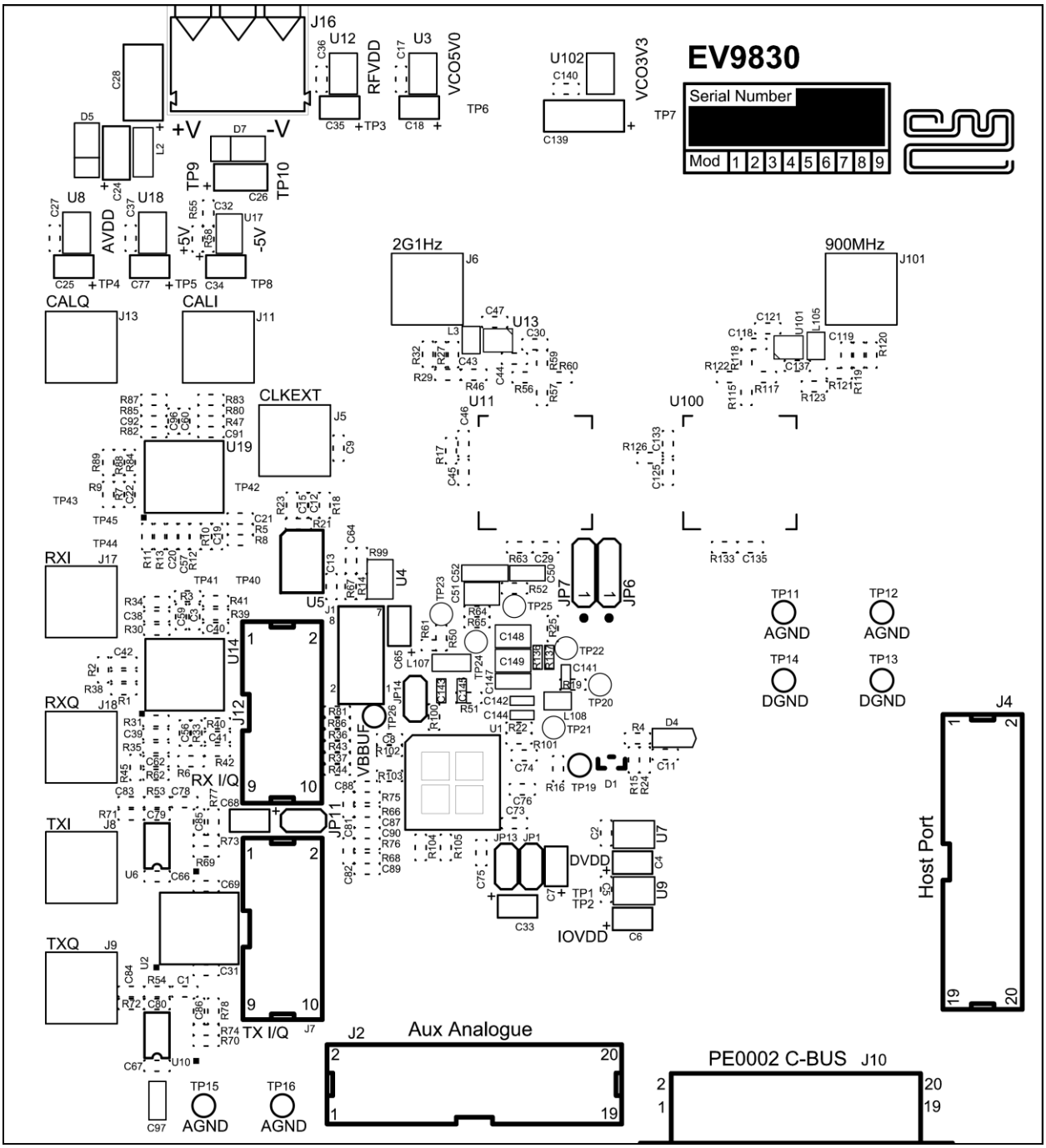


Figure 4 EV9830 PCB Layout: Top

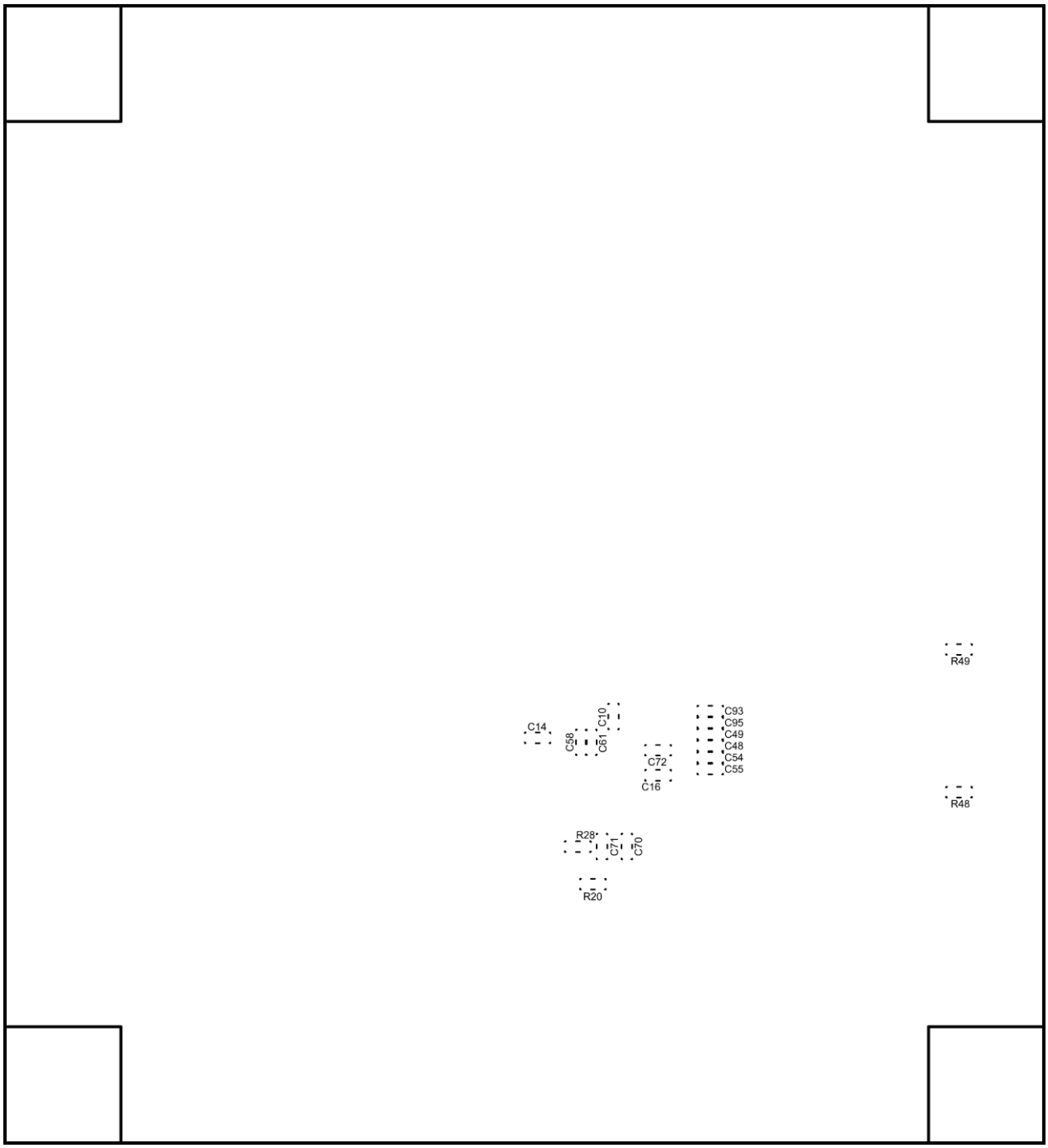


Figure 5 EV9830 PCB Layout: Bottom

5.2 HB9830

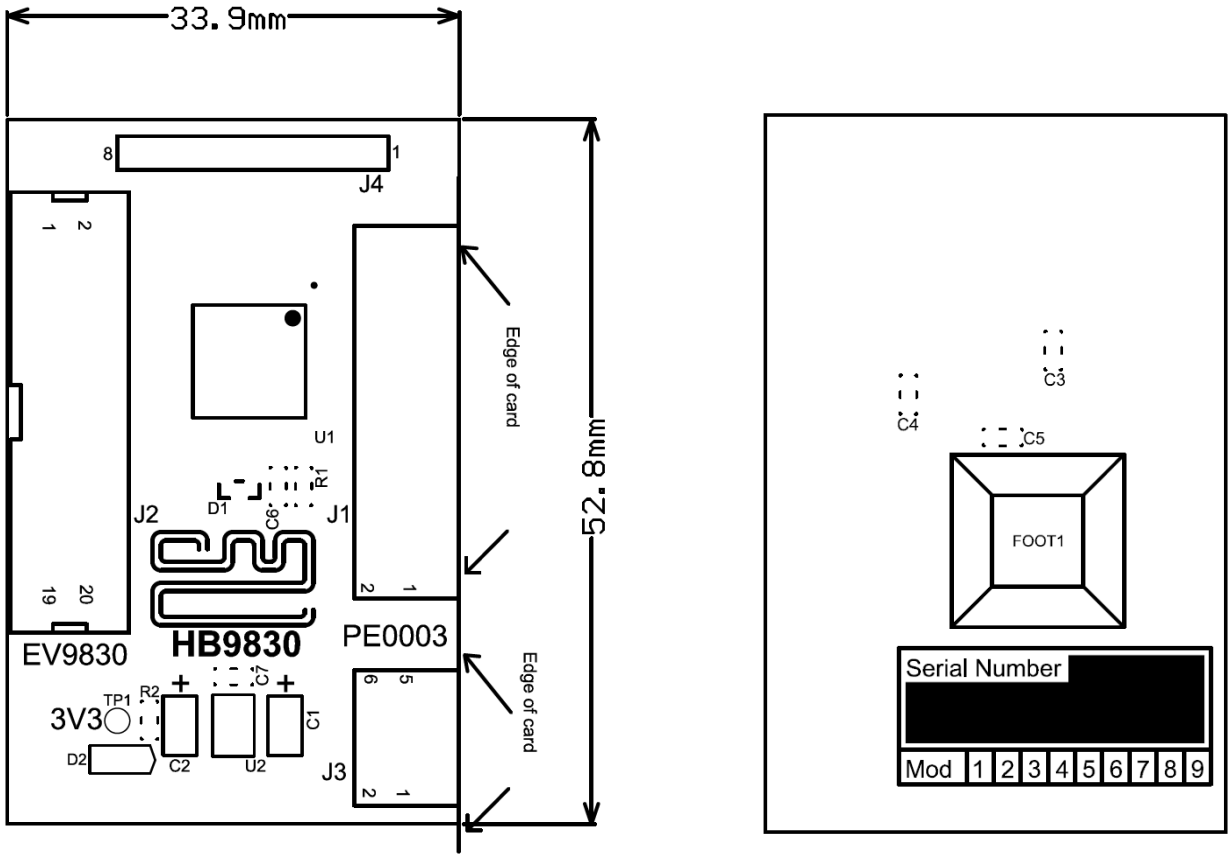


Figure 6 HB9830 PCB Layout: Top and Bottom

6 Detailed Description

The EV9830 functionality includes:

- Two phase locked loops (PLLs) with fractional-N dividers and selectable modular VCOs for each PLL. The CMX983 synthesiser frequency operation is between 100MHz and 2.1GHz.
- Additional test pads are provided for connection to an external VCO.
- Receive I and Q input channels with single-ended to differential instrumentation interface.
- Transmit I and Q output channels with differential to single-ended instrumentation interface.
- Auxiliary ADCs and DACs.
- Host Interface incorporating serial data ports for both transmit and receive channels with separate C-BUS serial interface for device configuration.
- C-BUS Interface that allows the board to be connected to a host microcontroller. Interface to a PC for initial test and customer evaluation is available separately with suitable PC software that allows control of all device functions.

6.1 Hardware Description

6.1.1 Power Supplies

All on-board power rails are derived from an external +/- 6V supply. Each power rail has a test point where it can be monitored, see Table 2.

6.1.2 RF Synthesisers

The CMX983 has two fractional-N synthesisers.

SYNTH1 can be connected to either a 900MHz VCO or an external VCO via test pads.

SYNTH2 can be connected to either a 2.1GHz VCO or an external VCO via test pads.

The charge pump supplies (VCPn) are separate for both channels and can individually be set to 3.3V dc or 5V dc.

6.1.3 Clock Options

The PCB design provides two master clock options for the test chip: A 19.2MHz TCXO module is fitted or an external clock source input at J5 may be selected. Either of these sources may be buffered before feeding to the CMX983 MCLK input. Buffering is not necessary if the CMX983 internal MCLK amplifier is enabled.

Header J1 is used with jumper sockets to select the required option as shown in Table 5:

Table 5 Clock Select Jumper Positions

Clock Option	Fit J1 jumpers on pins:
19.2MHz TCXO	1->2, 3->4
External	3->4 5->6
19.2MHz TCXO, Buffered	2->4, 7->8
External, Buffered	4->6, 7->8

6.1.4 Instrumentation Interface

An instrumentation interface has been provided to enable connection of the differential I and Q signals to laboratory equipment that has only single-ended connections. Use of this section of the EV9830 requires an additional negative supply rail, nominally –6V.

The input path has an effective gain of 6dB. The input path is configured for, nominally, 0V offset in the differential signal input to the CMX983.

There are also two spare op-amps in this section that are configured as unity-gain buffers with the input tied to analogue ground. Further component footprints are provided so that these can be reconfigured and test pads are provided for input and output.

6.1.5 Host Port

The host port, on J4, carries the C-BUS serial interface for CMX983 configuration and the transmit and receive serial ports that are the data interface for these channels. Using the HB9830 header board and ribbon cable the host port can be connected to the PE0003 interface card's host port.

6.1.5.1 HB9830

The HB9830 converts the EV9830 transmit and receive data port format to I^2S format for compatibility with the PE0003 host port.

6.1.6 C-BUS

The C-BUS is also brought out on connector J10. This is a legacy format that is compatible with the C-BUS only connections on PE0003 and its predecessor, the PE0002

6.2 PC Control Software

The EV9830 itself does not require any embedded firmware. However, it does require C-BUS control from an external microcontroller. The CML PE0003 Evaluation Kit Interface Card can be used with the EV9830, HB9830 and PC software files in '**`ES9830xx.zip`**'. To use the software, connect the EV9830, HB9830 and PE0003 as shown in Figure 3. First ensure that the drivers supplied for the PE0003 are installed correctly. The executable file must be in the same folder on the PC as the '**`EF9830xx.bin`**' file. Run the '**`ES9830xx.exe`**' and the main application window will open with a progress bar for the initialisation process. Once the initialisation process is complete, one of seven tabs can be selected.

Additional to the basic C-BUS control tab, there are:

- Four tabs that cover the major functional blocks of the CMX983
- The 'Tx/Rx Ports' tab for handling data flow from/to the receive/transmit data ports
- The CML script handler tab. Scripts can be used for additional features that are not covered in the other tabs, e.g. the auxiliary circuits of the CMX983.

To select a tab simply click on the corresponding name in the row at the top of the program window. Setting or clearing the check box associated with a bit of a register will cause that bit to be set or cleared when the register is next written to. The program can be closed at any time by clicking the 'Close' button or by pressing 'Alt' and 'F4' keys simultaneously.

The buttons 'Save State' and 'Load State' allow the user to save or load a particular control configuration for all tabs of the GUI. These buttons only save or load the configuration and do not update the CMX983 registers on the EV9830 board. After loading, the write buttons for each tab must be used to execute the new configuration. The configurations are saved with '.sta' file extension.

6.2.1 The C-BUS Control Tab

The C-BUS Control Tab allows the user to read from or write to any 8 or 16-bit register and initialise the CMX983 device on the target EV9830 board ('Init. Board'), see Figure 7. Additionally the CMX983 internal system clock settings are included as these will be used by the 'Init. Board' control.

From power up, or after reset, the internal system clock of the CMX983 is disabled. Executing an 'Init Board' from this tab will issue a C-BUS General Reset and configure the CMX983 internal system clock to the settings entered in the 'System Clock generator' area of the tab. The user must enter the MCLK frequency supplied to the CMX983 on the EV9830, which when shipped is 19.2MHz.

Every time the 'Init. Board' control is used all controls in all tabs of the GUI are reset to their default values. To retain the control settings in the other tabs, the 'Reset GUI' checkbox can be unticked. In this case, the CMX983 device is reset but the GUI Controls retain their previous values. However, to configure the CMX983 device registers to these retained values, the write buttons for each tab must be used.

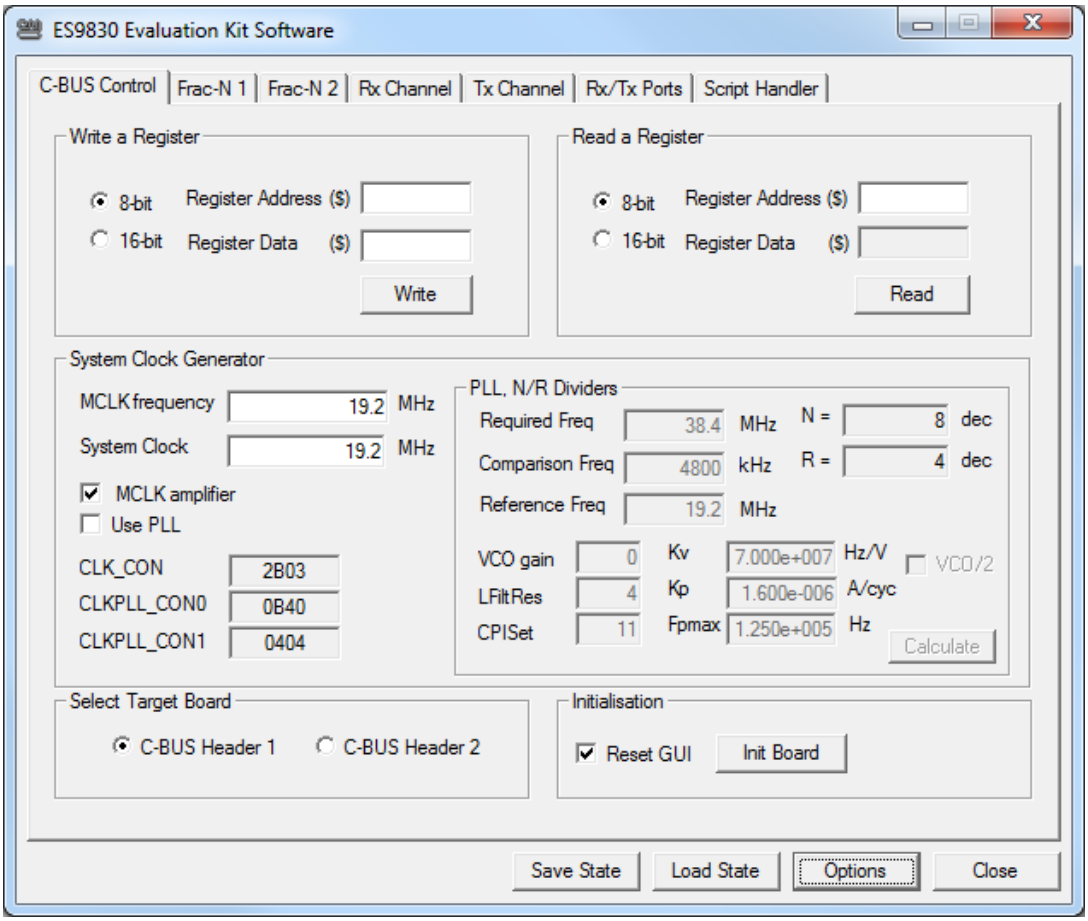


Figure 7 The C-BUS Control Tab

6.2.2 Fractional-N Synthesiser Control

There are two instances of this tab, one for each of PLL1 and PLL2. Figure 8 shows the instance for PLL1.

The device 'Registers' section is updated as a result of altering the various controls on the tab. For the 'Dividers' section, register values are only updated when the 'Calculate' button is clicked. When the 'Write Frac-N 1(2)' button is clicked, the values shown in the 'Registers' section are written to the CMX983 in the correct order, as given in the CMX983 datasheet.

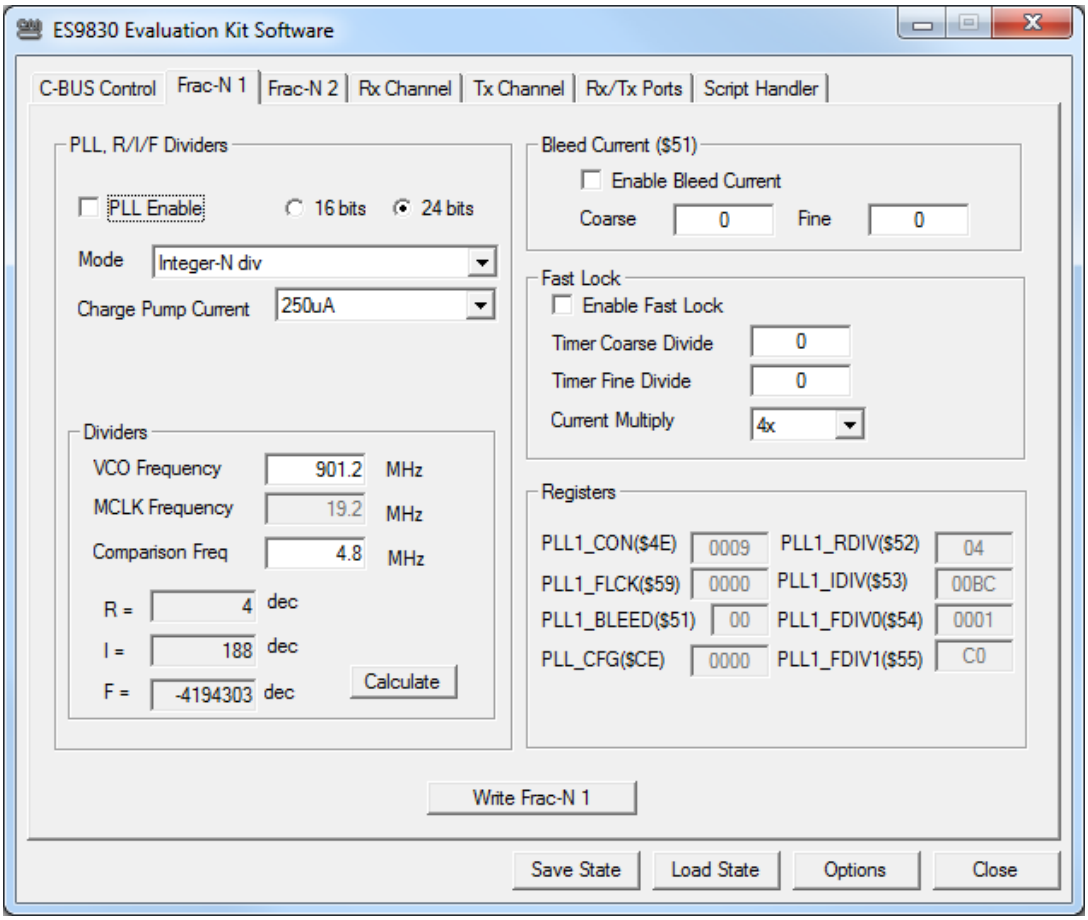


Figure 8 Fractional-N Synthesiser Control Tab

6.2.3 Receive Channel Control

The device 'Registers' section is updated as a result of altering the various controls on the tab. When the 'Write Rx' button is clicked the values shown in the 'Registers' section are written to the CMX983.

Filter coefficients may be read from files that are in the 'c' header format. Browse to the file and click 'Load' to write the coefficients to the selected coefficient bank on the CMX983. This must be done before the receive channel is enabled.

To load the filter coefficients of the selected filter in 'Coeff Bank' at the same time as the Rx registers are written, tick the 'Auto Load Filter' checkbox.

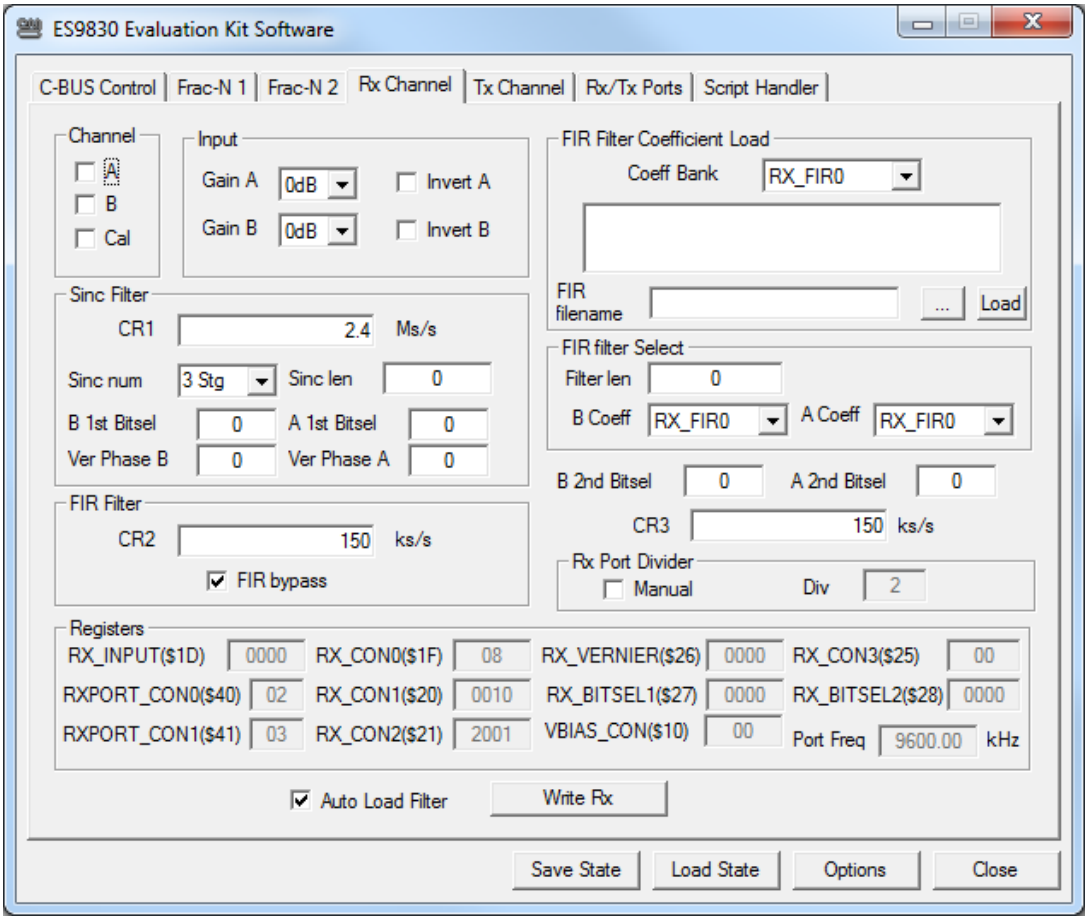


Figure 9 Receive Channel Control Tab

6.2.4 Transmit Channel Control

The device 'Registers' section is updated as a result of altering the various controls on the tab. When the 'Write Tx' button is clicked the values shown in the 'Registers' section are written to the CMX983.

Filter coefficients may be read from files that are in the 'c' header format. Browse to the file and click 'Load' to write the coefficients to the selected coefficient bank on the CMX983. This must be done before the transmit channel is enabled. CT1 and CT2 MUST be assigned before loading filter values.

To load the filter coefficients of the selected filter in 'Coeff Bank' at the same time as the Tx registers are written, tick the 'Auto Load Filter' checkbox.

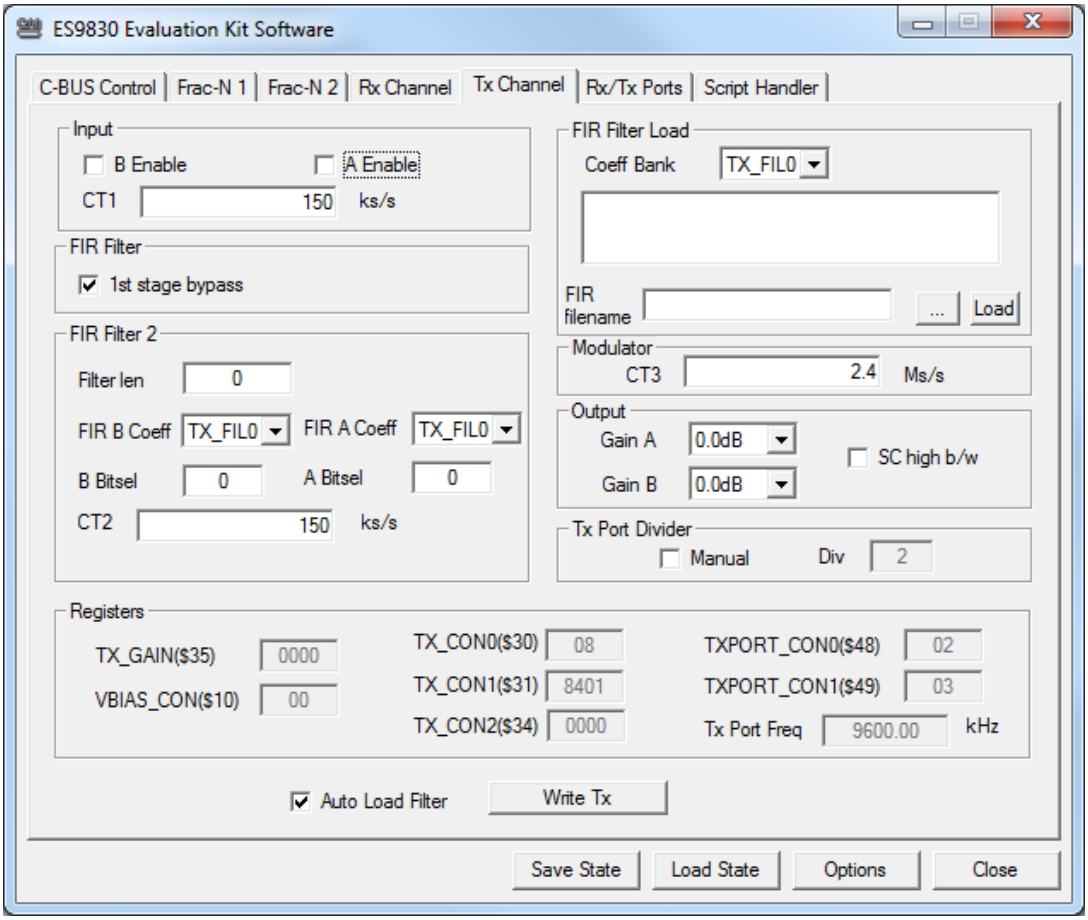


Figure 10 Transmit Channel Control Tab

6.2.5 Rx/Tx Ports Tab

The Rx/Tx Port tab allows the capture of, or writing of, samples over the receive and transmit serial ports respectively of the EV9830. To make use of this tab a micro SD card is required to be plugged into the socket on the underside of the PE0003. See Section 6.3.2 for card requirements and preparation details. If the micro SD card is not prepared, the program can still run but pre-existing data stored in the SD card might be corrupted.

The controls are divided into four operations, one for each button:

- Receive button – Receive the samples and store them into the micro SD card.
- Transmit button – Read the samples from the micro SD card and transmit them.
- Save button – Read the received samples from the micro SD card and write them to a file in the PC.
- Load button – Read a file from the PC and store the samples for transmission in the micro SD card.

The file format is a '.csv' comma delimited, with "Isample, Qsample" per line, in ASCII. The file can be processed in Excel.

In the event of a problem with the micro SD card, the GUI shows a message indicating the nature of the problem, see Section 6.4.2.

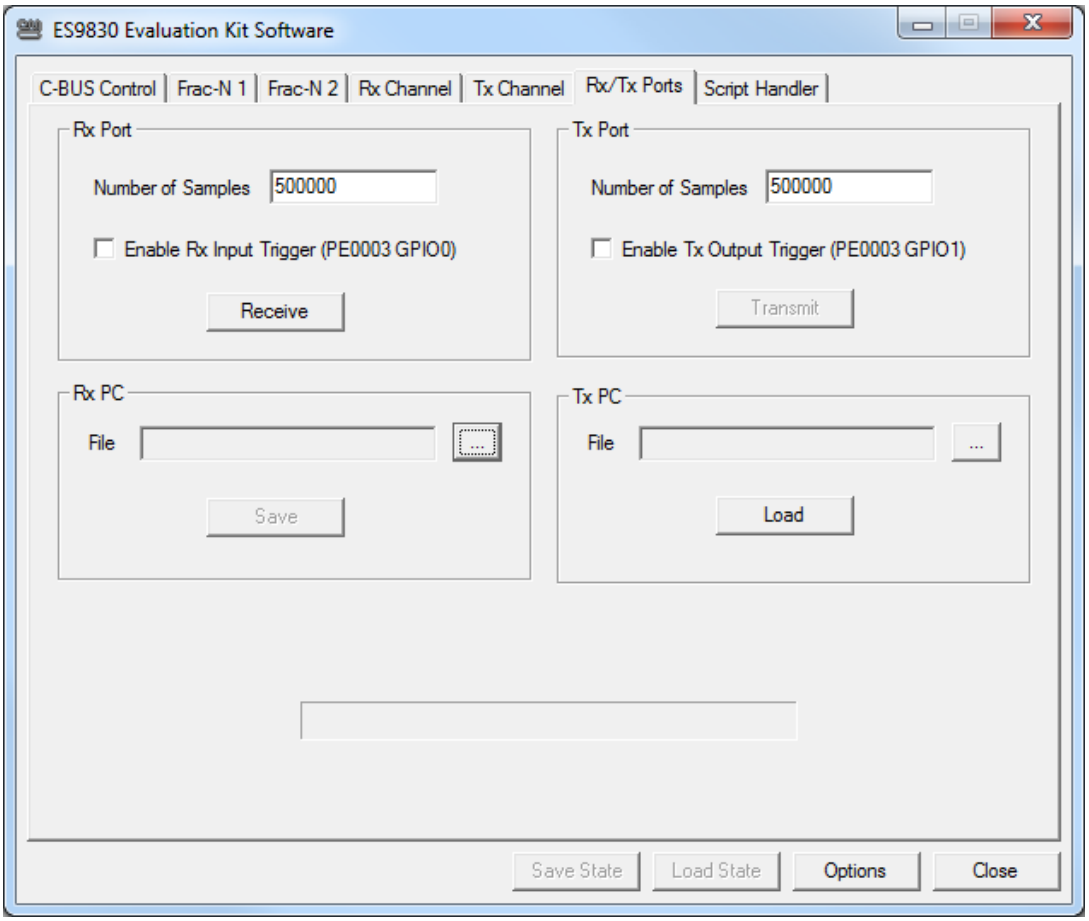


Figure 11 Rx/Tx Ports Control Tab

The optional receive input trigger and transmit output trigger signals can be found on the PE0003 as shown below:

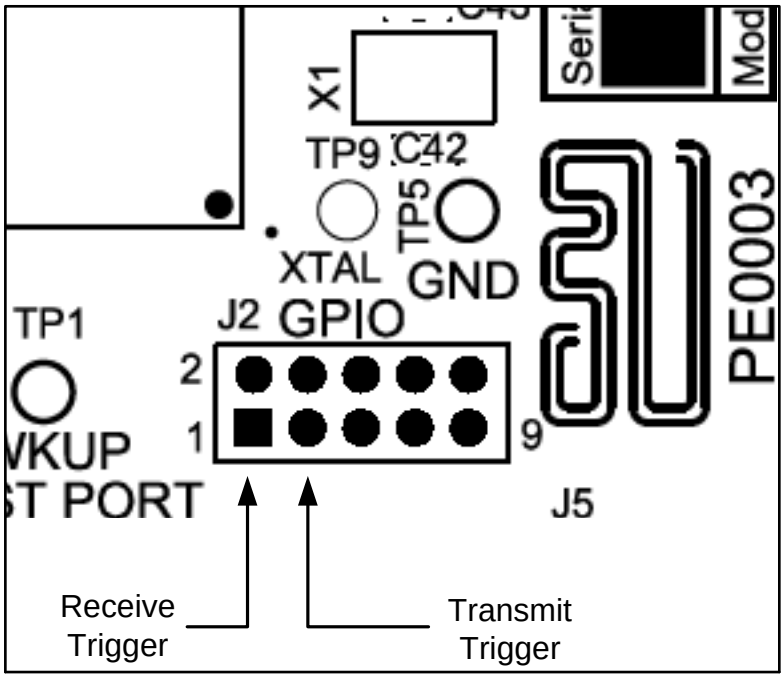


Figure 12 Receive and Transmit Trigger Locations

6.2.6 The Script Handler Tab

The Script Handler Tab (shown in Figure 13) allows the execution of script files consisting of register write, read, and delay commands. These are plain text files on the PC, which are compiled via the GUI but executed by the Microprocessor on the PE0003 board. The script language is documented separately in the “Script Language Reference” document, which can be downloaded with the PE0003 support package from the CML website. The script handler may be used for additional features that are not covered in the other tabs, e.g. the auxiliary circuits of the CMX983.

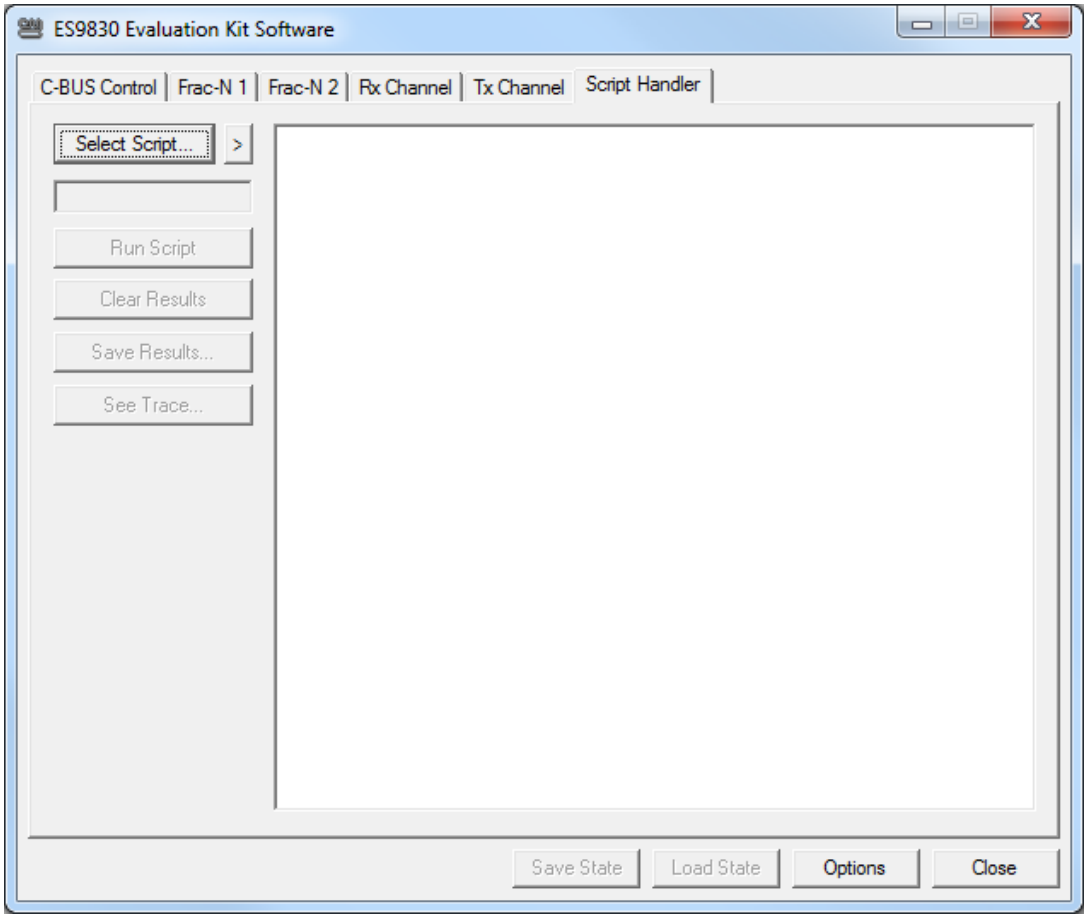


Figure 13 Script Handler Tab

To select a script file click on the 'Select Script' button. The Open File Dialog is displayed. Browse and select the script file. The folder that contains the script file will be the working folder of the script (i.e. all the files referenced in the script will be searched in this folder). Alternatively, select a script file from the recent files list. Click on the '>' button to display the list.

The results window displays the values returned by the script. These results can be saved to a text file or discarded by clicking on the 'Save Results' or 'Clear Results' buttons, respectively. When a script file is being executed the 'Run Script' button will change to the 'Abort' button, the rest of the tab will be disabled and the other tabs cannot be selected.

After a script has finished running, and when trace data is available, the 'See Trace…' button will be enabled. Up to 131072 C-BUS transactions can be logged in the PE0003 board. Click in the 'See Trace…' button to display the Trace dialog box. Note that the C-BUS transactions are only logged if the feature has been enabled in the script. See the "PE0003 Script Language Reference" document for details.

6.3 Application Information

See Section 3 for details of board setup and operation of the EV9830.

6.3.1 Filter Coefficients

If using the ES9830 GUI, filter coefficients can be loaded into the receive and transmit channels when coefficients are supplied in a ‘c’ header file format.

Example ‘c’ header file format for filter coefficients:

```
/*

FIR filter

fixed point precision: 16 bits


*/

#define FILTER_TAP_NUM 115

static int filter_taps[FILTER_TAP_NUM] = {
        138,
        -256,
        -198,
        -183,
       // Until 'FILTER_TAP_NUM' number of coefficents have been included,
       // one coefficient value per line.
        -183,
        -198,
        -256,
        138
        };
```

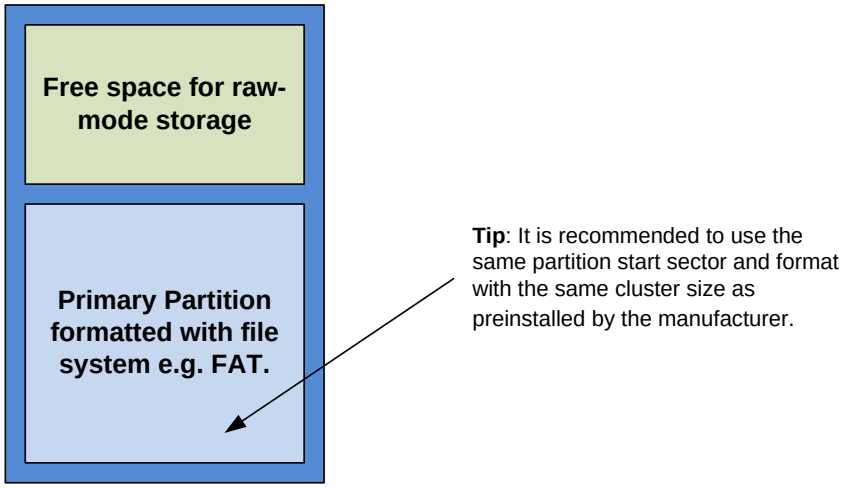
6.3.2 SD Card Preparation

Note: A class 10 micro SD card should be used.

6.3.2.1 Introduction

When using the PE0003 board to receive or transmit data in real-time the SD card is accessed directly in raw-mode. A file system cannot be used as the file storage is often non-linear and fragmented which can significantly impede reads or writes resulting in loss of data. A file system may still be required to coexist on the card for example to store Function Images. This is possible by shrinking the first partition containing the file system leaving enough space for the raw mode data storage.

Note: The SD card must have a standard master boot record (MBR) and partition table installed. The partition table is read by PE0003 and used to determine if any space exists on the card. It is usual for manufacturers to supply cards with an MBR preinstalled, however in instances where a card has been completely re-formatted it is possible for the MBR to be replaced with a FAT or NTFS boot sector. In such cases the MBR and partition table should be reinstalled which can be done using the fdisk or parted tool on Linux or the Diskpart tool on Windows.



Warning: Failure to create space for the raw-mode data storage may result in corruption of the file system and loss of data!

In order to maximise performance, SD card manufacturers often arrange the start of the first partition to be aligned with a significant boundary (4MB is typical). Also the file system allocation unit or cluster size is optimised to suit the memory architecture. The following procedure tries to ensure that these settings are maintained.

6.3.2.2 Shrink Partition Using Linux

There are many options available such as the graphical tool GParted. It is highly recommended to back up all the files on the SD card before proceeding in case something should go wrong with the resizing. The following instructions use commonly installed command line tools.

1) Backup the files on the SD card by copying them to a separate drive.
2) Open a command line interface and type **sudo fdisk –l**. Identify the disk device node for the SD card e.g. /dev/sdd.
3) Identify the file system cluster size on the first partition using fsck e.g. **sudo fsck /dev/sdd1 –vp**.

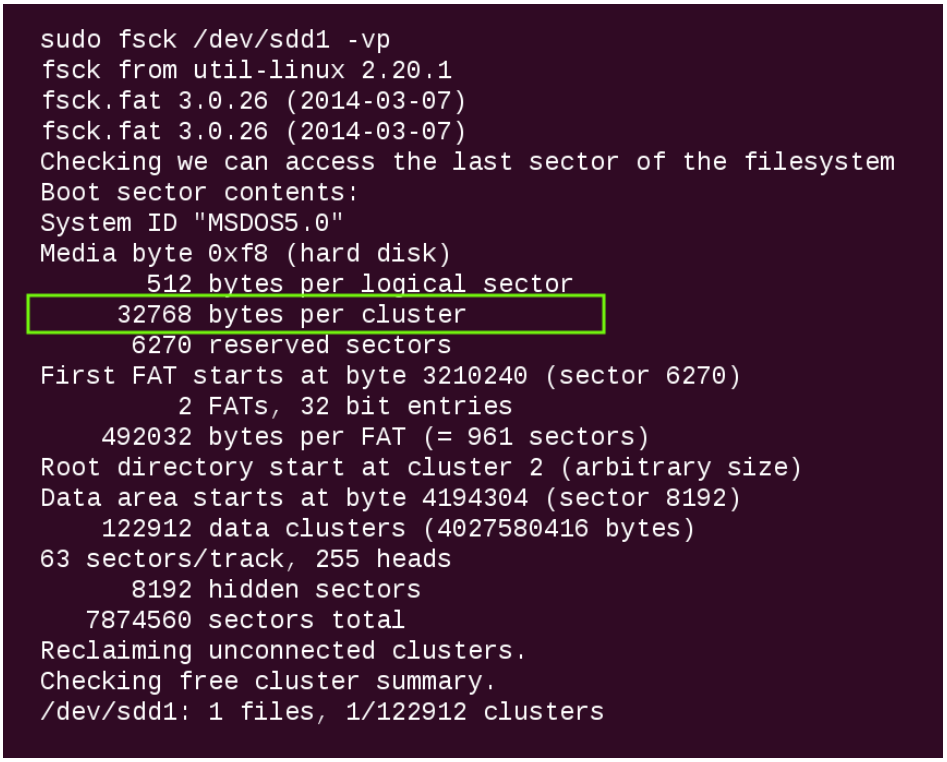


Figure 14 SD Card – Linux - fsck

4) Run the Parted tool on the disk device node identified in Figure 14**Error! Reference source not found.**, e.g. **sudo parted /dev/sdd**. Double check that the correct device is selected as the wrong one could result in loss of data.
5) Shrink the partition keeping the same start address and file system using the resize command. The following example shrinks by 500MB (Note: Parted version 2.3 was found to fail when resizing a FAT file system, if this is the case use the **resizepart** command instead and then reformat using **mkfs)**.

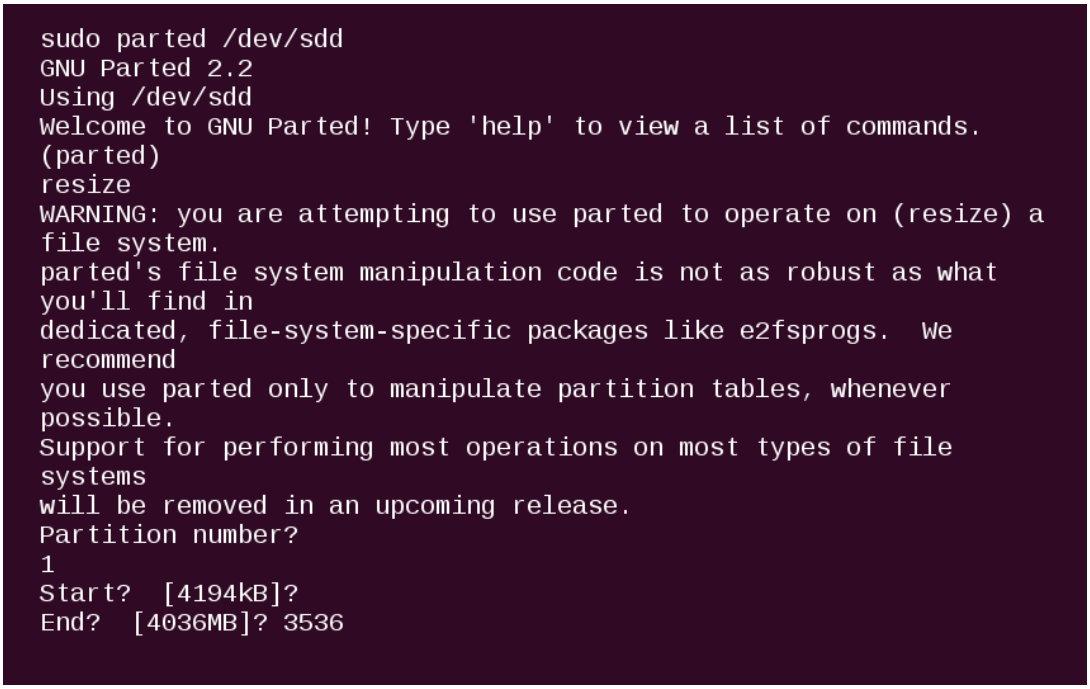


Figure 15 SD Card – Linux - parted

6) Copy the files onto the SD card from the backup.

6.3.2.3 Shrink Partition on Windows

Note: If the diskpart tool is unable to shrink the volume it is likely that the card is installed with a boot sector rather than a master boot record. In this case see section 6.3.2.3.1 for instructions on installing one.

The standard Disk Management that is preinstalled on a Windows machine does not allow shrinking of partitions on removable drives. Other third party tools are available to do this, however it is still possible to achieve the same outcome using the command line Diskpart tool as follows:

1. Backup the files on the SD card by copying them to a separate drive.
2. At a command prompt, type: diskpart.
3. List the volumes available using the **LIST VOLUME** command. Identify the volume that the SD card is mounted as. The following example shows a 4GB SD card mounted as volume E.

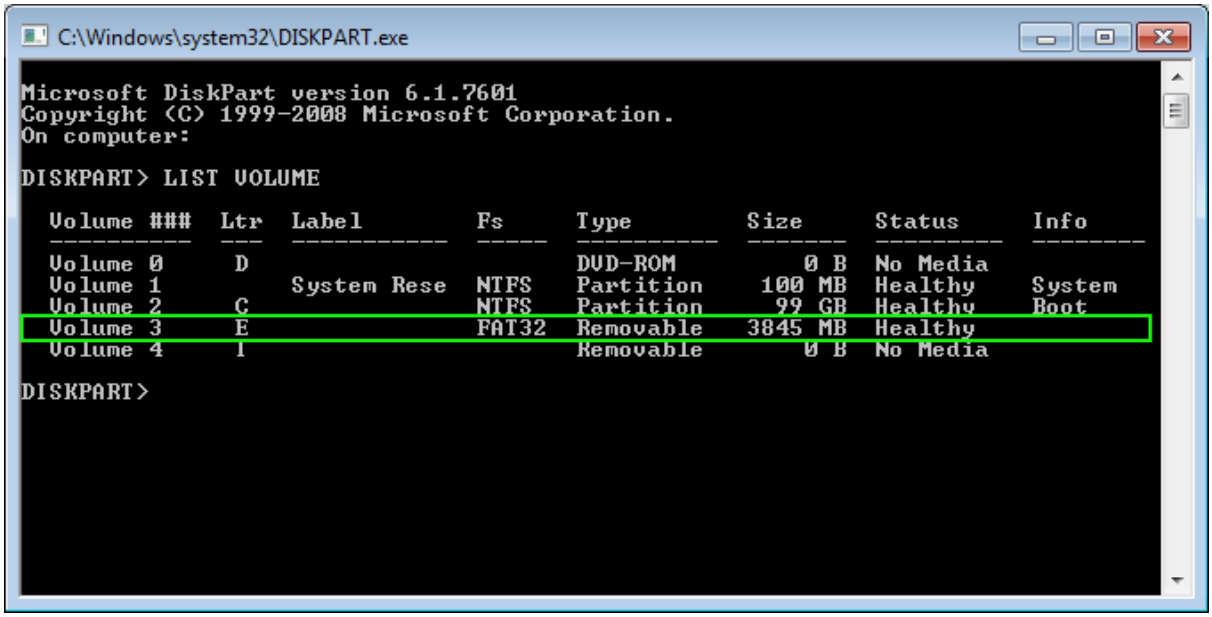


Figure 16 SD Card – Windows Diskpart - List Volumes

4. Use the **SELECT VOLUME** command to select the SD card e.g. **SELECT VOLUME E**.
5. Double check that the correct disk is selected by using the **LIST VOLUME** command again. The selected volume should have a * character in front of it. This step is very important as the wrong selection could result in corruption and data loss of other drives.

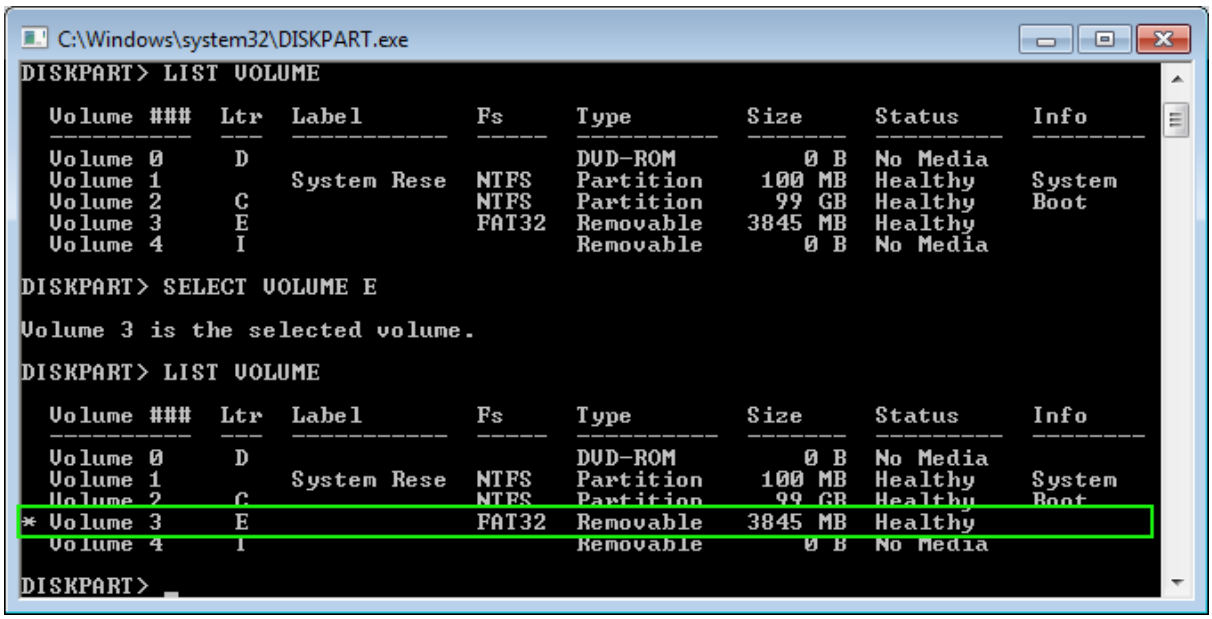


Figure 17 SD Card – Windows Diskpart - Selected Volume

6. List details about the file system using FILESYSTEM command. Make a note of the type and the allocation unit size, e.g.

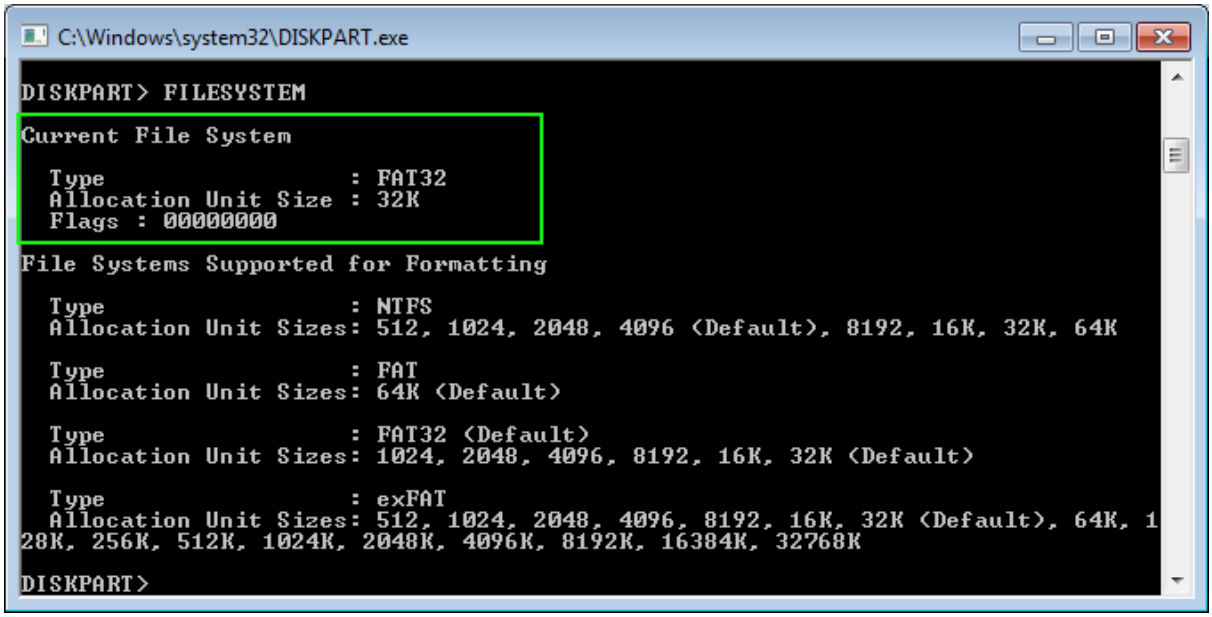


Figure 18 SD Card – Windows Diskpart - FileSystem

7. Reformat the file system to NTFS using the command **FORMAT fs=NTFS QUICK** (skip this step if the type is already NTFS). The Diskpart tool can only shrink NTFS file systems.
8. Shrink the partition by the required amount where the size is specified in Megabytes e.g. to shrink by 500MB use **SHRINK DESIRED=500**.

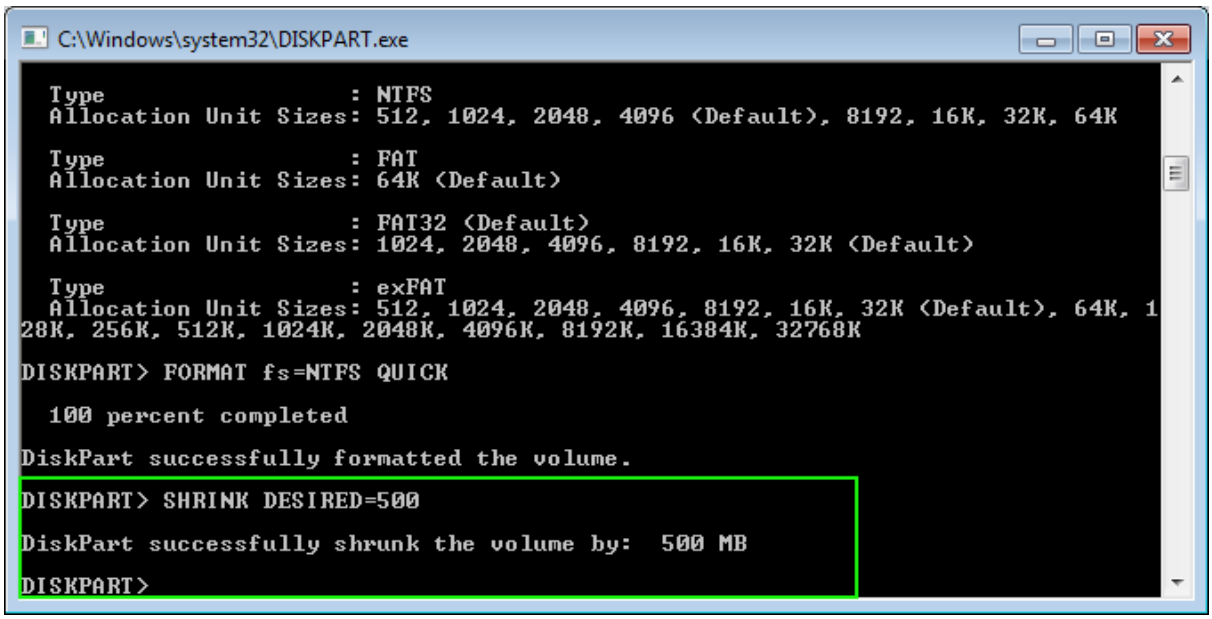


Figure 19 SD Card – Windows Diskpart - Shrink

9. Reformat to the required file system type (this is not necessary for NTFS). Use the allocation unit size as noted above e.g. to format as FAT32 with a cluster size of 32kb use **FORMAT fs=FAT32 unit=32K**.

10. Exit the diskpart tool using the **EXIT** command.
11. Copy the files onto the SD card from the backup.

6.3.2.3.1 Install a Master Boot Record and Partition Table using Windows

The following instructions show how to install a new master boot record with a shrunken primary partition and format it using the Diskpart tool.

1) Backup the files on the SD card by copying them to a separate drive.
2) At a command prompt, type: diskpart.
3) List the disks available using the **LIST DISK** command. Identify the disk number that the SD card is mounted as.
4) Having identified the disk number use the **SELECT DISK** command to select the SD card disk e.g. **SELECT DISK 3**.
5) Double check the correct disk is selected by using the **LIST DISK** command again. The selected disk should have * character in front of it. This step is very important as the wrong selection could result in corruption and data loss of other drives.
6) Use the **CLEAN** command to clear all the information off the disk (all data will be lost).
7) Create a new partition using **CREATE PARTITION PRIMARY** command.
8) Select the partition using **SELECT PARTITION 1**.
9) Shrink the partition by the required amount where the size is specified in Megabytes e.g. to shrink by 500MB use **SHRINK DESIRED=500**.
10) Format the partition as required e.g. **FORMAT fs=FAT32 unit=32k**.
11) Exit the diskpart tool using the **EXIT** command.
12) Copy the files onto the SD card from the backup.

6.4 Troubleshooting

6.4.1 Modification State

The modification state (mod state) of the EV9830 can be determined from the 'Board Mod' box printed on the PCB silkscreen. The highest number in the box that is blacked out gives the mod state. The following examples indicate a mod state of 2.

Figure 20 Examples of Mod State Identification

6.4.2 SD Card

In order to improve the performance of the micro SD card operations, the use of a filesystem is discarded. PE0003 uses non-allocated memory as storage, this unallocated memory should be after the first partition. If no such space is detected, PE0003 uses some specific micro SD card memory positions (512MB, by default). Therefore if any data is stored in these positions, they will get corrupted.

Figure 21 shows the warning that will be displayed if no unallocated memory is detected.

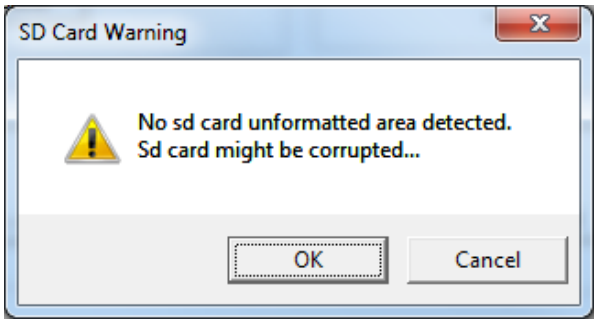


Figure 21 Warning Message for No Unallocated SD Card Memory Detected

If the SD card write cycle is too slow for the rate at which samples are read from the EV9830 board, an overrun in internal buffers will occur. In transmit, a similar underrun error will occur if the SD card read cycle is too slow. Either of these events will produce the error shown in Figure 22.

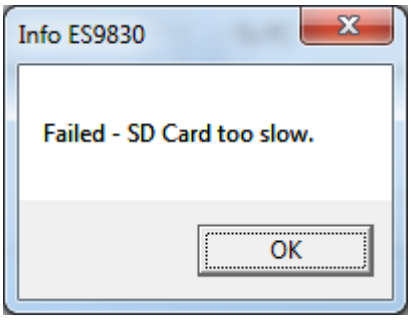


Figure 22 Error Message Informing of Speed Problems with the SD Card

7 Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the evaluation kit.

	Min.	Max.	Units
Supply (+V – 0V)	-0.3	9.0[1]	V
Supply (-V – 0V)	0.3	-9.0	V
Voltage on any connector pin (excluding supply pins) to V_{SS}	-0.3	3.6	V
Current into or out of +V and V_{SS} pins	0	+0.45	A
Current into or out of any other connector pin	-20	+20	mA

7.1.2 Operating Limits

Correct operation of the Evaluation Kit outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (+V – 0V)		5.5	6.5	V
Supply (-V – 0V)		-5.5	-6.5	V
External Clock Frequency		5.0	30	MHz

[1] If the PE0003 is used with the EV9830 then the maximum supply voltage is 6.8V.

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Evaluation device clock frequency = 19.2MHz, +V = 6.0V, -V = -6.0V, T_{AMB} = +25°C.

For CMX983 parameters, see relevant CMX983 datasheet.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD}	1, 2	-	225	-	mA
- I_{DD}	1, 2	-	70	-	mA
VDD		-	1.8	-	V
RFVDD		-	1.8	-	V
IOVDD		-	3.3	-	V
AVDD		-	3.3	-	V
+3V3-VCO		-	3.3	-	V
+5V0		-	5.0	-	V
+5V0-VCO		-	5.0	-	V
-5V0		-	-5.0	-	V
Analogue Parameters					
Input Impedances					
RXI/Q P/N	3				
RXI/Q	4	-	51	-	Ω
Output Impedances					
TXI/Q P/N	3				
TXI/Q	4	-	51	-	Ω
External Clock Input					
'High' Pulse Width	5	16	-	-	ns
'Low' Pulse Width		16	-	-	ns
Input Impedance		10	-	-	MΩ
VCO Tuning Range					
900MHz	6	875	-	960	MHz
2100MHz	6	2060	-	2125	MHz

Notes:

1. PCB current consumption, not the current consumption of the CMX983.
2. Not including any current drawn from pins by external circuitry.
3. CMX983 parameter, see relevant datasheet.
4. Small signal impedance.
5. If external buffer selected by jumpers on J1, otherwise see CMX983 datasheet.
6. Charge pump supplies set to 5.0 volts at jumpers JP6 and JP7.

7.1.4 Operating Characteristics - Timing Diagrams

Please refer to the CMX983 datasheet for details.

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