CY9D560 Series

32-bit Microcontroller Traveo™ Family

CY9D560 series has Cypress 32-bit microcontrollers for automobile motor control. They use the Arm® Cortex®-R5 MPCore™ CPU that is compatible with the Arm family.

Features

Technology

- CMOS 90 nm technology

CPU

- Arm Cortex-R5F
- 32-bit Arm architecture
- 2-instruction issuance super scalar
- 8-stage pipeline
- Armv7 / Thumb®-2 instruction set
- Floating-Point Unit (FPU)
  - Double precision
- Memory protection Unit (MPU)
  - 16 area
- ECC support for the TCM port
  - 1-bit error correction, 2-bit error detection ECC (SEC-DED)
- TCM port
  - 2 TCM ports
- ATCM port
- BTCM 2 ports (B0TCM, B1TCM)
- VIC port
  - Low latency interrupt
- AXI master interface
  - 64-bit AXI interface (instruction / data access)
  - 32-bit AXI interface (I/O access)
- AXI slave interface
  - 64-bit AXI interface (accessible to TCM port)
- CPU configuration
  - 2 CPUs (AMP operation)
- Operating frequency
  - Maximum 200 MHz
- Trace with ETM-R5

Debugging

- Arm CoreSight™ Technology
  - Each CPU embedded Embedded Trace Macro (ETM), trace support of CPU operation
- Debugging interface
  - JTAG (5 pin)
  - Support clock: maximum 20 MHz
- Debugging security support
  - 128-bit security key (Device security key)
- Wakeup function on JTAG

Operation Mode

- User mode
  - Normal mode (internal memory activation)
- Serial writer mode

Clock Control

- Internal clock source
  - Fast-CR oscillation (8 MHz)
  - Slow-CR oscillation (100 kHz)
- External oscillation input
  - Main clock input
- Embedded PLL
  - Main PLL (Multiplying clock of main oscillation)
- Oscillator stabilized timer
  - Support oscillator stabilized timer for all clock source independently
  - After a lapse of oscillator stabilized time, it is able to use source clock timer (Except PLL for FlexRay/RDC)

Reset Control

- Reset level
  - Hardware reset (system initialization)
  - Software reset (programing initialization)
- Reset factor (Hardware reset)
  - Power-on reset (PONR), external reset input (RSTX, NMIX+RSTX), clock stop waiting with time-out reset, low-voltage detection reset (internal low-voltage detection reset, 5V external low-voltage detection reset), watchdog reset (hardware watchdog reset, software watchdog reset), clock supervisor reset (main clock monitor, PLL clock monitor), software trigger hardware reset , profile error reset
- Reset factor (software reset)
  - Software reset

Low Power Consumption Control

- Device state
  - RUN (Run State, CPU is operation status)
  - PSS (Power Saving State, CPU wait event from WFI)
- Setting parameter of each devise state
  - Clock (clock source enable, clock source selection, clock divider, clock domain enable)
  - Clock monitor
  - Low-voltage detection

Memory Protection Unit (MPU)

- Memory protection as master except processor
- Target master
  - DMA controller
- 8 area
- NMI generation when violation detection

Timing Protection Unit (TPU)

- TPU 1 unit as CPU 1 unit
- 24-bit timer x 8 channels per unit
- Support execution time protection, locking time protection, inter-arrival time protection, deadline protection
- Support normal mode and over flow mode
- Prescaler of each channel
  - Timer clock divider (1/1 to 1/64)
- Independent prescaler of each channel
  - Timer clock divider (1/1, 1/2, 1/4, 1/16)

Clock Supervisor (CSV)

- Monitor target clock
  - Main oscillation input, main PLL output
- Monitor method
  - Monitor of frequency range
- Operation after error detection
  - Reset or NMI

Watchdog Timer (WDT)

- Watchdog timer embedded
  - Hardware watchdog timer
  - Software watchdog timer
- Hardware watchdog timer
  - 1 unit per system
  - 32-bit watchdog timer with window function
  - Clock source: fast-CR or slow-CR
  - Set by boot program (BootROM maker)
  - Not set by user program
- Software watchdog timer
  - 1 unit per CPU
  - 32-bit watchdog timer with window function
  - Clock source: fast-CR, slow-CR, main clock
  - One time set on user program (not set again)

Low-voltage Detection (LVD)

- Select voltage monitor
  - External low-voltage detection (5 V power line monitor): 3.9 V, 4.1 V, 4.3 V
  - Internal low-voltage detection (1.2 V power line monitor): 0.9 V
- Internal low-voltage detection: always valid
- External low-voltage detection: valid/invalid set
- External low-voltage detection: set threshold voltage independently on RUN / PSS
- Output when low-voltage detection
  - External low-voltage detection: reset or NMI
  - Internal low-voltage detection: reset

Main Flash Memory (TCFLASH)

- Cortex-R5F ATCM connection
  - 1 Main Flash memory as CPU 1 unit
- HPM connection with 64-bit AXI
- Flash memory configuration
  - Interleave with 64-bit Flash 2 units
- 2 address areas
  - TCM (read only)
  - AXI (read / write)
- ECC support (SEC-DED)
- Parallel programming support
- Flash security

Work Flash Memory (WorkFLASH)

- 2 Work Flash memories
  - 1 Work Flash memory as CPU 1 unit
- ECC support (SEC-DED)
- Parallel programming support
- Flash security

Main SRAM (TCRAM)

- BTCM connection of Cortex-R5F
  - 1 main SRAM as CPU 1 unit
  - Interleave with 2 ports of B0TCM and B1TCM
- ECC support (SEC-DED)

BootROM

- Size: 16K byte
- Boot operation support
- Serial writer program support

DMA Controller (DMAC)

- 16 channels
- Transfer mode
  - Block transfer, Burst transfer
- Addressing mode
  - Fixed, increment
- Priority between channels
  - Fixed, Dynamic, Round robin

Interrupt Control (IRC)

- Support normal interrupt (IRQ) and non-maskable interrupt (NMI)
- Normal interrupt (IRQ)
  - Use Interrupt Request (IRQ) of Cortex-R5F
  - 512 channels
  - 32 level for priority
- Support low latency interrupt response from VIC port of Cortex-R5F
- Non-maskable interrupt (NMI)
  - Use fast interrupt request (FIQ) of Cortex-R5F
  - 32 channels
  - 16 level for priority
- Support software interrupt generation

External Interrupt (EXT-IRQ)

- Input
  - Normal interrupt (IRQ): 8 input
  - Non-maskable interrupt (NMI): 1 input
- Detection method
  - H level, L level, rise edge, fall edge, both edge

Inter-processor Communications Unit (IPCU)

- Mailbox function
  - Data communication for CPU core communication by 8 Mailbox
  - Support of interrupt between CPU core

Exclusion Access Memory (EAM)

- Small size memory to support exclusion control on exclusion access instruction
- Use for semaphore
- Size: 48 byte

Bit-band Unit (BBU)

- The bit operation of specified register bit on Bit band area, it is mapping 1 bit of bit band area to support bit band alias area for 1 byte. The target of bit band access is specified register bit on I/O area

CRC

- Output to register of CRC code according real time writing to input register

Base Timer

- 16-bit timer
  - Any of four PWM/PPG/reload/PWC timer functions can be selected and used.
  - A 32-bit timer can be used in 2 channels of cascade mode as reload/PWC timer.

16-bit Free-run Timer (FRT)

- 16 bit up/down counter (2 channels for motor control only)

32-bit free-run timer

- 32 bit up/down counter

16-bit Input Capture (ICU)

- Input capture
  - 16-bit capture register that detects rise edge, Fall edge, both edge
  - Generate interrupt request after latch of counter number of 16 bit
  - Free-run timer with edge detection of pin input

32-bit Input Capture

- Input capture
  - 32-bit capture register that detects rise edge, fall edge, both edge
  - Generate interrupt request after latch of counter number of 32 bit
  - Free-run timer with edge detection of pin input
- LIN sync break/sync field relation is following.
  - Input capture ch.0 → Multi-function serial interface ch.0
  - Input capture ch.1 → Multi-function serial interface ch.1
  - Input capture ch.2 → Multi-function serial interface ch.2
  - Input capture ch.3 → Multi-function serial interface ch.3
  - Input capture ch.4 → Multi-function serial interface ch.4

16-bit output compare (OCU)

- Output interrupt signal when compare with 16-bit free-run timer

Waveform Generator (WFG)

- Generate variable output
  - Real time output
  - 16-bit PPG waveform output
  - PPG uses 16-bit PPG timer of base timer
  - The relation is following
  - WFG(ch.0 to ch.5)
    - Base timer ch.0 → PPG0
    - Base timer ch.2 → PPG2
    - Base timer ch.4 → PPG4
  - WFG(ch.6 to ch.11)
    - Base timer ch.6 → PPG6
    - Base timer ch.8 → PPG8
    - Base timer ch.10 → PPG10
  - Non overlap three-phase waveform output (inverter control)
  - DC chopper waveform output
- Dead time timer function
- GATE function
- DTTI function

A/D Converter (ADC)

- 12-bit resolution A/D converter: 1 unit (32 channels)
- Sampling analog value from input port of 32 channels
- Conversion time: 1 μs
- External trigger activation (ADTG)
- Activation from internal timer (base timer)

4ch Sample-hold A/D Converter

- 12 bit resolution A/D converter: 2 units (8 channels)

Multi-function Serial Interface (MFS)

- UART / CSIO / LIN interface (v2.1) communication available by selecting the function
- Transmission FIFO: 64 Byte, reception FIFO: 64 Byte
- Reception interrupt factor (3 types)
  - Reception error detection (parity, over run, frame error)
  - Reception to FIFO for data of setting value
  - Reception data under setting value in FIFO, idle term detection of over 8 clocks with baud rate clock
- Transmission interrupt factor (2 types)
  - No transmission operation
  - Transmission FIFO empty (contain transmission operation)
- SPI (serial peripheral interface) support
- LIN protocol revision 2.1 support

Up/Down Counter (UDC)

- 8/16-bit up/down counter (2 channels uses for R/D converter)

CAN Interface

- The CAN is based on the CAN protocol ver. 2.0A/B
- 64 message buffers x 3 channels
- An identification mask is applied to each message object
- Up to 1Mbps support
- Clock support CAN prescaler
- CAN wakeup functions

FlexRay Controller

- Supports FlexRay protocol specification v2.1
- Maximum 128 message buffers
- 8K Byte message RAM
- Variable length of message buffers
- Each message buffer can be allocated as a part of reception buffer, transmission buffer or reception FIFO
- Host access to the message buffer via input and output buffers
- Filtering for slot counter, cycle counter and channels
- Maskable interrupts are supported

R/D Converter (RDC)

- Connect to resolver interface

D/A Converter (DAC)

- 10-bit resolution

Motor Vector Operation Accelerator (MVA)

- Assist for three-phase current normalizing, three-phase to two-phase DC conversion / two-phase to three- phase AC conversion, angler calculation, PID control calculation.
- Error detection in processing (overflow/under flow/non normalizing error of FLOP)
- Amplitude diagnosis /angle diagnosis function of R/D converter
- Error current diagnosis function

Key Code

- Key code supports
  - A part of General-purpose I/O (GPIO) register
  - Port pin configuration (PPC) register
  - Analog input control register (ADER)
  - 4ch ADC analog input control register (ADER4CH_1, ADER4CH_0)
  - Analog output control register (DAC00_DAER, DAC01_DAER)

Contents

1. Product Lineup

Memory Size

Parameter	CY9DF566
FLASH size (program)	(1024 KB+128 KB)×2
FLASH size (Work)	64 KB×2
RAM size	128 KB×2

Functions

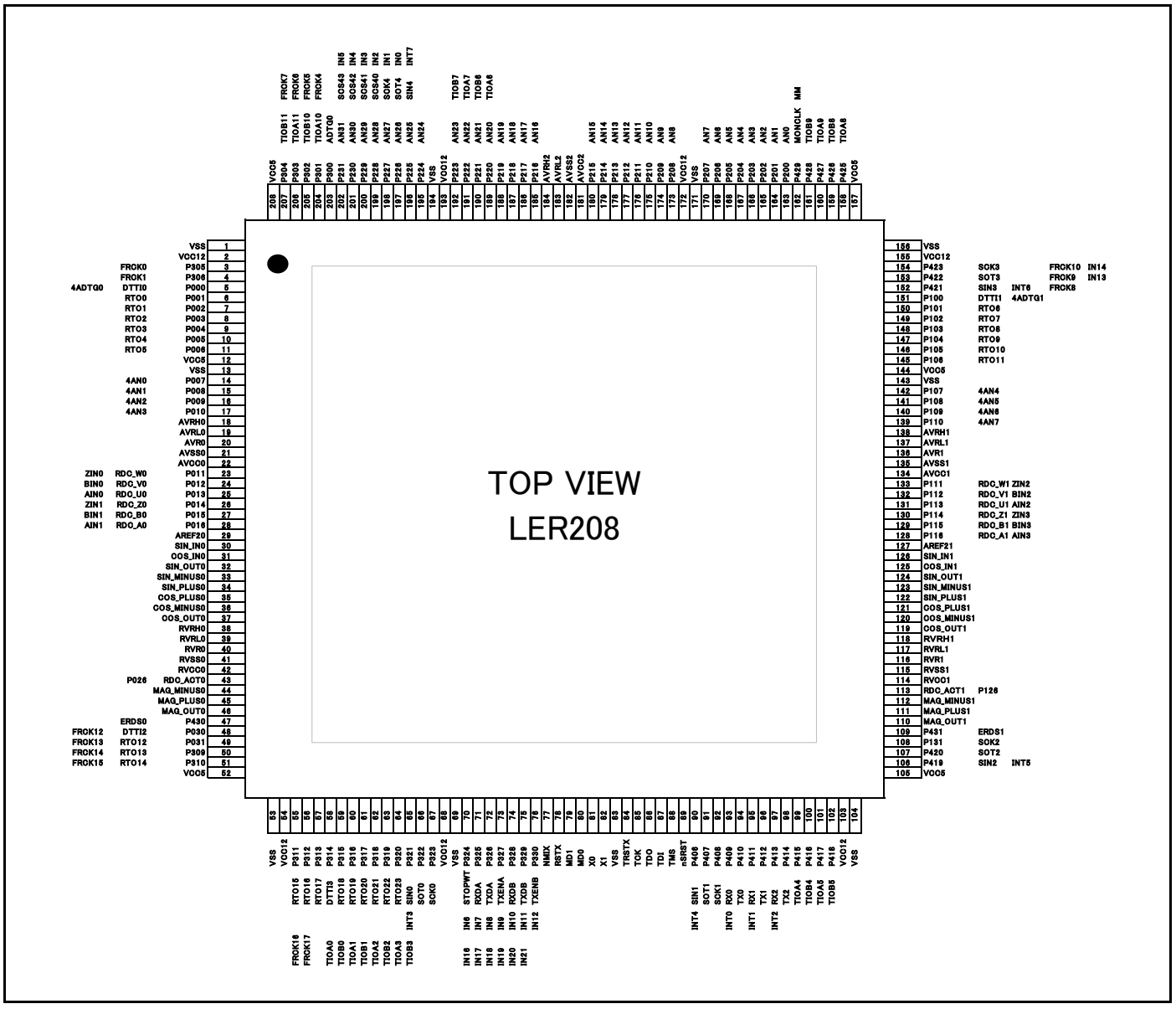
Pin Number	208 pin
System clock	On-chip PLL clock multiplication system Minimum instruction execution time :5 ns (200 MHz)
CR oscillator (fast/slow)	Yes
DMAC	16 channels
Base timer	12 channels (0 to 11)
32-bit free-run timer	5 channels
32-bit input capture	3 units (6 channels)
16-bit free-run timer	20 channels*1
16-bit input capture	8 units (0 to 7) (15 channels (0 to 14))
16-bit output compare	12 units (0 to 11) (24 channels (0 to 23))
Waveform generator	4 units (0 to 3) (24 channels (0 to 23))
External interrupt	8 channels (0 to 7)
A/D converter	1 unit (32 channels)
4ch sample-hold A/D converter	2 units (8 channels)
R/D converter	2 units*2
D/A converter	2 channels*2
Up/Down counter	4 channels
Motor vector operation accelerator	2 units
Multi-function serial interface	5 channels (0 to 4)
CAN	3 channels
FlexRay	128 msb x 1 unit (ch.A / ch.B)*2
Inter-processor communications unit	Yes
Exclusive access memory	Yes
Software watchdog timer	Yes
Hardware watchdog timer	Yes
CRC	2 channels
Internal power supply low-voltage detection	Yes
External power supply low-voltage detection	Yes
Key code	Yes*2
Package	LER208
Debugging interface	JTAG interface

*1: 2 channels for motor control

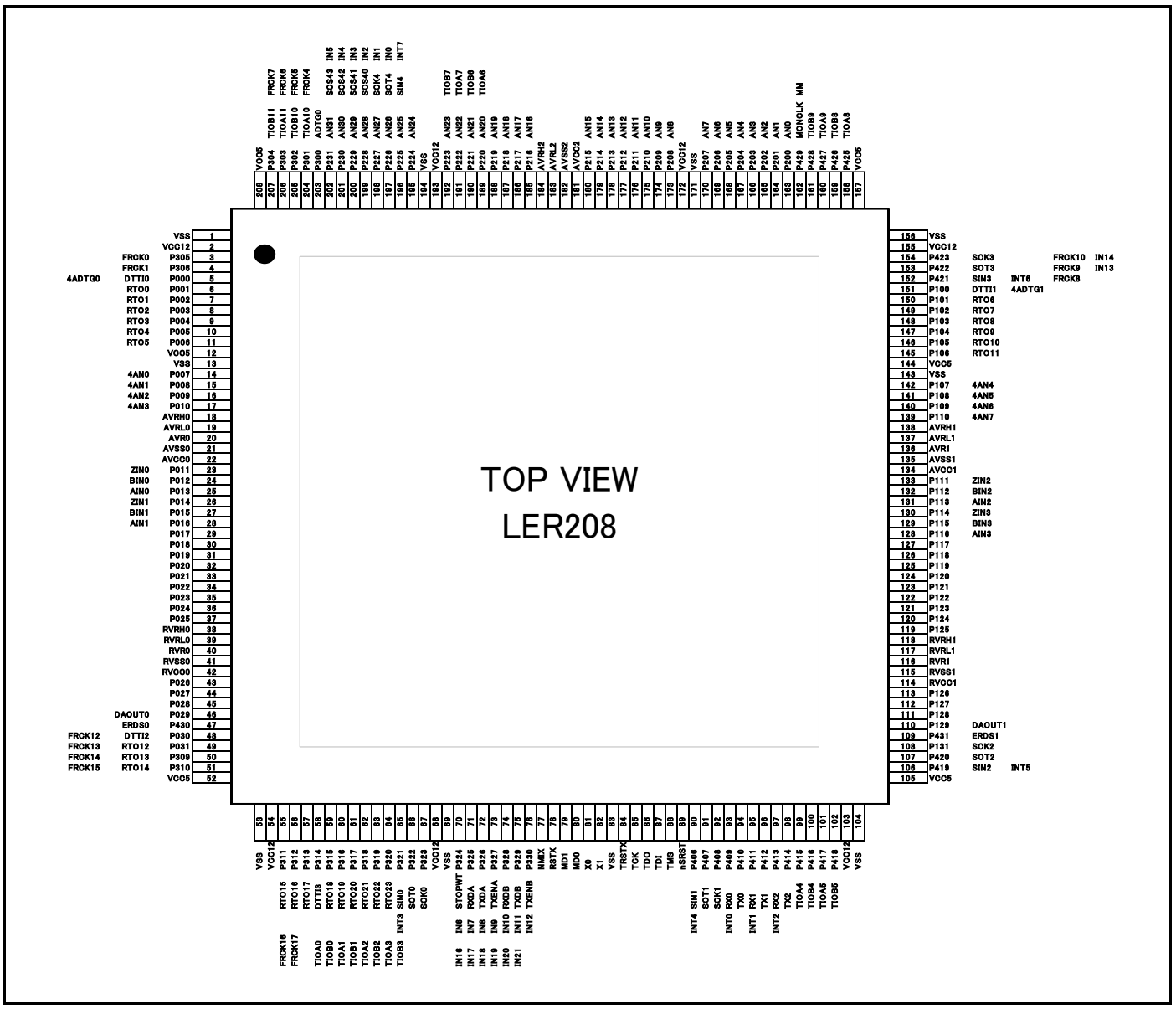
*2: The function is different according to the part number. See “13. Part Number Option”.

2. Pin Assignment

208 Pin Part Number with RDC



208 Pin Part Number without RDC



3. Pin Description

Part Number with RDC

Pin Number 208 pin	Pin Name	I/O Circuit Type	Functions
3	P305 FRCK0	E	General-purpose I/O port 16-bit free-run timer ch.0 external clock input pin
4	P306 FRCK1	E	General-purpose I/O port 16-bit free-run timer ch.1 external clock input pin
5	P000 DTTI0 4ADTG0	E	General-purpose I/O port Waveform generator output stop signal input pin 0 4ch sample-hold A/D converter unit0 external trigger input pin
6	P001 RTO0	E	General-purpose I/O port Waveform generator ch.0 output pin
7	P002 RTO1	E	General-purpose I/O port Waveform generator ch.1 output pin
8	P003 RTO2	E	General-purpose I/O port Waveform generator ch.2 output pin
9	P004 RTO3	E	General-purpose I/O port Waveform generator ch.3 output pin
10	P005 RTO4	E	General-purpose I/O port Waveform generator ch.4 output pin
11	P006 RTO5	E	General-purpose I/O port Waveform generator ch.5 output pin
14	P007 4AN0	F	General-purpose I/O port 4ch sample-hold A/D converter unit0 analog 0 input pin
15	P008 4AN1	F	General-purpose I/O port 4ch sample-hold A/D converter unit0 analog 1 input pin
16	P009 4AN2	F	General-purpose I/O port 4ch sample-hold A/D converter unit0 analog 2 input pin
17	P010 4AN3	F	General-purpose I/O port 4ch sample-hold A/D converter unit0 analog 3 input pin
23	P011 RDC_W0 ZIN0	E	General-purpose I/O port R/D converter unit0 W-phase output pin Up/Down counter ch.0 ZIN input pin
24	P012 RDC_V0 BIN0	E	General-purpose I/O port R/D converter unit0 V-phase output pin Up/Down counter ch.0 BIN input pin
25	P013 RDC_U0 AIN0	E	General-purpose I/O port R/D converter unit0 U-phase output pin Up/Down counter ch.0 AIN input pin
26	P014 RDC_Z0 ZIN1	E	General-purpose I/O port R/D converter unit0 Z-phase output pin Up/Down counter ch.1 ZIN input pin
27	P015 RDC_B0 BIN1	E	General-purpose I/O port R/D converter unit0 B-phase output pin Up/Down counter ch.1 BIN input pin
28	P016 RDC_A0 AIN1	E	General-purpose I/O port R/D converter unit0 A-phase output pin Up/Down counter ch.1 AIN input pin
29	AREF20	L	R/D converter unit0 Aref output pin(RVCC0/2)
30	SIN_IN0	K	R/D converter unit0 SIN coil earth leakage detection input pin
31	COS_IN0	K	R/D converter unit0 COS coil earth leakage detection input pin
32	SIN_OUT0	L	R/D converter unit0 SIN output pin
33	SIN_MINUS0	K	R/D converter unit0 SIN input pin-
34	SIN_PLUS0	K	R/D converter unit0 SIN input pin+
35	COS_PLUS0	K	R/D converter unit0 COS input pin+
36	COS_MINUS0	K	R/D converter unit0 COS input pin-
37	COS_OUT0	L	R/D converter unit0 COS output pin
43	RDC_ACT0 P026	E	R/D converter unit0 operation status output pin General-purpose I/O port
44	MAG_MINUS0	K	R/D converter unit0 excitation external input pin-

Pin Number 208 pin	Pin Name	I/O Circuit Type	Functions
45	MAG_PLUS0	K	R/D converter unit0 excitation external input pin+
46	MAG_OUT0	L	R/D converter unit0 excitation signal output pin
47	P430 ERDS0	E	General-purpose I/O port Error detection output pin ch.0
48	P030 DTTI2 FRCK12	E	General-purpose I/O port Waveform generator output stop signal input pin 2 16-bit free-run timer ch.12 external clock input pin
49	P031 RTO12 FRCK13	E	General-purpose I/O port Waveform generator ch.12 output pin 16-bit free-run timer ch.13 external clock input pin
50	P309 RTO13 FRCK14	E	General-purpose I/O port Waveform generator ch.13 output pin 16-bit free-run timer ch.14 external clock input pin
51	P310 RTO14 FRCK15	E	General-purpose I/O port Waveform generator ch.14 output pin 16-bit free-run timer ch.15 external clock input pin
55	P311 RTO15 FRCK16	E	General-purpose I/O port Waveform generator ch.15 output pin 16-bit free-run timer ch.16 external clock input pin
56	P312 RTO16 FRCK17	E	General-purpose I/O port Waveform generator ch.16 output pin 16-bit free-run timer ch.17 external clock input pin
57	P313 RTO17	E	General-purpose I/O port Waveform generator ch.17 output pin
58	P314 DTTI3 TIOA0	E	General-purpose I/O port Waveform generator output stop signal input pin 3 Base timer ch.0 TIOA output pin
59	P315 RTO18 TIOB0	E	General-purpose I/O port Waveform generator ch.18 output pin Base timer ch.0 TIOB input pin
60	P316 RTO19 TIOA1	E	General-purpose I/O port Waveform generator ch.19 output pin Base timer ch.1 TIOA I/O pin
61	P317 RTO20 TIOB1	E	General-purpose I/O port Waveform generator ch.20 output pin Base timer ch.1 TIOB input pin
62	P318 RTO21 TIOA2	E	General-purpose I/O port Waveform generator ch.21 output pin Base timer ch.2 TIOA output pin
63	P319 RTO22 TIOB2	E	General-purpose I/O port Waveform generator ch.22 output pin Base timer ch.2 TIOB input pin
64	P320 RTO23 TIOA3	E	General-purpose I/O port Waveform generator ch.23 output pin Base timer ch.3 TIOA I/O pin
65	P321 SIN0 INT3 TIOB3	E	General-purpose I/O port Multi-function serial interface ch.0 serial data input pin INT3 external interrupt input pin Base timer ch.3 TIOB input pin
66	P322 SOT0	E	General-purpose I/O port Multi-function serial interface ch.0 serial data output pin
67	P323 SCK0	E	General-purpose I/O port Multi-function serial interface ch.0 clock I/O pin
70	P324 STOPWT IN6 IN16	E	General-purpose I/O port FlexRay stop watch input pin 16-bit input capture ch.6 external pulse input pin 32-bit input capture ch.0 external pulse input pin
71	P325 RXDA IN7 IN17	H	General-purpose I/O port FlexRay ch.A data input pin 16-bit input capture ch.7 external pulse input pin 32-bit input capture ch.1 external pulse input pin

Pin Number 208 pin	Pin Name	I/O Circuit Type	Functions
72	P326 TXDA IN8 IN18	H	General-purpose I/O port FlexRay ch.A data output pin 16-bit input capture ch.8 external pulse input pin 32-bit input capture ch.2 external pulse input pin
73	P327 TXENA IN9 IN19	H	General-purpose I/O port FlexRay ch.A operation enable output pin 16-bit input capture ch.9 external pulse input pin 32-bit input capture ch.3 external pulse input pin
74	P328 RXDB IN10 IN20	H	General-purpose I/O port FlexRay ch.B data input pin 16-bit input capture ch.10 external pulse input pin 32-bit input capture ch.4 external pulse input pin
75	P329 TXDB IN11 IN21	H	General-purpose I/O port FlexRay ch.B data output pin 16-bit input capture ch.11 external pulse input pin 32-bit input capture ch.5 external pulse input pin
76	P330 TXENB IN12	H	General-purpose I/O port FlexRay ch.B operation enable output pin 16-bit input capture ch.12 external pulse input pin
77	NMIX	B	Non-maskable interrupt input pin
78	RSTX	B	External reset input pin
79	MD1	C	Mode pin 1 (with high-voltage control)
80	MD0	C	Mode pin 0 (with high-voltage control)
81	X0	A	Main clock oscillation input pin
82	X1		Main clock oscillation output pin
84	TRSTX	J	JTAG test reset input
85	TCK	J	JTAG test clock input
86	TDO	I	JTAG test data output
87	TDI	J	JTAG test data input
88	TMS	J	JTAG test mode status input
89	nSRST	J	System reset input for debugger
90	P406 SIN1 INT4	E	General-purpose I/O port Multi-function serial interface ch.1 serial data input pin INT4 external interrupt input pin
91	P407 SOT1	E	General-purpose I/O port Multi-function serial interface ch.1 serial data output pin
92	P408 SCK1	E	General-purpose I/O port Multi-function serial interface ch.1 clock I/O pin
93	P409 RX0 INT0	E	General-purpose I/O port CAN ch.0 reception data input pin INT0 external interrupt input pin
94	P410 TX0	E	General-purpose I/O port CAN ch.0 transmission data output pin
95	P411 RX1 INT1	E	General-purpose I/O port CAN ch.1 reception data input pin INT1 external interrupt input pin
96	P412 TX1	E	General-purpose I/O port CAN ch.1 transmission data output pin
97	P413 RX2 INT2	E	General-purpose I/O port CAN ch.2 reception data input pin INT2 external interrupt input pin
98	P414 TX2	E	General-purpose I/O port CAN ch.2 transmission data output pin
99	P415 TIOA4	E	General-purpose I/O port Base timer ch.4 TIOA output pin
100	P416 TIOB4	E	General-purpose I/O port Base timer ch.4 TIOB input pin
101	P417 TIOA5	E	General-purpose I/O port Base timer ch.5 TIOA I/O pin

Pin Number 208 pin	Pin Name	I/O Circuit Type	Functions
102	P418 TIOB5	E	General-purpose I/O port Base timer ch.5 TIOB input pin
106	P419 SIN2 INT5	E	General-purpose I/O port Multi-function serial interface ch.2 serial data input pin INT5 external interrupt input pin
107	P420 SOT2	E	General-purpose I/O port Multi-function serial interface ch.2 serial data output pin
108	P131 SCK2	E	General-purpose I/O port Multi-function serial interface ch.2 clock I/O pin
109	P431 ERDS1	E	General-purpose I/O port Error detection output pin ch.1
110	MAG_OUT1	L	R/D converter unit1excitation signal output pin
111	MAG_PLUS1	K	R/D converter unit1excitation external input pin+
112	MAG_MINUS1	K	R/D converter unit1excitation external input pin-
113	RDC_ACT1 P126	E	R/D converter unit1 operation status output pin General-purpose I/O port
119	COS_OUT1	L	R/D converter unit1 COS output pin
120	COS_MINUS1	K	R/D converter unit1 COS input pin-
121	COS_PLUS1	K	R/D converter unit1 COS input pin+
122	SIN_PLUS1	K	R/D converter unit1 SIN input pin+
123	SIN_MINUS1	K	R/D converter unit1 SIN input pin-
124	SIN_OUT1	L	R/D converter unit1 SIN output pin
125	COS_IN1	K	R/D converter unit1 COS coil earth leakage detection input pin
126	SIN_IN1	K	R/D converter unit1 SIN coil earth leakage detection input pin
127	AREF21	L	R/D converter unit1 Aref output pin(RVCC1/2)
128	P116 RDC_A1 AIN3	E	General-purpose I/O port R/D converter unit1 A phase output pin Up/Down counter ch.3 AIN input pin
129	P115 RDC_B1 BIN3	E	General-purpose I/O port R/D converter unit1 B phase output pin Up/Down counter ch.3 BIN input pin
130	P114 RDC_Z1 ZIN3	E	General-purpose I/O port R/D converter unit1 Z phase output pin Up/Down counter ch.3 ZIN input pin
131	P113 RDC_U1 AIN2	E	General-purpose I/O port R/D converter unit1 U phase output pin Up/Down counter ch.2 AIN input pin
132	P112 RDC_V1 BIN2	E	General-purpose I/O port R/D converter unit1 V phase output pin Up/Down counter ch.2 BIN input pin
133	P111 RDC_W1 ZIN2	E	General-purpose I/O port R/D converter unit1 W phase output pin Up/Down counter ch.2 ZIN input pin
139	P110 4AN7	F	General-purpose I/O port 4ch sample-hold A/D converter unit1 analog 7 input pin
140	P109 4AN6	F	General-purpose I/O port 4ch sample-hold A/D converter unit1 analog 6 input pin
141	P108 4AN5	F	General-purpose I/O port 4ch sample-hold A/D converter unit1 analog 5 input pin
142	P107 4AN4	F	General-purpose I/O port 4ch sample-hold A/D converter unit1 analog 4 input pin
145	P106 RTO11	E	General-purpose I/O port Waveform generator ch.11 output pin
146	P105 RTO10	E	General-purpose I/O port Waveform generator ch.10 output pin
147	P104 RTO9	E	General-purpose I/O port Waveform generator ch.9 output pin
148	P103 RTO8	E	General-purpose I/O port Waveform generator ch.8 output pin

Pin Number 208 pin	Pin Name	I/O Circuit Type	Functions
149	P102 RTO7	E	General-purpose I/O port Waveform generator ch.7 output pin
150	P101 RTO6	E	General-purpose I/O port Waveform generator ch.6 output pin
151	P100 DTTI1 4ADTG1	E	General-purpose I/O port Waveform generator output stop signal input pin1 4ch sample-hold A/D converter unit1 external trigger input pin
152	P421 SIN3 INT6 FRCK8	E	General-purpose I/O port Multi-function serial interface ch.3 serial data input pin INT6 external interrupt input pin 16-bit free-run timer ch.8 external clock input pin
153	P422 SOT3 FRCK9 IN13	E	General-purpose I/O port Multi -function serial interface ch.3 serial data output pin 16-bit free-run timer ch.9 external clock input pin 16-bit input capture ch.13 external pulse input pin
154	P423 SCK3 FRCK10 IN14	E	General-purpose I/O port Multi-function serial interface ch.3 clock I/O pin 16-bit free-run timer ch.10 external clock input pin 16-bit input capture ch.14 external pulse input pin
158	P425 TIOA8	E	General-purpose I/O port Base timer ch.8 TIOA output pin
159	P426 TIOB8	E	General-purpose I/O port Base timer ch.8 TIOB input pin
160	P427 TIOA9	E	General-purpose I/O port Base timer ch.9 TIOA I/O pin
161	P428 TIOB9	E	General-purpose I/O port Base timer ch.9 TIOB input pin
162	P429 MONCLK MM	E	General-purpose I/O port Clock monitor output pin Clock supervisor main clock error detection output pin
163	P200 AN0	F	General-purpose I/O port A/D converter analog 0 input pin
164	P201 AN1	F	General-purpose I/O port A/D converter analog 1 input pin
165	P202 AN2	F	General-purpose I/O port A/D converter analog 2 input pin
166	P203 AN3	F	General-purpose I/O port A/D converter analog 3 input pin
167	P204 AN4	F	General-purpose I/O port A/D converter analog 4 input pin
168	P205 AN5	F	General-purpose I/O port A/D converter analog 5 input pin
169	P206 AN6	F	General-purpose I/O port A/D converter analog 6 input pin
170	P207 AN7	F	General-purpose I/O port A/D converter analog 7 input pin
173	P208 AN8	F	General-purpose I/O port A/D converter analog 8 input pin
174	P209 AN9	F	General-purpose I/O port A/D converter analog 9 input pin
175	P210 AN10	F	General-purpose I/O port A/D converter analog 10 input pin
176	P211 AN11	F	General-purpose I/O port A/D converter analog 11 input pin
177	P212 AN12	F	General-purpose I/O port A/D converter analog 12 input pin
178	P213 AN13	F	General-purpose I/O port A/D converter analog 13 input pin
179	P214 AN14	F	General-purpose I/O port A/D converter analog 14 input pin

Pin Number 208 pin	Pin Name	I/O Circuit Type	Functions
180	P215 AN15	F	General-purpose I/O port A/D converter analog 15 input pin
185	P216 AN16	F	General-purpose I/O port A/D converter analog 16 input pin
186	P217 AN17	F	General-purpose I/O port A/D converter analog 17 input pin
187	P218 AN18	F	General-purpose I/O port A/D converter analog 18 input pin
188	P219 AN19	F	General-purpose I/O port A/D converter analog 19 input pin
189	P220 AN20 TIOA6	F	General-purpose I/O port A/D converter analog 20 input pin Base timer ch.6 TIOA output pin
190	P221 AN21 TIOB6	F	General-purpose I/O port A/D converter analog 21 input pin Base timer ch.6 TIOB input pin
191	P222 AN22 TIOA7	F	General-purpose I/O port A/D converter analog 22 input pin Base timer ch.7 TIOA I/O pin
192	P223 AN23 TIOB7	F	General-purpose I/O port A/D converter analog 23 input pin Base timer ch.7 TIOB input pin
195	P224 AN24	F	General-purpose I/O port A/D converter Analog 24 input pin
196	P225 AN25 SIN4 INT7	F	General-purpose I/O port A/D converter analog 25 input pin Multi-function serial interface ch.4 serial data input pin INT7 external interrupt input pin
197	P226 AN26 SOT4 IN0	F	General-purpose I/O port A/D converter analog 26 input pin Multi-function serial interface ch.4 serial data output pin 16-bit input capture ch.0 external pulse input pin
198	P227 AN27 SCK4 IN1	F	General-purpose I/O port A/D converter analog 27 input pin Multi-function serial interface ch.4 clock I/O pin 16-bit input capture ch.1 external pulse input pin
199	P228 AN28 SCS40 IN2	F	General-purpose I/O port A/D converter analog 28 input pin Multi-function serial interface ch.4 serial chip select 0 I/O pin 16-bit input capture ch.2 external pulse input pin
200	P229 AN29 SCS41 IN3	F	General-purpose I/O port A/D converter analog 29 input pin Multi-function serial interface ch.4 serial chip select 1 I/O pin 16-bit input capture ch.3 external pulse input pin
201	P230 AN30 SCS42 IN4	F	General-purpose I/O port A/D converter analog 30 input pin Multi-function serial interface ch.4 serial chip select 2 I/O pin 16-bit input capture ch.4 external pulse input pin
202	P231 AN31 SCS43 IN5	F	General-purpose I/O port A/D converter analog 31 input pin Multi-function serial interface ch.4 serial chip select 3 I/O pin 16-bit input capture ch.5 external pulse input pin
203	P300 ADTG0	E	General-purpose I/O port A/D converter external trigger input pin
204	P301 TIOA10 FRCK4	E	General-purpose I/O port Base timer ch.10 TIOA output pin 16-bit free-run timer ch.4 external clock input pin
205	P302 TIOB10 FRCK5	E	General-purpose I/O port Base timer ch.10 TIOB input pin 16-bit free-run timer ch.5 external clock input pin

Pin Number 208 pin	Pin Name	I/O Circuit Type	Functions
206	P303 TIOA11 FRCK6	E	General-purpose I/O port Base timer ch.11 TIOA I/O pin 16-bit free-run timer ch.6 external clock input pin
207	P304 TIOB11 FRCK7	E	General-purpose I/O port Base timer ch.11 TIOB input pin 16-bit free-run timer ch.7 external clock input pin
18	AVRH0	-	4ch sample-hold A/D converter unit0 upper limit reference voltage
19	AVRL0	-	4ch sample-hold A/D converter unit0 lower limit reference voltage
20	AVR0	-	4ch sample-hold A/D converter unit0 reference voltage
21	AVSS0	-	4ch sample-hold A/D converter unit0 analog GND
22	AVCC0	-	4ch sample-hold A/D converter unit0 analog power supply
134	AVCC1	-	4ch sample-hold A/D converter unit1 analog power supply
135	AVSS1	-	4ch sample-hold A/D converter unit1 analog GND
136	AVR1	-	4ch sample-hold A/D converter unit1 reference voltage
137	AVRL1	-	4ch sample-hold A/D converter unit1 lower limit reference voltage
138	AVRH1	-	4ch sample-hold A/D converter unit1 upper limit reference voltage
38	RVRH0	-	R/D converter unit0 upper limit reference voltage
39	RVRL0	-	R/D converter unit0 lower limit reference voltage
40	RVR0	-	R/D converter unit0 reference voltage
41	RVSS0	-	R/D converter unit0 analog GND
42	RVCC0	-	R/D converter unit0 analog power supply
114	RVCC1	-	R/D converter unit1 analog power supply
115	RVSS1	-	R/D converter unit1 analog GND
116	RVR1	-	R/D converter unit1 reference voltage
117	RVRL1	-	R/D converter unit1 lower limit reference voltage
118	RVRH1	-	R/D converter unit1 upper limit reference voltage
181	AVCC2	-	A/D converter analog power supply
182	AVSS2	-	A/D converter analog GND
183	AVRL2	-	A/D converter lower limit reference voltage
184	AVRH2	-	A/D converter upper limit reference voltage
2 54 68 103 155 172 193	VCC12	-	1.2V power supply
12 52 105 144 157 208	VCC5	-	5.0V power supply
1 13 53 69 83 104 143 156 171 194	VSS	-	GND

Part Number without RDC

Pin Number 208pin	Pin Name	I/O Circuit Type	Functions
3	P305 FRCK0	E	General-purpose I/O port 16-bit free-run timer ch.0 external clock input pin
4	P306 FRCK1	E	General-purpose I/O port 16-bit free-run timer ch.1 external clock input pin
5	P000 DTTI0 4ADTG0	E	General-purpose I/O port Waveform generator output stop signal input pin 0 4ch sample-hold A/D converter unit0 external trigger input pin
6	P001 RTO0	E	General-purpose I/O port Waveform generator ch.0 output pin
7	P002 RTO1	E	General-purpose I/O port Waveform generator ch.1 output pin
8	P003 RTO2	E	General-purpose I/O port Waveform generator ch.2 output pin
9	P004 RTO3	E	General-purpose I/O port Waveform generator ch.3 output pin
10	P005 RTO4	E	General-purpose I/O port Waveform generator ch.4 output pin
11	P006 RTO5	E	General-purpose I/O port Waveform generator ch.5 output pin
14	P007 4AN0	F	General-purpose I/O port 4ch sample-hold A/D converter unit0 analog 0 input pin
15	P008 4AN1	F	General-purpose I/O port 4ch sample-hold A/D converter unit0 analog 1 input pin
16	P009 4AN2	F	General-purpose I/O port 4ch sample-hold A/D converter unit0 analog 2 input pin
17	P010 4AN3	F	General-purpose I/O port 4ch sample-hold A/D converter unit0 analog 3 input pin
23	P011 ZIN0	E	General-purpose I/O port Up/Down counter ch.0 ZIN input pin
24	P012 BIN0	E	General-purpose I/O port Up/Down counter ch.0 BIN input pin
25	P013 AIN0	E	General-purpose I/O port Up/Down counter ch.0 AIN input pin
26	P014 ZIN1	E	General-purpose I/O port Up/Down counter ch.1 ZIN input pin
27	P015 BIN1	E	General-purpose I/O port Up/Down counter ch.1 BIN input pin
28	P016 AIN1	E	General-purpose I/O port Up/Down counter ch.1 AIN input pin
29	P017	E	General-purpose I/O port
30	P018	E	General-purpose I/O port
31	P019	E	General-purpose I/O port
32	P020	E	General-purpose I/O port
33	P021	E	General-purpose I/O port
34	P022	E	General-purpose I/O port
35	P023	E	General-purpose I/O port
36	P024	E	General-purpose I/O port
37	P025	E	General-purpose I/O port
43	P026	E	General-purpose I/O port
44	P027	E	General-purpose I/O port
45	P028	E	General-purpose I/O port
46	P029 DAOUT0	G	General-purpose I/O port D/A converter ch.0 analog output pin
47	P430 ERDS0	E	General-purpose I/O port Error detection output pin ch.0
48	P030 DTTI2 FRCK12	E	General-purpose I/O port Waveform generator output stop signal input pin 2 16-bit free-run timer ch.12 external clock input pin

Pin Number 208pin	Pin Name	I/O Circuit Type	Functions
49	P031 RTO12 FRCK13	E	General-purpose I/O port Waveform generator ch.12 output pin 16-bit free-run timer ch.13 external clock input pin
50	P309 RTO13 FRCK14	E	General-purpose I/O port Waveform generator ch.13 output pin 16-bit free-run timer ch.14 external clock input pin
51	P310 RTO14 FRCK15	E	General-purpose I/O port Waveform generator ch.14 output pin 16-bit free-run timer ch.15 external clock input pin
55	P311 RTO15 FRCK16	E	General-purpose I/O port Waveform generator ch.15 output pin 16-bit free-run timer ch.16 external clock input pin
56	P312 RTO16 FRCK17	E	General-purpose I/O port Waveform generator ch.16 output pin 16-bit free-run timer ch.17 external clock input pin
57	P313 RTO17	E	General-purpose I/O port Waveform generator ch.17 output pin
58	P314 DTTI3 TIOA0	E	General-purpose I/O port Waveform generator output stop signal input pin 3 Base timer ch.0 TIOA output pin
59	P315 RTO18 TIOB0	E	General-purpose I/O port Waveform generator ch.18 output pin Base timer ch.0 TIOB input pin
60	P316 RTO19 TIOA1	E	General-purpose I/O port Waveform generator ch.19 output pin Base timer ch.1 TIOA I/O pin
61	P317 RTO20 TIOB1	E	General-purpose I/O port Waveform generator ch.20 output pin Base timer ch.1 TIOB input pin
62	P318 RTO21 TIOA2	E	General-purpose I/O port Waveform generator ch.21 output pin Base timer ch.2 TIOA output pin
63	P319 RTO22 TIOB2	E	General-purpose I/O port Waveform generator ch.22 output pin Base timer ch.2 TIOB input pin
64	P320 RTO23 TIOA3	E	General-purpose I/O port Waveform generator ch.23 output pin Base timer ch.3 TIOA I/O pin
65	P321 SIN0 INT3 TIOB3	E	General-purpose I/O port Multi-function serial interface ch.0 serial data input pin INT3 external interrupt input pin Base timer ch.3 TIOB input pin
66	P322 SOT0	E	General-purpose I/O port Multi-function serial interface ch.0 serial data output pin
67	P323 SCK0	E	General-purpose I/O port Multi-function serial interface ch.0 clock I/O pin
70	P324 STOPWT IN6 IN16	E	General-purpose I/O port FlexRay stop watch input pin 16-bit input capture ch.6 external pulse input pin 32-bit input capture ch.0 external pulse input pin
71	P325 RXDA IN7 IN17	H	General-purpose I/O port FlexRay ch.A data input pin 16-bit input capture ch.7 external pulse input pin 32-bit input capture ch.1 external pulse input pin
72	P326 TXDA IN8 IN18	H	General-purpose I/O port FlexRay ch.A data output pin 16-bit input capture ch.8 external pulse input pin 32-bit input capture ch.2 external pulse input pin

Pin Number 208pin	Pin Name	I/O Circuit Type	Functions
73	P327 TXENA IN9 IN19	H	General-purpose I/O port FlexRay ch.A operation enable output pin 16-bit input capture ch.9 external pulse input pin 32-bit input capture ch.3 external pulse input pin
74	P328 RXDB IN10 IN20	H	General-purpose I/O port FlexRay ch.B data input pin 16-bit input capture ch.10 external pulse input pin 32-bit input capture ch.4 external pulse input pin
75	P329 TXDB IN11 IN21	H	General-purpose I/O port FlexRay ch.B data output pin 16-bit input capture ch.11 external pulse input pin 32-bit input capture ch.5 external pulse input pin
76	P330 TXENB IN12	H	General-purpose I/O port FlexRay ch.B operation enable output pin 16-bit input capture ch.12 external pulse input pin
77	NMIX	B	Non-maskable interrupt input pin
78	RSTX	B	External reset input pin
79	MD1	C	Mode pin 1 (with high-voltage control)
80	MD0	C	Mode pin 0 (with high-voltage control)
81	X0	A	Main clock oscillation input pin
82	X1		Main clock oscillation output pin
84	TRSTX	J	JTAG test reset input
85	TCK	J	JTAG test clock input
86	TDO	I	JTAG test data output
87	TDI	J	JTAG test data input
88	TMS	J	JTAG test mode status input
89	nSRST	J	System reset input for debugger
90	P406 SIN1 INT4	E	General-purpose I/O port Multi-function serial interface ch.1 serial data input pin INT4 external interrupt input pin
91	P407 SOT1	E	General-purpose I/O port Multi-function serial interface ch.1 serial data output pin
92	P408 SCK1	E	General-purpose I/O port Multi-function serial interface ch.1 clock I/O pin
93	P409 RX0 INT0	E	General-purpose I/O port CAN ch.0 reception data input pin INT0 external interrupt input pin
94	P410 TX0	E	General-purpose I/O port CAN ch.0 transmission data output pin
95	P411 RX1 INT1	E	General-purpose I/O port CAN ch.1 reception data input pin INT1 external interrupt input pin
96	P412 TX1	E	General-purpose I/O port CAN ch.1 transmission data output pin
97	P413 RX2 INT2	E	General-purpose I/O port CAN ch.2 reception data input pin INT2 external interrupt input pin
98	P414 TX2	E	General-purpose I/O port CAN ch.2 transmission data output pin
99	P415 TIOA4	E	General-purpose I/O port Base timer ch.4 TIOA output pin
100	P416 TIOB4	E	General-purpose I/O port Base timer ch.4 TIOB input pin
101	P417 TIOA5	E	General-purpose I/O port Base timer ch.5 TIOA I/O pin
102	P418 TIOB5	E	General-purpose I/O port Base timer ch.5 TIOB input pin
106	P419 SIN2 INT5	E	General-purpose I/O port Multi-function serial interface ch.2 serial data input pin INT5 external interrupt input pin

Pin Number 208pin	Pin Name	I/O Circuit Type	Functions
107	P420 SOT2	E	General-purpose I/O port Multi-function serial interface ch.2 serial data output pin
108	P131 SCK2	E	General-purpose I/O port Multi-function serial interface ch.2 clock I/O pin
109	P431 ERDS1	E	General-purpose I/O port Error detection output pin ch.1
110	P129 DAOUT1	G	General-purpose I/O port D/A converter ch.1 analog output pin
111	P128	E	General-purpose I/O port
112	P127	E	General-purpose I/O port
113	P126	E	General-purpose I/O port
119	P125	E	General-purpose I/O port
120	P124	E	General-purpose I/O port
121	P123	E	General-purpose I/O port
122	P122	E	General-purpose I/O port
123	P121	E	General-purpose I/O port
124	P120	E	General-purpose I/O port
125	P119	E	General-purpose I/O port
126	P118	E	General-purpose I/O port
127	P117	E	General-purpose I/O port
128	P116 AIN3	E	General-purpose I/O port Up/Down counter ch.3 AIN input pin
129	P115 BIN3	E	General-purpose I/O port Up/Down counter ch.3 BIN input pin
130	P114 ZIN3	E	General-purpose I/O port Up/Down counter ch.3 ZIN input pin
131	P113 AIN2	E	General-purpose I/O port Up/Down counter ch.2 AIN input pin
132	P112 BIN2	E	General-purpose I/O port Up/Down counter ch.2 BIN input pin
133	P111 ZIN2	E	General-purpose I/O port Up/Down counter ch.2 ZIN input pin
139	P110 4AN7	F	General-purpose I/O port 4ch sample-hold A/D converter unit1 analog 7 input pin
140	P109 4AN6	F	General-purpose I/O port 4ch sample-hold A/D converter unit1 analog 6 input pin
141	P108 4AN5	F	General-purpose I/O port 4ch sample-hold A/D converter unit1 analog 5 input pin
142	P107 4AN4	F	General-purpose I/O port 4ch sample-hold A/D converter unit1 analog 4 input pin
145	P106 RTO11	E	General-purpose I/O port Waveform generator ch.11 output pin
146	P105 RTO10	E	General-purpose I/O port Waveform generator ch.10 output pin
147	P104 RTO9	E	General-purpose I/O port Waveform generator ch.9 output pin
148	P103 RTO8	E	General-purpose I/O port Waveform generator ch.8 output pin
149	P102 RTO7	E	General-purpose I/O port Waveform generator ch.7 output pin
150	P101 RTO6	E	General-purpose I/O port Waveform generator ch.6 output pin
151	P100 DTTI1 4ADTG1	E	General-purpose I/O port Waveform generator output stop signal input pin 1 4ch sample-hold A/D converter unit1 external trigger input pin
152	P421 SIN3 INT6 FRCK8	E	General-purpose I/O port Multi-function serial interface ch.3 serial data input pin INT6 external interrupt input pin 16-bit free-run timer ch.8 external clock input pin

Pin Number 208pin	Pin Name	I/O Circuit Type	Functions
153	P422 SOT3 FRCK9 IN13	E	General-purpose I/O port Multi -function serial interface ch.3 serial data output pin 16-bit free-run timer ch.9 external clock input pin 16-bit input capture ch.13 external pulse input pin
154	P423 SCK3 FRCK10 IN14	E	General-purpose I/O port Multi-function serial interface ch.3 clock I/O pin 16-bit free-run timer ch.10 external clock input pin 16-bit input capture ch.14 external pulse input pin
158	P425 TIOA8	E	General-purpose I/O port Base timer ch.8 TIOA output pin
159	P426 TIOB8	E	General-purpose I/O port Base timer ch.8 TIOB input pin
160	P427 TIOA9	E	General-purpose I/O port Base timer ch.9 TIOA I/O pin
161	P428 TIOB9	E	General-purpose I/O port Base timer ch.9 TIOB input pin
162	P429 MONCLK MM	E	General-purpose I/O port Clock monitor output pin Clock supervisor main clock error detection output pin
163	P200 AN0	F	General-purpose I/O port A/D converter analog 0 input pin
164	P201 AN1	F	General-purpose I/O port A/D converter analog 1 input pin
165	P202 AN2	F	General-purpose I/O port A/D converter analog 2 input pin
166	P203 AN3	F	General-purpose I/O port A/D converter analog 3 input pin
167	P204 AN4	F	General-purpose I/O port A/D converter analog 4 input pin
168	P205 AN5	F	General-purpose I/O port A/D converter analog 5 input pin
169	P206 AN6	F	General-purpose I/O port A/D converter analog 6 input pin
170	P207 AN7	F	General-purpose I/O port A/D converter analog 7 input pin
173	P208 AN8	F	General-purpose I/O port A/D converter analog 8 input pin
174	P209 AN9	F	General-purpose I/O port A/D converter analog 9 input pin
175	P210 AN10	F	General-purpose I/O port A/D converter analog 10 input pin
176	P211 AN11	F	General-purpose I/O port A/D converter analog 11 input pin
177	P212 AN12	F	General-purpose I/O port A/D converter analog 12 input pin
178	P213 AN13	F	General-purpose I/O port A/D converter analog 13 input pin
179	P214 AN14	F	General-purpose I/O port A/D converter analog 14 input pin
180	P215 AN15	F	General-purpose I/O port A/D converter analog 15 input pin
185	P216 AN16	F	General-purpose I/O port A/D converter analog 16 input pin
186	P217 AN17	F	General-purpose I/O port A/D converter analog 17 input pin
187	P218 AN18	F	General-purpose I/O port A/D converter analog 18 input pin
188	P219 AN19	F	General-purpose I/O port A/D converter analog 19 input pin

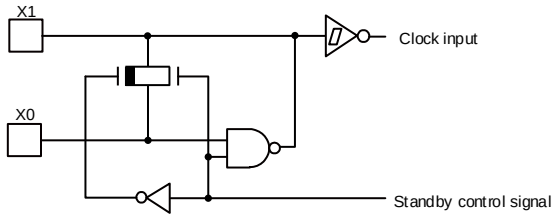
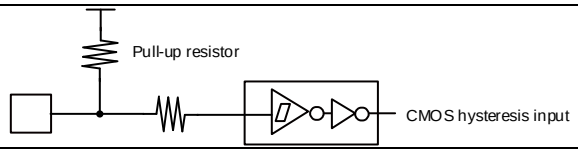
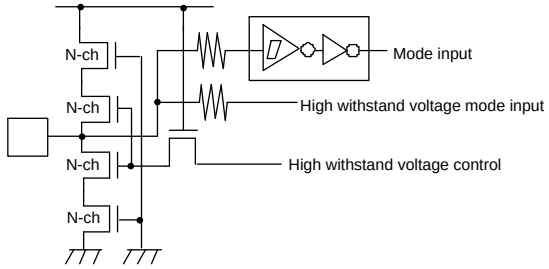
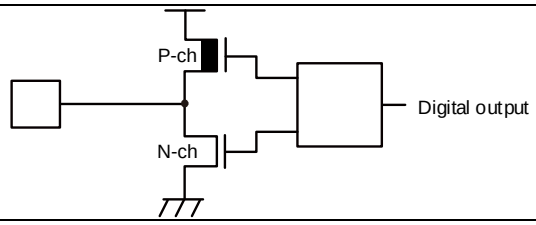
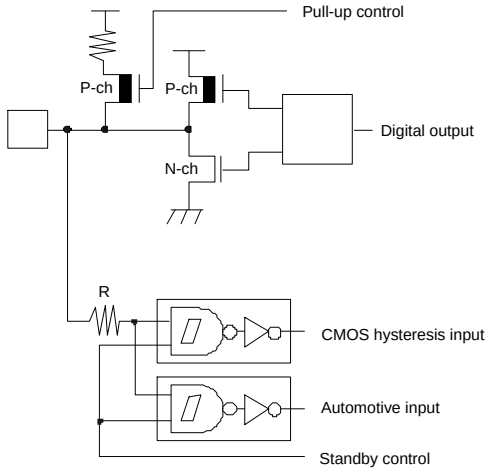
Pin Number 208pin	Pin Name	I/O Circuit Type	Functions
189	P220 AN20 TIOA6	F	General-purpose I/O port A/D converter analog 20 input pin Base timer ch.6 TIOA output pin
190	P221 AN21 TIOB6	F	General-purpose I/O port A/D converter analog 21 input pin Base timer ch.6 TIOB input pin
191	P222 AN22 TIOA7	F	General-purpose I/O port A/D converter analog 22 input pin Base timer ch.7 TIOA I/O pin
192	P223 AN23 TIOB7	F	General-purpose I/O port A/D converter analog 23 input pin Base timer ch.7 TIOB input pin
195	P224 AN24	F	General-purpose I/O port A/D converter analog 24 input pin
196	P225 AN25 SIN4 INT7	F	General-purpose I/O port A/D converter analog 25 input pin Multi-function serial interface ch.4 serial data input pin INT7 external interrupt input pin
197	P226 AN26 SOT4 IN0	F	General-purpose I/O port A/D converter analog 26 input pin Multi-function serial interface ch.4 serial data output pin 16-bit input capture ch.0 external pulse input pin
198	P227 AN27 SCK4 IN1	F	General-purpose I/O port A/D converter analog 27 input pin Multi-function serial interface ch.4 clock I/O pin 16-bit input capture ch.1 external pulse input pin
199	P228 AN28 SCS40 IN2	F	General-purpose I/O port A/D converter analog 28 input pin Multi-function serial interface ch.4 serial chip select 0 I/O pin 16-bit input capture ch.2 external pulse input pin
200	P229 AN29 SCS41 IN3	F	General-purpose I/O port A/D converter analog 29 input pin Multi-function serial interface ch.4 serial chip select 1 I/O pin 16-bit input capture ch.3 external pulse input pin
201	P230 AN30 SCS42 IN4	F	General-purpose I/O port A/D converter analog 30 input pin Multi-function serial interface ch.4 serial chip select 2 I/O pin 16-bit input capture ch.4 external pulse input pin
202	P231 AN31 SCS43 IN5	F	General-purpose I/O port A/D converter analog 31 input pin Multi-function serial interface ch.4 serial chip select 3 I/O pin 16-bit input capture ch.5 external pulse input pin
203	P300 ADTG0	E	General-purpose I/O port A/D converter external trigger input pin
204	P301 TIOA10 FRCK4	E	General-purpose I/O port Base timer ch.10 TIOA output pin 16-bit free-run timer ch.4 external clock input pin
205	P302 TIOB10 FRCK5	E	General-purpose I/O port Base timer ch.10 TIOB input pin 16-bit free-run timer ch.5 external clock input pin
206	P303 TIOA11 FRCK6	E	General-purpose I/O port Base timer ch.11 TIOA I/O pin 16-bit free-run timer ch.6 external clock input pin
207	P304 TIOB11 FRCK7	E	General-purpose I/O port Base timer ch.11 TIOB input pin 16-bit free-run timer ch.7 external clock input pin
18	AVRH0	-	4ch sample-hold A/D converter unit0 upper limit reference voltage
19	AVRL0	-	4ch sample-hold A/D converter unit0 lower limit reference voltage
20	AVR0	-	4ch sample-hold A/D converter unit0 reference voltage
21	AVSS0	-	4ch sample-hold A/D converter unit0 analog GND
22	AVCC0	-	4ch sample-hold A/D converter unit0 analog power supply

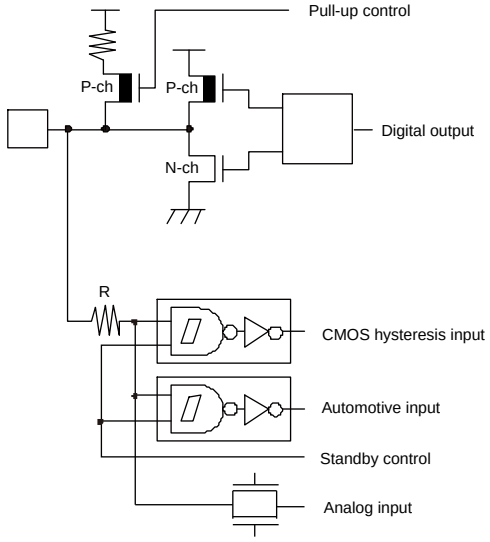
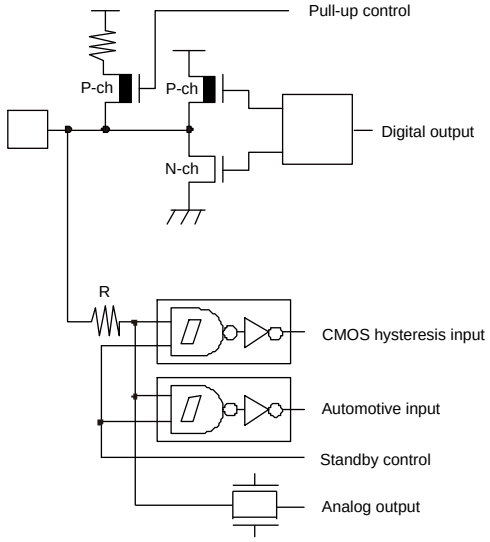
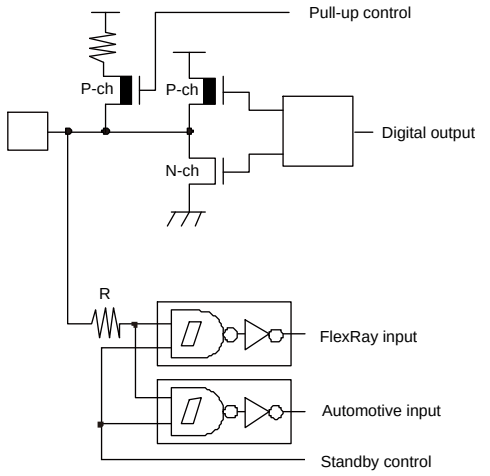
Pin Number 208pin	Pin Name	I/O Circuit Type	Functions
134	AVCC1	-	4ch sample-hold A/D converter unit1 analog power supply
135	AVSS1	-	4ch sample-hold A/D converter unit1 analog GND
136	AVR1	-	4ch sample-hold A/D converter unit1 reference voltage
137	AVRL1	-	4ch sample-hold A/D converter unit1 lower limit reference voltage
138	AVRH1	-	4ch sample-hold A/D converter unit1 upper limit reference voltage
38	RVRH0	-	*1
39	RVRL0	-	*2
40	RVR0	-	*2
41	RVSS0	-	*2
42	RVCC0	-	*1
114	RVCC1	-	*1
115	RVSS1	-	*2
116	RVR1	-	*2
117	RVRL1	-	*2
118	RVRH1	-	*1
181	AVCC2	-	A/D converter analog power supply
182	AVSS2	-	A/D converter analog GND
183	AVRL2	-	A/D converter lower limit reference voltage
184	AVRH2	-	A/D converter upper limit reference voltage
2 54 68 103 155 172 193	VCC12	-	1.2V power supply
12 52 105 144 157 208	VCC5	-	5.0V power supply
1 13 53 69 83 104 143 156 171 194	VSS	-	GND

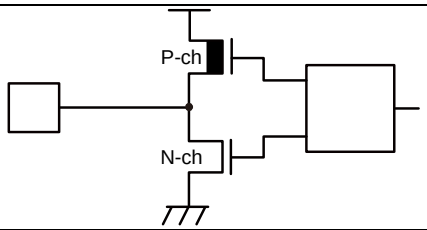
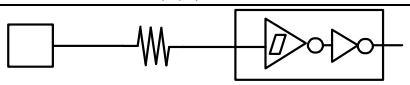
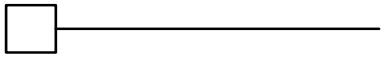
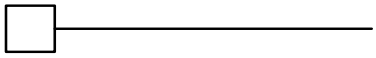
*1: The part number without RDC does not use this pin. Connect it with the VCC5 pin.

*2: The part number without RDC does not use this pin. Connect it with the VSS pin.

4. I/O Circuit Type

Type	Circuit	Remarks
A		• Oscillation feedback resistor: Approx. 1 MΩ
B		• CMOS hysteresis input • With 50 kΩ pull-up resistor
C		• Schmitt input • With high withstand voltage control
D		• CMOS level output I_{OH}=-1/-2 mA, I_{OL}=1/2 mA
E		• General-purpose I/O port • CMOS level output I_{OH}=-1/-2 mA, I_{OL}=1/2 mA • With 50 kΩ pull-up resistor • CMOS hysteresis input (0.7Vcc/0.3Vcc) • Automotive input (0.8Vcc/0.5Vcc)

Type	Circuit	Remarks
F		• With Analog input, General-purpose I/O port • CMOS level output I_{OH}=-1/-2 mA, I_{OL}=1/2 mA • With 50 kΩ pull-up resistor • CMOS hysteresis input (0.7Vcc/0.3Vcc) During standby, the input value retains the previous value. • Automotive input (0.8Vcc/0.5Vcc) During standby, the input value retains the previous value.
G		• With Analog output , General-purpose I/O port • CMOS level output I_{OH}=-1/-2 mA, I_{OL}=1/2 mA • With 50 kΩ pull-up resistor • CMOS hysteresis input (0.7Vcc/0.3Vcc) During standby, the input value retains the previous value. • Automotive input (0.8Vcc/0.5Vcc) During standby, the input value retains the previous value.
H		• General-purpose I/O port • CMOS level output I_{OH}=-1/-2/-4 mA, I_{OL}=1/2/4 mA • With 50 kΩ pull-up resistor • FlexRay input (0.7Vcc/0.3Vcc) During standby, the input value retains the previous value. • Automotive input (0.8Vcc/0.5Vcc) During standby, the input value retains the previous value.

Type	Circuit	Remarks
I		• CMOS level output I_{OH}=-5 mA, I_{OL}=5 mA
J		• TTL hysteresis input (2 V/0.8 V)
K		• Analog input
L		• Analog output

5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

5.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

   Therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

5.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product.
   Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 ˚C and 30 ˚C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125 ˚C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%.
   Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

5.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

6. Handling Devices

For Latch-up Prevention

If a voltage higher than VCC5 or VCC12, or a voltage lower than VSS is applied to an I/O pin, or if a voltage exceeding the ratings is applied between VCC5 to VSS and VCC12 to VSS pins, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

Also, the analog power supplies (AVCC0, AVCC1, AVCC2, AVRH0, AVRH1, AVRH2, RVCC0, RVCC1, RVRH0, RVEH1) and analog input must not exceed the digital power supply (VCC5) when the power supply to the analog system is turned on or off.

In the correct power-on sequence, turn on the digital power supply voltage (VCC5, VCC12) and analog power supply voltages (AVCC0, AVCC1, AVCC2, AVRH0, AVRH1, AVRH2, RVCC0, RVCC1, RVRH0, RVRH1) simultaneously. Alternatively, turn on the digital power supply voltage (VCC5) first, and then turn on the analog power supplies (AVCC0, AVCC1, AVCC2, AVRH0, AVRH1, AVRH2, RVCC0, RVCC1,

RVRH0, RVRH1).

Treatment of Unused Pins

If unused input pins are left open, they may cause a permanent damage to the device due to device malfunction or latch-up. Connect a 2 kΩ or higher resistor to each of unused input pins for pull-up or pull-down processing.

Also, if I/O pins are not used, they must be set to the output state for releasing or they must be set to the input state and treated in the same way as for the input pins.

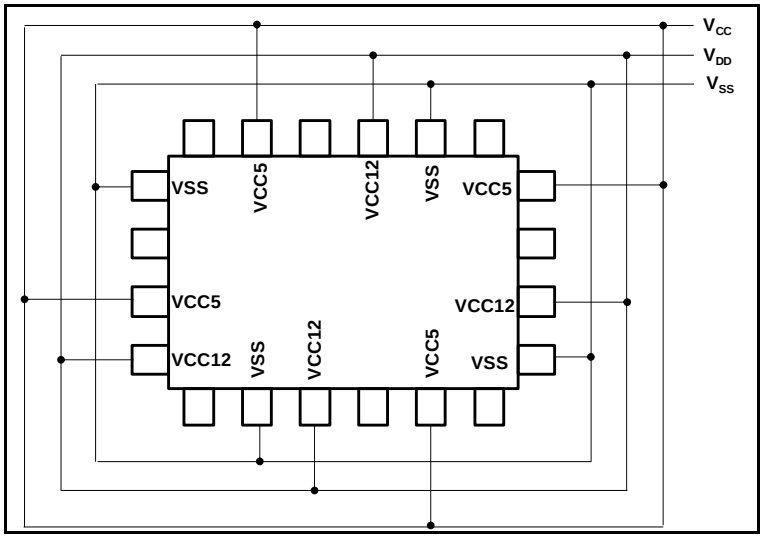
Power Supply Pins

The device is designed to ensure that if the device contains multiple VCC5, VCC12 and VSS pins, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions.

Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown below, all VSS power supply pins must be treated in the similar way. If multiple VCC5 or

VCC12 or VSS systems are connected, the device cannot operate correctly even within the guaranteed operating range.

Power Supply Input Pin



The power supply pins should be connected to VCC5, VCC12 and VSS of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between VCC5, VCC12 and VSS pins

Crystal Oscillation Circuit

An external noise to the X0 or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out X0 and X1 pins, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.

The printed circuit board artwork is recommended to surround the X0 and X1 pins by ground circuits.

Mode Pin (MD1, MD0)

Connect the MD1, MD0 mode pin to the VCC5 or VSS pin directly. To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and VCC5 or VSS pin on the printed circuit board. Also, use the low-impedance pin connection.

Notes during PLL Clock Operation

When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self oscillator circuit built in the PLL. This operation is not guaranteed.

Treatment of R/D Converter and A/D Converter Power Supply Pins

If unuse R/D converter and A/D converter, needs connection as follows.

- AVCC0 = AVCC1= AVCC2 = AVRH0= AVRH1 = AVRH2 = RVCC0 = RVCC1 = RVRH0 =RVRH1 = VCC5
- AVSS0 = AVSS1 = AVSS2 = AVRL0 = AVRL1 = AVRL2 = AVR0 = AVR1 = RVSS0 = RVSS1 = RVRL0 = RVRL1 = RVR0 = RVR1 = VSS

Note on Using External Clock

The external clock is unsupported.

External direct clock input cannot use.

Power-on Sequence of R/D Converter and A/D Converter Power Supply Analog Inputs

Be sure to turn on the digital power supply (VCC5, VCC12) first, and then turn on the R/D converter and A/D converter power supplies[*1] and analog inputs[*2]. Also, turn off the R/D converter and A/D converter power supplies[*1] and analog inputs[*2] first, and then turn off the digital power supply (VCC5, VCC12).

When the AVRH0, AVRH1, AVRH2, RVRH0 and RVRH1 pin voltages are turned on or off, they must not exceed AVCC0, AVCC1, AVCC2, RVCC0 and RVCC1. Even if a common analog input pin is used as an input port, its input voltage must not exceed AVCC0, AVCC1 or AVCC2. (However, the analog power supply voltage and digital power supply voltage can be turned on or off simultaneously.)

*1: AVCC0, AVCC1, AVCC2, AVRH0, AVRH1, AVRH2, AVRL0, AVRL1, AVRL2, RVCC0, RVCC1, RVRH0, RVRH1, RVRL0, RVRL1

*2: MAG_PLUS0, MAG_MINUS0, COS_PLUS0, COS_MINUS0, SIN_PLUS0, SIN_MINUS0, COS_IN0, SIN_IN0, MAG_PLUS1, MAG_MINUS1, COS_PLUS1, COS_MINUS1, SIN_PLUS1, SIN_MINUS1, COS_IN1, SIN_IN1, 4AN0 to 4AN7, AN0 to AN31

Notes When Writing Data in a Register Having the Status Flag

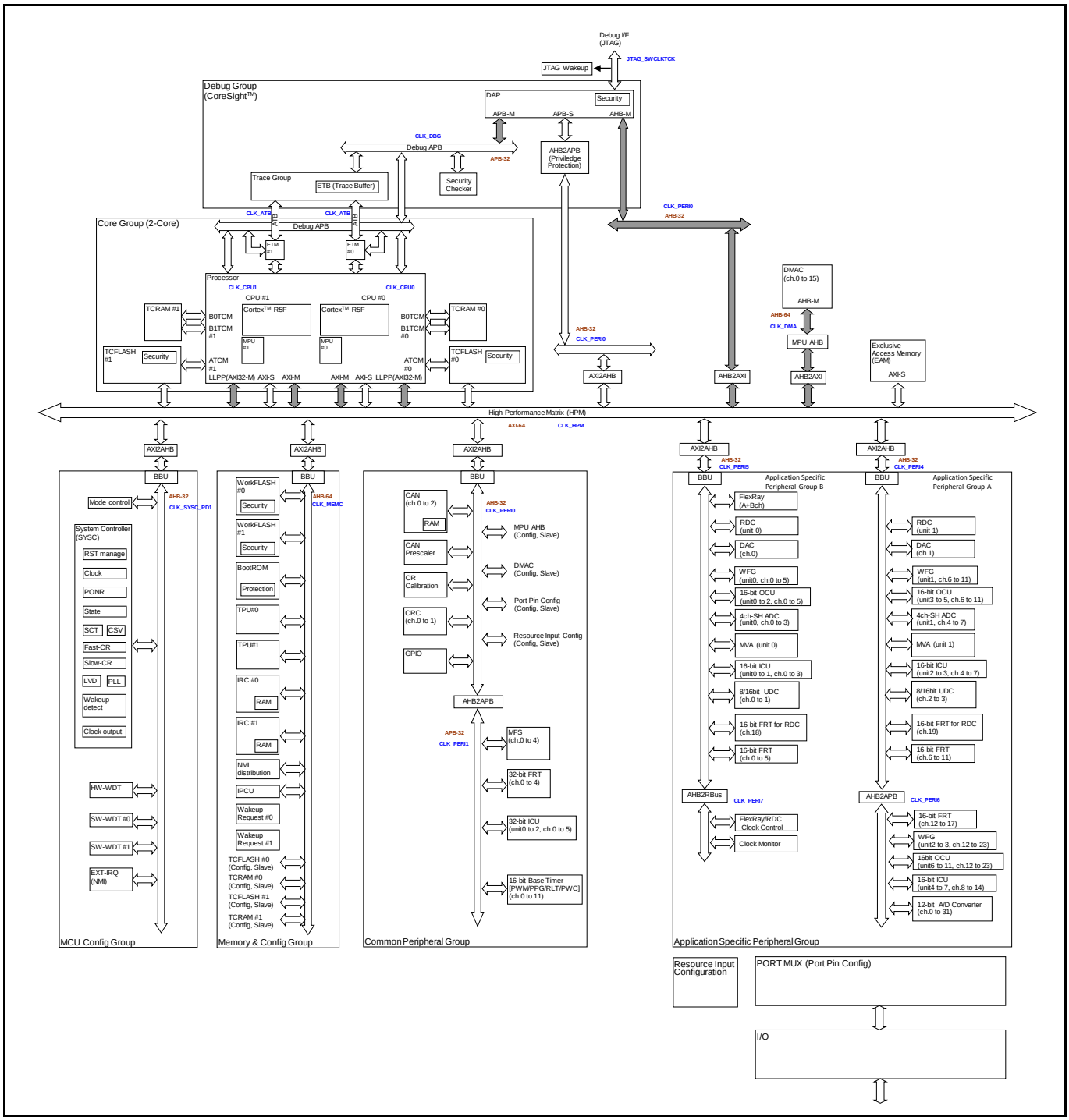
When writing data in the register that has a status flag (especially, an interrupt request flag) to control function, take care not to clear its status flag erroneously. The program must be written not to clear the flag to the status bit, and to set the control bits to have the desired value.

Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) The Byte, Half-word, or Word access must be used to write data in the control bits and status flag simultaneously. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

Note:

- These points can be ignored because the bit instructions already take the points into consideration for registers that are supported by bit-band unit. These points must be considered when using the bit instruction for registers that are not supported by bit-band unit.

7. Block Diagram



Note:

- In the block diagram, block name (Config, Slave) describe bus connection for register setting of control block.

Group

Group Name	Description
Core Group	CPU and TCM connected memory group
Debug Group	CoreSight of Debugging group
MCU Config Group	System control and supervision IP group
Memory & Config Group _	CPU related function and memory group
Common Peripheral Group	Common peripheral IP group for vehicle application
Application Specific Peripheral Group	Product specified peripheral group

Independent IP

Name	Description
HPM	Bus matrix of AXI Bus bridge (AXI-to-AHB, AHB-to-AXI)
DMAC	DMA controller
EAM	Exclusive access memory
Resource input configuration	Input selection circuit of MCU peripheral
Port MUX	Port MUX circuit
I/O	I/O circuit

Note:

- Each master connects to HPM. Each master has different transaction ID on AXI, Out-Of-Order for transaction completion.

8. Memory Map

Address		Block	
Start	End	Overview	Function
0x0000_0000	64KB: 0x0000_FFFF 96KB: 0x0001_7FFF 128KB: 0x0001_FFFF	Memory (Each CPU exclusive space)	TCRAM
0x0002_0000	0x007F_FFFF		Reserved
0x0080_0000	512KB: 0x0087_FFFF 768KB: 0x008B_FFFF 1024KB: 0x008F_FFFF		TCFLASH large sector area (TCM connection)
0x0090_0000	0x00FD_FFFF		Reserved
0x00FE_0000	0x00FF_FFFF		TCFLASH small sector area (TCM connection)
0x0100_0000	512KB: 0x0107_FFFF 768KB: 0x010B_FFFF 1024KB: 0x010F_FFFF		TCFLASH large sector area (AXI connection)
0x0110_0000	0x01FD_FFFF		Reserved
0x01FE_0000	0x01FF_FFFF		TCFLASH small sector area (AXI connection)
0x0200_0000	0x027F_FFFF	Memory (Common space)	Reserved
0x0280_0000	0x0280_0FFF		EAM
0x0280_1000	0x03FF_FFFF		Reserved
0x0400_0000	64KB: 0x0400_FFFF 96KB: 0x0401_7FFF 128KB: 0x0401_FFFF		CPU0 space TCRAM
0x0402_0000	0x047F_FFFF		Reserved
0x0480_0000	512KB: 0x0487_FFFF 768KB: 0x048B_FFFF 1024KB: 0x048F_FFFF		CPU0 space TCFLASH large sector area (TCM connection)
0x0490_0000	0x04FD_FFFF		Reserved
0x04FE_0000	0x04FF_FFFF		CPU0 space TCFLASH small sector area (TCM connection)
0x0500_0000	512KB: 0x0507_FFFF 768KB: 0x050B_FFFF 1024KB: 0x050F_FFFF		CPU0 space TCFLASH large sector area (AXI connection)
0x0510_0000	0x05FD_FFFF		Reserved
0x05FE_0000	0x05FF_FFFF		CPU0 space TCFLASH small sector area (AXI connection)
0x0600_0000	64KB: 0x0600_FFFF 96KB: 0x0601_7FFF 128KB: 0x0601_FFFF		CPU1 space TCRAM
0x0602_0000	0x067F_FFFF		Reserved
0x0680_0000	512KB: 0x0687_FFFF 768KB: 0x068B_FFFF 1024KB: 0x068F_FFFF		CPU1 space TCFLASH large sector area (TCM connection)
0x0690_0000	0x06FD_FFFF		Reserved

Address		Block	
Start	End	Overview	Function
0x06FE_0000	0x06FF_FFFF	Memory (Common space)	CPU1 space TCFLASH small sector area (TCM connection)
0x0700_0000	512KB: 0x0707_FFFF 768KB: 0x070B_FFFF 1024KB: 0x070F_FFFF		CPU1 space TCFLASH large sector area (AXI connection)
0x0710_0000	0x07FD_FFFF		Reserved
0x07FE_0000	0x07FF_FFFF		CPU1 space TCFLASH small sector area (AXI connection)
0x0800_0000	0x0DFF_FFFF		Reserved
0x0E00_0000	0x0E00_FFFF		WorkFLASH0 mirror area 1
0x0E01_0000	0x0E01_FFFF		WorkFLASH1 mirror area 1
0x0E02_0000	0x0E0F_FFFF		Reserved
0x0E10_0000	0x0E10_FFFF		WorkFLASH0 Reserved mirror area 2
0x0E11_0000	0x0E11_FFFF		WorkFLASH1 Reserved mirror area 2
0x0E12_0000	0x0E1F_FFFF		Reserved
0x0E20_0000	0x0E20_FFFF		WorkFLASH0 mirror area 3
0x0E21_0000	0x0E21_FFFF		WorkFLASH1 mirror area 3
0x0E22_0000	0x0FFF_FFFF		Reserved
0x1000_0000	0x9FFF_FFFF	Reserved	Reserved
0xA000_0000	0xA1FF_FFFF	Bit band alias area	Reserved
0xA200_0000	0xA27F_FFFF		Bit band alias area (Memory & Config Group)
0xA280_0000	0xA2FF_FFFF		Reserved
0xA300_0000	0xA37F_FFFF		Bit band alias area (MCU Config Group)
0xA380_0000	0xA47F_FFFF		Bit band alias area (Common Peripheral Group)
0xA480_0000	0xA7FF_FFFF		Reserved
0xA800_0000	0xA87F_FFFF		Bit band alias area (Application Specific Peripheral Group A)
0xA880_0000	0xA8FF_FFFF		Bit band alias area (Application Specific Peripheral Group B)
0xA900_0000	0xAFFF_FFFF		Reserved
0xB000_0000	0xBFFF_FFFF	I/O area (Bit band area)	I/O
0xC000_0000	0xEFFF_FFFF	Reserved	Reserved
0xF000_0000	0xFFFE_DFFF	BootROM area	Reserved
0xFFFE_E000	0xFFFE_FFFF		Error Config
0xFFFF_0000	0xFFFF_FFFF		BootROM

Notes:

- Each CPU exclusive space define memory space for each CPU specified. The other master cannot access (Reserved area). If the other master access to each CPU exclusive space, access from common space.
- Reserved area access cause bus error.
- However, following access of reserved area will be not bus error.
  0x0090_0000 to 0x00FD_FFFF

  0x0110_0000 to 0x01FD_FFFF

  0x0490_0000 to 0x04FD_FFFF

  0x0510_0000 to 0x05FD_FFFF

  0x0690_0000 to 0x06FD_FFFF

  0x0710_0000 to 0x07FD_FFFF

  0x1000_0000 to 0x1FFF_FFFF

  0x2000_0000 to 0x2FFF_FFFF
- The following area should be set device attribution or strongly ordered attribution as core access.
  1. I/O area

  2. Bit band alias area

  3. Error Config (BootROM area)

  4. WorkFLASH (when program)

  5. TCFLASH (when program)

  About device attribute and Strongly Ordered attribute, see "Arm®Architecture Reference Manual Arm®v7-A and Arm®v7-R edition (Arm DDI 0406B)".
- TCFLASH has a TCM-connected region and an AXI-connected region. AXI-connected region is dedicated for flash memory programming/erasing. When read operation in user mode, use TCM-connected region.

9. I/O Map

I/O Address Map (HPM, etc.)

Address		Area	
Start	End	Overview	Function
0xB000_0000	0xB03F_FFFF	Reserved	Reserved

I/O Address Map (Memory & Config Group)

Address		Area	
Start	End	Overview	Function
0xB040_0000	0xB040_0FFF	Memory & Config Group	IRC0
0xB040_1000	0xB040_1FFF		IRC1
0xB040_2000	0xB040_6FFF		Reserved
0xB040_7000	0xB040_73FF		NMI distributor
0xB040_7400	0xB040_7FFF		Reserved
0xB040_8000	0xB040_83FF		TPU0
0xB040_8400	0xB040_8FFF		Reserved
0xB040_9000	0xB040_93FF		TPU1
0xB040_9400	0xB040_FFFF		Reserved
0xB041_0000	0xB041_03FF		TCRAM0 IF
0xB041_0400	0xB041_07FF		TCRAM1 IF
0xB041_0800	0xB041_0FFF		Reserved
0xB041_1000	0xB041_13FF		TCFLASH0 IF
0xB041_1400	0xB041_17FF		TCFLASH1 IF
0xB041_1800	0xB041_1FFF		Reserved
0xB041_2000	0xB041_23FF		WorkFLASH0 IF
0xB041_2400	0xB041_27FF		WorkFLASH1 IF
0xB041_2800	0xB041_4FFF		Reserved
0xB041_5000	0xB041_5FFF		IPCU
0xB041_6000	0xB04F_FFFF		Reserved

I/O Address Map (Debug Group)

Address		Area	
Start	End	Overview	Function
0xB050_0000	0xB050_0FFF	Debug Group	DAPROM
0xB050_1000	0xB050_1FFF		ETB
0xB050_2000	0xB050_2FFF		CTI4
0xB050_3000	0xB050_3FFF		TPIU
0xB050_4000	0xB050_4FFF		TRACE_FUNNEL
0xB050_5000	0xB057_FFFF		Reserved
0xB058_0000	0xB058_0FFF		CORTEXROM0
0xB058_1000	0xB058_FFFF		Reserved
0xB059_0000	0xB059_0FFF		CORE0
0xB059_1000	0xB059_1FFF		Reserved
0xB059_2000	0xB059_2FFF		CORE1
0xB059_3000	0xB059_7FFF		Reserved
0xB059_8000	0xB059_8FFF		CTI0
0xB059_9000	0xB059_9FFF		CTI1
0xB059_A000	0xB059_BFFF		Reserved
0xB059_C000	0xB059_CFFF		ETM0
0xB059_D000	0xB059_DFFF		ETM1
0xB059_E000	0xB05F_FFFF		Reserved

I/O Address Map (MCU Config Group)

Address		Area	
Start	End	Overview	Function
0xB060_0000	0xB060_07FF	MCU Config Group	SYSC
0xB060_0800	0xB060_0FFF		MODEC
0xB060_1000	0xB060_7FFF		Reserved
0xB060_8000	0xB060_83FF		SW-WDT0
0xB060_8400	0xB060_8FFF		Reserved
0xB060_9000	0xB060_93FF		SW-WDT1
0xB060_9400	0xB060_BFFF		Reserved
0xB060_C000	0xB060_C3FF		HW-WDT
0xB060_C400	0xB061_FFFF		Reserved
0xB062_0000	0xB062_03FF		EXT-IRQ
0xB062_0400	0xB06F_FFFF		Reserved

I/O Address Map (Common Peripheral Group)

Address		Area	
Start	End	Overview	Function
0xB070_0000	0xB070_3FFF	Common Peripheral Group (AHB32)	DMAC
0xB070_4000	0xB070_FFFF		Reserved
0xB071_0000	0xB071_0FFF		MPU AHB
0xB071_1000	0xB071_7FFF		Reserved
0xB071_8000	0xB071_87FF		CRC (ch.0 to 1)
0xB071_8800	0xB071_FFFF		Reserved
0xB072_0000	0xB072_0BFF		CAN (ch.0 to 2)
0xB072_0C00	0xB072_7FFF		Reserved
0xB072_8000	0xB072_83FF		CAN prescaler
0xB072_8400	0xB072_FFFF		Reserved
0xB073_0000	0xB073_03FF		CR calibration
0xB073_0400	0xB073_7FFF		Reserved
0xB073_8000	0xB073_8FFF		GPIO
0xB073_9000	0xB073_FFFF		Reserved
0xB074_0000	0xB074_3FFF		PPC
0xB074_4000	0xB074_7FFF		Reserved
0xB074_8000	0xB074_8FFF		RIC
0xB074_9000	0xB07F_FFFF		Reserved
0xB080_0000	0xB080_13FF	Common Peripheral Group (APB)	MFS (ch.0 to 4)
0xB080_1400	0xB080_7FFF		Reserved
0xB080_8000	0xB080_AFFF		Base timer (ch.0 to 11)
0xB080_B000	0xB081_FFFF		Reserved
0xB082_0000	0xB082_13FF		32-bit FRT (ch.0 to 4)
0xB082_1400	0xB082_7FFF		Reserved
0xB082_8000	0xB080_8BFF		32-bit ICU (ch.0 to 5)
0xB082_8C00	0xB08F_FFFF		Reserved

I/O Address Map (Product Specified Peripheral Bus)

Address		Area	
Start	End	Overview	Function
0xB090_0000	0xB0FF_FFFF	Reserved	Reserved
0xB100_0000	0xB100_00FF	Application Specific Peripheral Group A (AHB-32)	16-bit FRT (ch.6 to 11)
0xB100_0100	0xB100_01FF		16-bit OCU (ch.6 to 11)
0xB100_0200	0xB100_02FF		16-bit ICU (ch.4 to 7)
0xB100_0300	0xB100_03FF		4ch-SH ADC (unit1)
0xB100_0400	0xB100_04FF		WFG (ch.6 to 11)
0xB100_0500	0xB100_05FF		UDC (ch.2 to 3)
0xB100_0600	0xB100_07FF		Reserved
0xB100_0800	0xB100_09FF		MVA (unit1)
0xB100_0A00	0xB100_0BFF		Reserved
0xB100_0C00	0xB100_0CFF		RDC (unit1)
0xB100_0D00	0xB100_0DFF		DAC (ch.1)
0xB100_0E00	0xB100_0FFF		Reserved
0xB101_0000	0xB101_00FF	Application Specific Peripheral Group A (APB)	16-bit FRT (ch.12 to 17)
0xB101_0100	0xB101_01FF		16-bit OCU (ch.12 to 23)
0xB101_0200	0xB101_02FF		16-bit ICU (ch.8 to 14)
0xB101_0300	0xB101_03FF		Reserved
0xB101_0400	0xB101_05FF		12-bit ADC (ch.0 to 31)
0xB101_0600	0xB101_06FF		WFG(ch.12 to 23)
0xB101_0700	0xB101_0FFF		Reserved
0xB101_1000	0xB101_2FFF		Other (WFG)
0xB101_3000	0xB101_3FFF		Other (ADC, CSV)
0xB101_4000	0xB1FF_FFFF	Reserved	Reserved
0xB200_0000	0xB200_00FF	Application Specific Peripheral Group B (AHB-32)	16-bit FRT (ch.0 to 5)
0xB200_0100	0xB200_01FF		16-bit OCU (ch.0 to 5)
0xB200_0200	0xB200_02FF		16-bit ICU (ch.0 to 3)
0xB200_0300	0xB200_03FF		4ch-SH ADC (unit0)
0xB200_0400	0xB200_04FF		WFG (ch.0 to 5)
0xB200_0500	0xB200_05FF		UDC (ch.0 to 1)
0xB200_0600	0xB200_07FF		Reserved
0xB200_0800	0xB200_09FF		MVA (unit0)
0xB200_0A00	0xB200_0BFF		Reserved
0xB200_0C00	0xB200_0CFF		RDC (unit0)
0xB200_0D00	0xB200_0DFF		DAC (ch.0)
0xB200_0E00	0xB200_0EFF		Reserved
0xB200_0F00	0xB200_0FFF		Reserved
0xB200_1000	0xB200_17FF		FlexRay (ch.A/ch.B)
0xB200_1800	0xB200_FFFF		Reserved
0xB201_0000	0xB201_00FF	Application Specific Peripheral Group B (R-Bus)	FlexRay/RDC clock control
0xB201_0100	0xB201_01FF		Clock monitor
0xB201_0200	0xBFFF_FFFF	Reserved	Reserved

I/O address Map (Error Config)

Address		Area	
Start	End	Overview	Function
0xFFFE_E000	0xFFFE_E3FF	Error Config	IRC0 (NMIVASBR)
0xFFFE_E400	0xFFFE_E7FF		IRC1 (NMIVASBR)
0xFFFE_E800	0xFFFE_F7FF		Reserved
0xFFFE_F800	0xFFFE_FBFF		IRC (NMIVASBR) mirror*
0xFFFE_FC00	0xFFFE_FFFF		BootROM IF

*: CPU0 is IRC0, CPU1 is IRC1 able to access this area. The master of excepted CPU is reserved area.

Notes:

- I/O address map shows maximum area for possibility. It depends on functions. The detail information, see each address map.
- It causes bus error to access to reserved area. However, following reserved area access is not generation of bus error.
  0xB018_0000 to 0xB018_03FF

  0xB05C_0000 to 0xB05C_0FFF

  0xB05E_0000 to 0xB05E_03FF

  0xB05E_0400 to 0xB05E_07FF

  0xB05E_0800 to 0xB05E_0BFF

  0xB05E_0C00 to 0xB05E_0FFF

10. Pin Statuses in CPU Status

Pin Statuses (1/2)

Pin No.	Pin Name	GPORTEN control	External reset factor*1			External reset factor*2				Internal reset factor*3		Sleep mode	Stop mode		Watch mode	
			External factor generation in progress	After external factor releasing		External factor generation in progress		After external factor releasing								
208 pin			Internal reset issuance in progress	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)	Before internal reset issuance	Internal reset issuance in progress	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)	CPU sleep	High impedance disabled (SYSC_SSPECFGR: PSSPADCTRL=0)	High impedance enabled (SYSC_SSPECFGR: PSSPADCTRL=1)	High impedance disabled (SYSC_SSPECFGR: PSSPADCTRL=0)	High impedance enabled (SYSC_SSPECFGR: PSSPADCTRL=1)
3	P305/FRCK0	With control	Hi-Z/ Input blocked			Hi-Z/ Last status retained	Hi-Z/ Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Last status retained*6	Last status retained	Hi-Z/Input blocked	Last status retained	Hi-Z/Input blocked
4	P306/FRCK1															
5	P000/DTTI0/4ADTG0															
6	P001/RTO0															
7	P002/RTO1															
8	P003/RTO2															
9	P004/RTO3															
10	P005/RTO4															
11	P006/RTO5															
14	P007/4AN0															
15	P008/4AN1															
16	P009/4AN2															
17	P010/4AN3															
23	P011/RDC_W0/ZIN0															
24	P012/RDC_V0/BIN0															
25	P013/RDC_U0/AIN0															
26	P014/RDC_Z0/ZIN1															
27	P015/RDC_B0/BIN1															
28	P016/RDC_A0/AIN1															
29	AREF20	Without control	Analog output			Analog output				Analog output		Analog output	Analog output		Analog output	
30	SIN_IN0		Analog input			Analog input				Analog input		Analog input	Analog input		Analog input	
31	COS_IN0															
32	SIN_OUT0		Analog output			Analog output				Analog output		Analog output	Analog output		Analog output	
33	SIN_MINUS0		Analog input			Analog input				Analog input		Analog input	Analog input		Analog input	
34	SIN_PLUS0															
35	COS_PLUS0															
36	COS_MINUS0															
37	COS_OUT0		Analog output			Analog output				Analog output		Analog output	Analog output		Analog output	
43	RDC_ACT0/P026		L*5	L	H/L	L*5	L*5	L	H/L	L	H/L	H/L	L		L	
44	MAG_MINUS0		Analog input			Analog input				Analog input		Analog input	Analog input		Analog input	
45	MAG_PLUS0															
46	MAG_OUT0		Analog output			Analog output				Analog output		Analog output	Analog output		Analog output	
47	P430/ERDS0	With control	Hi-Z/Input blocked			Hi-Z/Input blocked	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Last status retained*6	Last status retained	Hi-Z/Input blocked	Last status retained	Hi-Z/Input blocked
48	P030/DTTI2/FRCK12															
49	P031/RTO12/FRCK13															
50	P309/RTO13/FRCK14															
51	P310/RTO14/FRCK15															
55	P311/RTO15/FRCK16															
56	P312/RTO16/FRCK17															
57	P313/RTO17															
58	P314/DTTI3/TIOA0															
59	P315/RTO18/TIOB0															
60	P316/RTO19/TIOA1															
61	P317/RTO20/TIOB1															
62	P318/RTO21/TIOA2															
63	P319/RTO22/TIOB2															
64	P320/RTO23/TIOA3															
65	P321/SIN0/INT3/TIOB3															
66	P322/SOT0	With control *7														
67	P323/SCK0															
70	P324/STOPWT/IN6/IN16	With control														
71	P325/RXDA/IN7/IN17															
72	P326/TXDA/IN8/IN18															
73	P327/TXENA/IN9/IN19															
74	P328/RXDB/IN10/IN20															
75	P329/TXDB/IN11/IN21															
76	P330/TXENB/IN12															
77	NMIX	Without control	Input enabled			Input enabled				Input enabled		Input enabled	Input enabled		Input enabled	
78	RSTX															
79	MD1															
80	MD0															
81	X0		-			-				-		-	-		-	
82	X1															
84	TRSTX		Input enabled			Input enabled				Input enabled		Input enabled	Input enabled		Input enabled	
85	TCK															
86	TDO		-			-				-		-	-		-	
87	TDI		Input enabled			Input enabled				Input enabled		Input enabled	Input enabled		Input enabled	
88	TMS															
89	nSRST															
90	P406/SIN1/INT4	With control	Hi-Z/Input blocked			Hi-Z/Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Last status retained*6	Last status retained	Hi-Z/Input blocked*4	Last status retained	Hi-Z/Input blocked*4
91	P407/SOT1													Hi-Z/Input blocked		Hi-Z/Input blocked
92	P408/SCK1															
93	P409/RX0/INT0		Hi-Z/Input blocked			Hi-Z/Last status retained	Hi-Z/Input blocked			Hi-Z/Input blocked		Last status retained*6	Last status retained	Hi-Z/Input blocked*4		Hi-Z/Input blocked*4
94	P410/TX0													Hi-Z/Input blocked		Hi-Z/Input blocked
95	P411/RX1/INT1													Hi-Z/Input blocked*4		Hi-Z/Input blocked*4
96	P412/TX1													Hi-Z/Input blocked		Hi-Z/Input blocked
97	P413/RX2/INT2													Hi-Z/Input blocked*4		Hi-Z/Input blocked*4
98	P414/TX2		Hi-Z/Input blocked			Hi-Z/Last status retained	Hi-Z/Input blocked			Hi-Z/Input blocked		Last status retained*6	Last status retained	Hi-Z/Input blocked		Hi-Z/Input blocked
99	P415/TIOA4															
100	P416/TIOB4															
101	P417/TIOA5															
102	P418/TIOB5															
106	P419/SIN2/INT5		Hi-Z/Input blocked			Hi-Z/Last status retained	Hi-Z/Input blocked			Hi-Z/Input blocked		Last status retained*6	Last status retained	Hi-Z/Input blocked*4		Hi-Z/Input blocked*4
107	P420/SOT2													Hi-Z/Input blocked		Hi-Z/Input blocked
108	P131/SCK2															
109	P431/ERDS1															

Pin Statuses (2/2)

Pin No.	Pin Name	GPORTEN control	External reset factor *1			External reset factor *2				Internal reset factor *3		Sleep Mode	Stop mode		Watch mode	
			External factor generation in progress	After external factor releasing		External factor generation in progress		After external factor releasing								
208 pin			Internal reset issuance in progress	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)	Before internal reset issuance	Internal reset issuance in progress	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)	Internal reset issuance in progress	After internal reset issuance (Before GPORT setting)	CPU sleep	High impedance disabled (SYSC_SSPECFGR: PSSPADCTRL=0)	High impedance enabled (SYSC_SSPECFGR: PSSPADCTRL=1)	High impedance disabled (SYSC_SSPECFGR: PSSPADCTRL=0)	High impedance enabled (SYSC_SSPECFGR: PSSPADCTRL=1)
110	MAG_OUT1	-	Analog output			Analog output				Analog output		Analog output	Analog output		Analog output	
111	MAG_PLUS1		Analog input			Analog input				Analog input		Analog input	Analog input		Analog input	
112	MAG_MINUS1															
113	RDC_ACT1/P126		L *5	L	H/L	L *5	L *5	L	H/L	L	H/L	H/L	L	L	L	L
119	COS_OUT1		Analog output			Analog output				Analog output		Analog output	Analog output		Analog output	
120	COS_MINUS1															
121	COS_PLUS1		Analog input			Analog input				Analog input		Analog input	Analog input		Analog input	
122	SIN_PLUS1															
123	SIN_MINUS1															
124	SIN_OUT1		Analog output			Analog output				Analog output		Analog output	Analog output		Analog output	
125	COS_IN1		Analog input			Analog input				Analog input		Analog input	Analog input		Analog input	
126	SIN_IN1															
127	AREF21		Analog output			Analog output				Analog output		Analog output	Analog output		Analog output	
128	P116/RDC_A1/AIN3	With control	Hi-Z/Input blocked			Hi-Z/ Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Last status retained *6	Last status retained	Hi-Z/Input blocked	Last status retained	Hi-Z/Input blocked
129	P115/RDC_B1/BIN3															
130	P114/RDC_Z1/ZIN3															
131	P113/RDC_U1/AIN2															
132	P112/RDC_V1/BIN2															
133	P111/RDC_W1/ZIN2															
139	P110/4AN7															
140	P109/4AN6															
141	P108/4AN5															
142	P107/4AN4															
145	P106/RTO11															
146	P105/RTO10															
147	P104/RTO9															
148	P103/RTO8															
149	P102/RTO7															
150	P101/RTO6															
151	P100/DTTI1/4ADTG1															
152	P421/SIN3/INT6/FRCK8		Hi-Z/Input blocked			Hi-Z/ Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Last status retained *6	Last status retained	Hi-Z/Input blocked *4	Last status retained	Hi-Z/Input blocked *4
153	P422/SOT3/FRCK9/IN13															
154	P423/SCK3/FRCK10/IN14															
158	P425/TIOA8		Hi-Z/Input blocked			Hi-Z/ Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Last status retained *6	Last status retained	Hi-Z/Input blocked	Last status retained	Hi-Z/Input blocked
159	P426/TIOB8															
160	P427/TIOA9															
161	P428/TIOB9															
162	P429/MONCLK/MM		Hi-Z/Input blocked			Hi-Z/ Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Last status retained *6	Last status retained *8	Hi-Z/Input blocked	Last status retained *8	Hi-Z/Input blocked
163	AN0/P200		Hi-Z/Input blocked			Hi-Z/Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Last status retained *6	Last status retained	Hi-Z/Input blocked	Last status retained	Hi-Z/Input blocked
164	AN1/P201															
165	AN2/P202															
166	AN3/P203															
167	AN4/P204															
168	AN5/P205															
169	AN6/P206															
170	AN7/P207															
173	AN8/P208															
174	AN9/P209															
175	AN10/P210															
176	AN11/P211															
177	AN12/P212															
178	AN13/P213															
179	AN14/P214															
180	AN15/P215															
185	AN16/P216															
186	AN17/P217															
187	AN18/P218															
188	AN19/P219															
189	AN20/P220/TIOA6															
190	AN21/P221/TIOB6															
191	AN22/P222/TIOA7															
192	AN23/P223/TIOB7															
195	AN24/P224															
196	AN25/P225/SIN4/INT7		Hi-Z/Input blocked			Hi-Z/Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Last status retained *6	Last status retained	Hi-Z/Input blocked *4	Last status retained	Hi-Z/Input blocked *4
197	AN26/P226/SOT4/IN0		Hi-Z/Input blocked			Hi-Z/Last status retained	Hi-Z/Input blocked	Hi-Z/Input blocked		Hi-Z/Input blocked		Last status retained *6	Last status retained	Hi-Z/Input blocked	Last status retained	Hi-Z/Input blocked
198	AN27/P227/SCK4/IN1															
199	AN28/P228/SCS40/IN2															
200	AN29/P229/SCS41/IN3															
201	AN30/P230/SCS42/IN4															
202	AN31/P231/SCS43/IN5															
203	P300/ADTG0															
204	P301/TIOA10/FRCK4															
205	P302/TIOB10/FRCK5															
206	P303/TIOA11/FRCK6															
207	P304/TIOB11/FRCK7															

*1: Power-on reset, internal power supply low-voltage detection and NMIX + RSTX pin are factors.
*2: External power supply low-voltage detection and external reset are factors.
*3: Software reset and software/hardware watchdog reset are factors.
*4: When external interrupt is valid, input blocked is invalid.
*5: When I/O is initialized, "L" is output.
*6: Operation is continued according to the peripheral function.
*7: If GPORTEN bit is 0 and CPORTEN bit is 1, input is enabled.
*8: When clock monitor output pin (MONCLK) is selected, pin state becomes high impedance.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	
Analog power supply voltage*1, *2	V_{DD}	V_{SS}-0.3	V_{SS}+1.8	V	
Analog reference voltage*1	AV_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	$AV_{CC} \leq V_{CC}$
Input voltage*1	RV_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	$RV_{CC} \leq V_{CC}$
Analog pin input voltage*1	AVRH	V_{SS}-0.3	V_{SS}+6.0	V	$AVRH \leq AV_{CC}$
	RVRH	V_{SS}-0.3	V_{SS}+6.0	V	$RVRH \leq RV_{CC}$
Input voltage*1	V_I	V_{SS}-0.3	V_{CC}+0.3	V	
Analog pin input voltage*1	V_{IA}	V_{SS}-0.3	V_{CC}+0.3	V	
Output voltage*1	V_O	V_{SS}-0.3	V_{CC}+0.3	V	
Max clamp current	I_{CLAMP}	-	4	mA	*8
Max total clamp current	$\Sigma\|I_{CLAMP}\|$	-	20	mA	*8
"L" level Max output current*3	I_{OL1}	-	3.5	mA	When setting to 1 mA*6
	I_{OL2}	-	7	mA	When setting to 2 mA
	I_{OL3}	-	14	mA	When setting to 4 mA*7
"L" level average output current*4	I_{OLAV1}	-	1	mA	When setting to 1 mA*6
	I_{OLAV2}	-	2	mA	When setting to 2 mA
	I_{OLAV3}	-	4	mA	When setting to 4 mA*7
"L" level total output current*5	ΣI_{OL}	-	40	mA	*6
"H" level Max output current*3	I_{OH1}	-	-3.5	mA	When setting to 1 mA*6
	I_{OH2}	-	-7	mA	When setting to 2 mA
	I_{OH3}	-	-14	mA	When setting to 4 mA*7
"H" level average output current*4	I_{OHAV1}	-	-1	mA	When setting to1 mA*6
	I_{OHAV2}	-	-2	mA	When setting to 2 mA
	I_{OHAV3}	-	-4	mA	When setting to 4 mA*7
"H" level total output current*5	ΣI_{OH}	-	-40	mA	*6
Power consumption	P_D	-	1500	mW	
Operating temperature	T_A	-40	+125	°C	*9
Storage temperature	T_{stg}	-55	+150	°C	

*1: These parameters are based on the condition that V_{SS}=AV_{SS}=0.0 V.

*2: Caution must be taken that AV_{CC} does not exceed V_{CC}.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

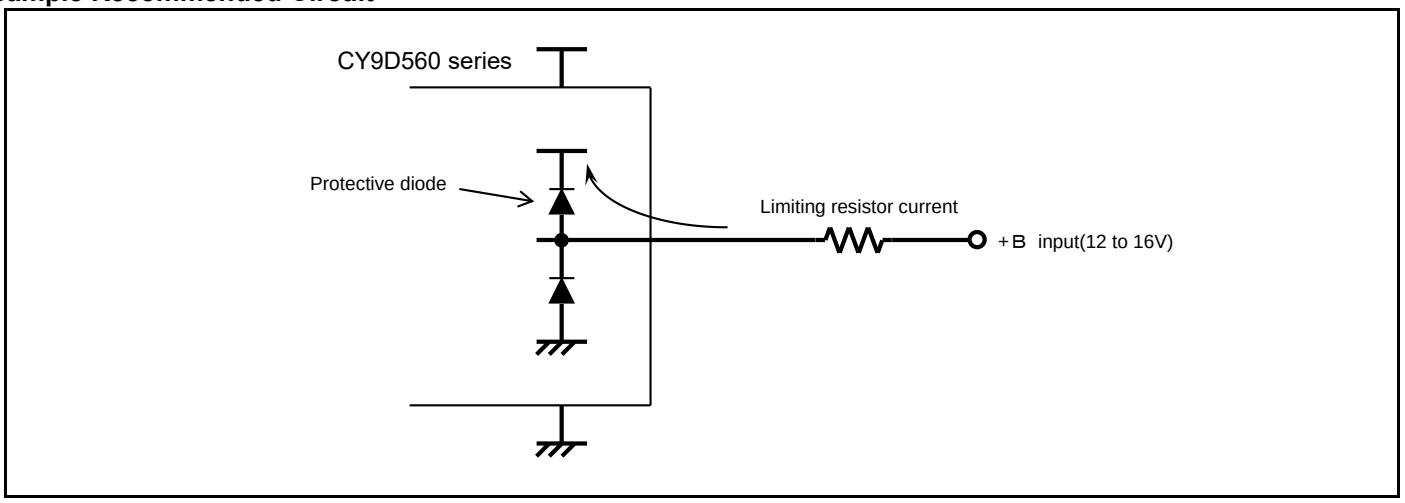
*6: Corresponding pins: general-purpose ports

*7: Corresponding pins: general-purpose ports of P325 to P330

*8: Corresponding pins: all general-purpose ports and analog input pin

- Use the devices within recommended operating conditions.
- Use the devices with direct voltage (current).
- The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
- Note that when the microcontroller drive current is low, such as in the low-power consumption modes, the + B input potential can increase the potential at the VCC pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

Sample Recommended Circuit



*9: To use this product at T_A = 125°C, equip this on a multilayer board with four or more layers.

To equip this on a single-layer board, change the operating conditions (operating frequency, power supply voltage, etc.) to use this at the power consumption P_D = 780 mW or lower, or use this at T_A = 100°C or lower.

Warning:

- Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

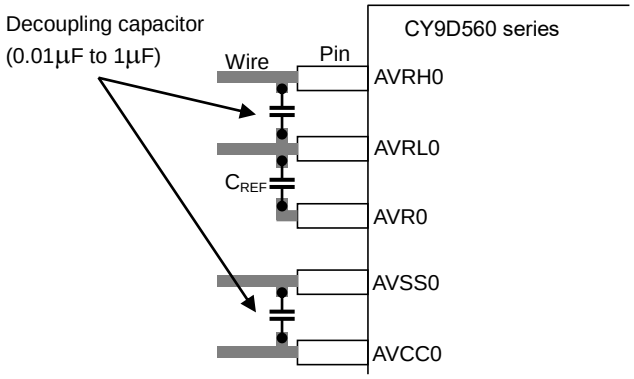
11.2 Recommended Operating Conditions

(V_{SS} = AV_{SS}-RV_{SS} = 0.0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	4.5	5.5	V	Recommended operation guarantee range
	V_{DD}	1.1	1.3	V	
	AV_{CC}	4.5	5.5	V	
	RV_{CC}	4.5	5.5	V	
	V_{CC}	3.7	5.5	V	Operation guarantee range
	V_{DD}	1.09	1.3	V	
	AV_{CC}	3.7	5.5	V	
	RV_{CC}	3.7	5.5	V	
Smoothing capacitor*	C_{REF}	0.33	1.0	µF	Tolerance within ±40%
Operating temperature	T_A	-40	+125	°C	

*: For connection of smoothing capacitor C_{REF}, see the figure below.

C_{REF} pin connection



It should be used smoothing capacitor for between AVR1 to AVRL1, RVR0 to RVRL0, RVR1 to RVRL1 as well.

C_{REF} capacitor size and A/D converter activation time

It depends on activation time of A/D converter with R/D converter and activation time of 4 channels same time sampling A/D converter by C_{REF} capacitor seize. The computation expression of activation time is as follows.

Activation time = 9 × C_{REF} × 1.2k + 1µ [s]

Activation time relate with following time from activation trigger, please use smoothing capacitor with system operation conditions.

If A/D converter of 4 channels same time sampling,

Set to "1" for ENBL bit of A/D enable setting register.

If A/D converter with R/D converter,

Set to "1" for RDCEN bit of operation control register 1.

Warning:

- The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
- Any use of semiconductor devices will be under their recommended operating condition.
- Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
- No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

11.3 DC Characteristics

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P000 to P016, P026, P030 to P031, P100 to P116, P126, P131, P200 to P231, P300 toP306, P309 to P324, P406 to P423, P425 to P431	When CMOS schmitt input level is selected	0.7×V_{CC}	-	Vcc+0.3	V	
	V_{IH2}	P000 to P016, P026, P030 to P031, P100 to P116, P126, P131, P200 to P231, P300 to P306, P309 to P330, P406 to P423, P425 to P431	When automotive input level is selected	0.8×V_{CC}	-	Vcc+0.3	V	
	V_{IH3}	P325 to P330	When FlexRay input level is selected	0.7×V_{CC}	-	Vcc+0.3	V	
	V_{IH4}	RSTX, NMIX	-	0.7×V_{CC}	-	Vcc+0.3	V	
	V_{IH5}	MD0, MD1	-	0.7×V_{CC}	-	Vcc+0.3	V	
	V_{IH6}	TRSTX, TCK, TDI, TMS, nSRST	-	2.3	-	Vcc+0.3	V	

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level input voltage	V_{IL1}	P000 to P016, P026, P030 to P031, P100 to P116, P126, P131, P200 to P231, P300 toP306, P309 to P324, P406 to P423, P425 to P431	When CMOS schmitt input level is selected	V_{SS}-0.3	-	0.3×V_{CC}	V	
	V_{IL2}	P000 to P016, P026, P030 to P031, P100 to P116, P126, P131, P200 to P231, P300 to P306, P309 to P330, P406 to P423, P425 to P431	When automotive input level is selected	V_{SS}-0.3	-	0.5×V_{CC}	V	
	V_{IL3}	P325 to P330	When FlexRay input level is selected	V_{SS}-0.3	-	0.3×V_{CC}	V	
	V_{IL4}	RSTX, NMIX	-	V_{SS}-0.3	-	0.3×V_{CC}	V	
	V_{IL5}	MD0, MD1	-	V_{SS}-0.3	-	0.3×V_{CC}	V	
	V_{IL6}	TRSTX, TCK, TDI, TMS, nSRST	-	V_{SS}-0.3	-	0.8	V	

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH1}	P000 to P016, P026, P030 to P031, P100 to P116, P126, P131, P200 to P231, P300 toP306, P309 to P330, P406 to P423, P425 to P431	V_{CC} = 4.5V I_{OH} = -2.0mA	V_{CC}-0.5	-	V_{CC}	V	
	V_{OH2}	P325 to P330	V_{CC} = 4.5V I_{OH} = -4.0mA	V_{CC}-0.5	-	V_{CC}	V	When FlexRay selected
	V_{OH3}	P000 to P016, P026, P030 to P031, P100 to P116, P126, P131, P200 to P231, P300 toP306, P309 to P330, P406 to P423, P425 to P431	V_{CC} = 4.5V I_{OH} = -1.0mA	V_{CC}-0.5	-	V_{CC}	V	
	V_{OH4}	TDO	V_{CC} = 4.5V I_{OH} = -5mA	V_{CC}-0.5	-	V_{CC}	V	

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL1}	P000 to P016, P026, P030 to P031, P100 to P116, P126, P131, P200 to P231, P300 toP306, P309 to P330, P406 to P423, P425 to P431	V_{CC} = 4.5V I_{OL} = 2.0mA	0	-	0.4	V	
	V_{OL2}	P325 to P330	V_{CC} = 4.5V I_{OL} = 4.0mA	0	-	0.4	V	When FlexRay selected
	V_{OL3}	P000 to P016, P026, P030 to P031, P100 to P116, P126, P131, P200 to P231, P300 toP306, P309 to P330, P406 to P423, P425 to P431	V_{CC} = 4.5V I_{OL}=1.0mA	0	-	0.4	V	
	V_{OL4}	TDO	V_{CC} = 4.5V I_{OL} = 5mA	0	-	0.4	V	

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current	I_{IL}	All input pin	V_{CC} = AV_{CC} = RV_{CC} = 5.5V V_{SS} < V_I < V_{CC}	-5	-	+5	µA	
Pull-up resistance	R_{UP1}	RSTX, NMIX	-	25	-	100	kΩ	
	R_{UP2}	P000 to P016, P026, P030 to P031, P100 to P116, P126, P131, P200 to P231, P300 to P306, P309 to P330, P406 to P423, P425 to P431	When pull-up resistance is selected	25	-	100	kΩ	
Input capacitor	C_{IN}	Other than VCC, VSS, AVCC, AVSS, RVCC, RVSS	-	-	5	15	pF	

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CC5}	VCC5	Normal operations 200 MHz	-	104	115	mA	F_{CD0_CLK} = 200 MHz F_{CLK_CPUx} = 200 MHz, F_{CLK_TFCLKx} = 66 MHz, F_{CLK_HPMPD2} = 200 MHz, F_{CLK_DMA} = 200 MHz, F_{CLK_MEMC} = 100 MHz, F_{CLK_WFCLKx} = 200 MHz, $F_{CLK\_SYSCPD1}$ = 100 MHz, F_{CLK_PERIy} = 100 MHz, F_{CLK_PERIz} = 50 MHz x = 0, 1 y = 0, 4, 5 z = 1, 6, 7
			Normal operations 160 MHz	-	105	116	mA	F_{CD0_CLK} = 160 MHz F_{CLK_CPUx} = 160 MHz, F_{CLK_TFCLKx} = 80 MHz, F_{CLK_HPMPD2} = 160 MHz, F_{CLK_DMA} = 160 MHz, F_{CLK_MEMC} = 80 MHz, F_{CLK_WFCLKx} = 160 MHz, $F_{CLK\_SYSCPD1}$ = 80 MHz, F_{CLK_PERIy} = 80 MHz, F_{CLK_PERIz} = 40 MHz x = 0, 1 y = 0, 4, 5 z = 1, 6, 7
			Flash write/erase* 200 MHz	-	115	126	mA	F_{CD0_CLK} = 200 MHz F_{CLK_CPUx} = 200 MHz, F_{CLK_TFCLKx} = 66 MHz, F_{CLK_HPMPD2} = 200 MHz, F_{CLK_DMA} = 200 MHz, F_{CLK_MEMC} = 100 MHz, F_{CLK_WFCLKx} = 200 MHz, $F_{CLK\_SYSCPD1}$ = 100 MHz, F_{CLK_PERIy} = 100 MHz, F_{CLK_PERIz} = 50 MHz x = 0, 1 y = 0, 4, 5 z = 1, 6, 7
			Flash write/erase* 160 MHz	-	116	127	mA	F_{CD0_CLK} = 160 MHz F_{CLK_CPUx} = 160 MHz, F_{CLK_TFCLKx} = 80 MHz, F_{CLK_HPMPD2} = 160 MHz, F_{CLK_DMA} = 160 MHz, F_{CLK_MEMC} = 80 MHz, F_{CLK_WFCLKx} = 160 MHz, $F_{CLK\_SYSCPD1}$ = 80 MHz, F_{CLK_PERIy} = 80 MHz, F_{CLK_PERIz} = 40 MHz x = 0, 1 y = 0, 4, 5 z = 1, 6, 7

*: This series has 2 types of flash; TCFLASH (4) and WorkFLASH (2); however, this is the specification when only one of those is written/erased.

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CC12}	VCC12	Normal operations 200 MHz	-	310	510	mA	F_{CD0_CLK} = 200 MHz F_{CLK_CPUx} = 200 MHz, F_{CLK_TFCLKx} = 66 MHz, F_{CLK_HPMPD2} = 200 MHz, F_{CLK_DMA} = 200 MHz, F_{CLK_MEMC} = 100 MHz, F_{CLK_WFCLKx} = 200 MHz, $F_{CLK\_SYSCPD1}$ = 100 MHz, F_{CLK_PERIy} = 100 MHz, F_{CLK_PERIz} = 50 MHz x = 0, 1 y = 0, 4, 5 z = 1, 6, 7
			Normal operations 160 MHz	-	290	490	mA	F_{CD0_CLK} = 160 MHz F_{CLK_CPUx} = 160 MHz, F_{CLK_TFCLKx} = 80 MHz, F_{CLK_HPMPD2} = 160 MHz, F_{CLK_DMA} = 160 MHz, F_{CLK_MEMC} = 80 MHz, F_{CLK_WFCLKx} = 160 MHz, $F_{CLK\_SYSCPD1}$ = 80 MHz, F_{CLK_PERIy} = 80 MHz, F_{CLK_PERIz} = 40 MHz x = 0, 1 y = 0, 4, 5 z = 1, 6, 7
			Flash write/erase* 200 MHz	-	312	512	mA	F_{CD0_CLK} = 200 MHz F_{CLK_CPUx} = 200 MHz, F_{CLK_TFCLKx} = 66 MHz, F_{CLK_HPMPD2} = 200 MHz, F_{CLK_DMA} = 200 MHz, F_{CLK_MEMC} = 100 MHz, F_{CLK_WFCLKx} = 200 MHz, $F_{CLK\_SYSCPD1}$ = 100 MHz, F_{CLK_PERIy} = 100 MHz, F_{CLK_PERIz} = 50 MHz x = 0, 1 y = 0, 4, 5 z = 1, 6, 7
			Flash write/erase* 160 MHz	-	292	492	mA	F_{CD0_CLK} = 160 MHz F_{CLK_CPUx} = 160 MHz, F_{CLK_TFCLKx} = 80 MHz, F_{CLK_HPMPD2} = 160 MHz, F_{CLK_DMA} = 160 MHz, F_{CLK_MEMC} = 80 MHz, F_{CLK_WFCLKx} = 160 MHz, $F_{CLK\_SYSCPD1}$ = 80 MHz, F_{CLK_PERIy} = 80 MHz, F_{CLK_PERIz} = 40 MHz x = 0, 1 y = 0, 4, 5 z = 1, 6, 7

*: This series has 2 types of flash; TCFLASH (4) and WorkFlash (2); however, this is the specification when only one of those is written/erased.

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RVSS = 0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCS5}	VCC5	CPU sleep mode 200 MHz	-	40	42	mA	F_{CD0_CLK} = 200 MHz F_{CLK_CPUx} = 200 MHz, F_{CLK_TFCLKx} = 66 MHz, F_{CLK_HPMPD2} = 200 MHz, F_{CLK_DMA} = 200 MHz, F_{CLK_MEMC} = 100 MHz, F_{CLK_WFCLKx} = 200 MHz, $F_{CLK\_SYSCPD1}$ = 100 MHz, F_{CLK_PERIy} = 100 MHz, F_{CLK_PERIz} = 50 MHz x = 0, 1 y = 0, 4, 5 z = 1, 6, 7
			CPU sleep mode 160 MHz	-	30	32	mA	F_{CD0_CLK} = 160 MHz F_{CLK_CPUx} = 160 MHz, F_{CLK_TFCLKx} = 80 MHz, F_{CLK_HPMPD2} = 160 MHz, F_{CLK_DMA} = 160 MHz, F_{CLK_MEMC} = 80 MHz, F_{CLK_WFCLKx} = 160 MHz, $F_{CLK\_SYSCPD1}$ = 80 MHz, F_{CLK_PERIy} = 80 MHz, F_{CLK_PERIz} = 40 MHz x = 0, 1 y = 0, 4, 5 z = 1, 6, 7
	I_{CCT5}		Watch mode, 4 MHz source oscillation	-	390	1030	µA	When using crystal T_A = 25°C
	I_{CCH5}		Stop mode	-	380	1010	µA	T_A = 25°C

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AVSS = RVSS = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCS12}	VCC12	CPU sleep mode 200 MHz	-	220	410	mA	F_{CD0_CLK} = 200 MHz F_{CLK_CPUx} = 200 MHz, F_{CLK_TFCLKx} = 66 MHz, F_{CLK_HPMPD2} = 200 MHz, F_{CLK_DMA} = 200 MHz, F_{CLK_MEMC} = 100 MHz, F_{CLK_WFCLKx} = 200 MHz, $F_{CLK\_SYSCPD1}$ = 100 MHz, F_{CLK_PERIy} = 100 MHz, F_{CLK_PERIz} = 50 MHz x = 0, 1 y = 0, 4, 5 z = 1, 6, 7
			CPU sleep mode 160 MHz	-	180	360	mA	F_{CD0_CLK} = 160 MHz F_{CLK_CPUx} = 160 MHz, F_{CLK_TFCLKx} = 80 MHz, F_{CLK_HPMPD2} = 160 MHz, F_{CLK_DMA} = 160 MHz, F_{CLK_MEMC} = 80 MHz, F_{CLK_WFCLKx} = 160 MHz, $F_{CLK\_SYSCPD1}$ = 80 MHz, F_{CLK_PERIy} = 80 MHz, F_{CLK_PERIz} = 40 MHz x = 0, 1 y = 0, 4, 5 z = 1, 6, 7
	I_{CCT12}		Watch mode, 4 MHz source oscillation	-	1280	9730	µA	When using crystal T_A = 25°C
	I_{CCH12}		Stop mode	-	860	9530	µA	T_A = 25°C

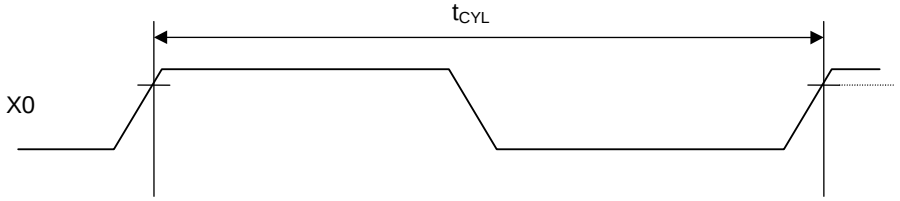
11.4 AC Characteristics

11.4.1 Source Clock Timing

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

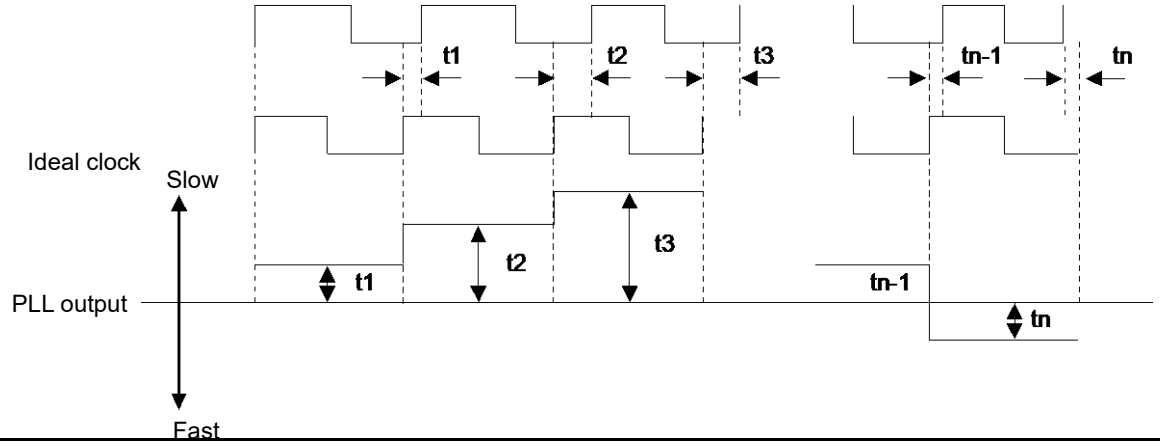
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1	-	4	-	20	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1	-	50	-	250	ns	
CAN PLL jitter (during lock)	t_{PJ}	-	-	-10	-	+10	ns	
Built-in slow-CR oscillation frequency	F_{CRS}	-	-	50	100	150	kHz	
Built-in fast-CR oscillation frequency	F_{CRF}	-	-	4	8	12	MHz	Without calibration
				7.2	8	8.8	MHz	With calibration

X0, X1 Clock Timing



CAN PLL Jitter

Deviation time from the ideal clock is assured per cycle out of 20,000 cycles.

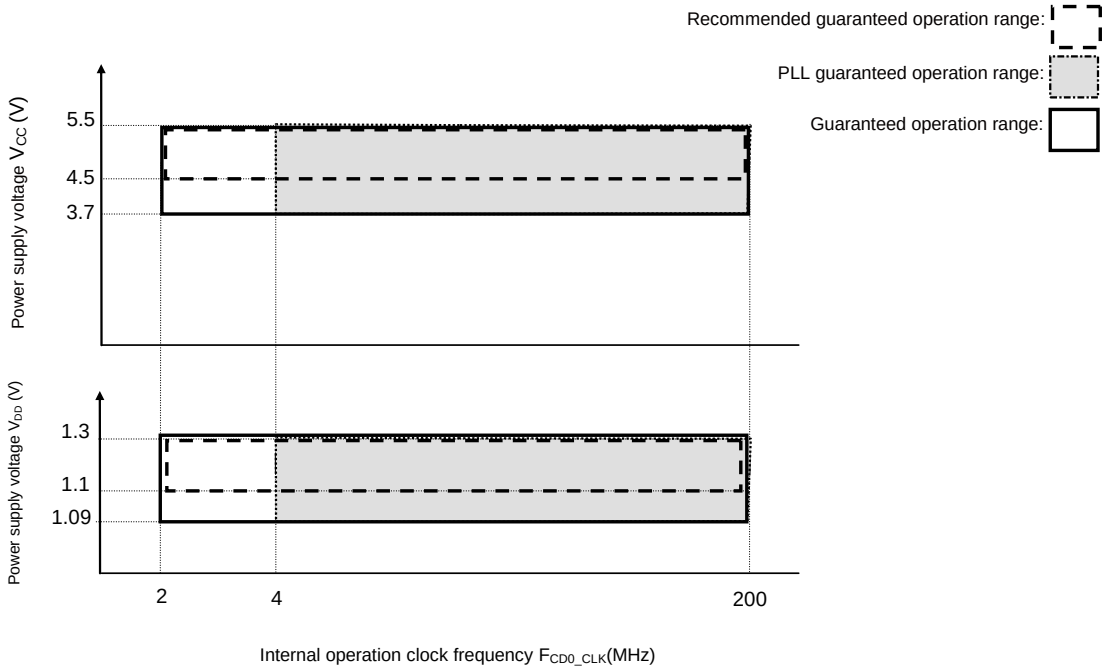


11.4.2 Internal Clock Timing

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Internal clock frequency	F_{CD0_CLK}	-	-	0	-	200	MHz	CD0_CLK
	F_{CD4_CLK}	-	-	0	-	200	MHz	CD4_CLK
	F_{CLK_CPU0}	-	-	0	-	200	MHz	CLK_CPU0
	F_{CLK_CPU1}	-	-	0	-	200	MHz	CLK_CPU1
	F_{CLK_TFCLK0}	-	-	0	-	80	MHz	CLK_TFCLK0
	F_{CLK_TFCLK1}	-	-	0	-	80	MHz	CLK_TFCLK1
	F_{CLK_ATB}	-	-	0	-	100	MHz	CLK_ATB
	F_{CLK_DBG}	-	-	0	-	50	MHz	CLK_DBG
	F_{CLK_HPMPD2}	-	-	0	-	200	MHz	CLK_HPMPD2
	F_{CLK_DMA}	-	-	0	-	200	MHz	CLK_DMA
	F_{CLK_MEMC}	-	-	0	-	200	MHz	CLK_MEMC
	F_{CLK_WFCLK0}	-	-	0	-	80	MHz	CLK_WFCLK0
	F_{CLK_WFCLK1}	-	-	0	-	80	MHz	CLK_WFCLK1
	$F_{CLK\_SYSCPD1}$	-	-	0	-	100	MHz	CLK_SYSCPD1
	F_{CLK_PERI0}	-	-	0	-	100	MHz	CLK_PERI0
	F_{CLK_PERI1}	-	-	0	-	50	MHz	CLK_PERI1
	F_{CLK_PERI4}	-	-	0	-	100	MHz	CLK_PERI4
	F_{CLK_PERI5}	-	-	0	-	100	MHz	CLK_PERI5
	F_{CLK_PERI6}	-	-	0	-	50	MHz	CLK_PERI6
	F_{CLK_PERI7}	-	-	0	-	50	MHz	CLK_PERI7
	F_{CLK_CLKO}	-	-	0	-	200	MHz	CLK_CLKO
Internal clock cycle time	t_{CD0_CLK}	-	-	5	-	-	ns	CD0_CLK
	t_{CD4_CLK}	-	-	5	-	-	ns	CD4_CLK
	t_{CLK_CPU0}	-	-	5	-	-	ns	CLK_CPU0
	t_{CLK_CPU1}	-	-	5	-	-	ns	CLK_CPU1
	t_{CLK_TFCLK0}	-	-	12.5	-	-	ns	CLK_TFCLK0
	t_{CLK_TFCLK1}	-	-	12.5	-	-	ns	CLK_TFCLK1
	t_{CLK_ATB}	-	-	10	-	-	ns	CLK_ATB
	t_{CLK_DBG}	-	-	20	-	-	ns	CLK_DBG
	t_{CLK_HPMPD2}	-	-	5	-	-	ns	CLK_HPMPD2
	t_{CLK_DMA}	-	-	5	-	-	ns	CLK_DMA
	t_{CLK_MEMC}	-	-	5	-	-	ns	CLK_MEMC
	t_{CLK_WFCLK0}	-	-	12.5	-	-	ns	CLK_WFCLK0
	t_{CLK_WFCLK1}	-	-	12.5	-	-	ns	CLK_WFCLK1
	$t_{CLK\_SYSCPD1}$	-	-	10	-	-	ns	CLK_SYSCPD1
	t_{CLK_PERI0}	-	-	10	-	-	ns	CLK_PERI0
	t_{CLK_PERI1}	-	-	20	-	-	ns	CLK_PERI1
	t_{CLK_PERI4}	-	-	10	-	-	ns	CLK_PERI4
	t_{CLK_PERI5}	-	-	10	-	-	ns	CLK_PERI5
	t_{CLK_PERI6}	-	-	20	-	-	ns	CLK_PERI6
	t_{CLK_PERI7}	-	-	20	-	-	ns	CLK_PERI7
	t_{CLK_CLKO}	-	-	5	-	-	ns	CLK_CLKO

Guaranteed Operation Range Internal Operation Clock Frequency vs. Power Supply Voltage

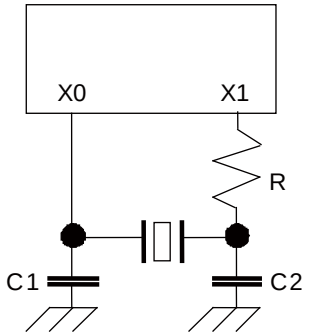


Note: The CPU will be reset at the power supply voltage of the low-voltage detection setting voltage or less.

Oscillation Clock Frequency vs. Internal Operation Clock Frequency

Oscillation Clock Frequency	Main Clock	PLL Multiplying Setting	PLL Output Divider Setting	PLL Clock
4 MHz	4 MHz	100	2	200 MHz
8 MHz	8 MHz	50	2	200 MHz
8 MHz	4 MHz	100	2	200 MHz
16 MHz	16 MHz	25	2	200 MHz
16 MHz	8 MHz	50	2	200 MHz

Example of Oscillation Circuit

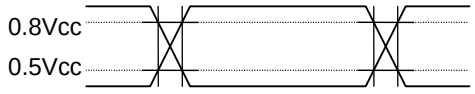


Note: when configuring the oscillator circuit, it is recommended to ask matching evaluation of the circuit to oscillator manufacturers for the design.

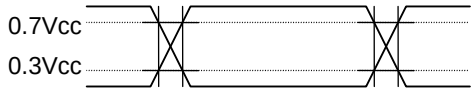
AC characteristics are specified by the following measurement reference voltage values.

Input Signal Waveform

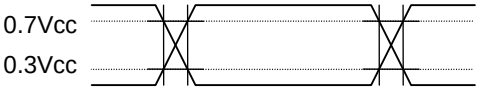
Hysteresis input pin (Automotive)



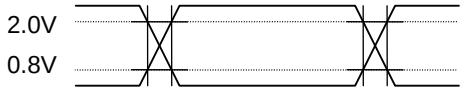
Hysteresis input pin (CMOS schmitt)



Hysteresis input pin (FlexRay)

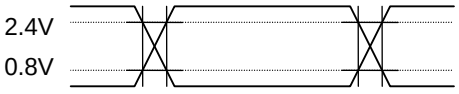


Hysteresis input pin (TTL)



Output Signal Waveform

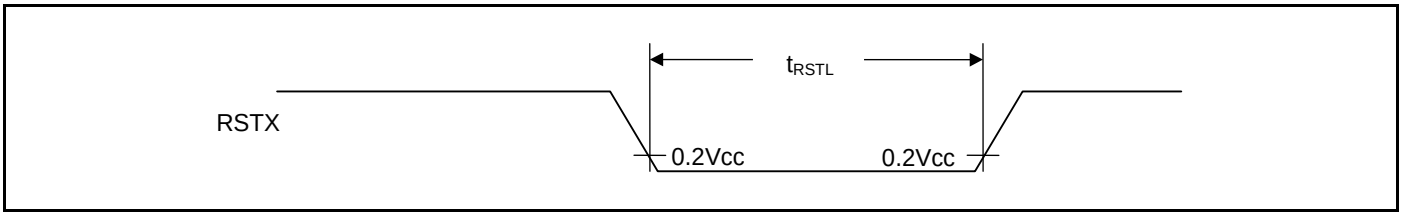
Output pin



11.4.3 Reset Input

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	-	10	-	µs	
Width for reset input removal				1	-	µs	



11.4.4 Power-on Conditions

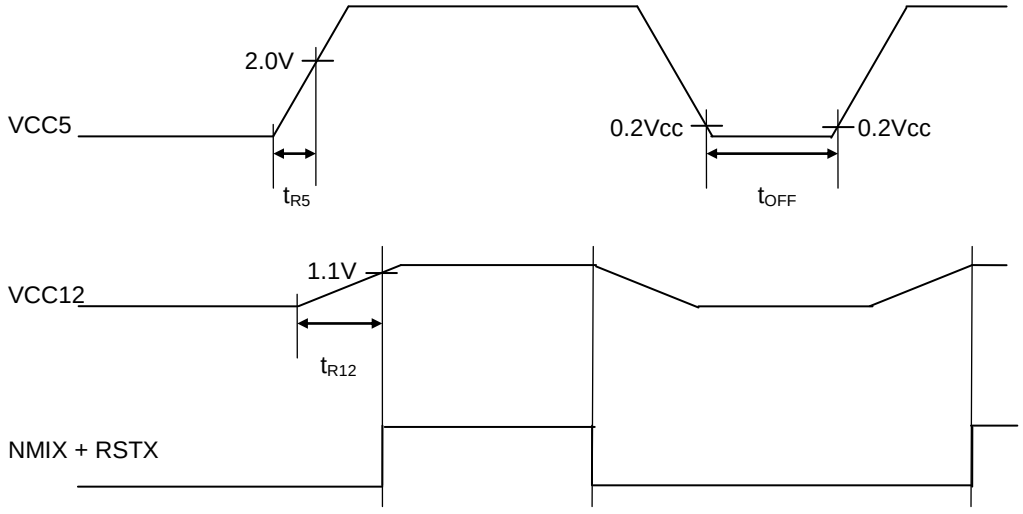
(T_A: Recommended operating conditions, V_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	-	VCC5	-	2.0	2.2	2.4	V	When turning on power
	-	VCC12	-	0.4	-	0.7	V	
Level detection hysteresis width	-	VCC5	-	-	-	150	mV	During voltage drop
	-	VCC12	-	-	-	50	mV	
Level detection time	-	-	-	-	-	30	µs	*1
Power-on time	t_{R5}	VCC5	-	0.11	-	30	ms	
	t_{R12}	VCC12	-	0.05	-	0.6	ms	
Power-off time	t_{OFF}	VCC5	-	1	-	-	ms	*2

*1: If the fluctuation of the power supply is faster than the low-voltage detection time, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: This time is to start the slope detection at next power on after power down and internal charge loss.

Power-on , Power-off Sequence



Notes:

- Power supply input procedure
  Power supply should input same time VCC5 and VCC12, or VCC5 to up step.
  Also, when power supply input, VCC12 is not over voltage of VCC5.
- Power supply shutdown procedure
  Power supply should shutdown same time VCC5 and VCC12, or VCC12 to up step.
  Also, when power supply shutdown, VCC12 is not over voltage of VCC5.
- Notes: When power supply input and power supply shutdown
  When power supply input, power supply voltage until achieve to recommend operation guarantee area, same time input for NMIX pin + RSTX pin.
  When power supply shutdown, power supply voltage until achieve to recommend operation guarantee area, same time input for NMIX pin + RSTX pin.

11.4.5 Multi-Function Serial Interface

11.4.5.1 CSIO Timing (SMR: MD[2:0] = 0b010)

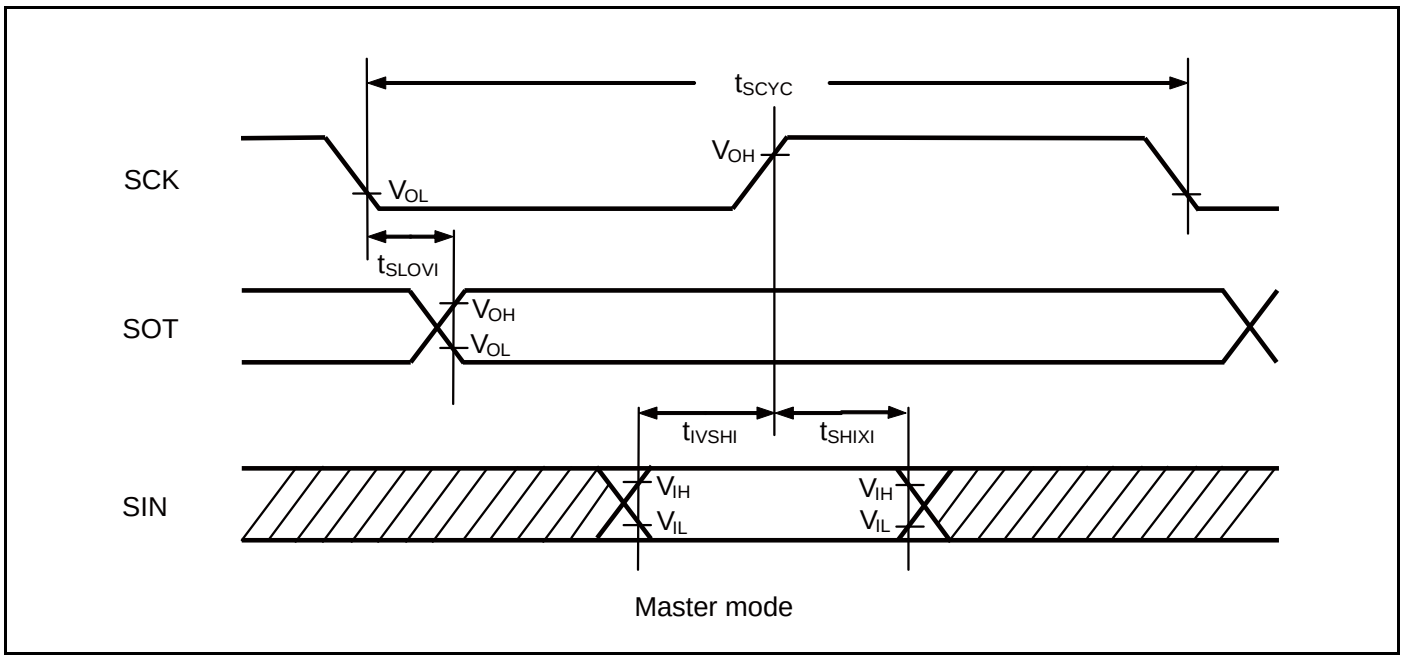
Normal Synchronous Transfer (SCR: SPI = 0) and Serial Clock Output Signal Detect Level "H"(SMR: SCINV = 0)

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

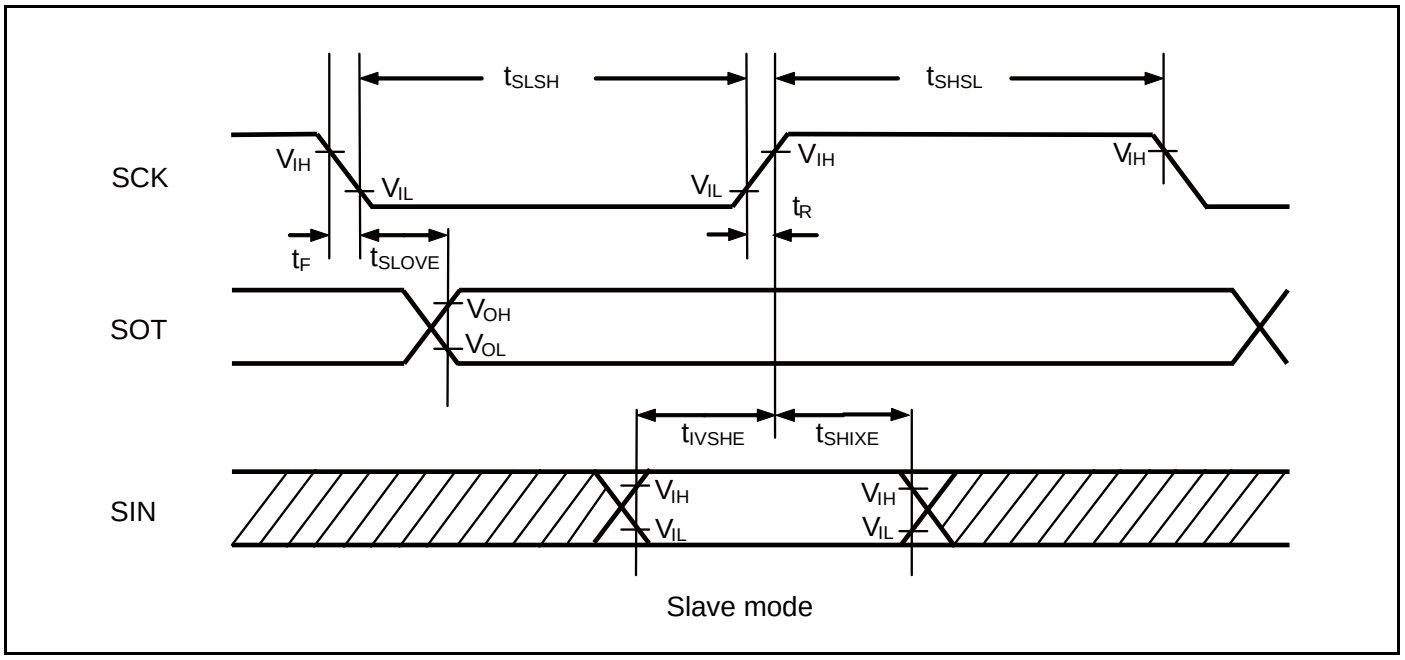
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4	Master mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	$4t_{CLK\_PERI1}$	-	ns	
SCK↓→SOT delay time	t_{SLOVI}	SCK0 to SCK4, SOT0 to SOT4		-30	+30	ns	
Valid SIN→SCK↑ setup time	t_{IVSHI}	SCK0 to SCK4, SIN0 to SIN4		30	-	ns	
SCK↑→Valid SIN hold time	t_{SHIXI}			0	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4	Slave mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CLK_PERI1}+10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CLK\_PERI1}$-10	-	ns	
SCK↓→SOT delay time	t_{SLOVE}	SCK0 to SCK4, SOT0 to SOT4		-	30	ns	
Valid SIN→SCK↑ setup time	t_{IVSHE}	SCK0 to SCK4, SIN0 to SIN4		10	-	ns	
SCK↑→Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK4		-	5	ns	
SCK rise time	t_R	SCK0 to SCK4		-	5	ns	
Transfer speed	-	-	C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA	-	5	Mbps	
	-	-	C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA	-	6	Mbps	

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master mode



Slave mode

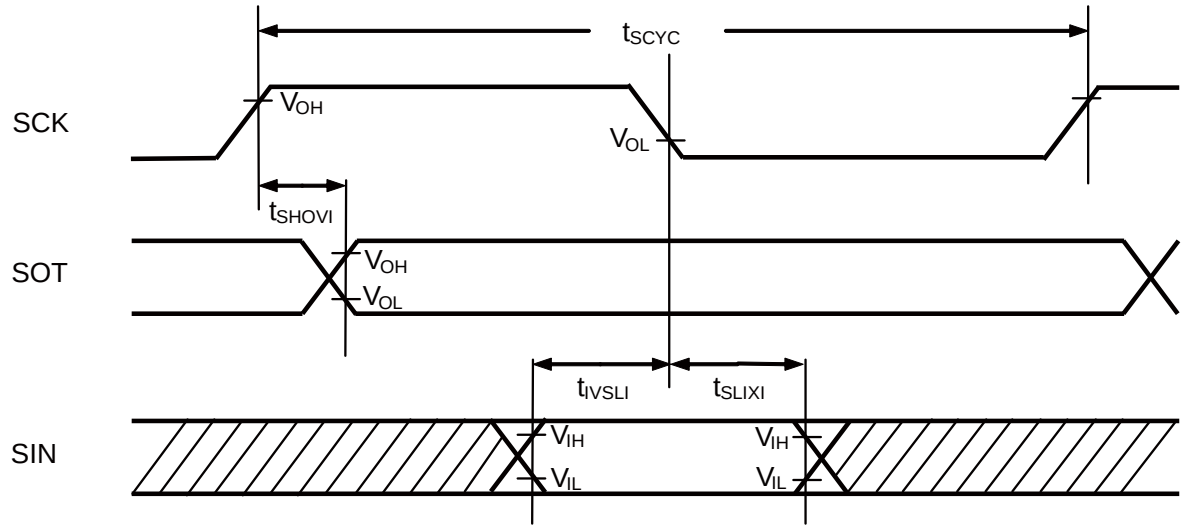
Normal Synchronous Transfer (SCR: SPI = 0) and Serial Clock Output Signal Detect Level "L" (SMR: SCINV = 1)

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

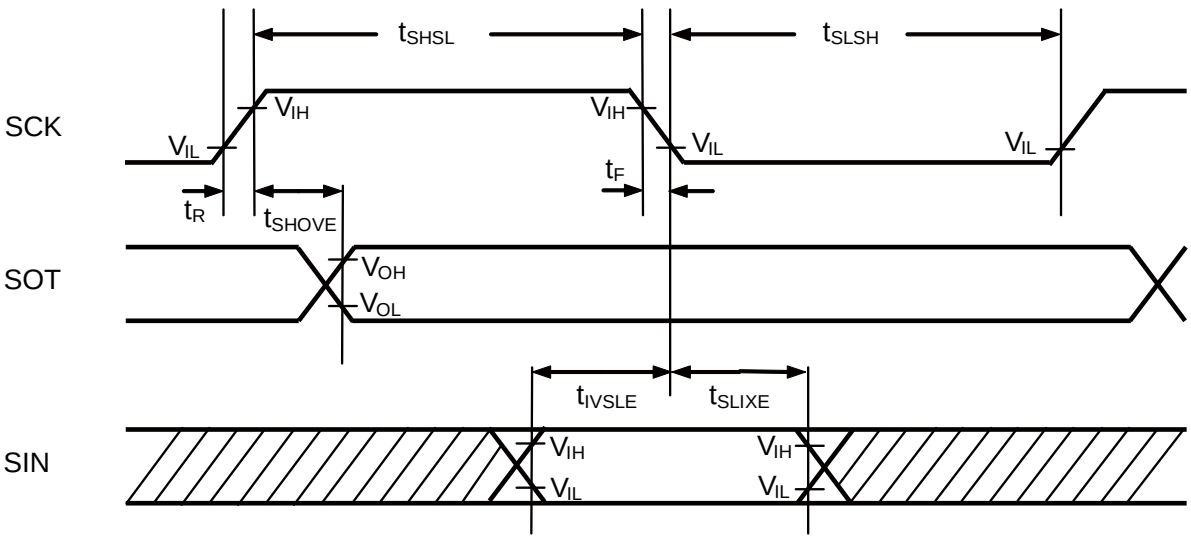
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4	Master mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	$4t_{CLK\_PERI1}$	-	ns	
SCK↑→SOT delay time	t_{SHOVI}	SCK0 to SCK4, SOT0 to SOT4		-30	+30	ns	
Valid SIN→SCK↓ setup time	t_{IVSLI}	SCK0 to SCK4, SIN0 to SIN4		30	-	ns	
SCK↓→valid SIN hold time	t_{SLIXI}			0	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4	Slave mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CLK_PERI1}+10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CLK\_PERI1}$-10	-	ns	
SCK↑→SOT delay time	t_{SHOVE}	SCK0 to SCK4, SOT0 to SOT4		-	30	ns	
valid SIN→SCK↓ setup time	t_{IVSLE}	SCK0 to SCK4, SIN0 to SIN4		10	-	ns	
SCK↓→valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK4		-	5	ns	
SCK rise time	t_R	SCK0 to SCK4		-	5	ns	
Transfer speed	-	-	C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA	-	5	Mbps	
	-	-	C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA	-	6	Mbps	

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master mode



Slave mode

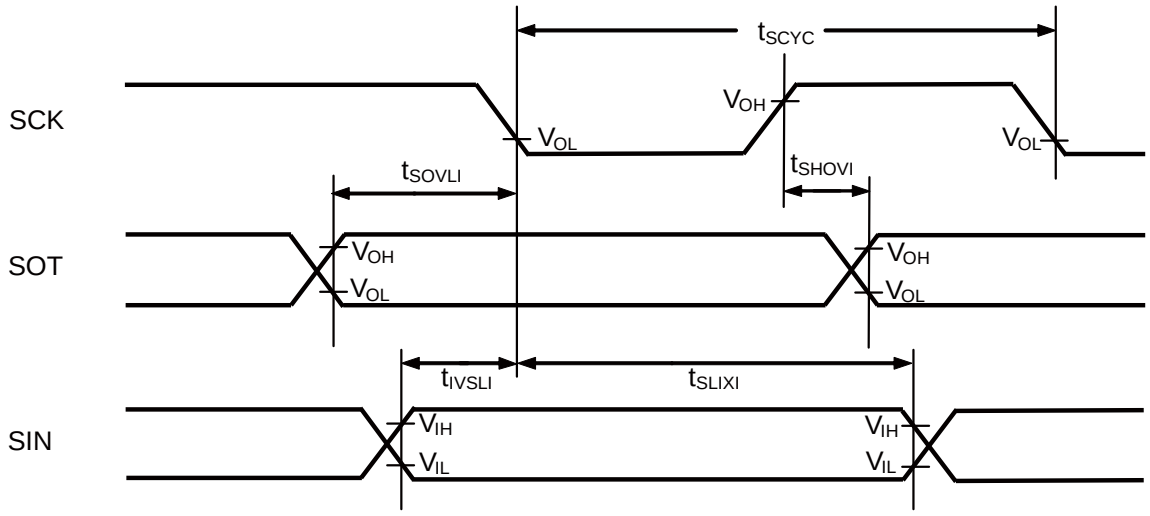
SPI Compatible (SCR: SPI = 1) and Serial Clock Output Signal Detect Level "H" (SMR: SCINV = 0)

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

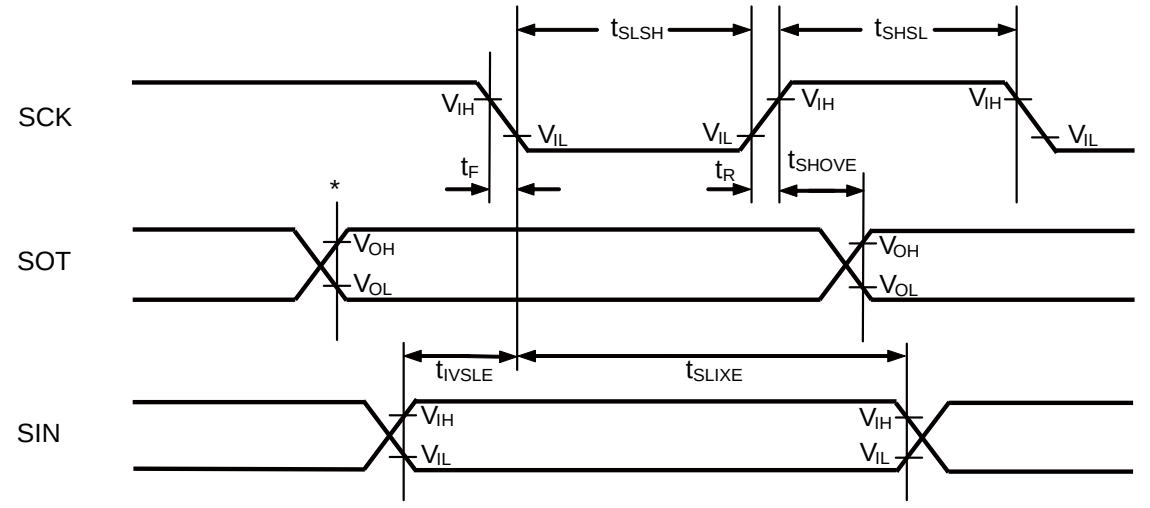
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4	Master mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	$4t_{CLK\_PERI1}$	-	ns	
SCK↑→SOT delay time	t_{SHOVI}	SCK0 to SCK4, SOT0 to SOT4		-30	+30	ns	
Valid SIN→SCK↓ setup time	t_{IVSLI}	SCK0 to SCK4, SIN0 to SIN4		30	-	ns	
SCK↓→valid SIN hold time	t_{SLIXI}			0	-	ns	
SOT→SCK↓ delay time	t_{SOVLI}	SCK0 to SCK4, SOT0 to SOT4		$2t_{CLK\_PERI1}$-30	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4	Slave mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CLK_PERI1}+10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CLK\_PERI1}$-10	-	ns	
SCK↑→SOT delay time	t_{SHOVE}	SCK0 to SCK4, SOT0 to SOT4		-	30	ns	
valid SIN→SCK↓ setup time	t_{IVSLE}	SCK0 to SCK4, SIN0 to SIN4		10	-	ns	
SCK↓→valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK4		-	5	ns	
SCK rise time	t_R	SCK0 to SCK4		-	5	ns	
Transfer speed	-	-	C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA	-	5	Mbps	
	-	-	C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA	-	6	Mbps	

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master mode



*: Changes when writing to TDR register

Slave mode

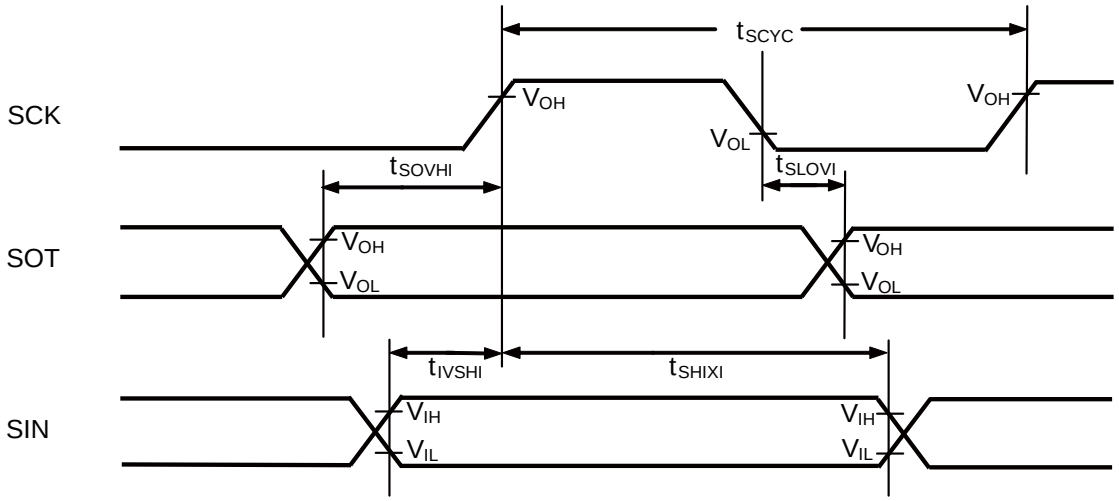
SPI Compatible (SCR: SPI = 1) and Serial Clock Output Signal Detect Level "L" (SMR: SCINV = 1)

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

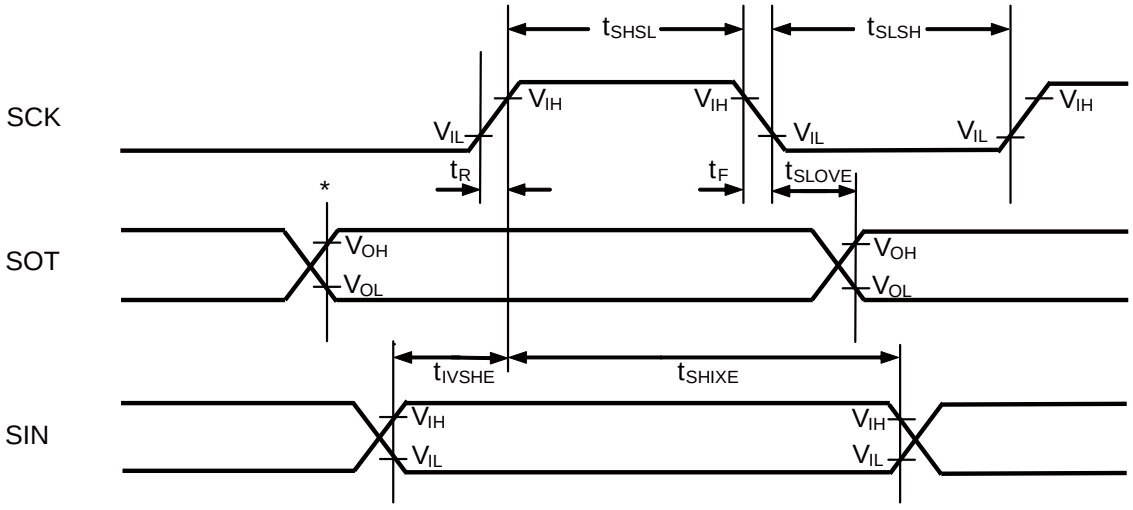
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4	Master mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	$4t_{CLK\_PERI1}$	-	ns	
SCK↓→SOT delay time	t_{SLOVI}	SCK0 to SCK4, SOT0 to SOT4		-30	+30	ns	
Valid SIN→SCK↑ setup time	t_{IVSHI}	SCK0 to SCK4, SIN0 to SIN4		30	-	ns	
SCK↑→valid SIN hold time	t_{SHIXI}			0	-	ns	
SOT→SCK↑ Delay time	t_{SOVHI}	SCK0 to SCK4, SOT0 to SOT4		$2t_{CLK\_PERI1}$-30	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SOT0 to SOT4	Slave mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CLK_PERI1}+10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CLK\_PERI1}$-10	-	ns	
SCK↓→SOT delay time	t_{SLOVE}	SCK0 to SCK4, SOT0 to SOT4		-	30	ns	
valid SIN→SCK↑ setup time	t_{IVSHE}	SCK0 to SCK4, SIN0 to SIN4		10	-	ns	
SCK↑→valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK4		-	5	ns	
SCK rise time	t_R	SCK0 to SCK4		-	5	ns	
Transfer speed	-	-	C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA	-	5	Mbps	
	-	-	C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA	-	6	Mbps	

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master mode



*: Changes when writing to TDR register

Slave mode

When the Serial Chip Select is Used (SCSCR: CSEN = 1)

■Serial clock output signal detect level "H" (SMR, SCSFR: SCINV = 0)

■Serial chip select inactive level "H" (SCSCR, SCSFR: CSLVL = 1)

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↓ setup time	t_{CSSI}	SCK4, SCS40 to SCS43	Master mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CSSU}*1-50	-	ns	
SCK↑→SCS↑ hold time	t_{CSHI}			t_{CSHD}*2+0	-	ns	
SCS deselect time	t_{CSDI}	SCS40 to SCS43		t_{CSDS}*3-50 +5 t_{CLK_PERI1}	-	ns	
SCS↓→SCK↓ setup time	t_{CSSE}	SCK4, SCS40 to SCS43	Slave mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	$3t_{CLK\_PERI1}$+30	-	ns	
SCK↑→SCS↑ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS40 to SCS43		$3t_{CLK\_PERI1}$+30	-	ns	
SCS↓→SOT delay time	t_{DSE}	SCS40 to SCS43, SOT4		-	40	ns	
SCS↑→SOT delay time	t_{DEE}			0	-	ns	
SCK↓→SCS↓ clock switch time	t_{SCC}	SCK4, SCS40 to SCS43	Master mode, Round operation (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	$3t_{CLK\_PERI1}$+0	$3t_{CLK\_PERI1}$ +50	ns	
Transfer speed	-	-	C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA	-	5	Mbps	
	-	-	C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA	-	6	Mbps	

*1: t_{CSSU} = SCSTR: CSSU[7:0] × serial chip select timing operation clock

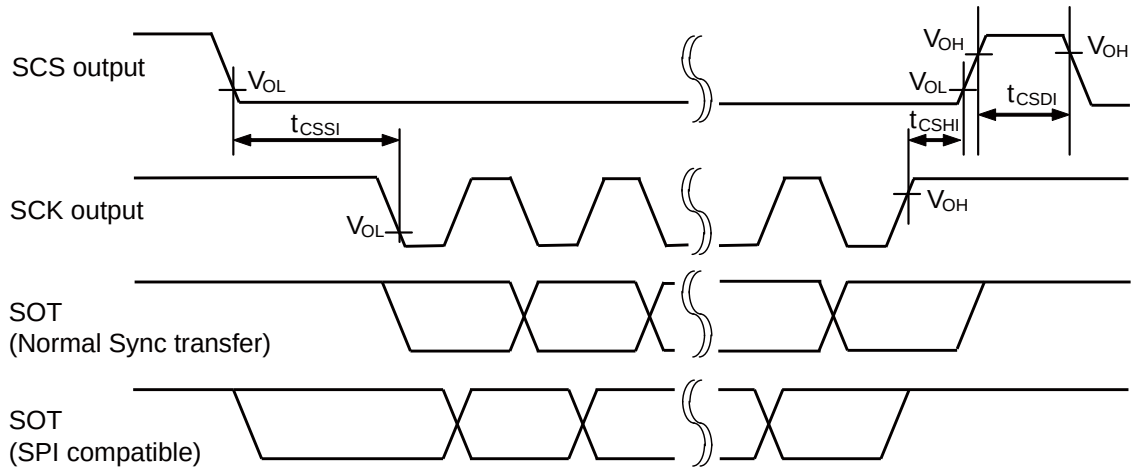
*2: t_{CSHD} = SCSTR: CSHD[7:0] × serial chip select timing operation clock

*3: t_{CSDS} = SCSTR: CSDS[15:0] × serial chip select timing operation clock

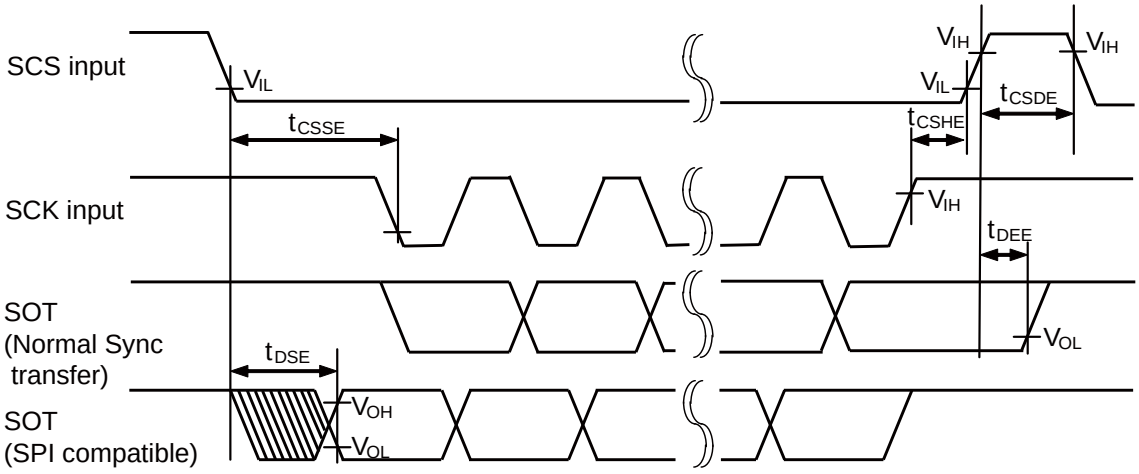
For details of *1, *2 and *3 above, see Hardware Manual.

Notes:

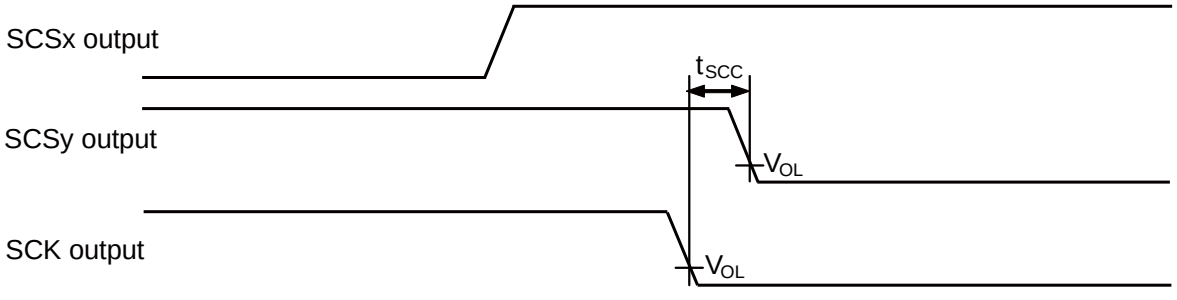
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master mode



Slave mode



Clock switching example by master mode round operation
(x, y = 40, 41, 42, 43: x and y are different value)

When the Serial Chip Select is Used (SCSCR: CSEN = 1)

■Serial clock output signal detect level "L"(SMR, SCSFR: SCINV = 1)

■Serial chip select inactive level "H"(SCSCR, SCSFR: CSLVL = 1)

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↑ setup time	t_{CSSI}	SCK4, SCS40 to SCS43	Master mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CSSU}*1-50	-	ns	
SCK↓→SCS↑ hold time	t_{CSHI}			t_{CSHD}*2+0	-	ns	
SCS deselect time	t_{CSDI}	SCS40 to SCS43		t_{CSDS}*3-50 +5t_{CLK_PERI1}	-	ns	
SCS↓→SCK↑ setup time	t_{CSSE}	SCK4, SCS40 to SCS43	Slave mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	3t_{CLK_PERI1}+30	-	ns	
SCK↓→SCS↑ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS40 to SCS43		3t_{CLK_PERI1}+30	-	ns	
SCS↓→SOT delay time	t_{DSE}	SCS40 to SCS43, SOT4		-	40	ns	
SCS↑→SOT delay time	t_{DEE}			0	-	ns	
SCK↑→SCS↓ clock switch time	t_{SCC}	SCK4, SCS40 to SCS43	Master mode, Round operation (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	3t_{CLK_PERI1}+0	3t_{CLK_PERI1}+50	ns	
Transfer speed	-	-	C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA	-	5	Mbps	
	-	-	C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA	-	6	Mbps	

*1: t_{CSSU} = SCSTR: CSSU[7:0] × serial Chip select timing operation clock

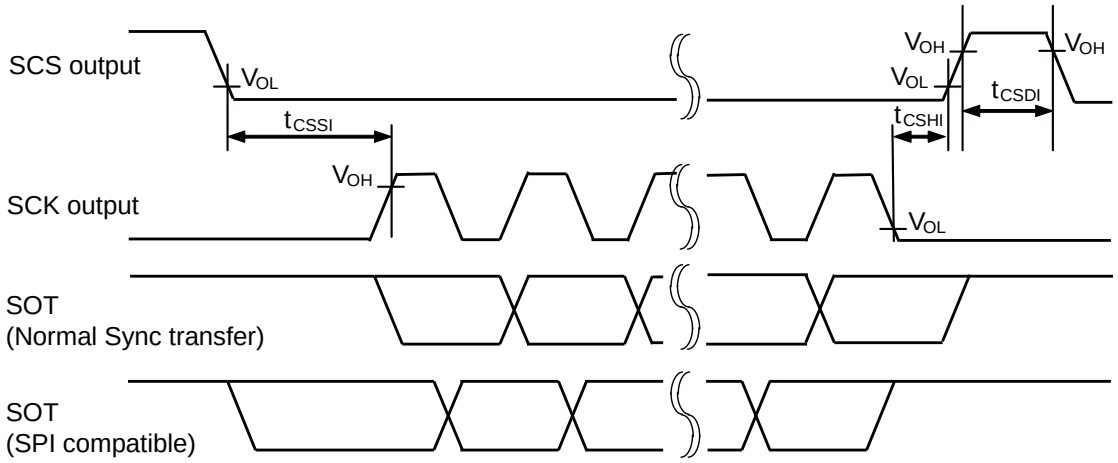
*2: t_{CSHD} = SCSTR: CSHD[7:0] × serial Chip select timing operation clock

*3: t_{CSDS} = SCSTR: CSDS[15:0] × serial Chip select timing operation clock

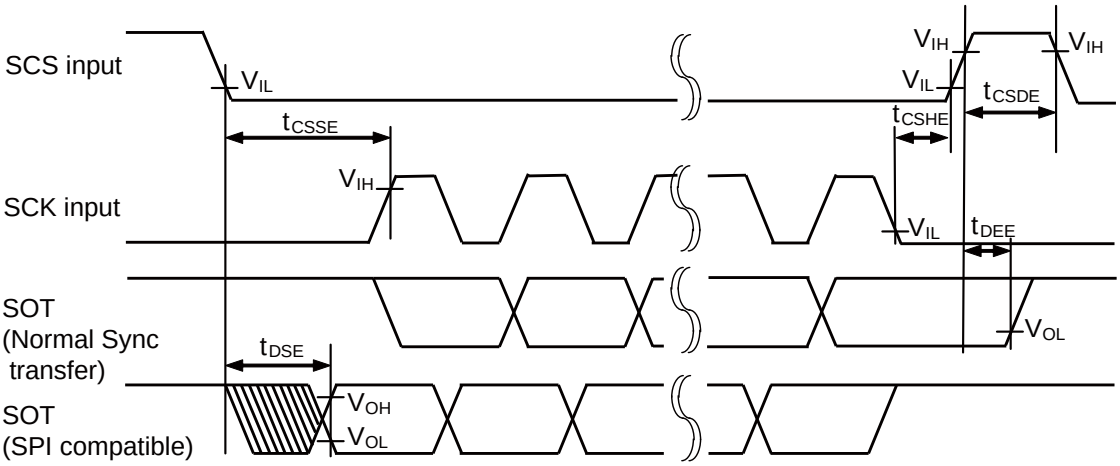
For details of *1, *2 and *3 above, see Hardware Manual.

Notes:

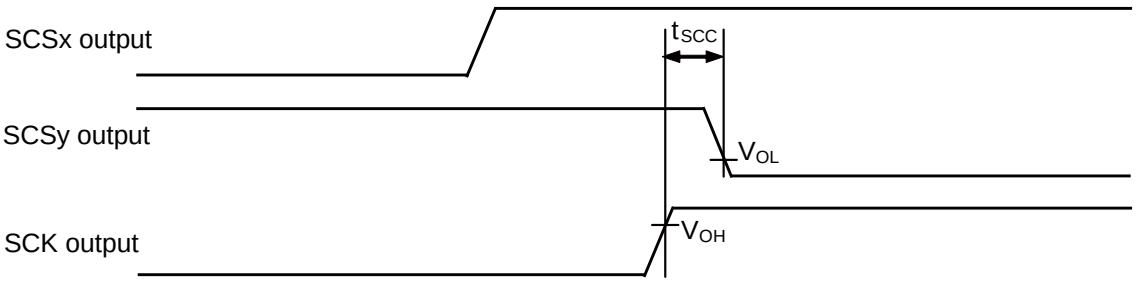
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master mode



Slave mode



Clock switching example by master mode round operation
(x, y = 40, 41, 42, 43: x and y are different value)

When the Serial Chip Select is Used (SCSCR: CSEN = 1)

■Serial clock output signal detect level "H"(SMR, SCSFR: SCINV = 0)

■Serial Chip select inactive level "L"(SCSCR, SCSFR: CSLVL = 0)

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SCK↓ setup time	t_{CSSI}	SCK4, SCS40 to SCS43	Master mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CSSU}*1-50	-	ns	
SCK↑→SCS↓ hold time	t_{CSHI}			t_{CSHD}*2+0	-	ns	
SCS deselect time	t_{CSDI}	SCS40 to SCS43		t_{CSDS}*3-50 +5t_{CLK_PERI1}	-	ns	
SCS↑→SCK↓ setup time	t_{CSSE}	SCK4, SCS40 to SCS43	Slave mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	3t_{CLK_PERI1}+30	-	ns	
SCK↑→SCS↓ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS40 to SCS43		3t_{CLK_PERI1}+30	-	ns	
SCS↑→SOT delay time	t_{DSE}	SCS40 to SCS43, SOT4		-	40	ns	
SCS↓→SOT delay time	t_{DEE}			0	-	ns	
SCK↓→SCS↑ clock switch time	t_{SCC}	SCK4, SCS40 to SCS43	Master mode, round operation (C_L = 50 pF, I_{OL} = -2 mA,I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	3t_{CLK_PERI1}+0	3t_{CLK_PERI1} +50	ns	
Transfer speed	-	-	C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA	-	5	Mbps	
	-	-	C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA	-	6	Mbps	

*1: t_{CSSU} = SCSTR: CSSU[7:0] × serial chip select timing operation clock

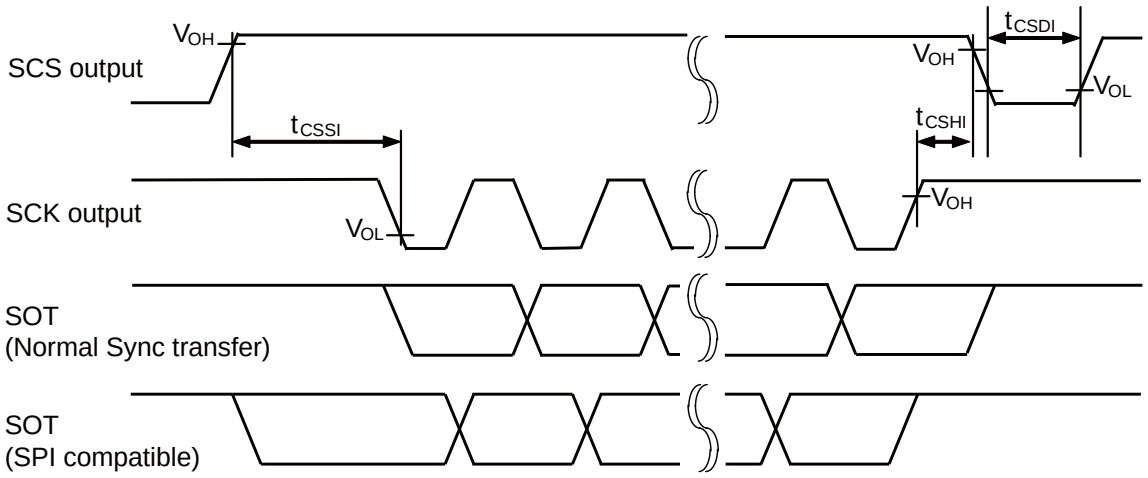
*2: t_{CSHD} = SCSTR: CSHD[7:0] × serial chip select timing operation clock

*3: t_{CSDS} = SCSTR: CSDS[15:0] × serial chip select timing operation clock

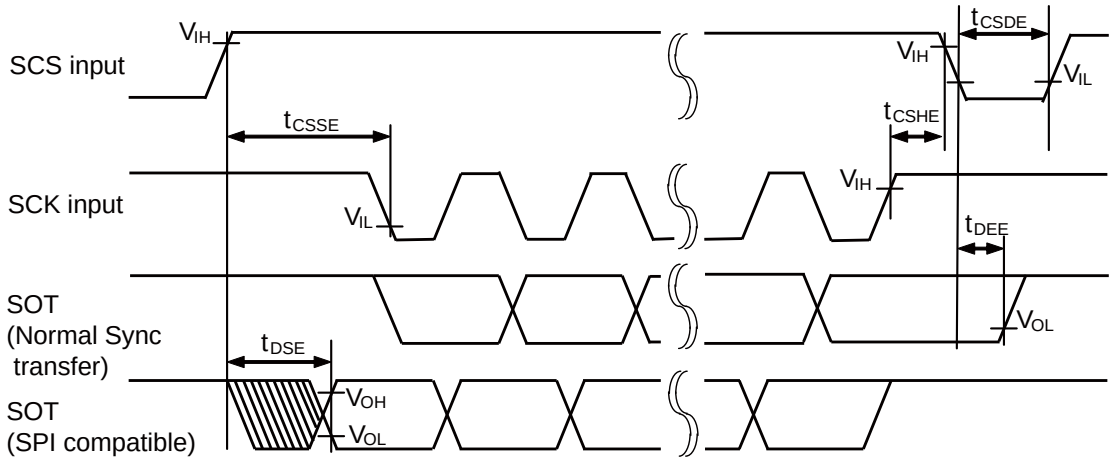
For details of *1, *2 and *3 above, see Hardware Manual.

Notes:

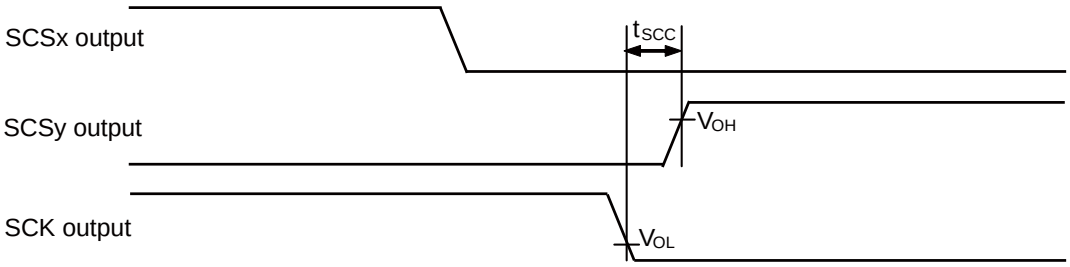
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master mode



Slvae mode



Clock switching example by master mode round operation
(x, y = 40, 41, 42, 43: x and y are different value)

When the Serial Chip Select is Used (SCSCR: CSEN = 1)

■Serial clock output signal detect level "L"(SMR, SCSFR: SCINV = 1)

■Serial Chip select inactive level "L"(SCSCR, SCSFR: CSLVL = 0)

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SCK↑ setup time	t_{CSSI}	SCK4, SCS40 to SCS43	Master mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CSSU}*1-50	-	ns	
SCK↓→SCS↓ hold time	t_{CSHI}			t_{CSHD}*2+0	-	ns	
SCS deselect t time	t_{CSDI}	SCS40 to SCS43		t_{CSDS}*3-50 +5t_{CLK_PERI1}	-	ns	
SCS↑→SCK↑ setup time	t_{CSSE}	SCK4, SCS40 to SCS43	Slave mode (C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	3t_{CLK_PERI1}+30	-	ns	
SCK↓→SCS↓ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS40 to SCS43		3t_{CLK_PERI1}+30	-	ns	
SCS↑→SOT delay time	t_{DSE}	SCS40 to SCS43, SOT4		-	40	ns	
SCS↓→SOT delay time	t_{DEE}			0	-	ns	
SCK↑→SCS↑ clock switch time	t_{SCC}	SCK4, SCS40 to SCS43	Master mode, Round operation (C_L = 50 pF, I_{OL} = -2 mA,I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	3t_{CLK_PERI1}+0	3t_{CLK_PERI1} +50	ns	
Transfer speed	-	-	C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA	-	5	Mbps	
	-	-	C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA	-	6	Mbps	

*1: t_{CSSU} = SCSTR:CSSU[7:0] × serial chip select timing operation clock

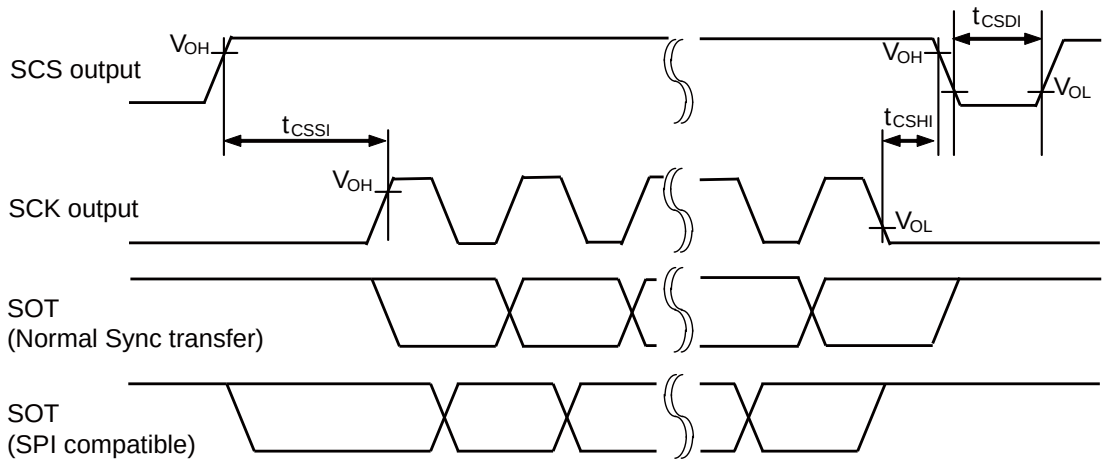
*2: t_{CSHD} = SCSTR:CSHD[7:0] × serial chip select timing operation clock

*3: t_{CSDS} = SCSTR:CSDS[15:0] × serial chip select timing operation clock

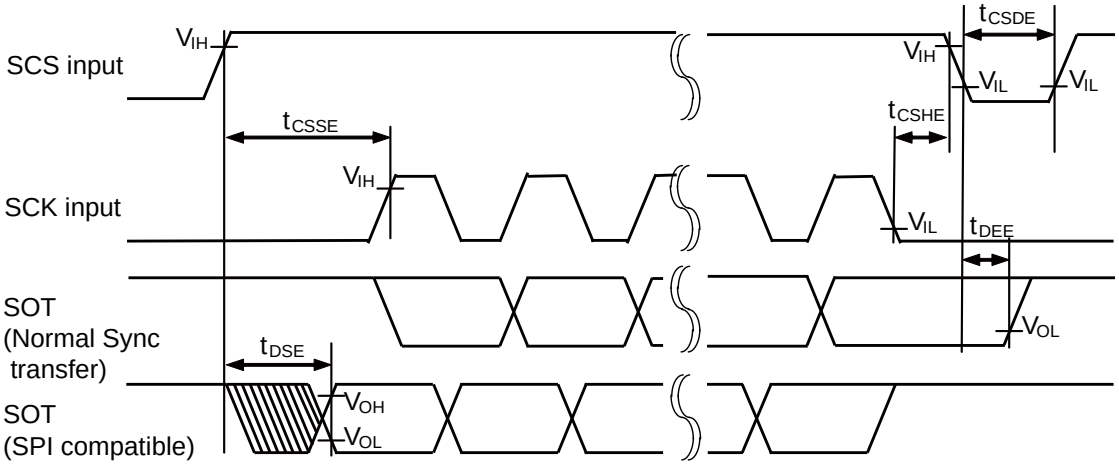
For details of *1, *2 and *3 above, see Hardware Manual.

Notes:

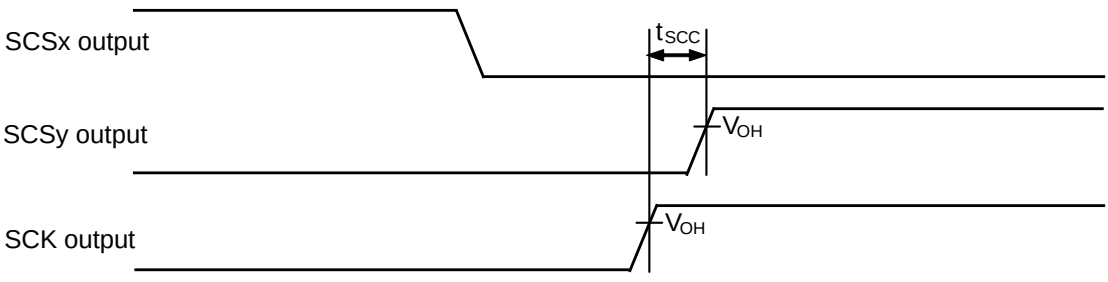
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master mode



Slave mode

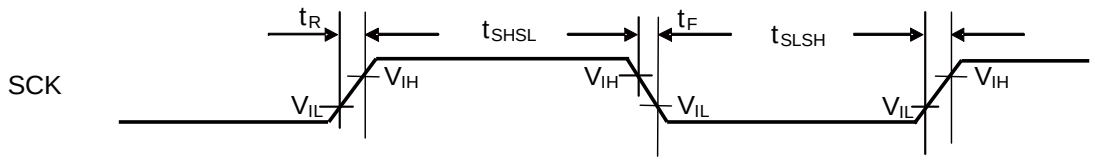


Clock switching example by master mode round operation
(x, y = 40, 41, 42, 43: x and y are different value)

11.4.5.2 UART (Async Serial Interface) Timing (SMR: MD[2:0] = 0b000, 0b001)
When the External Clock is Selected (BGR: EXT = 1)

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK4	(C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CLK_PERI1}+10	-	ns	
serial clock "H" pulse width	t_{SHSL}			t_{CLK_PERI1}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	

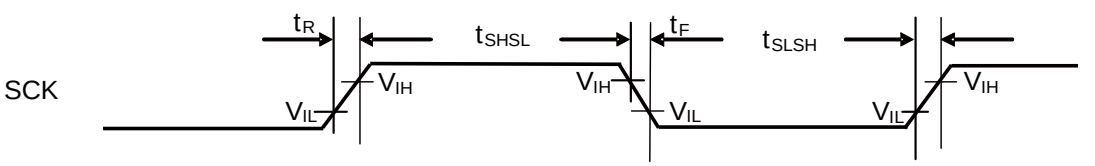


When the external clock is selected

11.4.5.3 LIN Interface (v2.1) (LIN Communication Control Interface (v2.1)) Timing (SMR: MD[2:0] = 0b011)
When the External Clock is Selected (BGR: EXT = 1)

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK4	(C_L = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (C_L = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CLK_PERI1}+10	-	ns	
serial clock "H" pulse width	t_{SHSL}			t_{CLK_PERI1}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



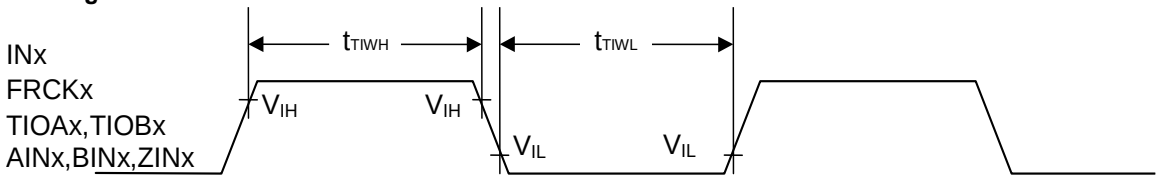
When the external clock is selected

11.4.6 Timer Input Timing

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	IN16 to IN21, TIOA0 to TIOA11, TIOB0 to TIOB11	-	$4t_{CLK\_PERI1}$	-	ns	
		IN4 to IN14, FRCK6 to FRCK10, FRCK12 to FRCK17	-	$4t_{CLK\_PERI4}$	-	ns	$4t_{CLK\_PERI4} \geq 70$ ns
				70			$4t_{CLK\_PERI4} < 70$ ns
		IN0 to IN3, FRCK0 to FRCK1, FRCK4 to FRCK5	-	$4t_{CLK\_PERI5}$	-	ns	$4t_{CLK\_PERI5} \geq 70$ ns
				70			$4t_{CLK\_PERI5} < 70$ ns
		AIN0, BIN0, ZIN0	-	$4t_{CLK\_PERI5}$	-	ns	$4t_{CLK\_PERI5} \geq 70$ ns
				70			$4t_{CLK\_PERI5} < 70$ ns
		AIN2, BIN2, ZIN2	-	$4t_{CLK\_PERI4}$	-	ns	$4t_{CLK\_PERI4} \geq 70$ ns
				70			$4t_{CLK\_PERI4} < 70$ ns

Timer input timing

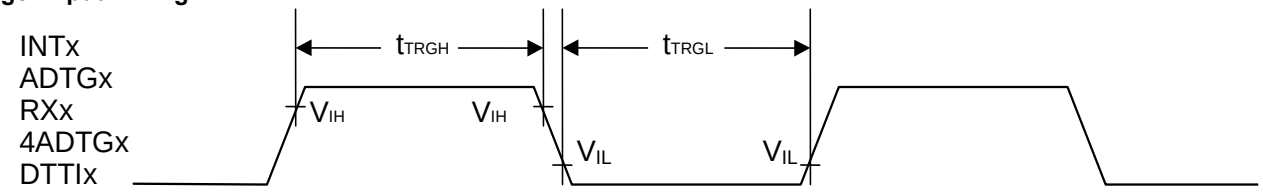


11.4.7 Trigger Input Timing

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT7	-	200	-	ns	
		RX0 to RX2	-	$5t_{CLK\_SYSCPD1}$	-	ns	
		ADTG0, DTTI2 to DTTI3	-	$5t_{CLK\_PERI6}$	-	ns	
		4ADTG0, DTTI0	-	$5t_{CLK\_PERI5}$	-	ns	$5t_{CLK\_PERI5}$≥70 ns
				70			$5t_{CLK\_PERI5}$<70 ns
		4ADTG1, DTTI1	-	$5t_{CLK\_PERI4}$	-	ns	$5t_{CLK\_PERI4}$≥70 ns
				70			$5t_{CLK\_PERI4}$<70 ns
		INT0 to INT7, ADTG0, 4ADTG0, 4ADTG1, RX0 to RX2, DTTI0 to DTTI3	-	1	-	µs	When stop mode

Trigger Input Timing

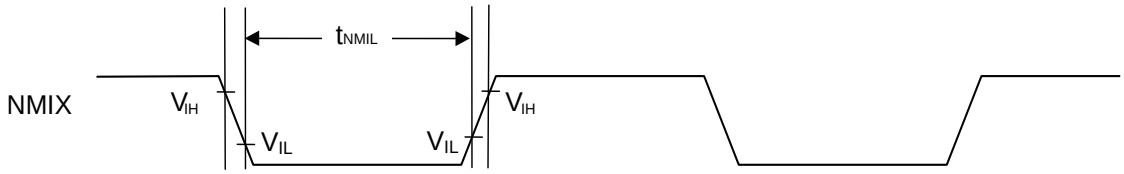


11.4.8 NMI Input Timing

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	-	200	-	ns	

NMIX Input Timing



11.4.9 External Low-Voltage Detection

(T_A: Recommended operating conditions, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{DP5}	VCC5	-	-	-	5.5	V	
Detection voltage	V_{DL}	VCC5	*1	3.7	3.9	4.1	V	When power supply voltage falls The original setting of detection level is 4.1 V±0.2 V
Hysteresis width	V_{HYS}	VCC5	-	75	100	150	mV	When power supply voltage rises
Low voltage detection time	T_d	-	-	-	-	30	µs	
Power supply voltage fluctuation rate	-	VCC5	-	-4	-	-	V/ms	*2

*1: If the fluctuation of the power supply has exceeded the detection voltage range within the time less than the low-voltage detection time (T_d), there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: In order to perform the low-voltage detection at the detection voltage (V_{DL}), be sure to suppress fluctuation of the power supply within the limits of the power supply voltage fluctuation rate.

11.4.10 Internal Low-Voltage Detection

(T_A: Recommended operating conditions, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{RDP5}	VCC12	-	-	-	1.3	V	
Detection voltage	V_{RDL}	VCC12	*1	0.8	0.9	1.0	V	When power supply voltage falls
Hysteresis width	V_{RHYS}	VCC12	-	20	30	50	mV	When power supply voltage rises
Low voltage detection time	T_{Rd}	-	-	-	-	30	µs	
Power supply voltage fluctuation rate	-	VCC12	-	-4	-	-	V/ms	*2

*1: If the fluctuation of the power supply has exceeded the detection voltage range within the time less than the low-voltage detection time (T_{Rd}), there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: In order to perform the low-voltage detection at the detection voltage (V_{RDL}), be sure to suppress fluctuation of the power supply within the limits of the power supply voltage fluctuation rate.

11.5 A/D Converter

11.5.1 Electrical Characteristics

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Non linearity error	-	-	-4.0	-	+4.0	LSB	
Differential linearity error	-	-	-1.9	-	+1.9	LSB	
Zero transition voltage	V_{ZT}	AN0 to AN31	AVRL +0.5LSB-20	-	AVRL +0.5LSB+20	mV	1LSB = (V_{FST}-V_{ZT})/4094
Full-scale transition voltage	V_{FST}	AN0 to AN31	AVRH -1.5LSB-20	-	AVRH -1.5LSB+20	mV	
Sampling time	t_{SMP}	-	0.3	-	12	µs	*1
Compare time	t_{CMP}	-	0.7	-	28	µs	*1
A/D conversion time	t_{CNV}	-	1.0	-	40	µs	*1
Analog port input current	I_{AIN}	AN0 to AN31	-2.0	-	2.0	µA	$V_{AVSS} \le V_{AIN} \le V_{AVCC}$
Analog input voltage	V_{AIN}	AN0 to AN31	AVSS	-	AVRH	V	
Reference voltage	AVRH	AVRH2	4.5	-	5.5	V	$AV_{CC} \ge$ AVRH
	AVRL	AVRL2	-	0.0	-	V	
Power supply current	I_A	AVCC2	-	500	680	µA	
	I_{AH}		-	-	17.7	µA	*2
	I_R	AVRH2	-	1	2	mA	
	I_{RH}		-	-	2.16	µA	*2
Variation between channels	-	AN0 to AN31	-	-	4	LSB	

*1: Time for each channel.

*2: The power supply current (V_{CC} = AV_{CC} = 5.0V) is specified if the A/D converter is not operating and CPU is stopped.

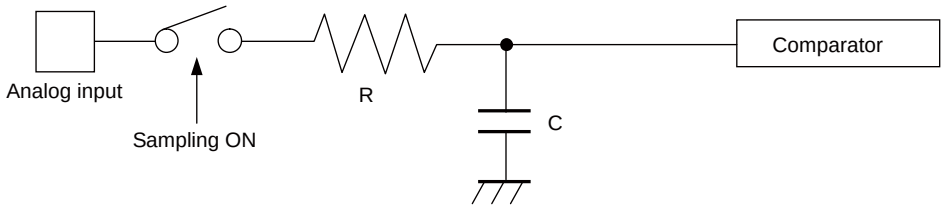
11.5.2 Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

When the external impedance is too high, the sampling time for analog voltages may not be sufficient.

In this case, it is recommended to connect the capacitor (approx. 0.1 µF) to the analog input pin.

Analog Input Circuit Model



	R	C	
12bit A/D	3.0kΩ (max)	8.30pF (max)	(4.5V ≤ AVcc ≤ 5.5V)

Note: Listed values must be considered as reference values.

11.6 4 Channels Same Time Sampling A/D Converter

11.6.1 Electrical Characteristics

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Non linearity error	-	-	-4.0	-	+4.0	LSB	
Differential linearity error	-	-	-1.9	-	+1.9	LSB	
Zero transition voltage	V_{ZT}	4AN0 to 4AN7	AVRL +0.5LSB-20	-	AVRL +0.5LSB+20	mV	1LSB = (V_{FST}-V_{ZT})/4094
Full-scale transition voltage	V_{FST}	4AN0 to 4AN7	AVRH -1.5LSB-20	-	AVRH -1.5LSB+20	mV	
Sampling time	t_{SMP}	-	0.6	-	1.2	µs	*1
Compare time	t_{CMP}	-	1.4	-	5.6	µs	*2
A/D conversion time	t_{CNV}	-	2	-	6.8	µs	*3
Analog port input current	I_{AIN}	4AN0 to 4AN7	-0.7	-	0.7	µA	$V_{AVSS} \le V_{AIN} \le V_{AVCC}$
Analog input voltage	V_{AIN}	4AN0 to 4AN7	AVSS	-	AVRH	V	
Reference voltage	AVRH	AVRH0, AVRH1	4.5	-	5.5	V	$AV_{CC} \ge$ AVRH
	AVRL	AVRL0, AVRL1	-	0.0	-	V	
Power supply current	I_A	AVCC0, AVCC1	-	1.0	1.5	mA	1 unit operation
	I_{AH}		-	-	27.5	µA	1 unit operation*4
	I_R	AVRH0, AVRH1	-	0.5	4.0	mA	1 unit operation
	I_{RH}		-	-	4.5	µA	1 unit operation*4
Variation between channels	-	4AN0 to 4AN3	-	-	20	mV	
	-	4AN4 to 4AN7	-	-	20	mV	

*1: 4 channels same time sampling time.

*2: Compare time for 4 channels.

*3: Conversion time for 4 channels.

*4: The power supply current (V_{CC} = AV_{CC} = 5.0 V) is specified if the A/D converter is not operating and CPU is stopped.

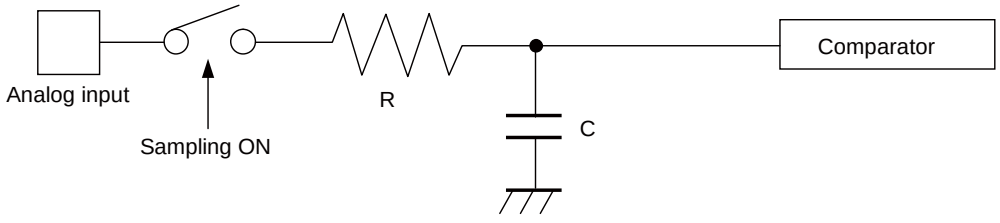
11.6.2 Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

When the external impedance is too high, the sampling time for analog voltages may not be sufficient.

In this case, it is recommended to connect the capacitor (approx. 0.1 µF) to the analog input pin.

Analog Input Circuit Model



	R	C	
4-SH 12bit A/D	3.8kΩ (max)	8.30pF (max)	(4.5V ≤ AVcc ≤ 5.5V)

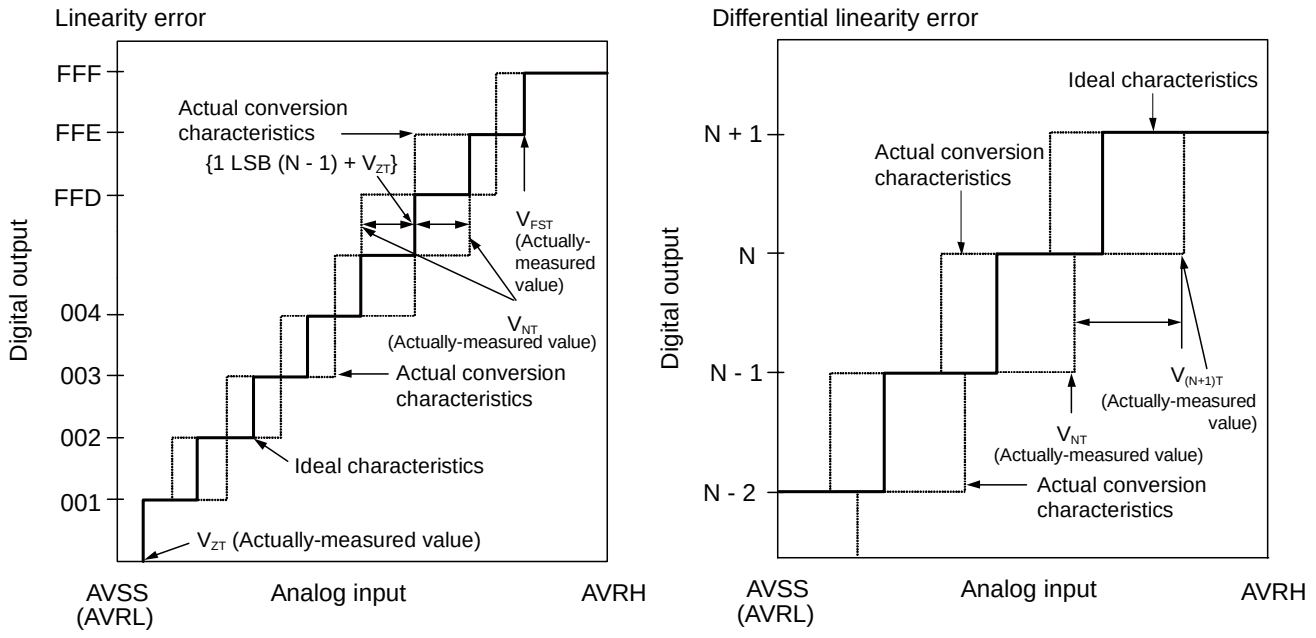
Note: Listed values must be considered as reference values.

11.6.3 Definition of Terms

Resolution: Analog variation that is recognized by an A/D converter.

Linearity error: Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("0000 0000 0000" ⟷ "0000 0000 0001") to the full-scale transition point ("1111 1111 1110" ⟷ "1111 1111 1111").

Differential linearity error: Deviation of the input voltage from the ideal value that is required to change the output code by 1LSB.



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N-1) + V_{ZT}\}}{1LSB} \quad [LSB]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1\ LSB \quad [LSB]$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094} \quad [V]$$

V_{ZT}: Voltage at which the digital output changes from "0x000" to "0x001".

V_{FST}: Voltage at which the digital output changes from "0xFFE" to "0xFFF".

11.7 Flash Memory

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	200	800	ms	8K Byte sector[*1] Excluding internal preprogramming time
	-	300	1100	ms	8K Byte sector [*1] Including internal preprogramming time
	-	400	2000	ms	64K Byte sector [*1] Excluding internal preprogramming time
	-	700	3700	ms	64K Byte sector [*1] Including internal preprogramming time
8bit writing time	-	9	288	µs	Excluding overhead time at system level[*1]
16bit writing time	-	12	384	µs	Excluding overhead time at system level[*1]
ECC writing time	-	9	288	µs	Excluding overhead time at system level[*1]
Erase cycle [*2]/ Data retention time	1,000 times /20 years, 10,000 times /10 years, 100,000 times / 5 years	-	-	-	Temperature at writing/erasing Average temperature T_A = +85°C[*3]

*1: The guaranteed value for erase up to 100,000 cycles

*2: Number of erase cycles for each sector

*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

Notes:

- While the Flash memory is written or erased, shutdown of the external power supply (V_{CC}, V_{DD}) is prohibited.
- In the application system where V_{CC} or V_{DD} might disappear while writing, be sure to turn the power off by using an external low-voltage detector and NMIX pin + RSTX pin for reset input at same time. Concretely, please execute two of the following.
  1. After simultaneous input from the NMIX and RSTX pins while V_{DD} is within the recommended operating range, maintain V_{DD} within the recommended operating range for at least 60 µs.
  2. After simultaneous input from the NMIX and RSTX pins while V_{CC} is within the recommended operating range, power off V_{CC} in observance of the standard regarding the supply voltage fluctuation rate of the external low-voltage detector.

11.8 R/D Converter

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Excitation signal output	Output voltage(amplitude)	0.4V_{CC}-1%	0.4V_{CC}	0.4V_{CC}+1%	V	
	Output voltage(displacement)	-0.4V_{CC}+(V_{CC}/2)	-	0.4V_{CC}+(V_{CC}/2)	V	
	output current	-	-	1	mA	
	Frequency	-	10 or 20	-	kHz	Setting with the register
Resolver response signal*1	Amplitude	AREF20-2.0	-	AREF20+2.0	V	Unit0
		AREF21-2.0	-	AREF21+2.0	V	Unit1
	Maximum input frequency	-	-	24	kHz	
Excitation input signal*2	Amplitude	0	-	RVCC0	V	Unit0 More than 2V_{p-p}
		0	-	RVCC1	V	Unit1 More than 2V_{p-p}
	Phase difference from resolver detection signal	-45	-	45	°	
Angle output	Angle accuracy (conversion accuracy)	-4	-	4	LSB	Variation when Pausing: ±1LSB
	Resolution	-	12	-	bit	
	Output delay	1.1	-	2.1	µs	
Angular velocity output	Maximum Angular velocity	-	-	4000	rps	When bandwidth 1.8 kHz mode
		-	-	3000	rps	When bandwidth 600 kHz mode
	Resolution	-	0.261	-	rps/LSB	
Reference output voltage	AREF2 output voltage	RVCC0/2-3%	-	RVCC0/2+3%	V	Unit0
		RVCC1/2-3%	-	RVCC1/2+3%	V	Unit1
Operating characteristics	Tracking loop characteristics (0dB cross frequency)	-	-	1.2	kHz	When bandwidth 1.8 kHz mode*3
		-	-	400	Hz	When bandwidth 600 Hz mode*3
	Tracking loop characteristics (-3dB cross frequency)	-	-	1.8	kHz	When bandwidth 1.8 kHz mode*3
		-	-	600	Hz	When bandwidth 600 Hz mode*3
	Maximum tracking rate	-	-	4000	rps	When bandwidth 1.8 kHz mode
		-	-	3000	rps	When bandwidth 600 Hz mode
	Settling time (179 degree step)	-	-	4	ms	When bandwidth 1.8 kHz mode
		-	-	12	ms	When bandwidth 600 Hz mode
	Maximum angular velocity	-	-	1,000,000	rad/s^2	When bandwidth 1.8 kHz mode
		-	-	150,000	rad/s^2	When bandwidth 600 Hz mode

*1: Corresponding pin: COS_PLUS, COS_MINUS, SIN_PLUS, SIN_MINUS
*2: Corresponding pin: MAG_PLUS, MAG_MINUS
*3: When signal amplitude is nominal

12. Ordering Information

Part Number	Package
CY9DF566MxEEQ-GTE1	208-pin plastic TEQFP (LER208)

Notes:

- "x" is option number. This option is following table. The detail of package, see "14. Package Dimensions".

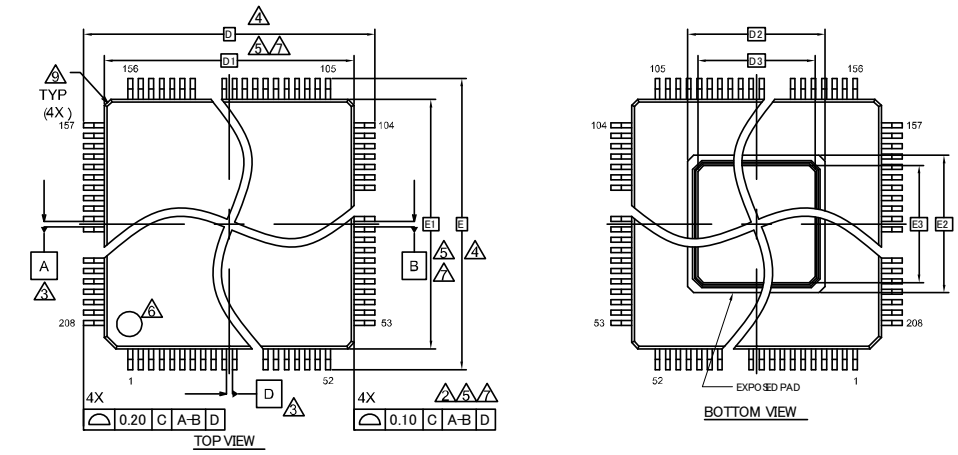
13. Part Number Option

Part Number Option	R/D Converter	FlexRay	Key Code
A	○	-	-
G	○	○	-

○: Supported

14. Package Dimensions

Package Type	Package Code
TEQFP 208	LER208



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.05	——	0.15
A2	1.35	1.40	1.45
D	30.00 BSC		
D1	28.00 BSC		
D2	9.26 REF		
D3	8.06 REF		
E	30.00 BSC		
E1	28.00 BSC		
E2	9.26 REF		
E3	8.06 REF		
R1	0.08	——	——
R2	0.08	——	0.20
θ	0°	4°	8°
c	0.12	——	0.20
b	0.17	0.22	0.27
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25		
e	0.50 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13654 *A

PACKAGE OUTLINE, 208 LEAD TEQFP
28.0X28.0X1.7 MM LER208 REV*A

15. Major Changes

Spansion Publication Number: DS708-00001

Page	Section	Change Results
Revision 1.0		
-	-	Initial release
Revision 2.0		
11	3. Product Lineup	Add 176 pin product
14, 15	4. Pin Assignment	Add 176 pin product
16 to 33	5. Pin Description	Add 176 pin product
46, 47	10. Memory Map	Add address information of MB9DF564 and MB9DF565
54, 55	12. Pin Statuses in CPU Status	Add 176 pin product
102	14. Ordering Information	Change package name Add 176 pin product
103, 104	16. Package Dimensions	Change package dimensions Add 176 pin product
Revision 3.0		
102	15. Part Number Option	Add part number option L, Q

Note: Please see “Document History” about later revised information.

Document History

Document Title: CY9D560 Series 32-bit Microcontroller Traveo™ Family
Document Number: 002-05679

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	KOJM	05/15/2015	Migrated to Cypress and assigned document number 002-05679. No change to document contents or format.
*A	5176126	KOJM	03/22/2016	Updated to Cypress format.
*B	6515227	KOJM	04/01/2019	Marketing Part Numbers changed from prefix MB to prefix CY. Deleted following parts number MB9D564MxEEQ-GTE1 MB9D564LxEEQ-GTE1 MB9D565LxEEQ-GTE1 MB9D566LxEEQ-GTE1 Updated 1. Product Lineup Deleted 176pin Part Number with/without RDC in 2. Pin Assignment Updated 3. Pin Description Updated 10. Pin Statuses in CPU Status Updated 12. Ordering Information Deleted L and Q option in 13. Part Number Option Deleted 176pin Package Dimensions Updated 208pin Package Dimensions

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