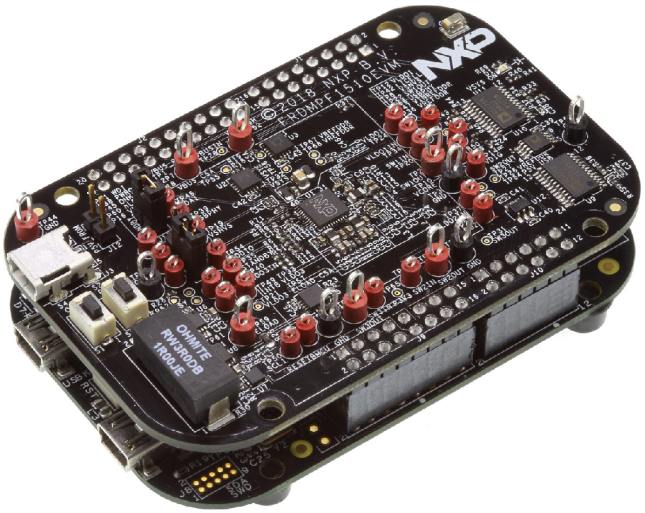
KTFRDMPF1510EVMUG

FRDM-PF1510EVM evaluation board

Rev. 1.0 — 18 June 2018 User guide

1 FRDM-PF1510EVM



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3 Overview of the PF1510 PMIC development environment

NXP offers a combination of boards that support the evaluation of the PF1510 power management integrated circuit (PMIC).

The FRDM-PF1510EVM boards serve as an evaluation platform that allows users to test and demo designs that incorporate the PF1510 PMIC. The evaluation board contains a preconfigured MC32PF1510A4EP device and provides numerous jumpers and test points that allow users to tailor the evaluation to their needs.

The kit comes with a FRDM-KL25Z already mounted and loaded with compatible microcode. The primary function of the FRDM-KL25Z is to control communication between the evaluation board and a PC.

4 Getting started

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. These development boards support a range of analog, mixed-signal, and power solutions. These boards incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost, and improved performance in powering state-of-the-art systems.

The tool summary page for FRDM-PF1510EVM is at http://www.nxp.com/FRDM-PF1510EVM. The overview tab on this page provides an overview of the device, a list of device features, a description of the kit contents, links to supported devices and a **Get Started** section.

The **Get Started** section provides information applicable to using the FRDM-PF1510EVM.

1. Go to http://www.nxp.com/FRDM-PF1510EVM.
2. On the **Overview** tab, locate the **Jump To** navigation feature on the left side of the window.
3. Select the **Get Started** link.
4. Review each entry in the **Get Started** section.
5. Download an entry by clicking the linked title.

After reviewing the **Overview** tab, visit the other related tabs for additional information:

- **Documentation**: Download current documentation.
- **Software & Tools**: Download current hardware and software tools.
- **Buy/Parametrics**: Purchase the product and view the product parametrics.

After downloading files, review each file, including the user guide, which includes setup instructions. If applicable, the bill of materials (BOM) and supporting schematics are also available for download in the **Get Started** section of the **Overview** tab.

4.1 Kit content/packing list

The FRDM-PF1510EVM content includes:

- Assembled and tested evaluation board in an anti-static bag
- Cable, USB type A male/type mini B male 3 ft
- Quick start guide

4.2 Required equipment

This kit requires the following items:

- 5.0 V DC power supply or USB with enough current capability (3.0 A for maximum performance)
- KITPF1510GUI installed on a Windows PC
- Optional voltmeters to measure regulator outputs
- Optional oscilloscope

4.3 System requirements

The kit requires the following to function properly with the software:

- USB-enabled computer running Windows XP, Vista 7, 8, or 10 (32 bit or 64 bit)

5 Getting to know the hardware

5.1 Board overview

The FRDM-PF1510EVM board is an easy-to-use circuit board, allowing the user to exercise all the functions of the PF1510 PMIC.

The FRDM-KL25Z is mounted to the EVB as an integral component and serves as an interface between the KITPF1510GUI and the PF1510 PMIC. The FRDM-KL25Z drives circuitry on the FRDM-PF1510EVM and provides an analog-to-digital converter (ADC) to monitor PF1510 regulator voltages which are displayed in the GUI.

5.2 Board features

The board features the following:

- PF1510 PMIC
- Integrated FRDM-KL25Z as a communication link between the EVB and a PC

5.3 Device features

The evaluation board features the following NXP product:

Table 1. Device features

Device	Description	Features
PF1510	power management integrated circuit (PMIC) for i.MX 7ULP, i.MX 6SL, 6UL, 6ULL, and 6SX processors	• Three adjustable high efficiency buck regulators with 1.0 A per regulator current capability • Three adjustable general-purpose linear regulators • Input voltage range on VIN: 4.1 V to 6.0 V • Low dropout (LDO)/switch supply • Double data rate (DDR) memory reference voltage • One time programmable (OTP) memory for device configuration

5.3.1 Device description

The PF1510 device populated on board features the A4 OTP; see Table 2.

Table 2. Startup configuration

Register	Pre-programmed OTP configuration – A4 configuration
OTP_VSNVS_VOLT[2:0]	3.0 V
OTP_SW1_VOLT[5:0]	1.1 V
OTP_SW1_PWRUP_SEQ[2:0]	4
OTP_SW2_VOLT[5:0]	1.2 V
OTP_SW2_PWRUP_SEQ[2:0]	3
OTP_SW3_VOLT[5:0]	1.8 V
OTP_SW3_PWRUP_SEQ[2:0]	2
OTP_LDO1_VOLT[4:0]	3.3 V
OTP_LDO1_PWRUP_SEQ[2:0]	1
OTP_LDO2_VOLT[3:0]	3.3 V
OTP_LDO2_PWRUP_SEQ[2:0]	2
OTP_LDO3_VOLT[4:0]	1.8 V
OTP_LDO3_PWRUP_SEQ[2:0]	1
OTP_VREFDDR_PWRUP_SEQ[2:0]	3
OTP_SW1_DVS_ENB	dynamic voltage scaling (DVS) mode
OTP_SW2_DVS_ENB	DVS mode
OTP_LDO1_LS_EN	LDO mode
OTP_LDO3_LS_EN	LDO mode
OTP_SW1_RDIS_ENB	enabled
OTP_SW2_RDIS_ENB	enabled
OTP_SW3_RDIS_ENB	enabled
OTP_SW1_DVSSPEED	12.5 mV step each 4.0 µs
OTP_SW2_DVSSPEED	12.5 mV step each 4.0 µs
OTP_SWx_EN_AND_STBY_EN	SW1, SW2, SW3 enabled in RUN and STANDBY
OTP_LDOx_EN_AND_STBY_EN	LDO1, LDO2, LDO3, VREFDDR enabled in RUN and STANDBY
OTP_PWRON_CFG	level sensitive
OTP_SEQ_CLK_SPEED	2 ms time slots
OTP_TGRESET[1:0]	4 s global reset timer
OTP_POR_DLY[2:0]	2 ms RESETBMCU power up delay
OTP_UVDET[1:0]	rising 3.0 V; falling 2.9 V
OTP_I2C_DEGLITCH_EN	I^2C-bus deglitch filter disabled
OTP_VSYSMIN[1:0]	VSYSMIN = 4.3 V

Register	Pre-programmed OTP configuration – A4 configuration
OTP_VIN_ILIM[4:0]	VIN ILIM = 1500 mA
OTP_USBPHYLDO	USBPHY LDO enabled
OTP_USBPHY	USBPHY = 3.3 V
OTP_ACTDISPHY	USBPHY active discharge enabled

5.4 Board description

Figure 1 describes the main elements on the FRDM-PF1510EVM.

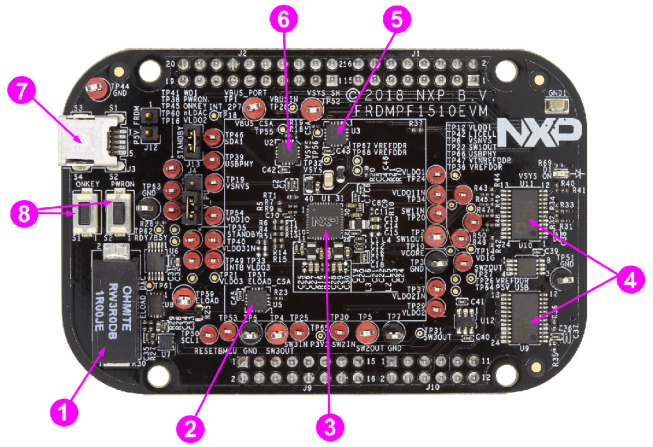


Figure 1. Board description

Table 3. Board description

Number	Name	Description
1	1A ELOAD	electronic load 1.0 A
2	ELOAD CSA	current sense amplifier for the electronic load
3	PF1510	PF1510 PMIC
4	analog MUX	analog multiplexers
5	VSYS CSA	current sense amplifier for VSYS
6	VIN CSA	current sense amplifier for VIN
7	VIN USB input	USB 5.0 V power supply for the VIN
8	ONKEY and PWRON buttons	buttons connected to the ONKEY and PWRON signals

5.4.1 LED description

The following LED is provided as visual output device for the board:

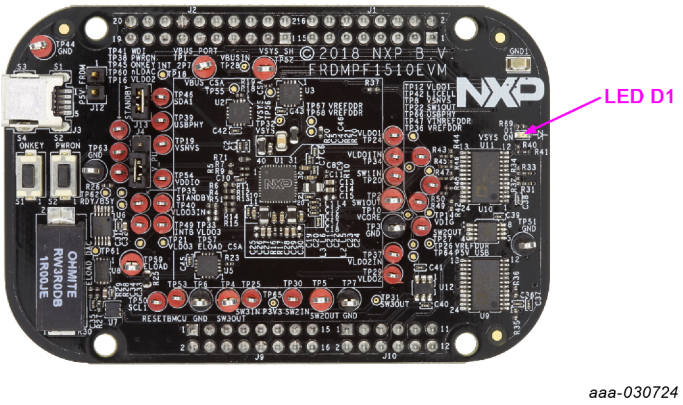


Figure 2. LED location

Table 4. LED description

LED ID	Description
D1	red LED, VSYS on state indicator

5.4.2 Jumper and switch definitions

Figure 3 shows the location of jumpers and switches on the evaluation board.

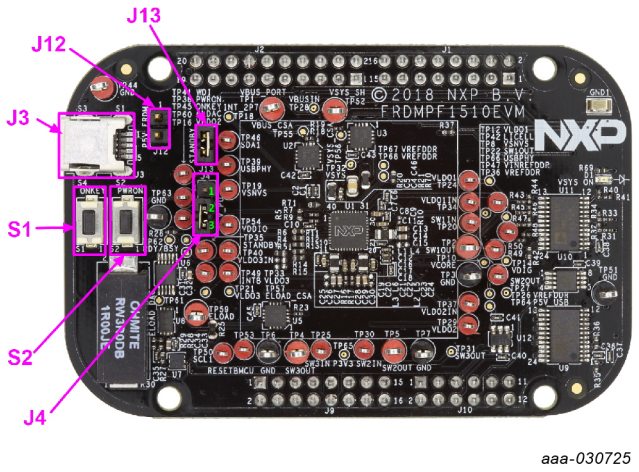


Figure 3. Jumper and switch locations

Table 5 describes the function and settings for each jumper and switch.

Table 5. Jumper and switch definitions

Jumper/switch	Description	Setting	Connection/result
S1	ONKEY	open	connects ONKEY pin to GND when pressed; if configured properly, it causes wake-up event
S2	PWRON	open	connects PWRON pin to GND when pressed; resets the PMIC device
J3	5.0 V USB	-	power supply for the board (J12 shall be opened)
J4	pullup configuration	[1-2]	pullup to VSNVS
		[2-3]	pullup to VDDIO which is supplied by P3V3 coming from the FRDM-KL25Z board
J12	5 V power supply	open	5.0 V from the J3 (USB) is used
		[1-2]	5.0 V is used from the FRDM-KL25Z board (current is limited)
J13	STANDBY pin configuration	open	pull STANDBY pin high
		connected	pull STANDBY pin low to GND

5.4.3 Test point definitions

The following test points provide access to various signals to and from the board.

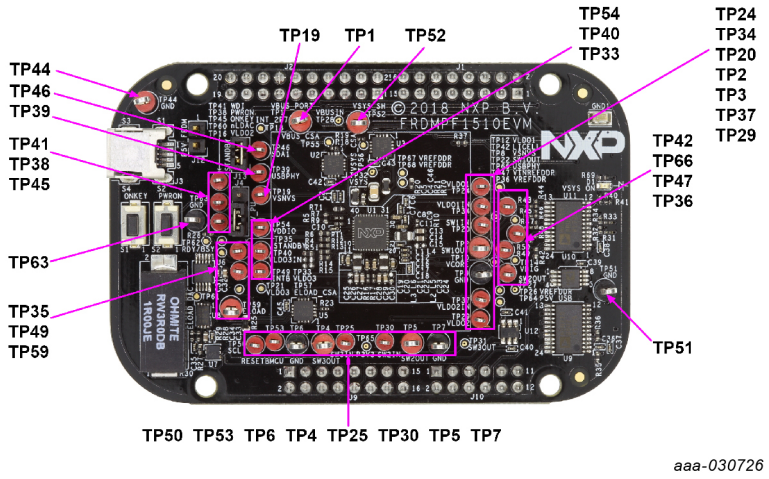


Figure 4. Test point locations

Table 6. Test point definitions

Test point name	Signal name	Description
TP1	VIN_PORT	5.0 V power supply (from USB connector J3)
TP2	SW1OUT	SW1 output
TP3	GND	ground (next to SW1OUT)
TP4	SW3OUT	SW3 output
TP5	SW2OUT	SW2 output
TP6	GND	ground (next to SW3OUT)
TP7	GND	ground (next to SW2OUT)
TP19	VSNVS	VSNVS regulator output
TP20	SW1IN	SW1 input
TP24	VLDO1	VLDO1 regulator output
TP25	SW3IN	SW3 input
TP29	VLDO2	VLDO2 regulator output
TP30	SW2IN	SW2 input
TP33	VLDO3	VLDO3 regulator output
TP34	VLDO1IN	VLDO1 regulator input
TP35	STANDBY	STANDBY input
TP36	VREFDDR	VREFDDR regulator output
TP37	VLDO2IN	VLDO2 regulator input
TP38	PWRON	PWRON input
TP39	USBPHY	USBPHY regulator output

Test point name	Signal name	Description
TP40	VLDO3IN	VLDO3 regulator input
TP41	WDI	watchdog input from microcontroller unit (MCU)
TP42	LICELL	coin cell input
TP44	GND	ground
TP45	ONKEY	ONKEY push-button input
TP46	SDA1	data signal of the I^2C-bus
TP47	VINREFDDR	VREFDDR regulator input
TP49	INTB	interrupt to the MCU
TP50	SCL1	clock signal of the I^2C-bus
TP51	GND	ground
TP52	VSYS_SH	VSYS of PMIC
TP53	RESETBMCU	MCU reset signal
TP54	VDDIO	I/O supply voltage of the PMIC
TP59	ELOAD	electronic load input (connect the tested power supply)
TP63	GND	ground (next to the electronic load)
TP66	USBPHY	USBPHY regulator output

6 FRDM-KL25Z Freedom development platform

The NXP Freedom development platform is a set of software and hardware tools for evaluation and development. It is ideal for rapid prototyping of microcontroller-based applications. The NXP Freedom KL25Z hardware, FRDM-KL25Z, is a simple, yet sophisticated design featuring a Kinetis L series microcontroller, the first microcontroller of the industry built on the Arm Cortex-M0+ core.

6.1 Connecting the FRDM-KL25Z to the board

The FRDM-KL25Z evaluation board was chosen specifically to work with the FRDM-PF1510EVM kit because of its low cost and features. The FRDM-KL25Z board uses the USB, built-in LEDs, and I/O ports available with NXPs Kinetis KL2x family of microcontrollers.

The FRDM-PF1510EVM connects to the FRDM-KL25Z using the four dual row Arduino R3 connectors on the bottom of the board.

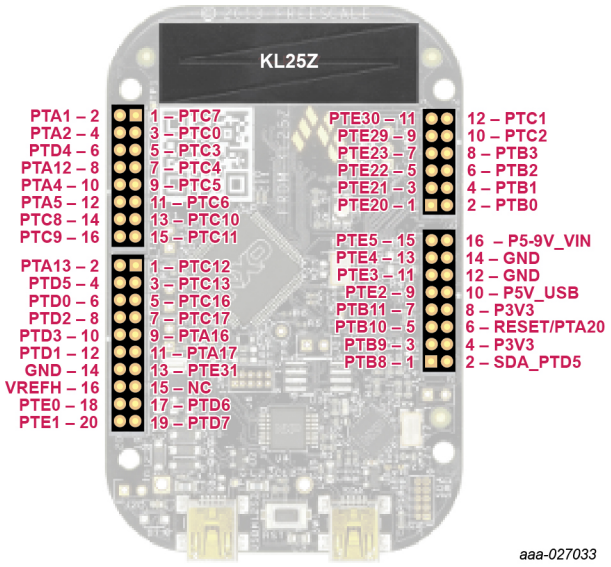


Figure 5. Connecting the FRDM-KL25Z to the FRDM-PF1510EVM

Table 7. FRDM-PF1510EVM to FRDM-KL25Z connections

FRDM-PF1510EVM		FRDM-KL25Z		Pin hardware name		Description
Header	Pin	Header	Pin	FRDM-PF1510EVM	FRDM-KL25Z	
J1	1	J1	1	n.c.	PTC7	not connected
J1	2	J1	2	INTB	PTA1	interrupt to the MCU
J1	3	J1	3	n.c.	PTC0	not connected
J1	4	J1	4	WDI	PTA2	watchdog input from MCU
J1	5	J1	5	n.c.	PTC3	not connected
J1	6	J1	6	nLDAC	PTD4	DAC configuration signal
J1	7	J1	7	n.c.	PTC4	not connected
J1	8	J1	8	RDY/BSY	PTA12	DAC control signal
J1	9	J1	9	n.c.	PTC5	not connected
J1	10	J1	10	MUX_RESETB	PTA4	multiplexer reset
J1	11	J1	11	n.c.	PTC6	not connected
J1	12	J1	12	VDDIO	PTA5	VDDIO power supply
J1	13	J1	13	n.c.	PTC10	not connected
J1	14	J1	14	SCL2	PTC8	clock signal of the I^2C-bus (for additional ICs)
J1	15	J1	15	n.c.	PTC11	not connected
J1	16	J1	16	SDA2	PTC9	data signal of the I^2C-bus (for additional ICs)
J2	1	J2	1	n.c.	PTC12	not connected
J2	2	J2	2	PWRON	PTA13	PWRON input

FRDM-PF1510EVM		FRDM-KL25Z		Pin hardware name		Description
Header	Pin	Header	Pin	FRDM-PF1510EVM	FRDM-KL25Z	
J2	3	J2	3	n.c.	PTC13	not connected
J2	4	J2	4	STANDBY	PTD5	STANDBY input
J2	5	J2	5	n.c.	PTC16	not connected
J2	6	J2	6	RESETBMCU	PTD0	MCU reset signal
J2	7	J2	7	n.c.	PTC17	not connected
J2	8	J2	8	VSYS_CSA_ALERT	PTD2	alert signal from the VSYS current shunt
J2	9	J2	9	ELOAD_CSA_ALERT	PTA16	alert signal from the ELOAD current shunt
J2	10	J2	10	n.c.	PTD3	not connected
J2	11	J2	11	n.c.	PTA17	not connected
J2	12	J2	12	VBUS_CSA_ALERT	PTD1	alert signal from the VBUS current shunt
J2	13	J2	13	n.c.	PTE31	not connected
J2	14	J2	14	GND	GND	ground
J2	15	J2	15	n.c.	n.c.	not connected
J2	16	J2	16	n.c.	VREFH	not connected
J2	17	J2	17	n.c.	PTD6	not connected
J2	18	J2	18	SDA1	PTE0	data signal of the I^2C-bus (PF1510)
J2	19	J2	19	n.c.	PTD7	open
J2	20	J2	20	SCL1	PTE1	clock signal of the I^2C-bus (PF1510)
J10	1	J10	1	n.c.	PTE20	not connected
J10	2	J10	2	n.c.	PTB0	not connected
J10	3	J10	3	n.c.	PTE21	not connected
J10	4	J10	4	n.c.	PTB1	not connected
J10	5	J10	5	n.c.	PTE22	not connected
J10	6	J10	6	2V5_ADC	PTB2	voltage reference for ADC
J10	7	J10	7	n.c.	PTE23	not connected
J10	8	J10	8	ADC_1	PTB3	analog signal to ADC1
J10	9	J10	9	n.c.	PTE29	not connected
J10	10	J10	10	ADC_0	PTC2	analog signal to ADC0
J10	11	J10	11	n.c.	PTE30	not connected
J10	12	J10	12	n.c.	PTC1	not connected
J9	1	J9	1	n.c.	PTB8	not connected
J9	2	J9	2	P3V3	SDA_PTD5	3.3 V coming from the Freedom board

FRDM-PF1510EVM		FRDM-KL25Z		Pin hardware name		Description
Header	Pin	Header	Pin	FRDM-PF1510EVM	FRDM-KL25Z	
J9	3	J9	3	n.c.	PTB9	not connected
J9	4	J9	4	P3V3	3V3	3.3 V coming from the Freedom board
J9	5	J9	5	n.c.	PTB10	not connected
J9	6	J9	6	P3V3	RESET/PTA20	3.3 V coming from the Freedom board
J9	7	J9	7	n.c.	PTB11	not connected
J9	8	J9	8	P3V3	3V3	3.3 V coming from the Freedom board
J9	9	J9	9	n.c.	PTE2	not connected
J9	10	J9	10	P5V_USB	5V	5 V coming from the Freedom board
J9	11	J9	11	n.c.	PTE3	not connected
J9	12	J9	12	GND	GND	ground
J9	13	J9	13	n.c.	PTE4	not connected
J9	14	J9	14	GND	GND	ground
J9	15	J9	15	n.c.	PTE5	not connected
J9	16	J9	16	n.c.	P5-9V_VIN	not connected

7 Installing the software and setting up the hardware

7.1 Set up PF1510GUI on your computer

1. Download **PF1510GUI.zip** from http://www.nxp.com/FRDM-PF1550EVM. Choose the 32-bit or 64-bit version regarding the system installed on your PC.
2. Extract all the files to any desired folder on your PC.
3. Plug the evaluation board.
4. Launch the GUI (no installation is necessary, GUI can be directly launched by clicking the file **PF1510_x_Bx.jar**).

7.2 Configuring the hardware and using the GUI for control and monitoring

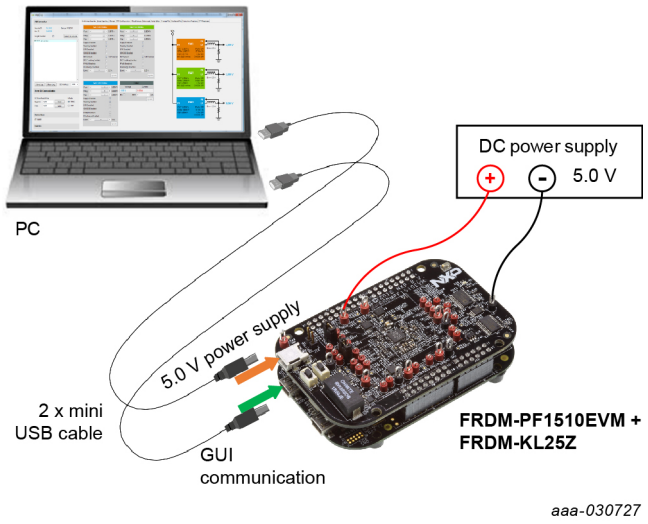
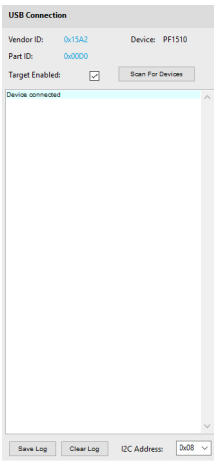


Figure 6. Hardware configuration

1. Apply input voltage to the board.
   - First solution is to use power directly from the FRDM-KL25Z by connecting J12 jumper. Advantage of this configuration is that only one USB port (USB for GUI communication) is needed. This solution may have limited performance because of the current capability of the USB port.
   - Second possibility is to use 5.0 V either from USB input (J3) or from DC power supply. In these cases, keep J12 open. The DC power supply connection is recommended for higher currents.
2. Connect the mini-USB cable from a PC to the KL25Z USB port on the FRDM-KL25Z board.
3. Windows automatically installs the necessary drivers. Wait for this operation to complete.
4. Launch the PF1510 GUI.
5. In the PF1510 GUI window, click the **Scan For Devices** button in the top-left corner. A confirmation message that a valid device is available is logged.



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6. Enable the communication by clicking the **Target Enabled:** checkbox. The window turns from gray to color.
7. The GUI installation and hardware setup now are complete.

7.3 Understanding and using the GUI

7.3.1 GUI structure for PF1510

Figure 7 shows the different components of the GUI.

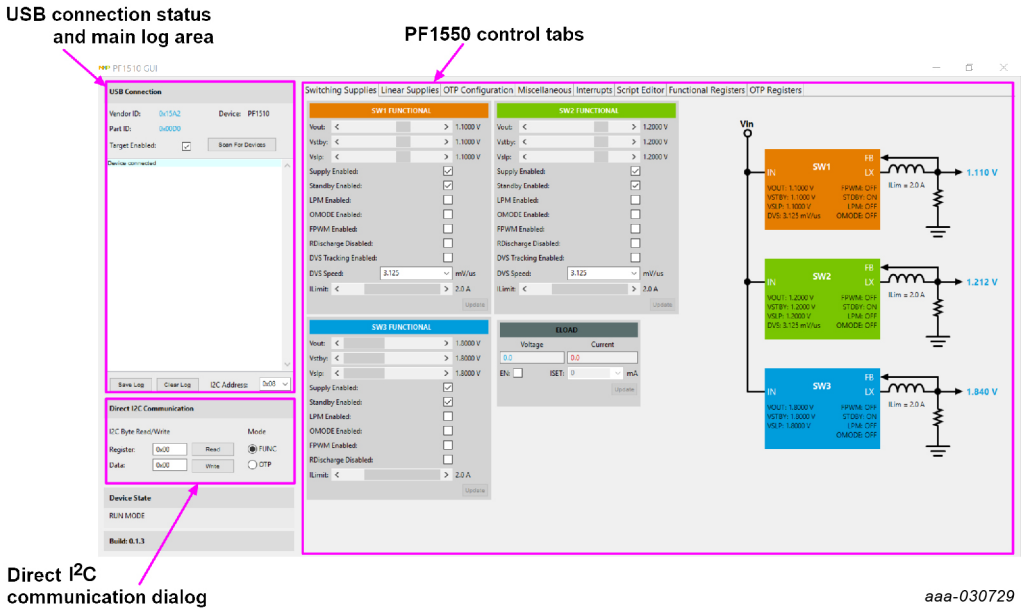

Figure 7. GUI components

7.3.2 GUI panels

When the GUI is launched, it looks for a PF1510 target board connected via the USB cable. If connected, the USB connection panel displays the vendor ID: 0x15A2, and part ID: 0x00D0.

The main log window displays messages, example, when the board is connected (PF1510 attached) and when the board was removed (PF1510 removed).

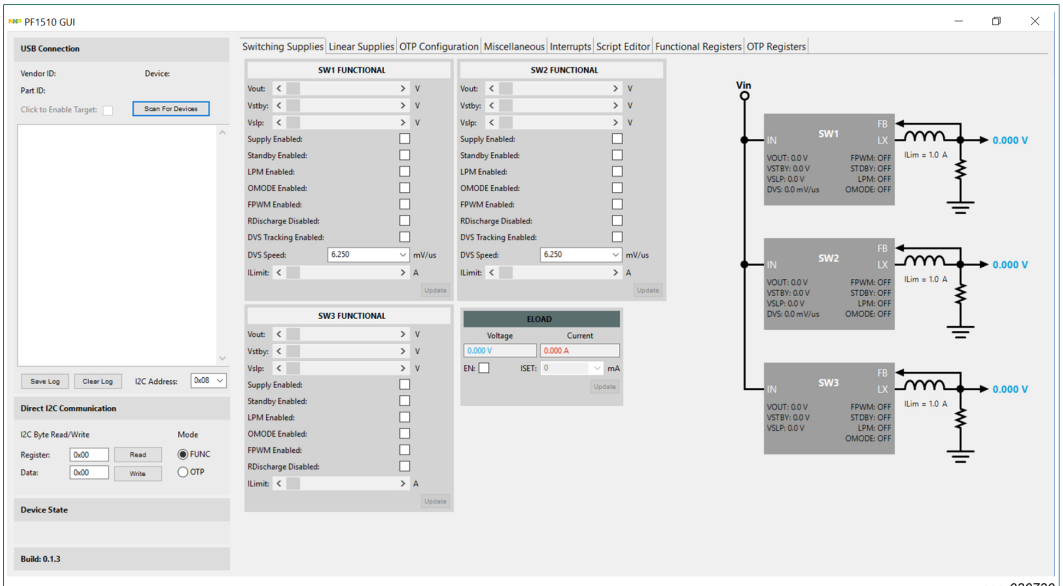

Figure 8. GUI startup

Pressing the **Scan For Devices** button attempts to read from each of the eight permissible I^2C-bus device addresses. The results are displayed in the main log window. If multiple PMIC devices are detected, the GUI can be configured to communicate with a particular device by selecting the corresponding device address.

Note: *The GUI can communicate with only one PMIC device at a time.*

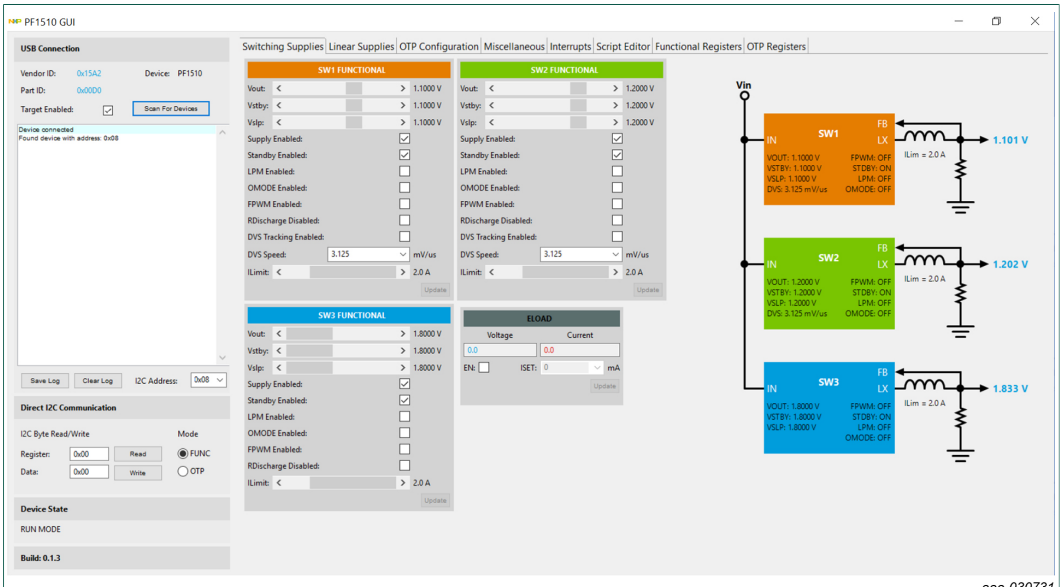

Figure 9. GUI connected to the target board

7.3.3 Switching supplies panel

The switching supplies panel allows users to adjust the functional parameters of each supply.

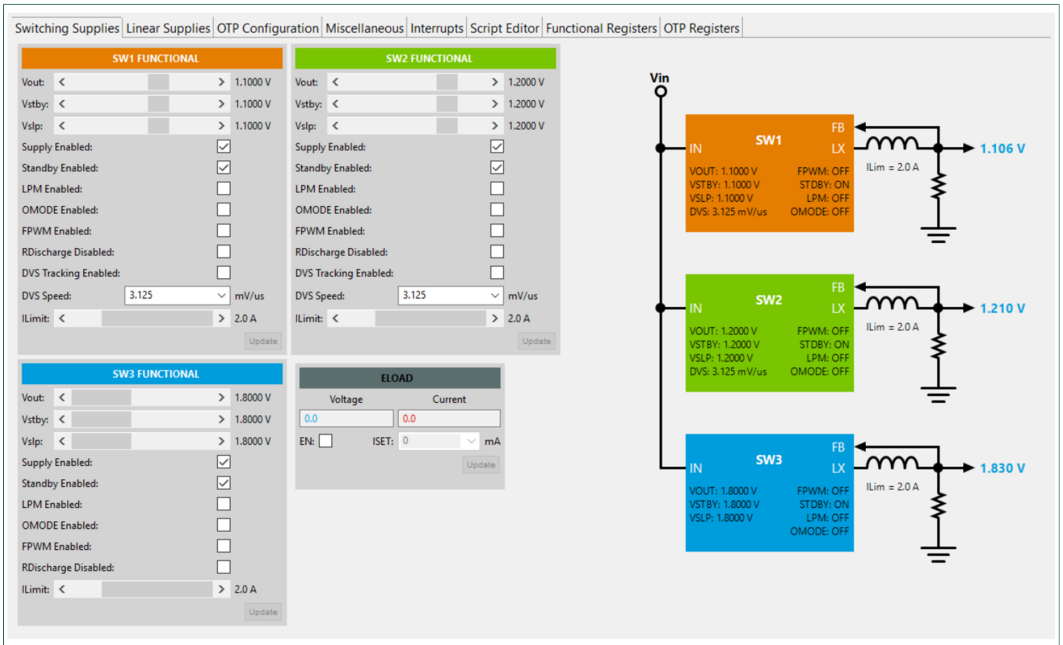

Figure 10. Switching supplies panel

To change supply parameters, click and adjust the desired control. An **Update** button appears whenever a change is made, and pressing the **Update** button writes the change to the PMIC.

Note: *Multiple changes can be made at a time, and all changes are written when the* ***Update*** *button is pressed.*

7.3.4 Linear supplies panel

The linear supplies panel allows users to adjust the functional parameters of each linear regulator. To change supply parameters, click and adjust the desired control.

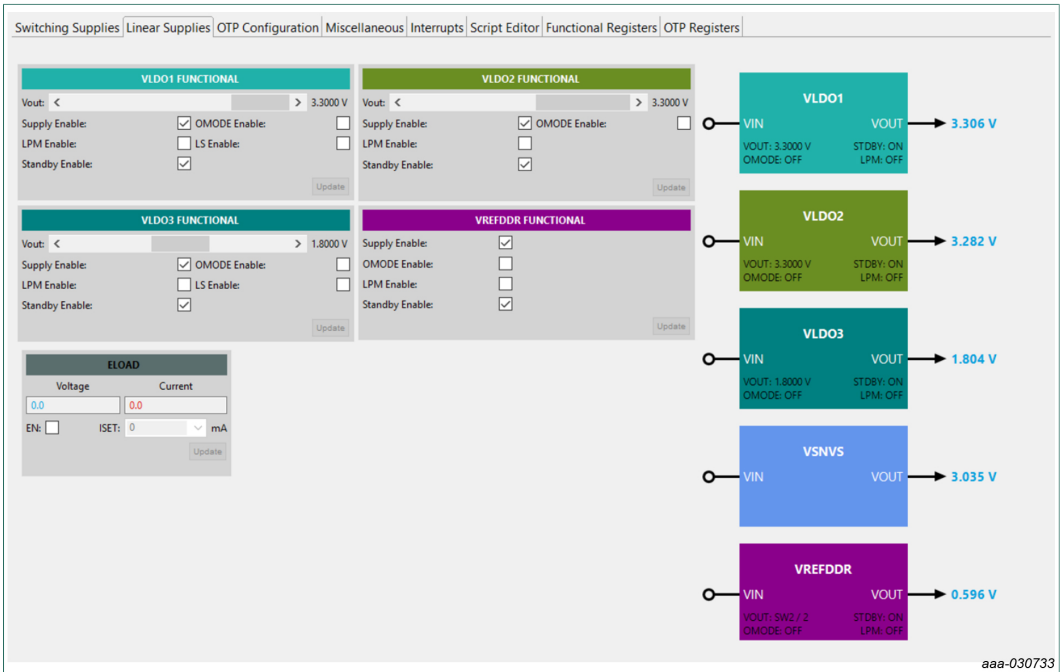

Figure 11. Linear supplies panel

An **Update** button appears whenever a change is made, and pressing the **Update** button writes the change to the PMIC.

Note: *Multiple changes can be made at a time, and all changes are written when the* ***Update*** *button is pressed.*

7.3.5 OTP configuration panel

The OTP configuration panel allows access and editing of the PF1510 startup parameters.

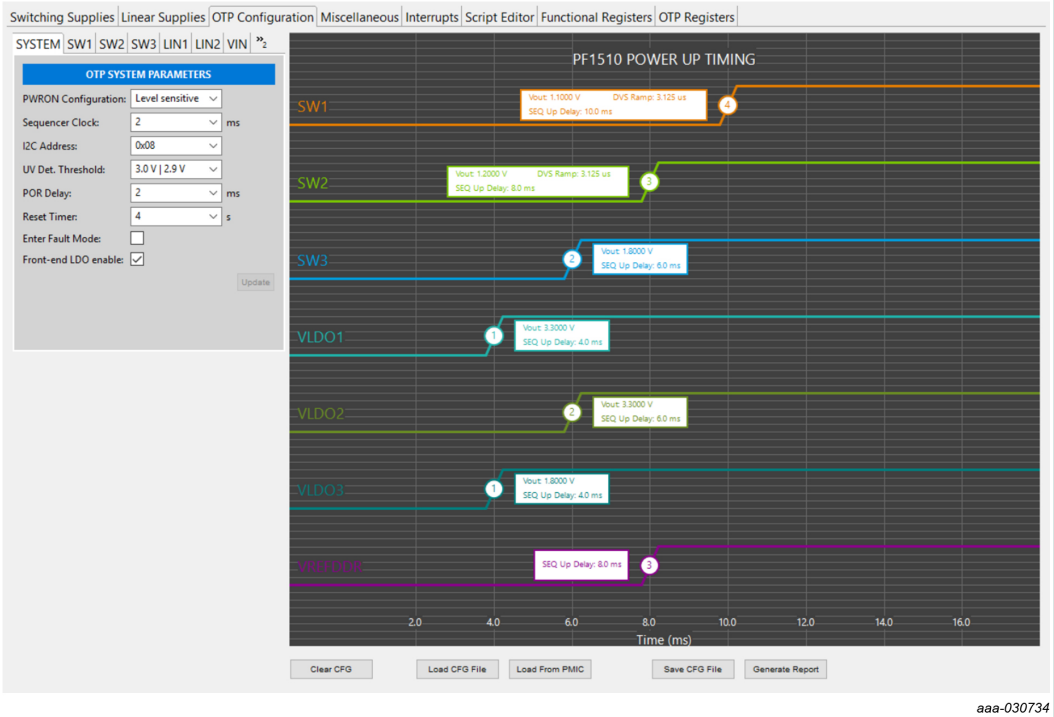

Figure 12. OTP configuration panel

Initially, the panel display is the OTP configuration read from PMIC PF1510.

The **Load CFG File** button opens the configuration file open dialog, and populates the panel with the parameters contained in this file.

The **Load From PMIC** button loads the OTP configuration data from the PMIC PF1510 of the evaluation board.

7.3.6 Miscellaneous panel

The miscellaneous panel contains general-purpose commands and power up and down sequencing configuration.

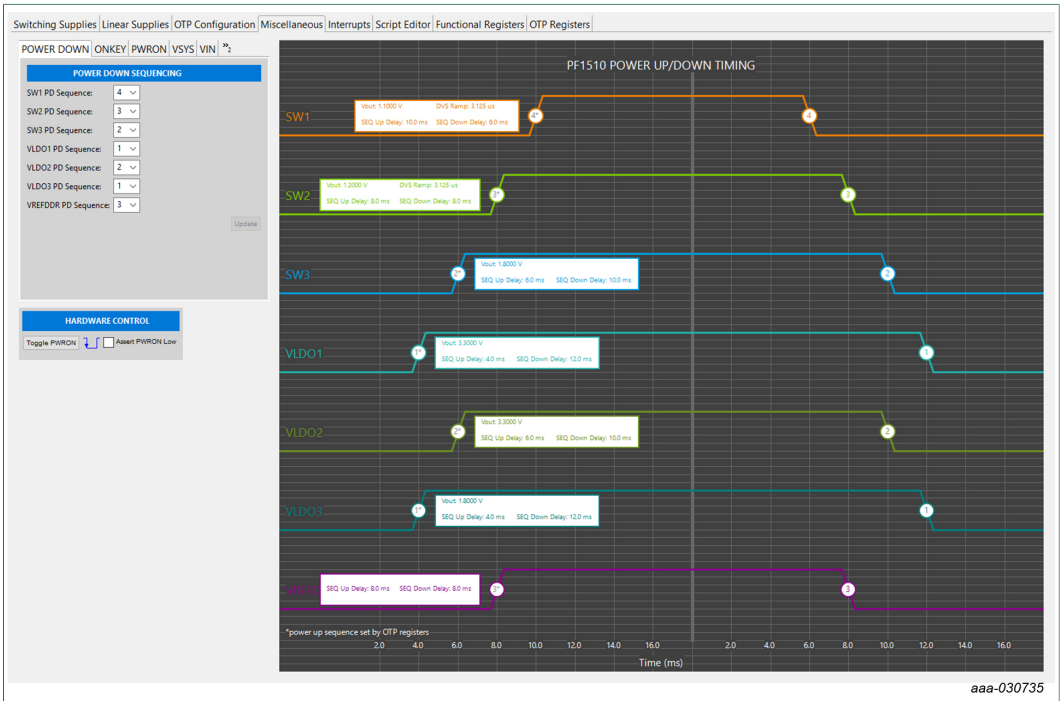

Figure 13. Miscellaneous panel

7.3.7 Interrupts panel

The interrupts panel displays the state of all PF1510 interrupts.

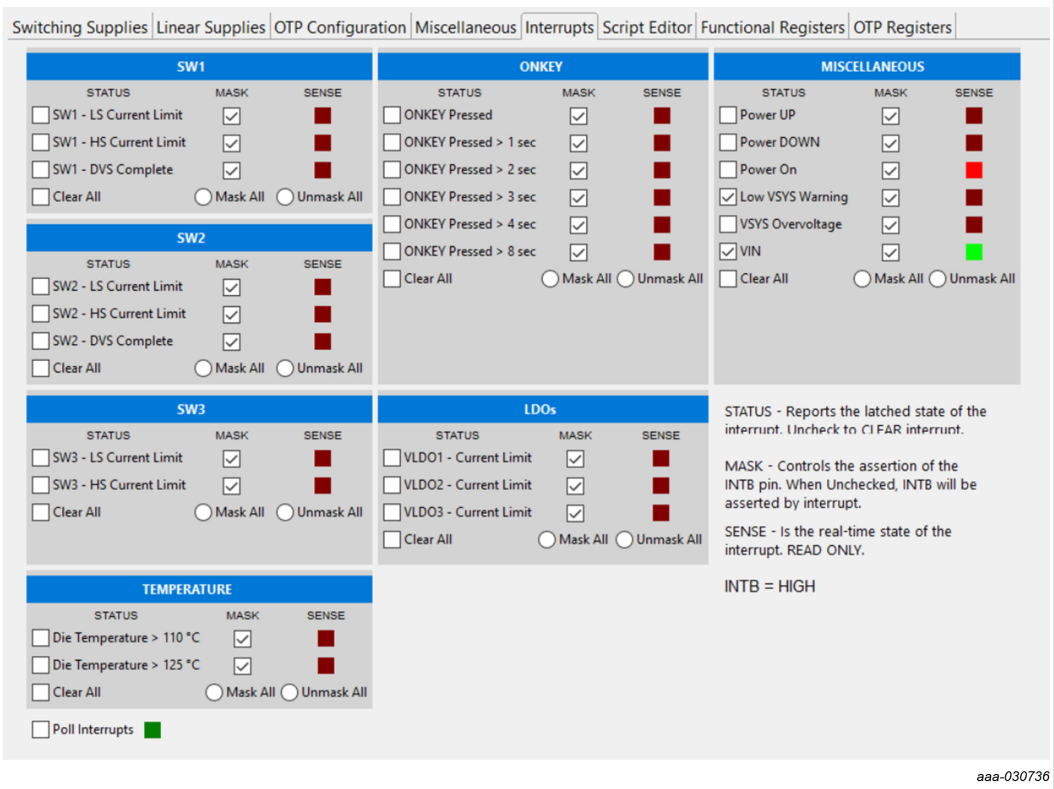

Figure 14. Interrupts panel

The **Interrupts** tab displays status, mask, and sense registers for INT0, INT1, INT3, and INT4. Selecting the **Poll Interrupts** checkbox enables update of this information with period of 500 ms. To activate interrupt, the appropriate mask has to be set. When an interrupt occurs, the appropriate checkbox is selected. Interrupt can be then cleared by unchecking this checkbox.

The state of the PF1510 INTB pin is displayed, and updated asynchronously. Interrupts that are unmasked, cause the INTB pin to go LOW while the interrupt condition exists.

The PF1510 target hardware detects when the INTB pin goes LOW, and sends a message to the GUI to indicate that an interrupt has occurred. The INTB label on the panel is LOW until the interrupt condition is cleared.

7.3.8 Script editor panel

The script editor panel allows the user to write and execute scripts that exercise various functions on the PF1510 PMIC. These functions include setting voltages on the regulators, reading and writing I^2C-bus addresses, and clearing interrupts. Script commands can be written directly in an editor window. Alternatively, the user can build the scripts by selecting commands from drop-down menus and entering the appropriate values.

The scripts are executed within the **Files:** section of the panel, and the results are displayed in the **Script Log** section.

Completed scripts can be saved as text files for later use. Commands can be generated easily.

Figure 15 shows the main elements in the **Script Editor** panel.

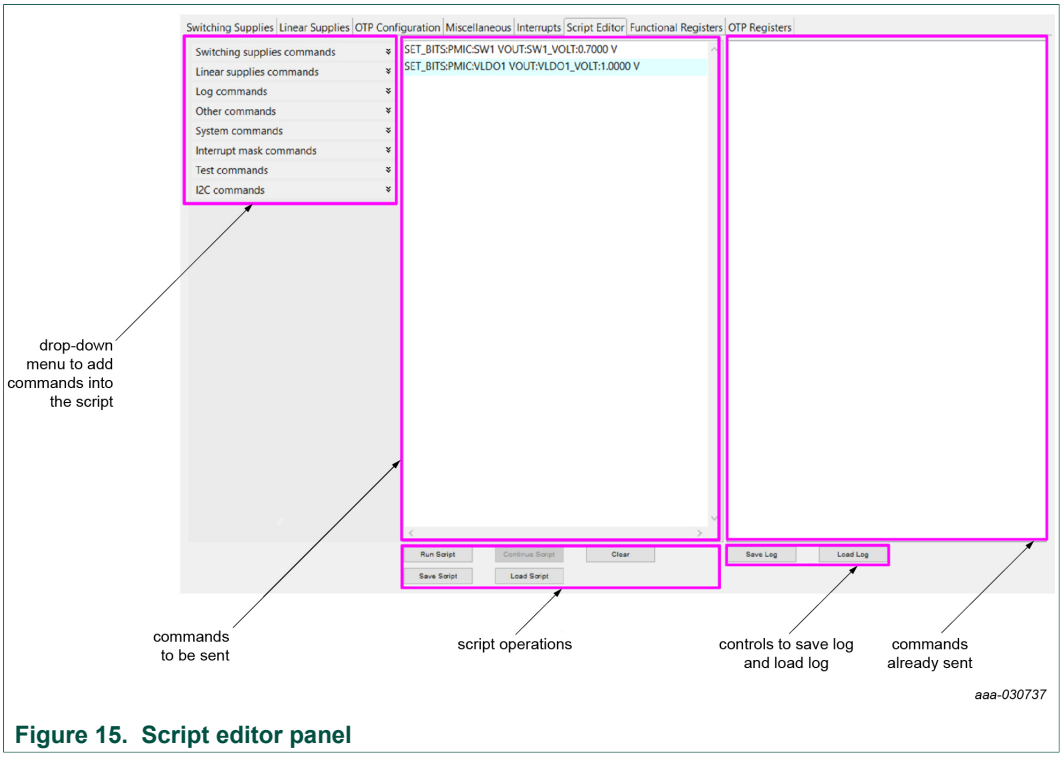

Figure 15. Script editor panel

7.3.9 Functional registers panel

In the functional registers panel, clicking a checkbox immediately sets or clears the corresponding register bit. Key bit fields in each register are decoded to help displaying the actual state of each parameter.

Registers are grouped within each tab by function.

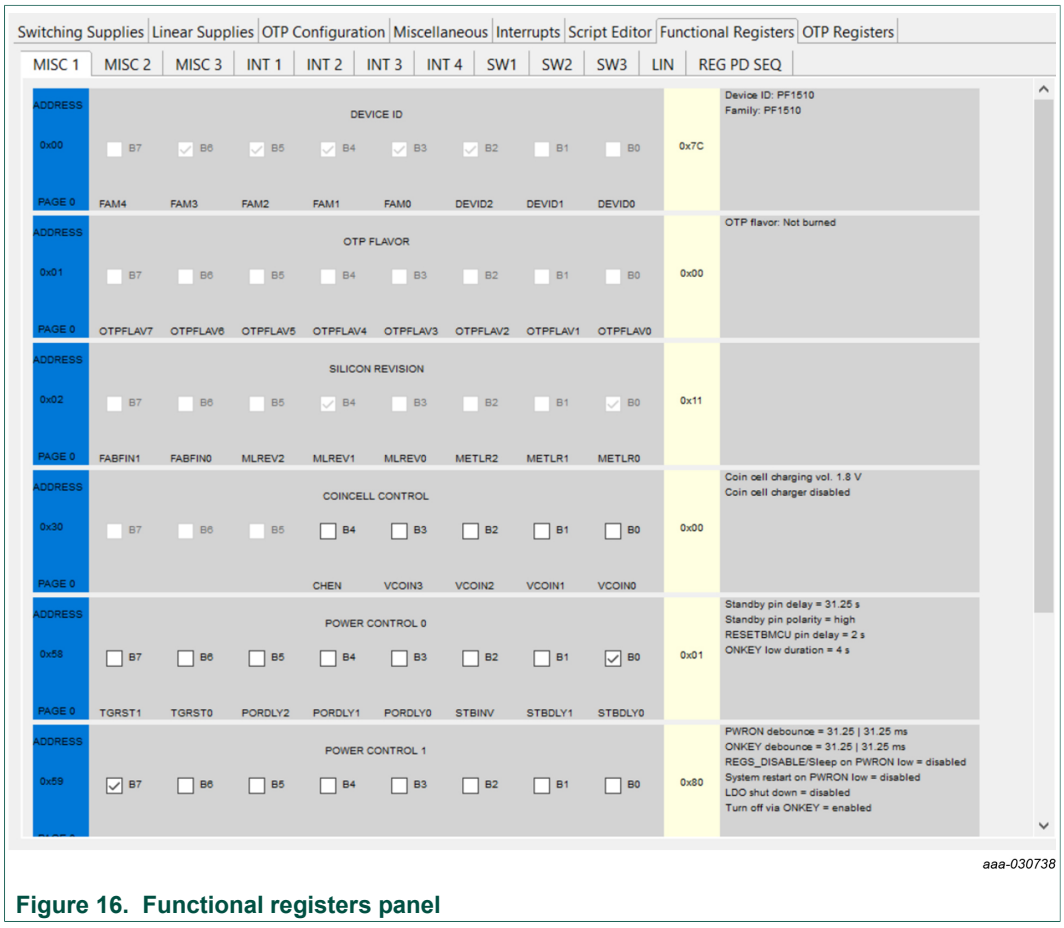

Figure 16. Functional registers panel

7.3.10 OTP registers panel

The OTP registers panel provides bit-level access to each register.

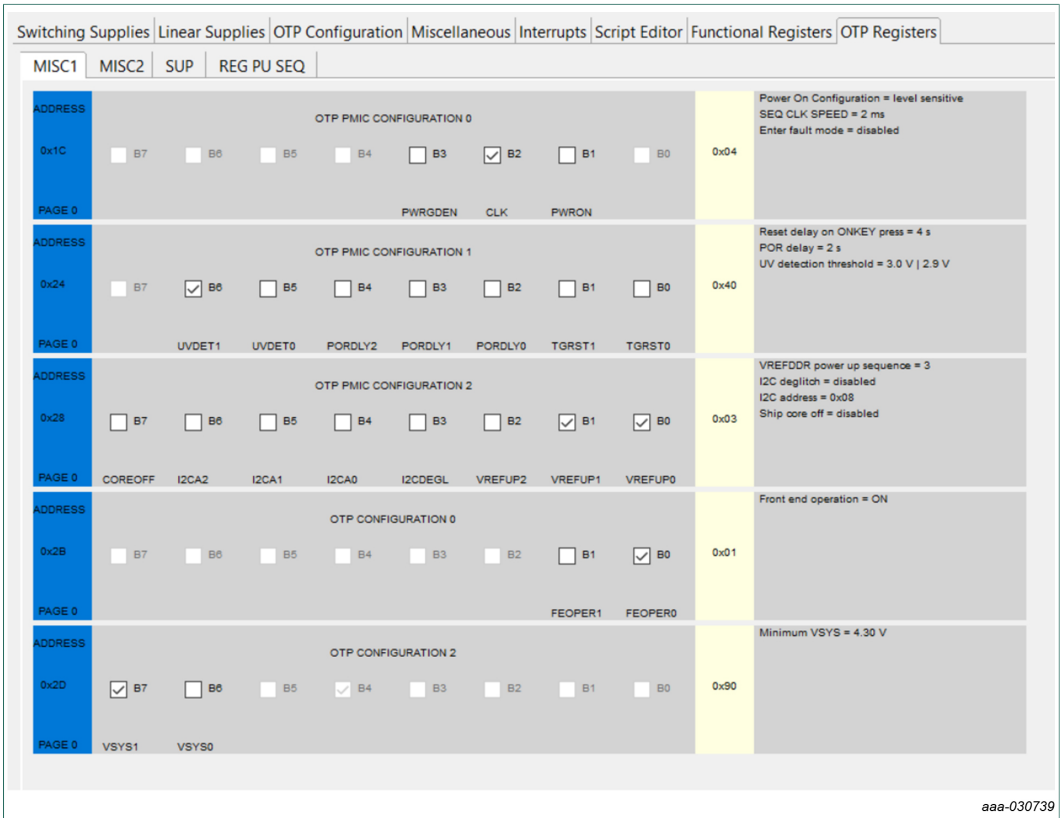

Figure 17. OTP registers panel

Clicking a checkbox immediately sets or clears the corresponding register bit. Key bit fields in each register are decoded to help displaying the actual state of each parameter.

Registers are grouped within each tab by function.

While in edit configuration (TBB mode), the OTP data import, export, and compare buttons are visible. The buttons function the same as the buttons on the OTP configuration panel.

8 Schematics, board layout and bill of materials

Schematics, board layout and bill of materials are available on the tool summary page: http://www.nxp.com/FRDM-PF1510EVM.

9 References

Following are URLs where you can obtain information on related NXP products and application solutions:

Support page	Description	URL
FRDM-PF1510EVM	tool summary page	http://www.nxp.com/FRDM-PF1510EVM
PF1510	product summary page	http://www.nxp.com/PF1510
FRDM-KL25Z	Freedom development platform	http://www.nxp.com/FRDM-KL25Z

10 Revision history

Revision history

Rev	Date	Description
v.1.0	20180618	initial version

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