

PIN Diode Shunt Switch Element

50 MHz to 10 GHz



MASW-011163

Rev. V2

Features

- 3 Terminal LPF Broadband Shunt Structure
- 50 MHz - 10 GHz Broadband Frequency
- >40 W Peak Power Handling
- <0.38 dB Shunt Insertion loss
- >31 dB Shunt Isolation
- RoHS* Compliant

Applications

- Wireless Telecommunications Infrastructure & Test Instrument Applications

Description

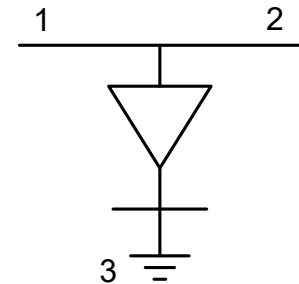
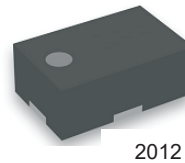
The MASW-011163 is a broadband, high linearity, medium power shunt switch element in a lead free 1.9 x 1.1 mm DFN surface mount plastic package.

This device is designed for wireless telecommunications infrastructure and test instrument applications. It is also suited for other applications in 0.05 ~ 10 GHz.

Ordering Information

Part Number	Package
MASW-011163-20120T	500 Piece Reel

Pin Out / Schematic



Pin Configuration³

Pin #	Pin Name	Description
1	RF _{IN}	RF Input
2	RF _{OUT}	RF Output
3	Paddle ⁴	Ground

- MACOM recommends connecting unused package pins to ground.
- The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

Electrical Specifications: T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Breakdown Voltage (V _B)	I _R = 10 μA	V	200	275	—
Insertion Loss (I _L)	V _R = 25 V, 512 MHz V _R = 25 V, 2.7 GHz	dB	—	0.10 0.38	—
Isolation (I _{SO})	I _F = 10 mA, 512 MHz I _F = 10 mA, 2.7 GHz	dB	—	39 31	—
Input / Output Return Loss	V _R = 25 V, 512 MHz V _R = 25 V, 2.7 GHz	dB	—	24 12	—
Minority Carrier Lifetime (T _L)	I _F = 10 mA, I _R = 6 mA, @ 50%	ns	—	1000	—

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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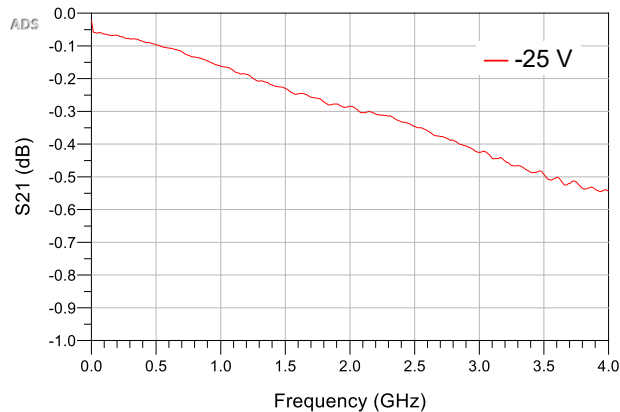
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Absolute Maximum Ratings

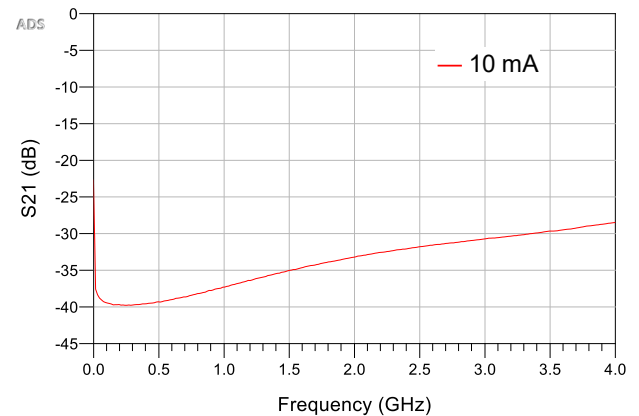
Parameter	Absolute Maximum
Breakdown Voltage	275 V
Forward Current	200 mA
Junction Temperature	+175°C
Storage Temperature	-65°C to +150°C
Assembly Temperature	+260°C Per JEDEC STD-J-20C

Typical Performance Curves

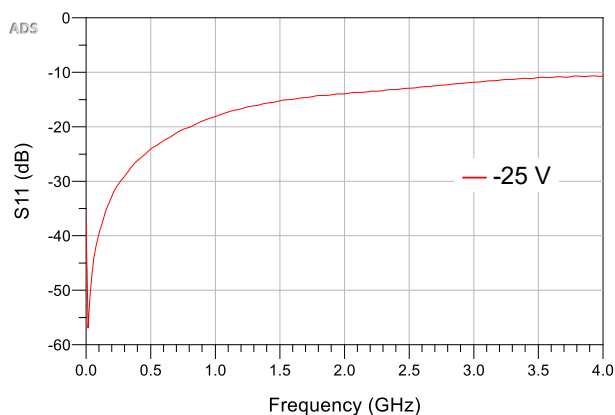
Insertion Loss



Isolation



Input Return Loss



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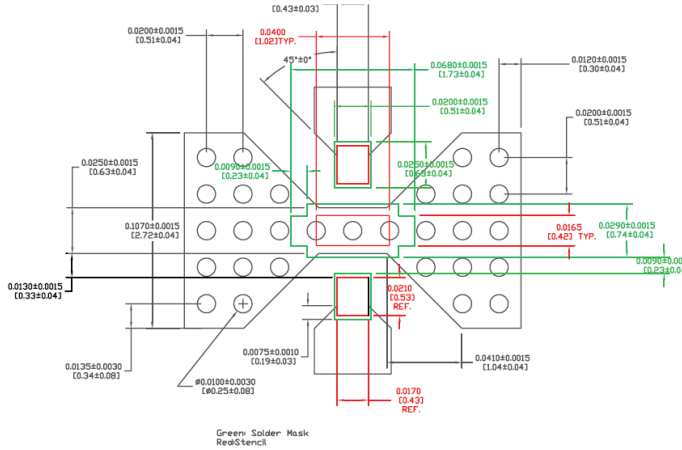
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Printed Circuit Board Layout

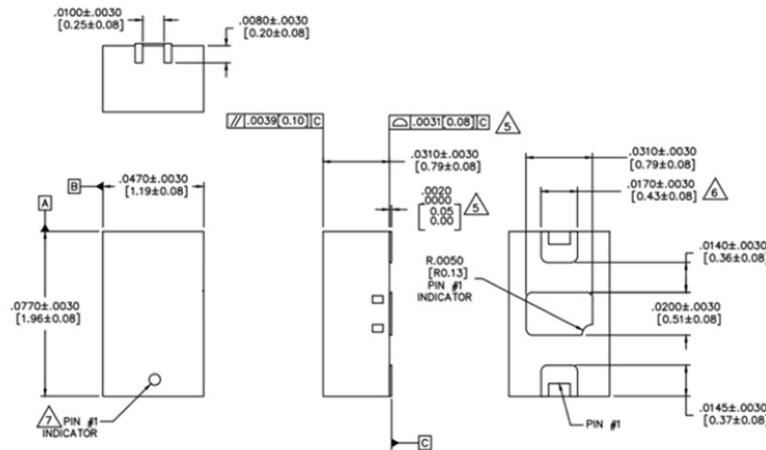


NOTE: If possible, use copper filled vias underneath pin 3 for better thermals; otherwise, use vias that are plated through, filled and plated over.

Solder mask should provide a 60 μm clearance between copper pad and solder mask. Rounded pkg pads should have matching rounded solder mask openings.

Use circles or squares for the thermal land stencil such that only get 50% to 80% solder paste coverage.

Outline (2012)



NOTES

1. DIMENSIONS DO NOT INCLUDE MOLD FLASHING
2. BURRS AND DUMBAR SHALL NOT EXCEED 0,002" PER SURFACE
3. LEAD CO-PLANARITY IS 0,003" MAXIMUM

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