LP2951JAN Series of Adjustable Micropower Voltage Regulators

Check for Samples: LP2951JAN

FEATURES

- **High Accuracy Output Voltage**
- **Ensured 100mA Output Current**
- **Extremely Low Quiescent Current**
- **Low Dropout Voltage**
- **Extremely Tight Load and Line Regulation**
- **Very Low Temperature Coefficient**
- **Use as Regulator or Reference**
- **Needs Minimum Capacitance for Stability**
- **Current and Thermal Limiting**
- **Stable with Low-ESR Output Capacitors (10mΩ to 6Ω)**
- **Error Flag Warns of Output Dropout**
- **Logic-Controlled Electronic Shutdown**
- **Output Programmable from 1.24 to 29V**

DESCRIPTION

The LP2951 is a micropower voltage regulator with very low quiescent current (75µA typ.) and very low dropout voltage (typ. 40mV at light loads and 380mV at 100mA). It is ideally suited for use in battery-powered systems. Furthermore, the quiescent current increases only slightly in dropout, prolonging battery life.

An additional feature is an error flag output which warns of a low output voltage, often due to falling batteries on the input. It may be used for a power-on reset. A second feature is the logic-compatible shutdown input which enables the regulator to be switched on and off. Also, the part may be pin-strapped for a 5V, 3V, or 3.3V output (depending on the version), or programmed from 1.24V to 29V with an external pair of resistors.

Careful design of the LP2951 has minimized all contributions to the error budget. This includes a tight initial tolerance (0.5% typ.), extremely good load and line regulation (0.05% typ.) and a very low output voltage temperature coefficient, making the part useful as a low-power voltage reference.

Connection Diagram

Top View

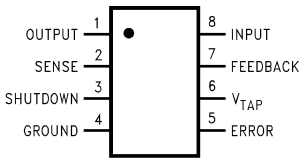
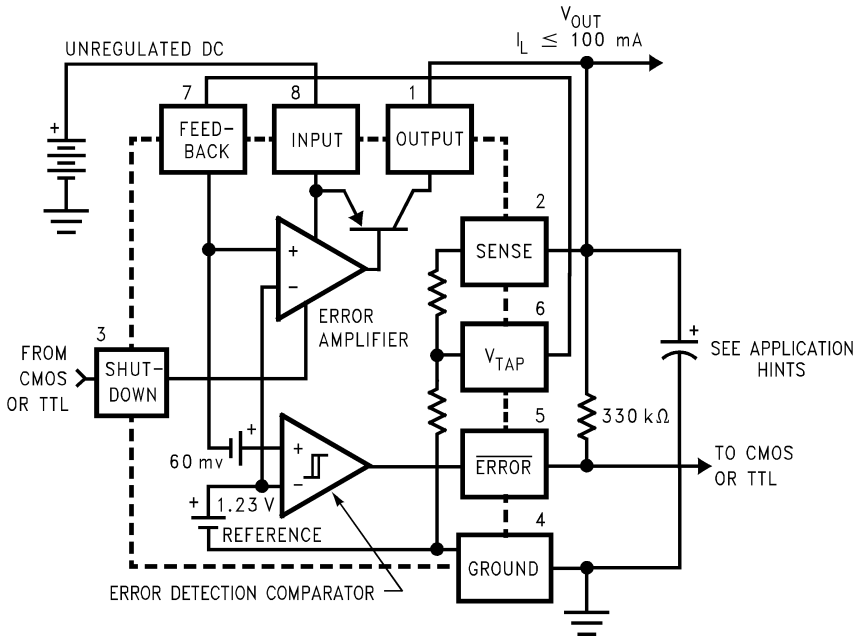
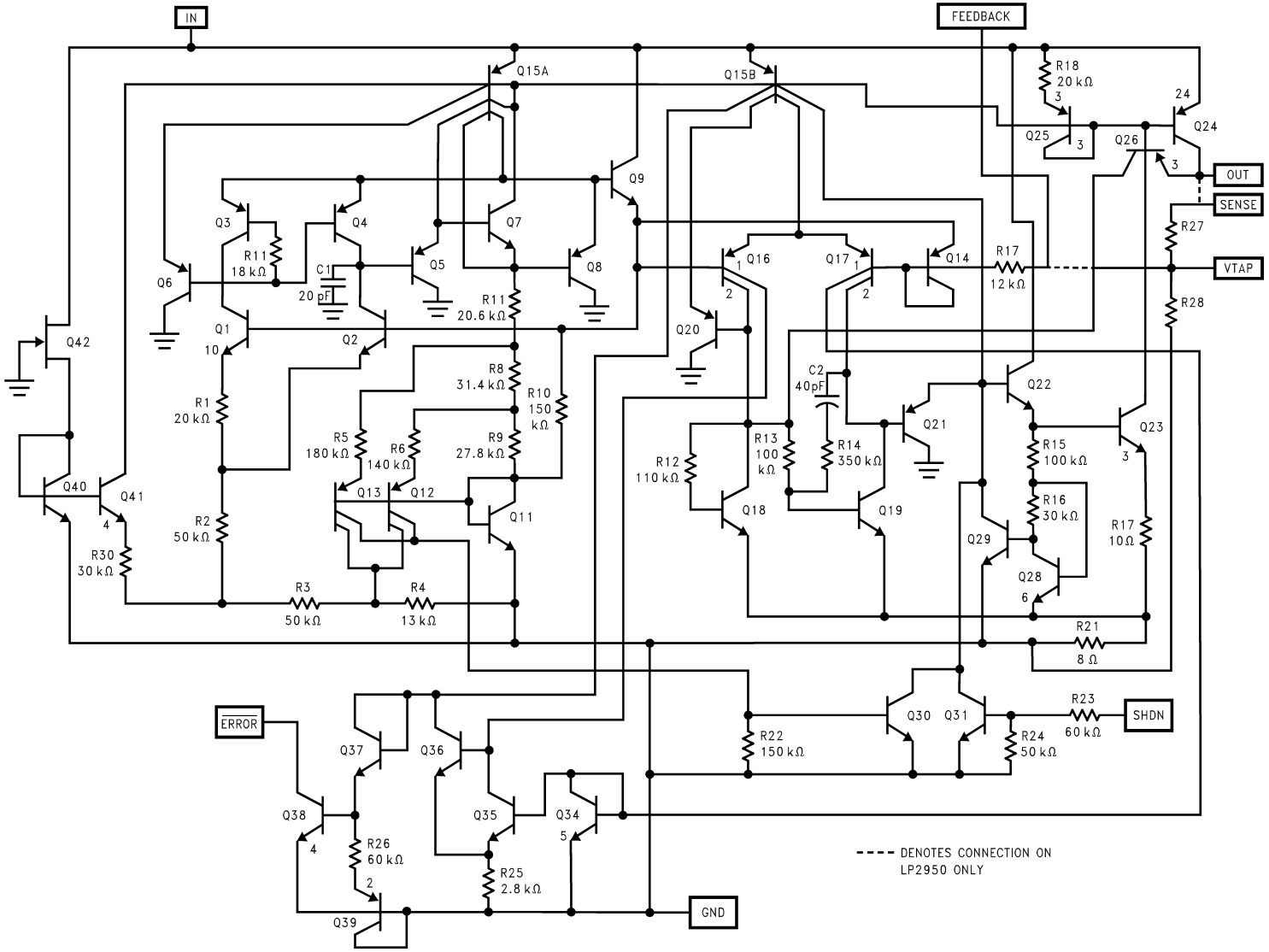


Figure 1. CDIP Package
See Package Number NAB0008A

Block Diagram



Schematic Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Input Supply Voltage			−0.3 to +30V
Shutdown Input Voltage(2)			−0.3 to +30V
Error Comparator Output Voltage(2)			−0.3 to +30V
Feedback Input Voltage(2)(3)			−1.5 to +30V
Power Dissipation(4)		CDIP	1.0 W at 25°C
Junction Temperature (T_J)			+160°C
Ambient Storage Temperature Range			−65°C ≤ T_A ≤ +150°C
Ambient Operating Temperature Range			−55°C ≤ T_A ≤ +125°C
Lead Temperature (Soldering 10 Seconds)			260°C
Thermal Resistance	θ_{JA}	CDIP (Still Air at 0.5W)	131°C/W
		CDIP (500LF/Min Air flow at 0.5W)	75°C/W
	θ_{JC}	CDIP	21°C/W
ESD Rating(5)			500V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The specified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) May exceed input supply voltage.
(3) When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(5) Human body model, 1.5 kΩ in series with 100 pF.

Table 1. Quality Conformance Inspection Mil-Std-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	–55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	–55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	–55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	–55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	–55

JL2951 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified. V_{IN} = 6V, I_L = −100µA, C_L = 3.3µF, V_O = 5V (Nominal), V_{SD} = 0.6V

PARAMETER		TEST CONDITIONS	NOTES	MIN	MAX	UNIT	SUBGROUPS
V_O	Output Voltage			4.975	5.025	V	1
				4.94	5.06	V	2, 3
$V_{O\ Line}$	Line Regulation	6V ≤ V_{IN} ≤ 30V, I_L = –1mA		–5.0	5.0	mV	1
				–25	25	mV	2, 3
$V_{O\ Load}$	Load Regulation	–100µA ≤ I_L ≤ –100mA		–5.0	5.0	mV	1
				–25	25	mV	2, 3
V_D	Dropout Voltage	I_L = –100mA			450	mV	1
					600	mV	2, 3
					80	mV	1
					150	mV	2, 3
I_G	Ground Current	I_L = –100mA,			12	mA	1
					14	mA	2, 3
					120	µA	1
					140	µA	2, 3
		V_O = 15V, V_{IN} = 30V			120	µA	1
					140	µA	2, 3
		V_{IN} = 30V, V_O = 15V			15	mA	1
					20	mA	2, 3
$I_{G\ Diff}$	Ground Current Change	6V ≤ V_{IN} ≤ 30V		–30	30	µA	1
				–50	50	µA	2, 3
I_{GDO}	Dropout Ground Current	V_{IN} = 4.5V			170	µA	1
					200	µA	2, 3
$V_{Th\ L}$	Error Comparator Lower Threshold Voltage			0.0	0.8	mV	1, 2, 3
$V_{Th\ U}$	Error Comparator Upper Threshold Voltage			2.0	30	mV	1, 2, 3
θ_R	Thermal Regulation	V_{IN} = 30V, I_L = –50mA, 2ms ≤ T ≤ 10ms		–12.5	12.5	mV	1
I_{SC}	Current Limit	V_O = 0V			200	mA	1
					220	mA	2, 3
I_{GSC}	Ground Current At Current Limit	V_O = 0V			20	mA	1
					25	mA	2, 3
V_{Ref}	Reference Voltage			1.22	1.25	V	1
				1.20	1.26	V	2, 3
$V_{R\ Line}$	Reference Voltage Line Regulation	2.3V ≤ V_{IN} ≤ 30V		–1.9	1.9	mV	1
				–10	10	mV	2, 3
$V_{R\ Load}$	Reference Voltage Output Regulation	1.2V ≤ V_O ≤ 29V, V_{IN} = 30V		–1.2	1.2	mV	1
				–5.0	5.0	mV	2, 3
I_{FB}	Feedback Pin Bias Current				40	nA	1
					60	nA	2, 3
I_{OH}	Error Comparator Output Leakage Current	V_O = 30V			1.0	µA	1
					2.0	µA	2, 3
V_{OL}	Error Comparator Output Low Voltage	V_{IN} = 4.5V, V_{SD} = 2V			250	mV	1
					400	mV	2, 3

JL2951 Electrical Characteristics DC Parameters (continued)

The following conditions apply, unless otherwise specified. V_{IN} = 6V, I_L = −100µA, C_L = 3.3µF, V_O = 5V (Nominal), V_{SD} = 0.6V

PARAMETER		TEST CONDITIONS	NOTES	MIN	MAX	UNIT	SUBGROUPS
I_{SD}	Shutdown Pin Input Current	V_{SD} = 2.4V			50	µA	1
					100	µA	2, 3
		V_{SD} = 30V			600	µA	1
					750	µA	2, 3
V_{SDL}	Shutdown Input Logic Voltage	Low	See (1)		0.6	V	1, 2, 3
V_{SDH}	Shutdown Input Logic Voltage	High	See (1)	2.0		V	1, 2, 3
I_{LKG}	Regular Output Bias Current In Shutdown	V_{SD} = 2V, V_{IN} = 30V, I_L = 0mA		–10	10	µA	1
				–20	20	µA	2, 3

(1) Parameter tested go-no-go only.

JL2951 Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified. V_{IN} = 6V, C_L = 3.3µF, V_{SD} = 0.6V

PARAMETER		TEST CONDITIONS	NOTES	MIN	MAX	UNIT	SUBGROUP
RR	Ripple Rejection	f = 120Hz, V_{IN} = 0.1V_{RMS}		50		dB	4
V_{Noise}	Output Noise	C_L = 1µF			600	µV_{RMS}	7
		C_L = 3.3µF			250	µV_{RMS}	7

Typical Performance Characteristics

Quiescent Current

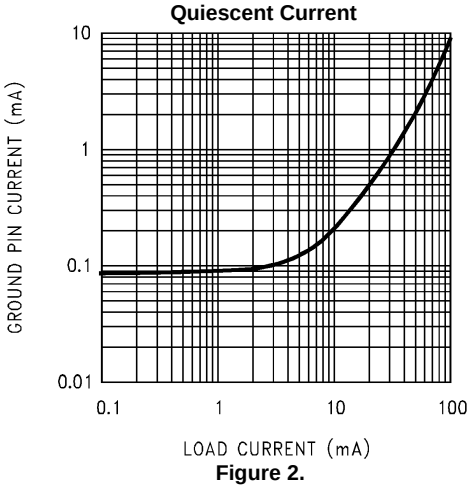


Figure 2.

Dropout Characteristics

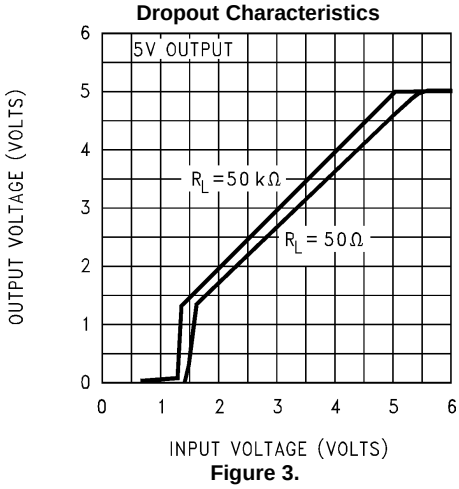


Figure 3.

Input Current

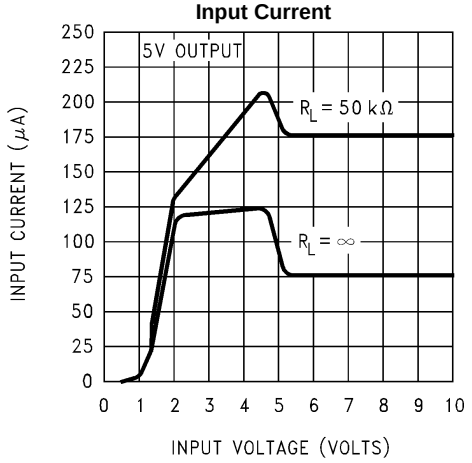


Figure 4.

Input Current

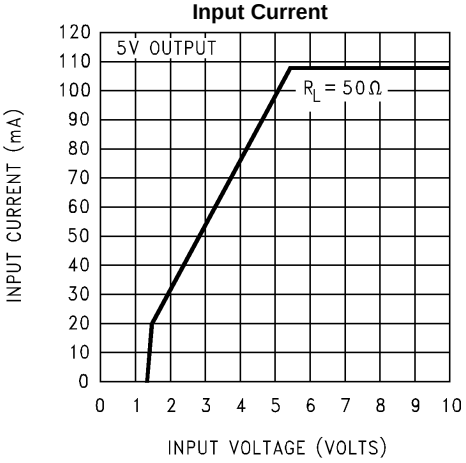


Figure 5.

Output Voltage vs. Temperature of 3 Representative Units

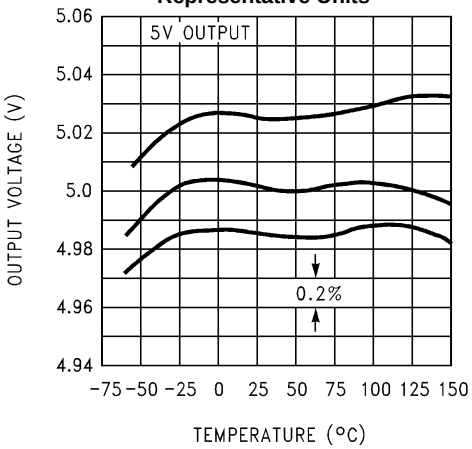


Figure 6.

Quiescent Current

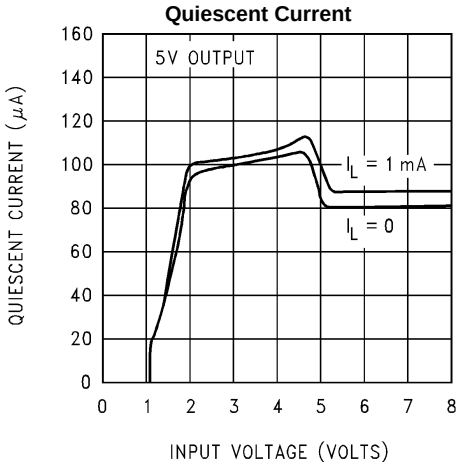


Figure 7.

Typical Performance Characteristics (continued)

Quiescent Current

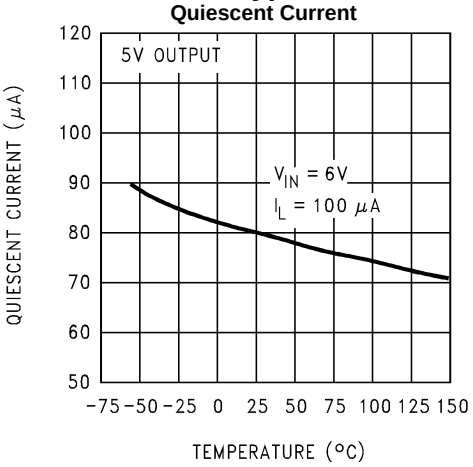


Figure 8.

Quiescent Current

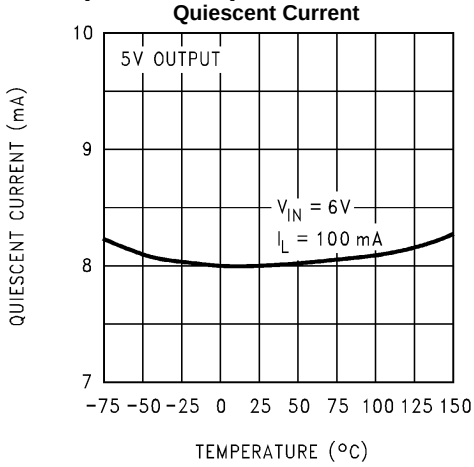


Figure 9.

Quiescent Current

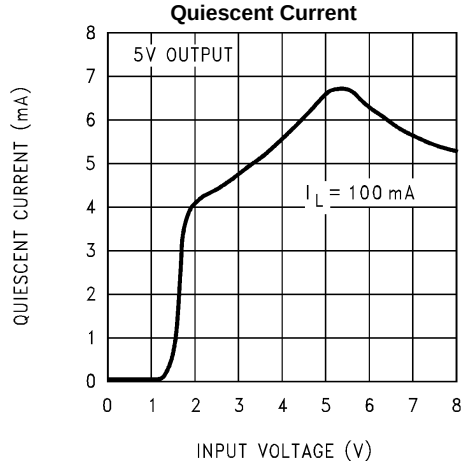


Figure 10.

Short Circuit Current

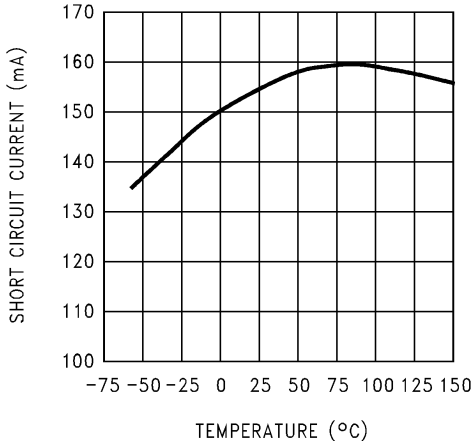


Figure 11.

Dropout Voltage

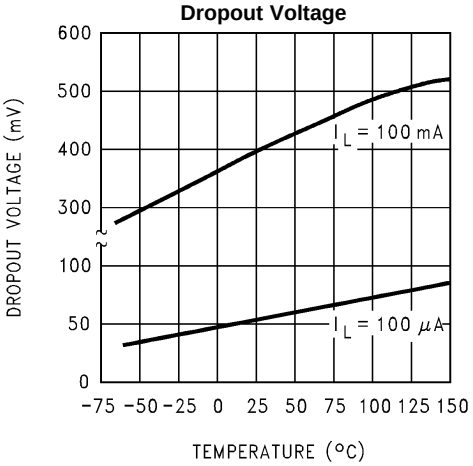


Figure 12.

Dropout Voltage

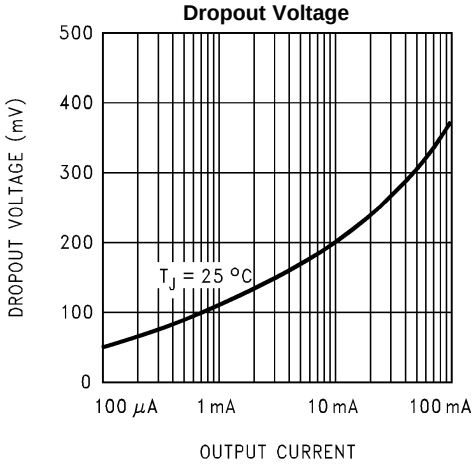


Figure 13.

Typical Performance Characteristics (continued)

Minimum Operating Voltage

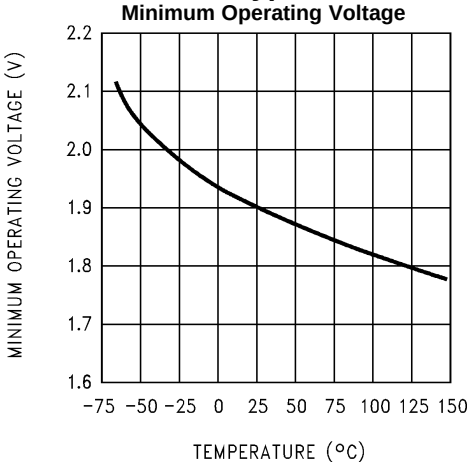


Figure 14.

Feedback Bias Current

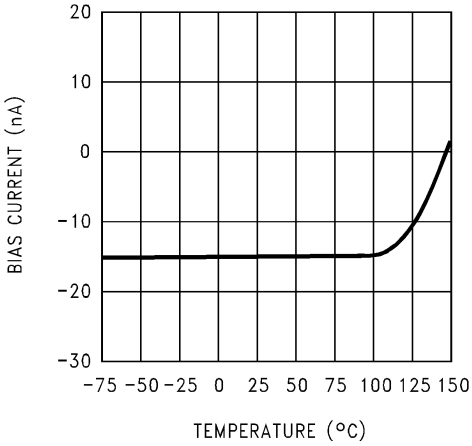


Figure 15.

Feedback Pin Current

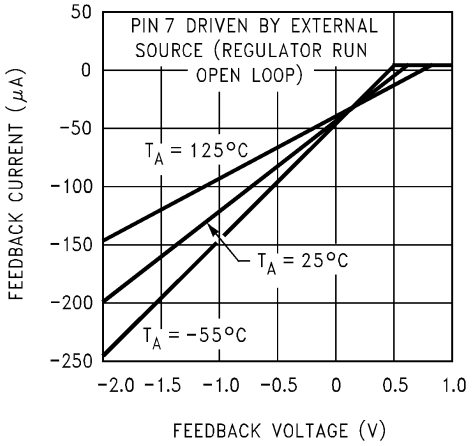


Figure 16.

Error Comparator Output

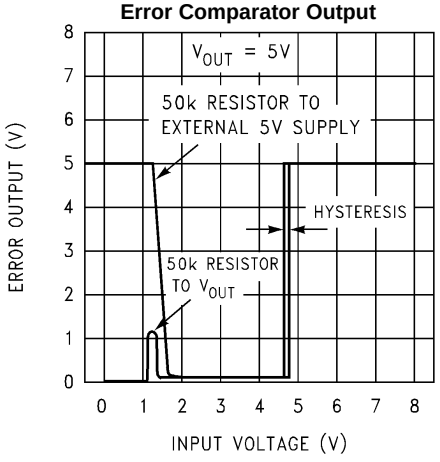


Figure 17.

Comparator Sink Current

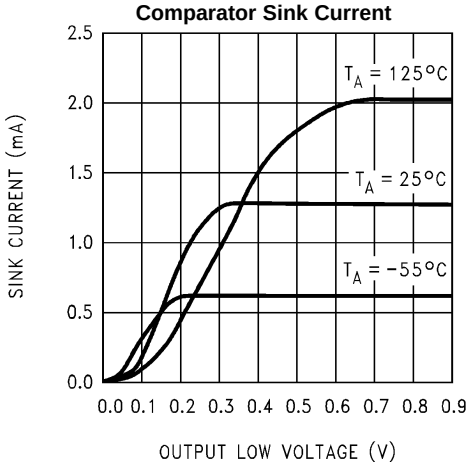


Figure 18.

Line Transient Response

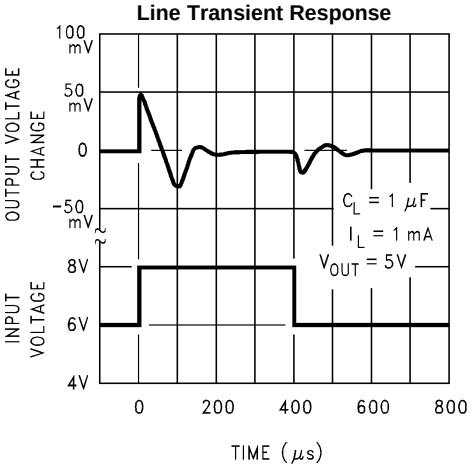


Figure 19.

Typical Performance Characteristics (continued)

Load Transient Response

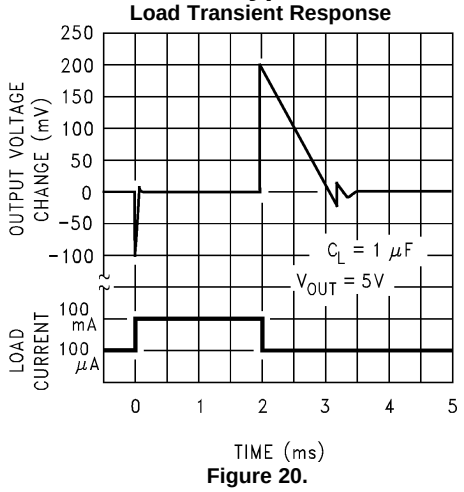


Figure 20.

Load Transient Response

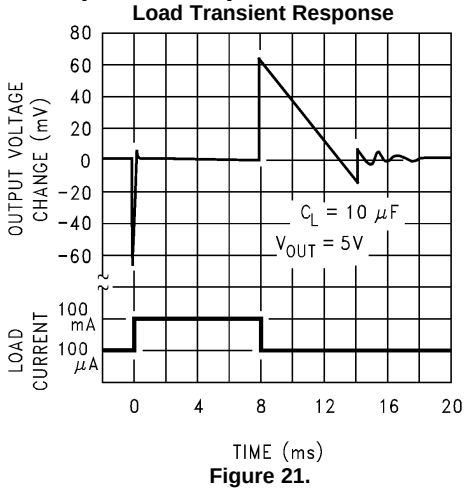


Figure 21.

Enable Transient

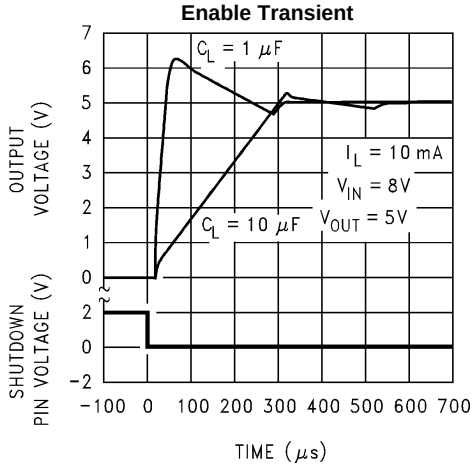


Figure 22.

Output Impedance

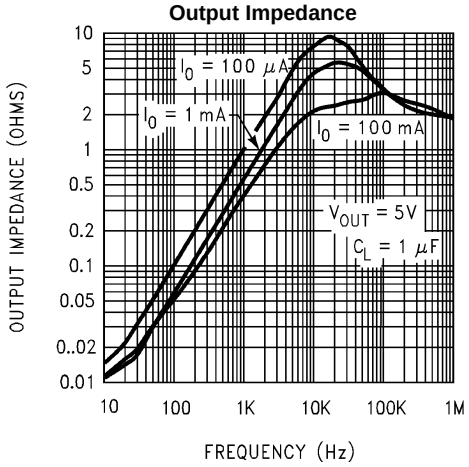


Figure 23.

Ripple Rejection

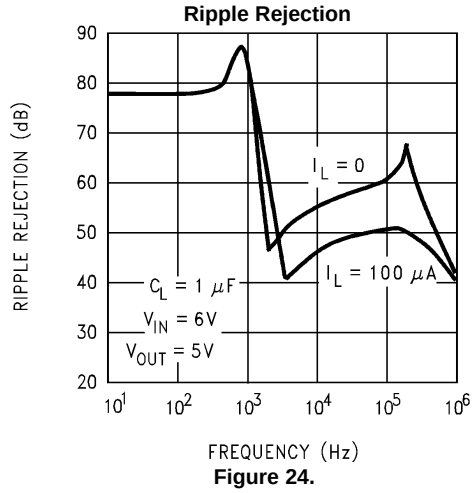


Figure 24.

Ripple Rejection

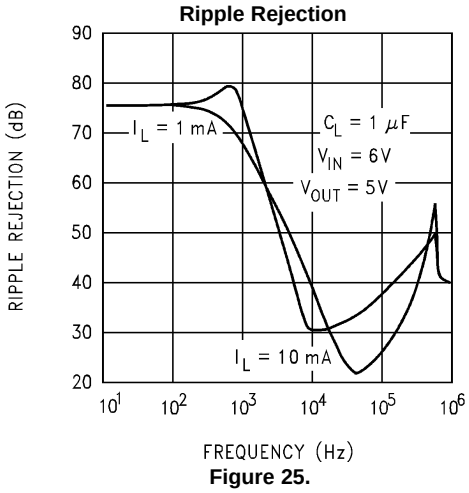


Figure 25.

Typical Performance Characteristics (continued)

Ripple Rejection

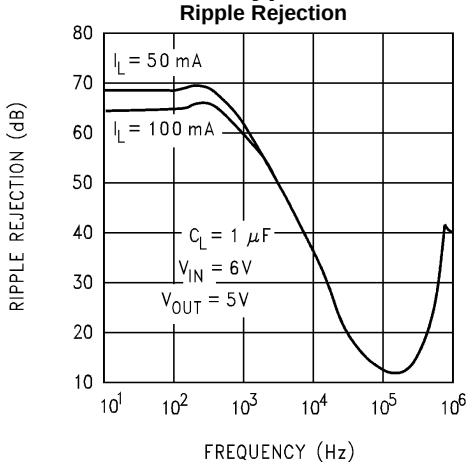


Figure 26.

Output Noise

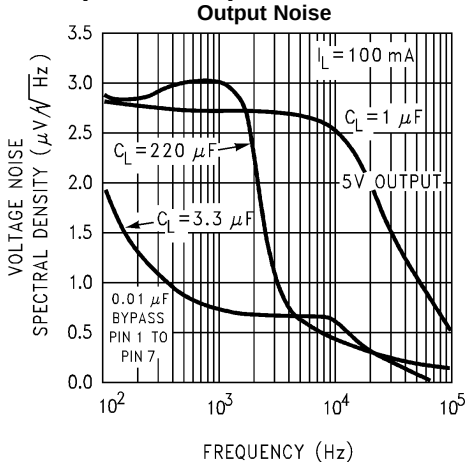


Figure 27.

Divider Resistance

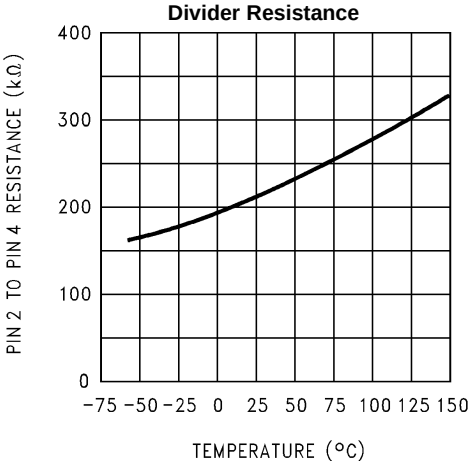


Figure 28.

Shutdown Threshold Voltage

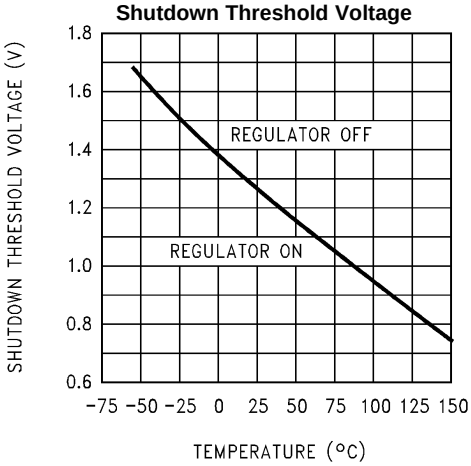


Figure 29.

Line Regulation

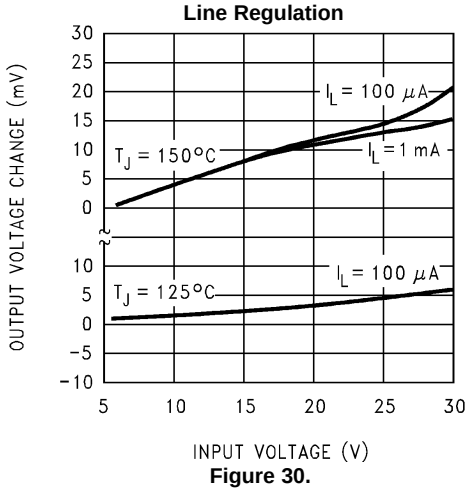


Figure 30.

Maximum Rated Output Current

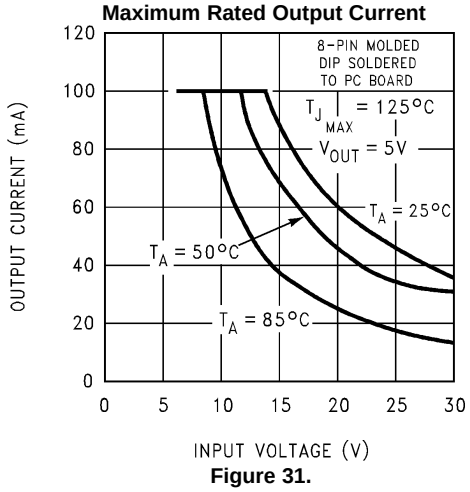


Figure 31.

Typical Performance Characteristics (continued)

Thermal Response

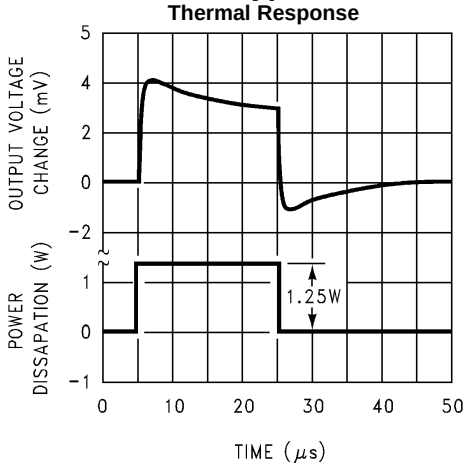


Figure 32.

Output Capacitor ESR Range

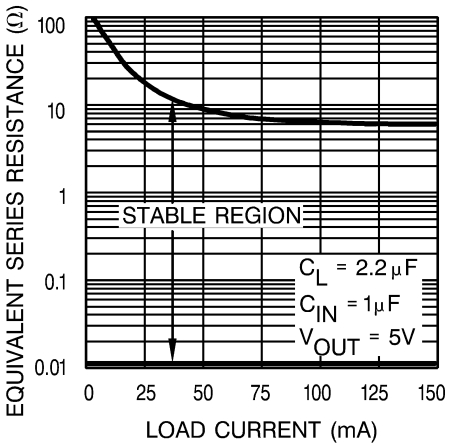


Figure 33.

APPLICATION HINTS

External Capacitors

A 1.0µF (or greater) capacitor is required between the output and ground for stability at output voltages of 5V or more. At lower output voltages, more capacitance is required (2.2µF or more is recommended for 3V and 3.3V versions). Without this capacitor the part will oscillate. Most types of tantalum or aluminum electrolytics work fine here; even film types work but are not recommended for reasons of cost. Many aluminum electrolytics have electrolytes that freeze at about −30°C, so solid tantalums are recommended for operation below −25°C. The important parameters of the capacitor are an ESR of about 5Ω or less and a resonant frequency above 500kHz. The value of this capacitor may be increased without limit.

Ceramic capacitors whose value is greater than 1000pF should not be connected directly from the LP2951 output to ground. Ceramic capacitors typically have ESR values in the range of 5 to 10mΩ, a value below the lower limit for stable operation (see Figure 33).

The reason for the lower ESR limit is that the loop compensation of the part relies on the ESR of the output capacitor to provide the zero that gives added phase lead. The ESR of ceramic capacitors is so low that this phase lead does not occur, significantly reducing phase margin. A ceramic output capacitor can be used if a series resistance is added (recommended value of resistance is about 0.1Ω to 2Ω).

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.33µF for currents below 10mA or 0.1µF for currents below 1mA. Using the adjustable versions at voltages below 5V runs the error amplifier at lower gains so that *more* output capacitance is needed. For the worst-case situation of a 100mA load at 1.23V output (Output shorted to Feedback) a 3.3µF (or greater) capacitor should be used.

When setting the output voltage of the LP2951 with external resistors, a minimum load of 1µA is recommended.

A 1µF tantalum, ceramic or aluminum electrolytic capacitor should be placed from the LP2951 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

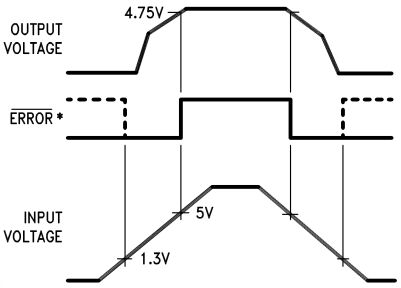
Stray capacitance to the LP2951 Feedback terminal can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100pF capacitor between Output and Feedback and increasing the output capacitor to at least 3.3µF will fix this problem.

Error Detection Comparator Output

The comparator produces a logic low output whenever the LP2951 output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60mV divided by the 1.235 reference voltage. (Refer to the Block Diagram) This trip level remains 5% below normal regardless of the programmed output voltage of the 2951. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

Figure 34 below gives a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the LP2951 input is ramped up and down. For 5V versions, the $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which V_{OUT} = 4.75V). Because the LP2951's dropout voltage is load-dependent (see Figure 12), the **input** voltage trip point (about 5V) will vary with the load current. The **output** voltage trip point (approx. 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pullup resistor. This resistor may be returned to the output or some other supply voltage depending on system requirements. In determining a value for this resistor, note that while the output is rated to sink 400µA, this sink current adds to battery drain in a low battery condition. Suggested values range from 100kΩ to 1 MΩ. The resistor is not required if this output is unused.



*When $V_{IN} \leq 1.3V$, the error flag pin becomes a high impedance, and the error flag voltage rises to its pull-up voltage. Using V_{OUT} as the pull-up voltage (see Figure 35), rather than an external 5V source, will keep the error flag voltage under 1.2V (typ.) in this condition. The user may wish to divide down the error flag voltage using equal-value resistors (10kΩ suggested), to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.

Figure 34. $\overline{\text{ERROR}}$ Output Timing

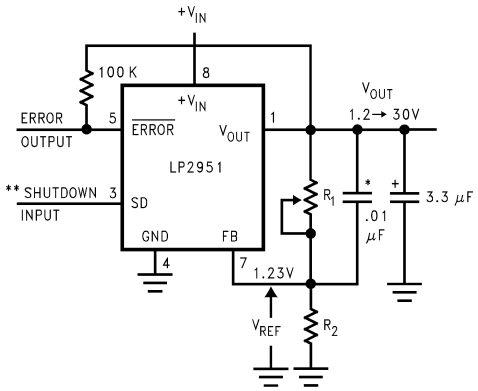
Programming The Output Voltage (LP2951)

The LP2951 may be pin-strapped for the nominal fixed output voltage using its internal voltage divider by tying the output and sense pins together, and also tying the feedback and V_{TAP} pins together. Alternatively, it may be programmed for any output voltage between its 1.235V reference and its 30V maximum rating. As seen in Figure 35, an external pair of resistors is required.

The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_1}{R_2}\right) + I_{FB}R_1 \quad (1)$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the feedback pin bias current, nominally −20nA. The minimum recommended load current of 1µA forces an upper limit of 1.2 MΩ on the value of R_2, if the regulator must work with no load (a condition often found in CMOS in standby). I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R_2 = 100kΩ reduces this error to 0.17% while increasing the resistor program current to 12µA. Since the LP2951 typically draws 60µA at no load with Pin 2 open-circuited, this is a small price to pay.



*See Application Hints

$V_{out} = V_{Ref}\left(1 + \frac{R_1}{R_2}\right)$

**Drive with TTL-high to shut down. Ground or leave open if shutdown feature is not to be used.

Note: Pins 2 and 6 are left open.

Figure 35. Adjustable Regulator

Reducing Output Noise

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor.

Noise can be reduced fourfold by a bypass capacitor across R_1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\ Hz} \quad (2)$$

or about 0.01µF. When doing this, the output capacitor must be increased to 3.3µF to maintain stability. These changes reduce the output noise from 430µV to 100µV rms for a 100kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

Typical Applications

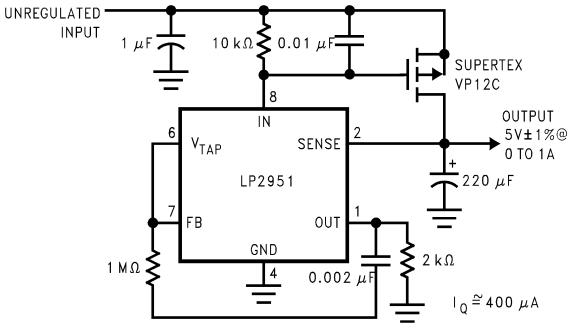


Figure 36. 1A Regulator with 1.2V Dropout

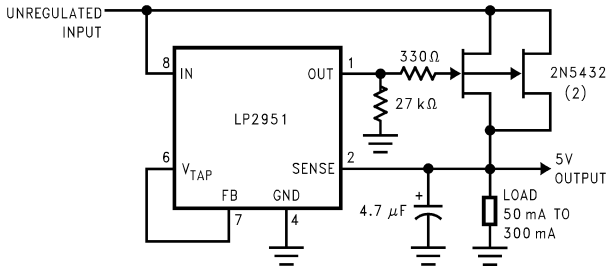
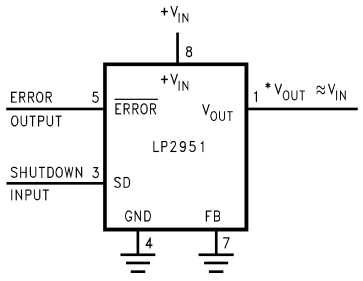


Figure 37. 300mA Regulator with 0.75V Dropout



*Minimum input-output voltage ranges from 40mV to 400mV, depending on load current. Current limit is typically 160mA.

Figure 38. Wide Input Voltage Range Current Limiter

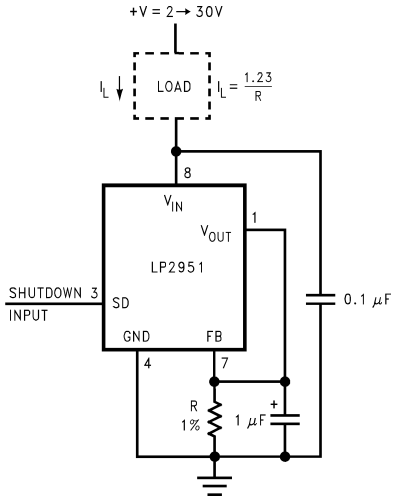
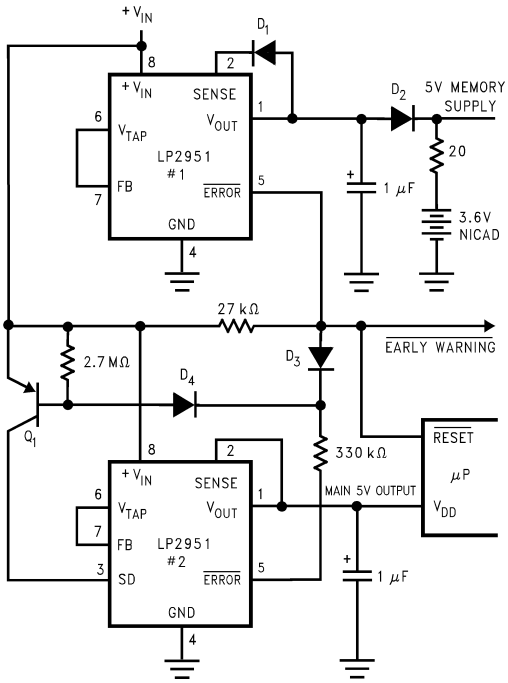


Figure 39. Low Drift Current Source



Early warning flag on low input voltage
Main output latches off at lower input voltages
Battery backup on auxiliary output
Operation: Reg. #1's V_{out} is programmed one diode drop above 5V. Its error flag becomes active when $V_{in} \leq 5.7V$. When V_{in} drops below 5.3V, the error flag of Reg. #2 becomes active and via Q1 latches the main output off. When V_{in} again exceeds 5.7V Reg. #1 is back in regulation and the early warning signal rises, unlatching Reg. #2 via D3.

Figure 40. Regulator with Early Warning and Auxiliary Output

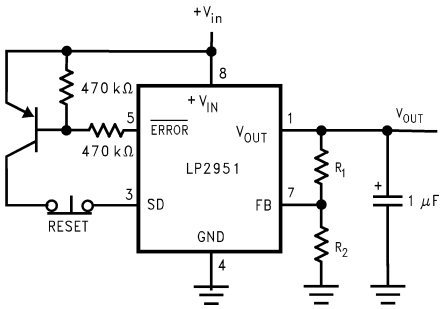
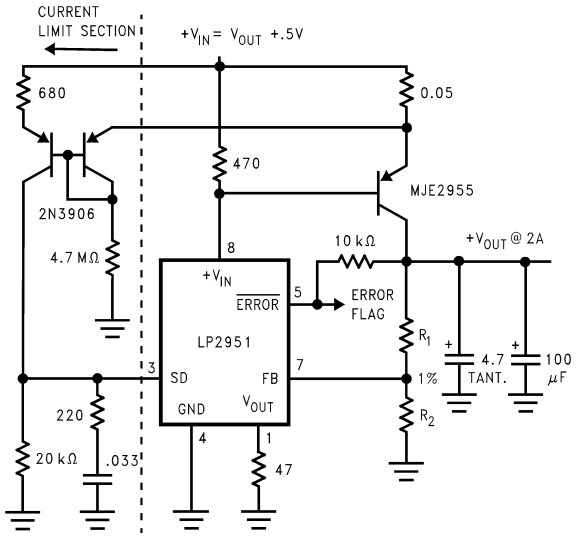


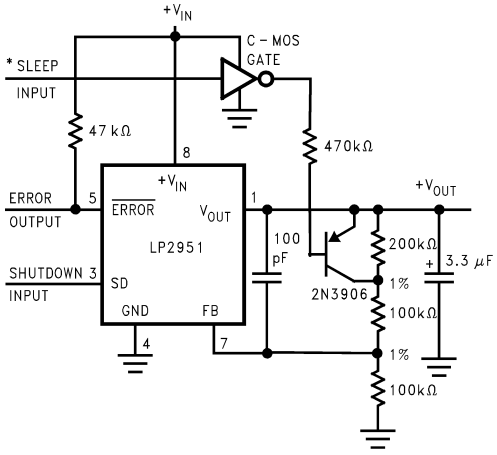
Figure 41. Latch Off When Error Flag Occurs



$$V_{out} = 1.23V \left(1 + \frac{R_1}{R_2}\right)$$

For $5V_{out}$, use internal resistors. Wire pin 6 to 7, & wire pin 2 to $+V_{out}$ Bus.

Figure 42. 2 Ampere Low Dropout Regulator



*High input lowers V_{out} to 2.5V

Figure 43. 5V Regulator with 2.5V Sleep Function

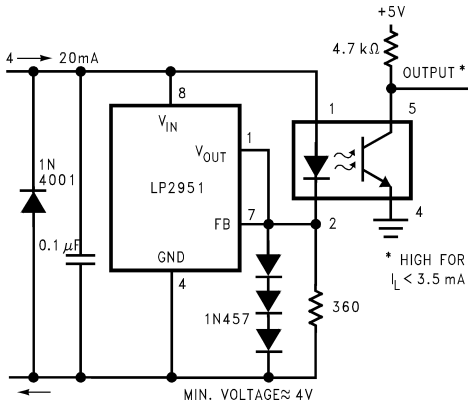
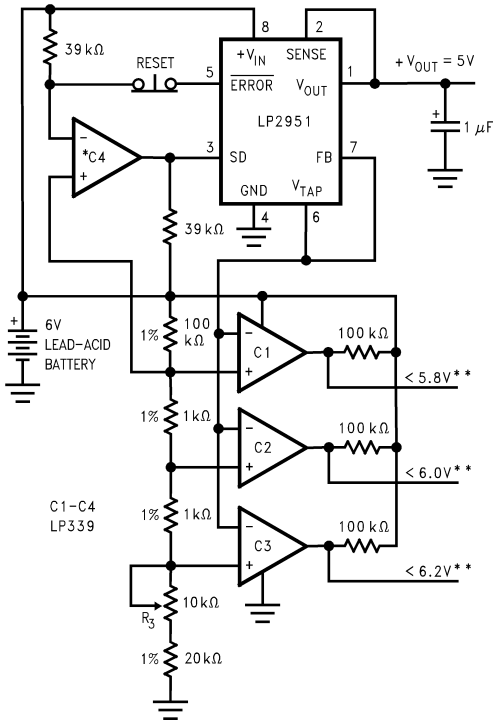
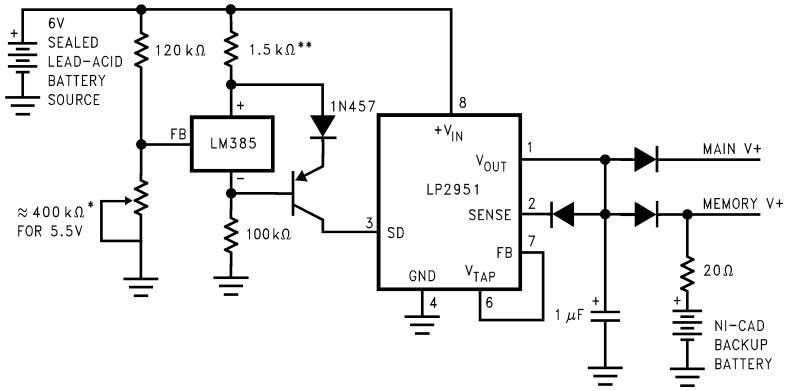


Figure 44. Open Circuit Detector for 4 to 20mA Current Loop



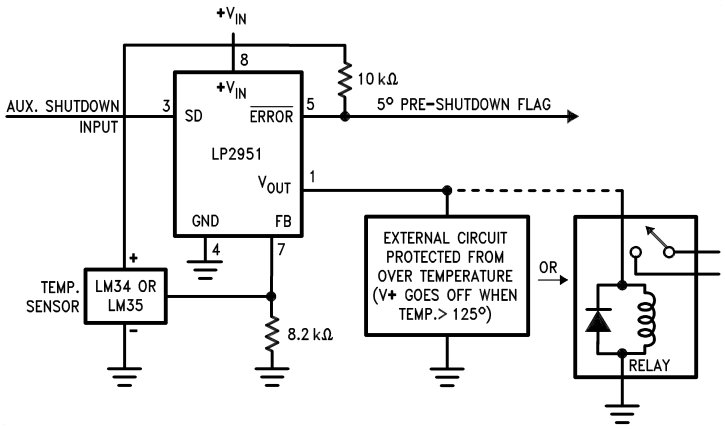
*Optional Latch off when drop out occurs. Adjust R3 for C2 Switching when V_{in} is 6.0V.
**Outputs go low when V_{in} drops below designated thresholds.

Figure 45. Regulator with State-of-Charge Indicator



For values shown, Regulator shuts down when V_{in} < 5.5V and turns on again at 6.0V. Current drain in disconnected mode is ≈ 150μA.
*Sets disconnect Voltage
**Sets disconnect Hysteresis

Figure 46. Low Battery Disconnect



LM34 for 125°F Shutdown
LM35 for 125°C Shutdown

Figure 47. System Overtemperature Protection Circuit

REVISION HISTORY

Released	Revision	Section	Changes
11/30/2010	A	New Release, Corporate format	1 MDS data sheet converted into one Corp. data sheet format. MJLP2951-X Rev 1B1 will be archived.

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-3870501BPA	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	JL2951BPA 5962-38705 01BPA Q ACO 01BPA Q >T	Samples
JL2951BPA	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	JL2951BPA 5962-38705 01BPA Q ACO 01BPA Q >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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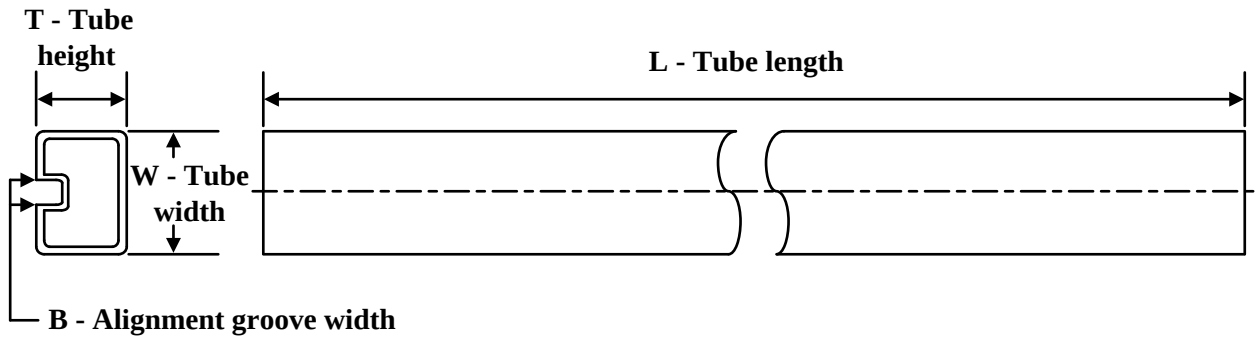
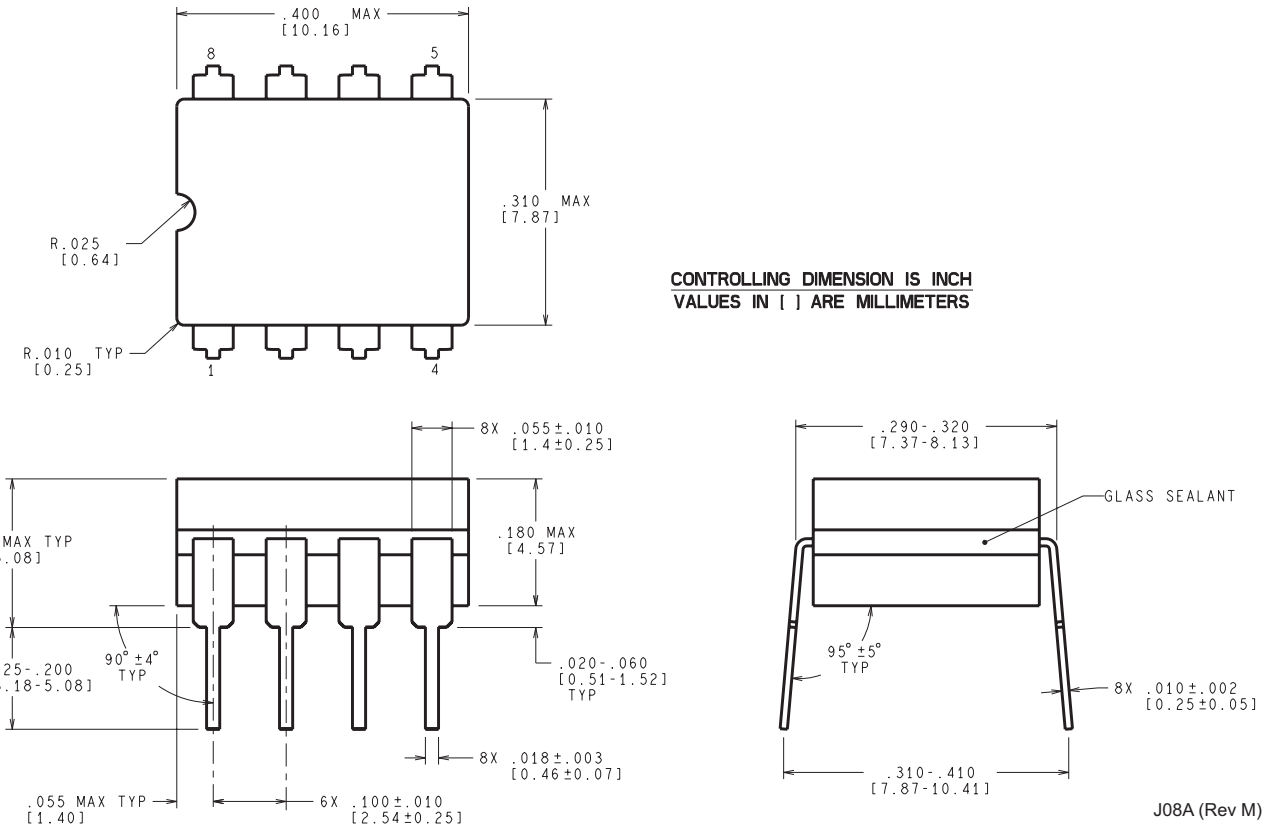
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-3870501BPA	NAB	CDIP	8	40	506.98	15.24	13440	NA
JL2951BPA	NAB	CDIP	8	40	506.98	15.24	13440	NA

NAB0008A


.400 MAX
[10.16]
8
5
.310 MAX
[7.87]
R.025
[0.64]
R.010 TYP
[0.25]
1
4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
8X .125-.200
[3.18-5.08]
90° ±4°
TYP
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
J08A (Rev M)

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