LOW-POWER DIFFERENTIAL LINE DRIVER AND RECEIVER PAIRS

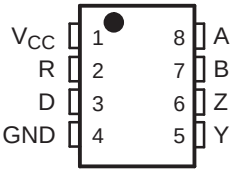
Check for Samples: SN65LBC179A, SN75LBC179A

FEATURES

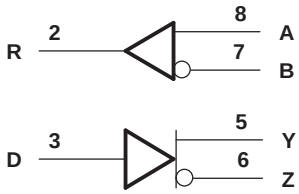
- **High-Speed Low-Power LinBiCMOS™ Circuitry Designed for Signaling Rates(1) of up to 30 Mbps**
- **Bus-Pin ESD Protection Exceeds 12 kV HBM**
- **Very Low Disabled Supply-Current Requirements . . . 700 µA Max**
- **Common-Mode Voltage Range of –7 V to 12 V**
- **Low Supply Current . . .15 mA Max**
- **Compatible With ANSI Standard TIA/EAI-485-A and ISO8482: 1987(E)**
- **Positive and Negative Output Current Limiting**
- **Driver Thermal Shutdown Protection**

(1)Signaling rate by TIA/EIA-485-A definition restrict transition times to 30% of the bit length, and much higher signaling rates may be achieved without this requirement as displayed in the *TYPICAL CHARACTERISTICS* of this device.

SN65LBC179AD (Marked as BL179A)
SN65LBC179AP (Marked as 65LBC179A)
SN75LBC179AD (Marked as LB179A)
SN75LBC179AP (Marked as 75LBC179A)
(TOP VIEW)



LOGIC DIAGRAM (POSITIVE LOGIC)



DESCRIPTION

The SN65LBC179A and SN75LBC179A differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication over long cables that take on the characteristics of transmission lines. They are balanced, or differential, voltage mode devices that are compatible with ANSI standard TIA/EIA-485-A and ISO 8482:1987(E). The A version offers improved switching performance over its predecessors without sacrificing significantly more power.

The SN65LBC179A and SN75LBC179A combine a differential line driver and differential input line receiver and operate from a single 5-V supply. The driver differential outputs and the receiver differential inputs are connected to separate terminals for full-duplex operation and are designed to present minimum loading to the bus when powered off (V_{CC} = 0). These parts feature a wide positive and negative common-mode voltage range making them suitable for point-to-point or multipoint data bus applications. The devices also provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions.

The SN65LBC179A is characterized over the industrial temperature range of –40°C to 85°C. The SN75LBC179A is characterized for operation over the commercial temperature range of 0°C to 70°C.

FUNCTION TABLE(1)

DRIVER			RECEIVER	
INPUT D	OUTPUTS		DIFFERENTIAL INPUTS A – B	OUTPUT R
	Y	Z		
H	H	L	V_{ID} ≥ 0.2 V	H
H	H	L	-0.2 V < V_{ID} < 0.2 V	?
L	L	H	V_{ID} ≤ -0.2 V	L
OPEN	H	L	Open circuit	H

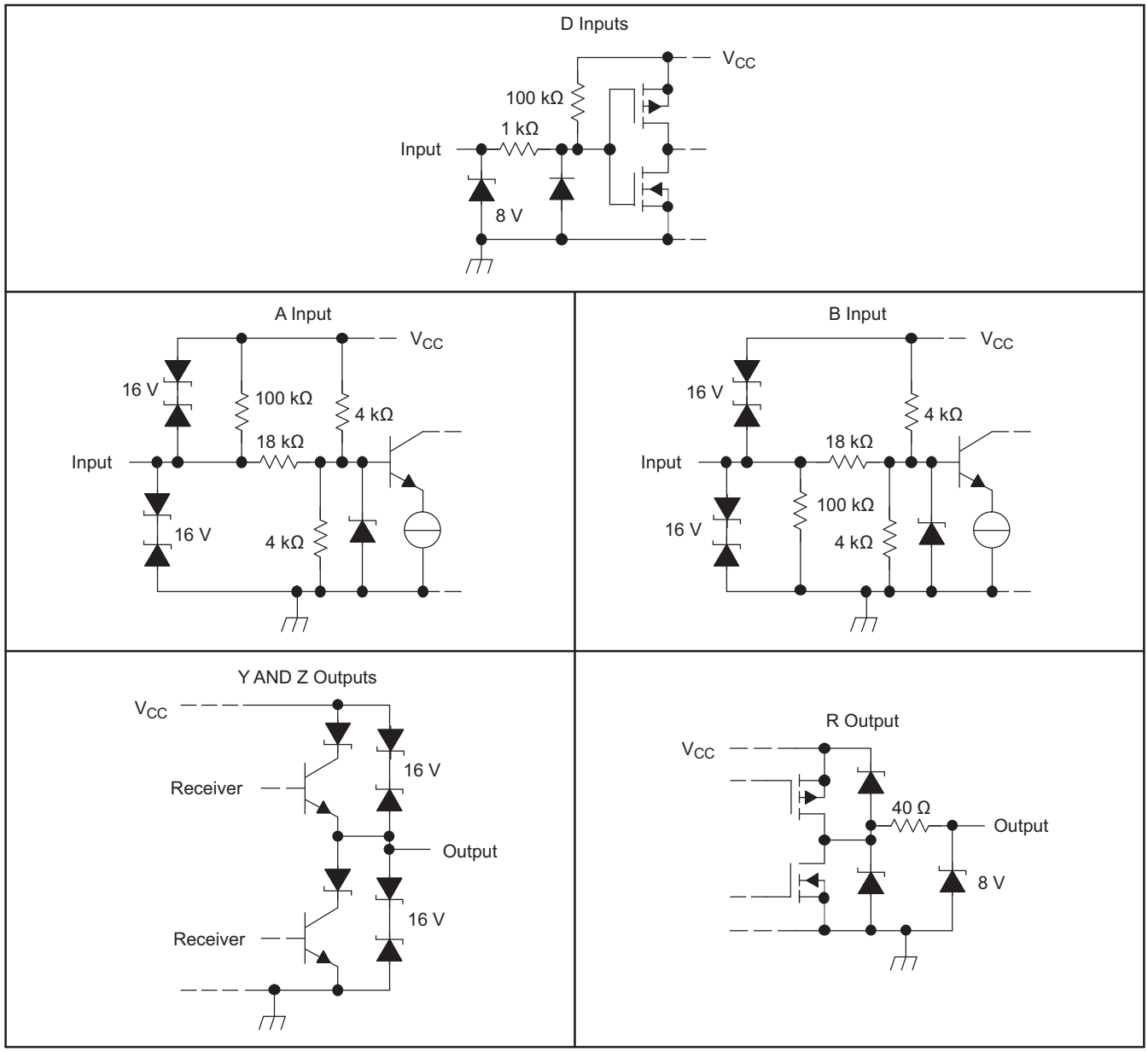
(1) H = high level, L = low level, ? = indeterminate

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T_A	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DUAL-IN-LINE
0°C to 70°C	SN75LBC179AD	SN75LBC179AP
–40°C to 85°C	SN65LBC179AD	SN65LBC179AP

SCHEMATICS OF INPUTS AND OUTPUTS



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			UNIT
V_{CC}	Supply voltage range(2)		–0.3 V to 6 V
	Voltage range	A, B, Y, or Z(2)	–10 V to 15 V
		D or R(2)	–0.3 V to V_{CC} + 0.5 V
I_O	Receiver output current		±20 mA
	Electrostatic discharge	Bus terminals and GND, Class 3, A(3)	12 kV
		Bus terminals and GND, Class 3, B(3)	400 V
		All terminals, Class 3, A	3 kV
		All terminals, Class 3, B	400 V
	Continuous total power dissipation(4)		Internally limited
	Total power dissipation		See Dissipation Rating Table

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to GND.
(3) Tested in accordance with MIL-STD-883C, Method 3015.7
(4) The maximum operating junction temperature is internally limited. Uses the dissipation rating table to operate below this temperature.

DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1100 mW	8.08 mW/°C	640 mW	520 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	D	2		V_{CC}	V
V_{IL}	Low-level input voltage	D	0		0.8	V
V_{ID}	Differential input voltage(1)		–12(2)		12	V
V_O, V_I, V_{IC}	Voltage at any bus terminal (separately or common-mode)	A, B, Y, or Z	–7		12	V
I_{OH}	High-level output current	Y or Z	–60			mA
		R	–8			
I_{OL}	Low-level output current	Y or Z			60	mA
		R			8	
T_A	Operating free-air temperature	SN65LBC179A	–40		85	°C
		SN75LBC179A	0		70	

(1) Differential input/output bus voltage is measured at the noninverting terminal with respect to the inverting terminal.
(2) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA		–1.5	–0.8		V
$\|V_{OD}\|$	Differential output voltage	R_L = 54 Ω, See Figure 1	SN65LBC179A	1	1.5	3	V
			SN75LBC179A	1.1	1.5	3	
		R_L = 60 Ω, –7 <$V_{(tot)}$ < 12, See Figure 2	SN65LBC179A	1	1.5	3	V
			SN75LBC179A	1.1	1.5	3	
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage (2)	See Figure 1 and Figure 2		–0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 1		1.8	2.4	2.8	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage(2)			–0.1		0.1	V
I_O	Output current with power off	V_{CC} = 0,	V_O = –7 V to 12 V	–10	±1	10	µA
I_{IH}	High-level input current	V_I = 2.V		–100			µA
I_{IL}	Low-level input current	V_I = 0.8 V		–100			µA
I_{OS}	Short-circuit output current	–7 V ≤ V_O ≤ 12 V		–250	±70	250	mA
I_{CC}	Supply current	No load,	V_I = 0 or V_{CC}		8.5	15	mA

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) Δ | V_{OD} | and Δ | V_{OC} | are the changes in the steady-state magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 54 Ω, C_L = 50 pF, See Figure 3	2	6	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2	6	12	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)			0.3	1	ns
t_r	Differential output signal rise time		4	7.5	11	ns
t_f	Differential output signal fall time		4	7.5	11	ns

RECEIVER SECTION

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA		–0.2			
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT-}$)				50		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA, See Figure 1		4	4.9		V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 8 mA, See Figure 1			0.1	0.8	V
I_I	Bus input current	V_{IH} = 12 V, V_{CC} = 5 V	Other input at 0 V		0.4	1	mA
		V_{IH} = 12 V, V_{CC} = 0			0.5	1	
		V_{IH} = –7 V, V_{CC} = 5 V		–0.8	–0.4		
		V_{IH} = –7 V, V_{CC} = 0		–0.8	–0.3		

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = –1.5 V to 1.5 V, See Figure 4	7	13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output		7	13	20	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PLH} – t_{PHL} \rvert$)			0.5	1.5	ns
t_r	Rise time, output			2.1	3.3	ns
t_f	Fall time, output	See Figure 4		2.1	3.3	ns

PARAMETER MEASURMENT INFORMATION

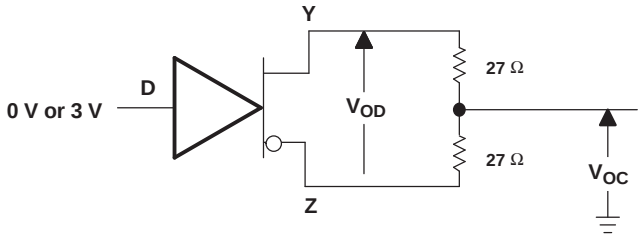


Figure 1. Driver V_{OD} and V_{OC}

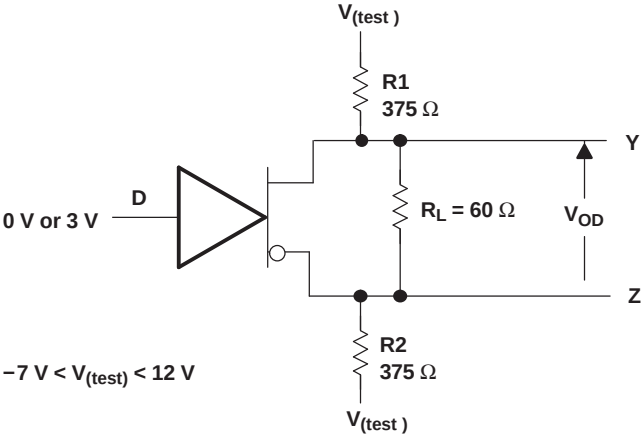
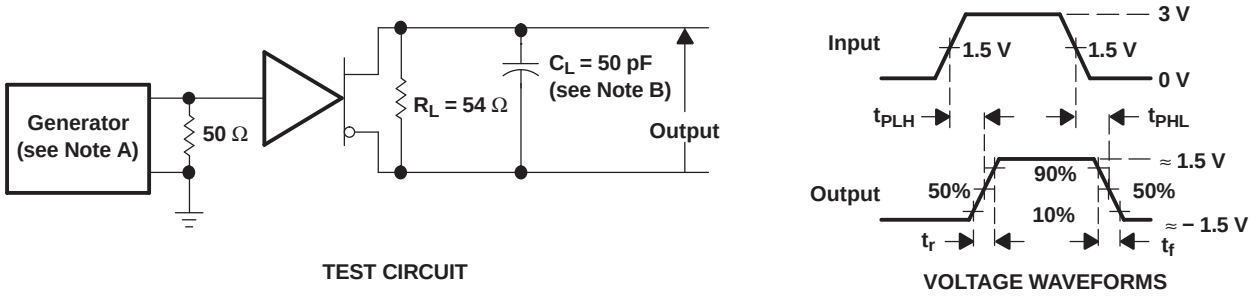


Figure 2. Driver V_{OD} With Common-Mode Loading

PARAMETER MEASURMENT INFORMATION (continued)

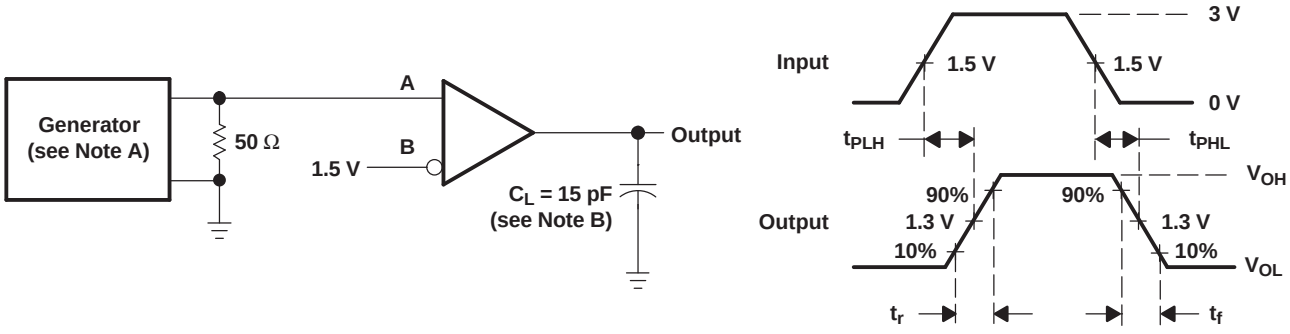


TEST CIRCUIT VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuits and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. CL includes probe and jig capacitance.

Figure 4. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

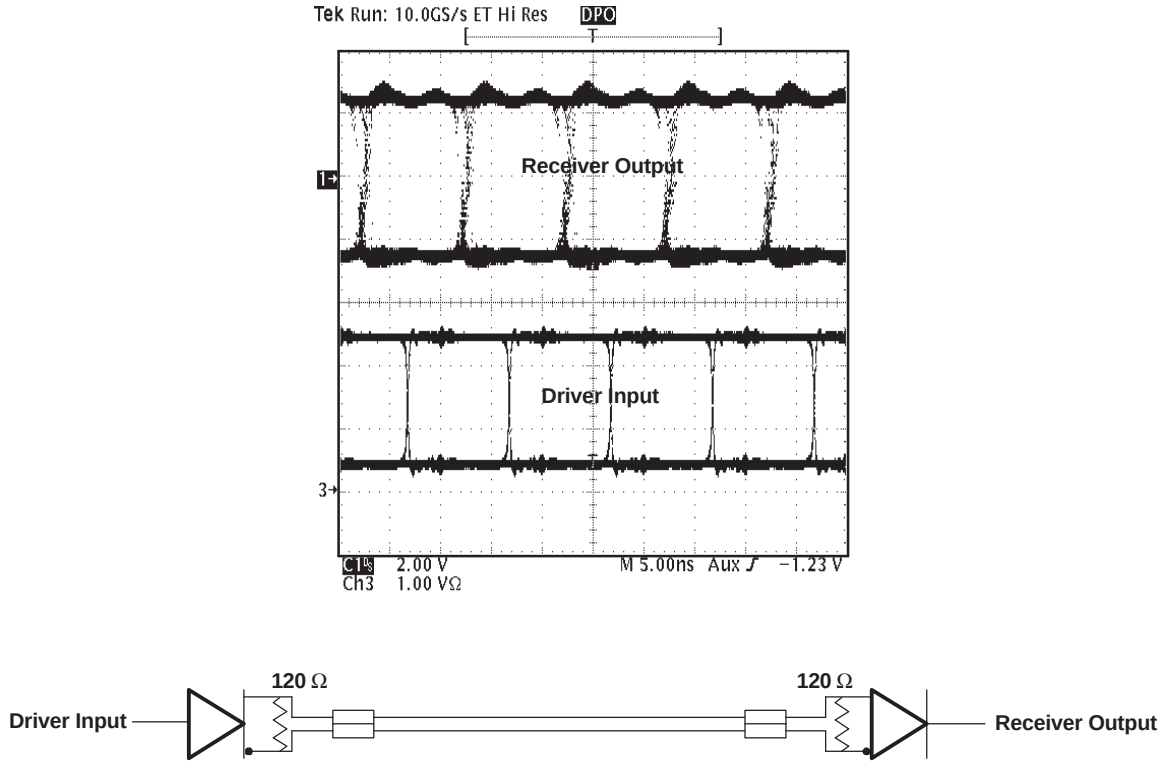


Figure 5. Typical Waveform of Non-Return-To-Zero (NRZ), Pseudorandom Binary Sequence (PRBS) Data at 100 Mbps Through 15m, of CAT 5 Unshielded Twisted Pair (UTP) Cable

TIA/EIA-485-A defines a maximum signaling rate as that in which the transition time of the voltage transition of a logic-state change remains less than or equal to 30% of the bit length. Transition times of greater length perform quite well even though they do not meet the standard by definition.

AVERAGE SUPPLY CURRENT vs FREQUENCY

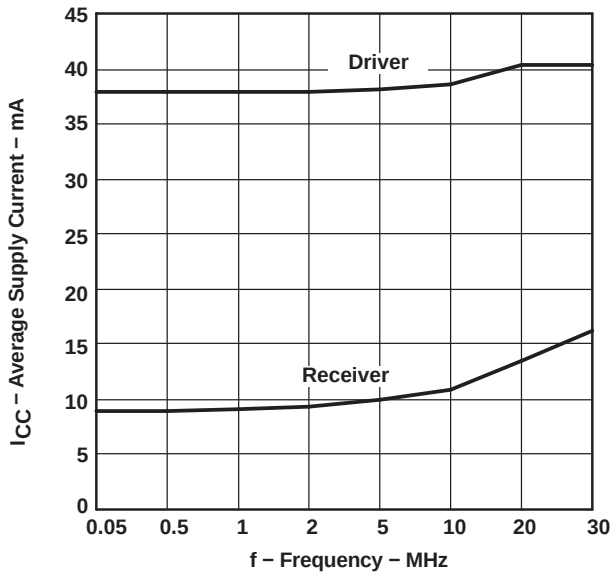


Figure 6.

LOGIC INPUT CURRENT vs INPUT VOLTAGE

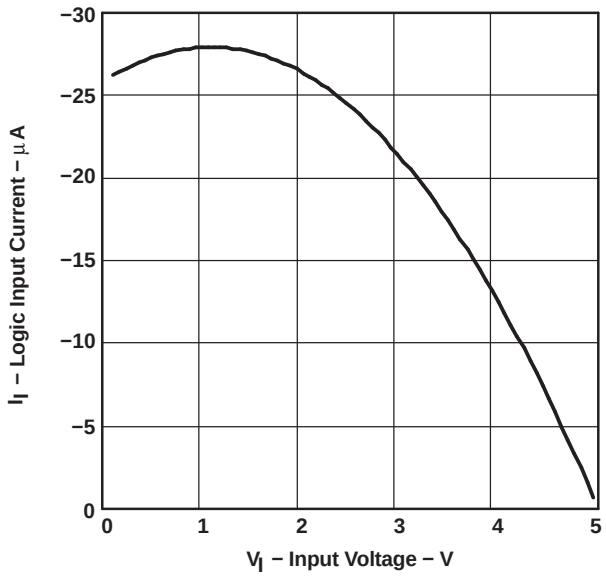


Figure 7.

TYPICAL CHARACTERISTICS (continued)

INPUT CURRENT vs INPUT VOLTAGE

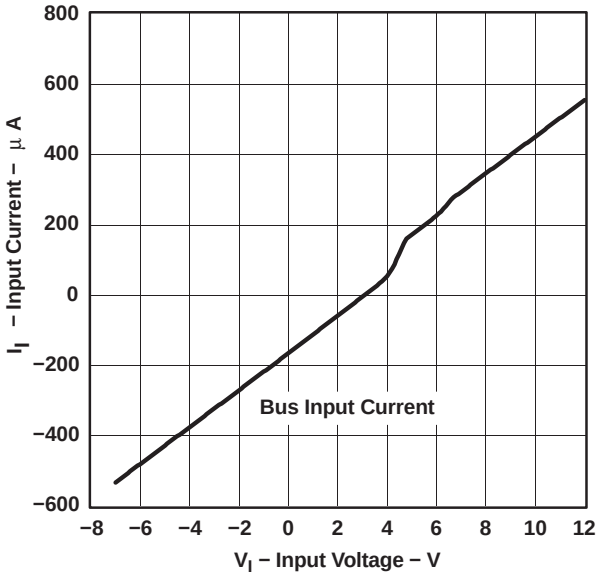


Figure 8.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

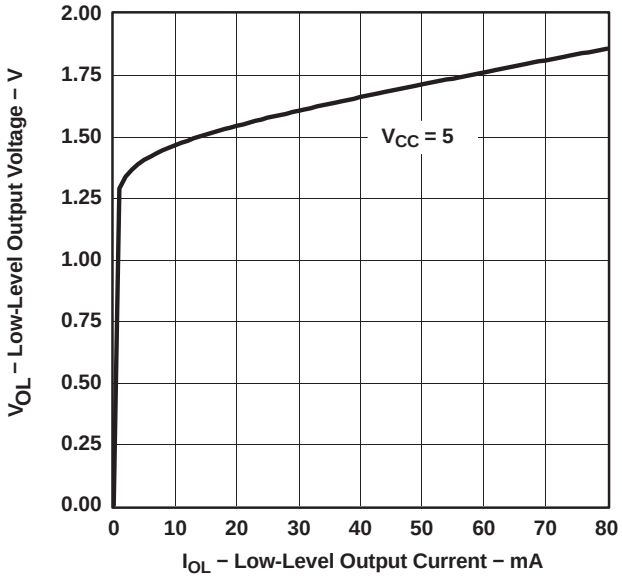


Figure 9.

DRIVER HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

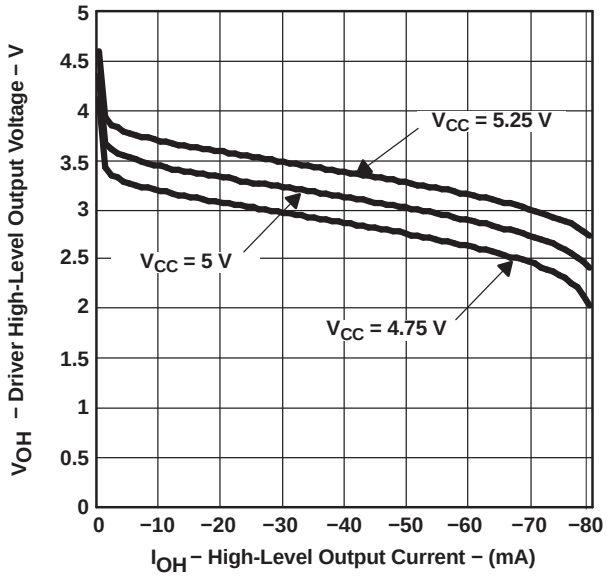


Figure 10.

DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs AVERAGE CASE TEMPERATURE

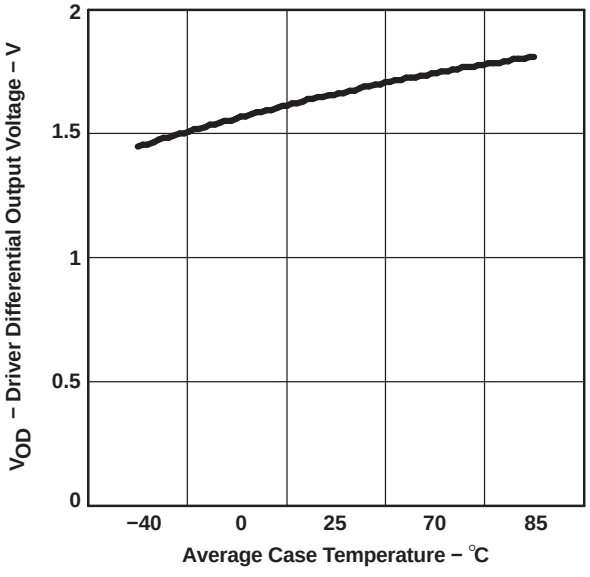


Figure 11.

TYPICAL CHARACTERISTICS (continued)

RECEIVER PROPAGATION TIME vs CASE TEMPERATURE

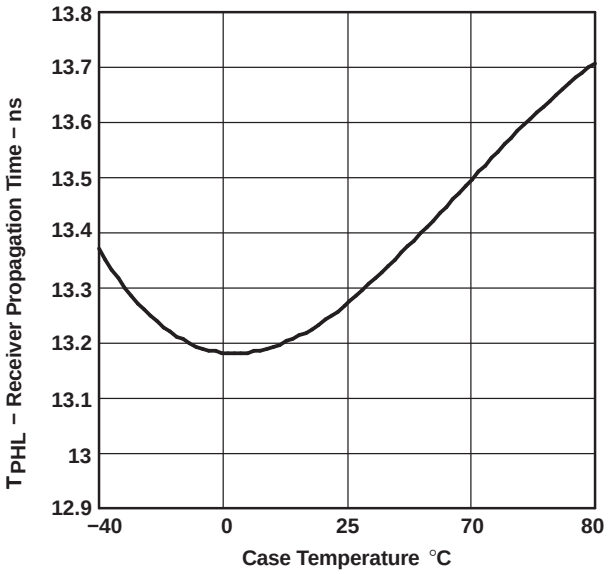


Figure 12.

DRIVER PROPAGATION DELAY TIME vs CASE TEMPERATURE

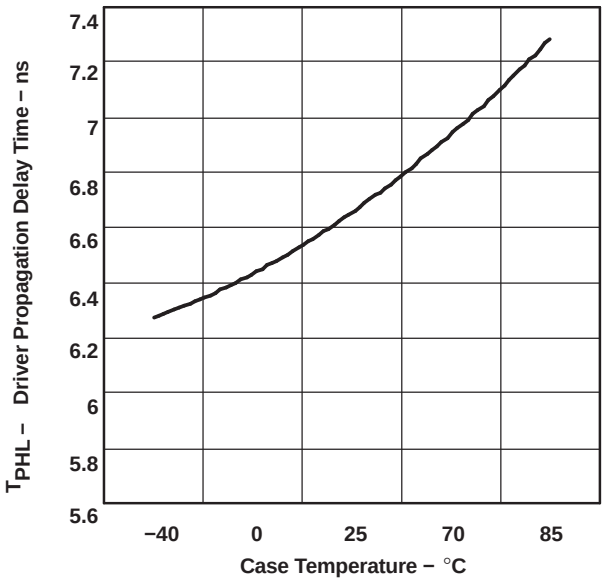


Figure 13.

DRIVER OUTPUT CURRENT vs SUPPLY VOLTAGE

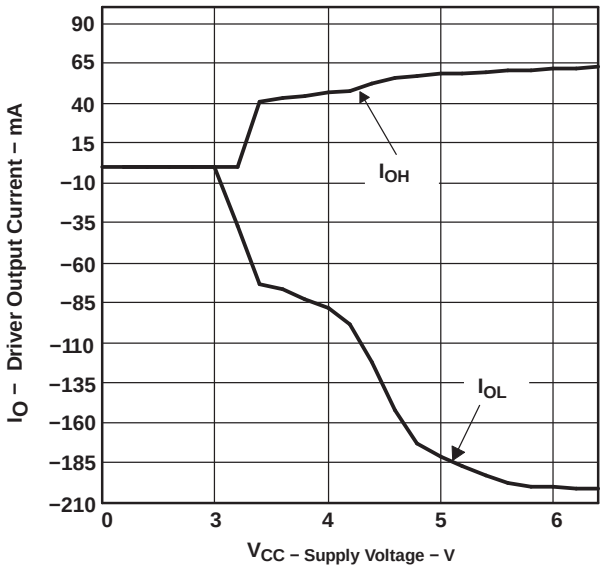


Figure 14.

REVISION HISTORY

Changes from Revision C (June 2001) to Revision D **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC179AD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL179A	Samples
SN65LBC179ADG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL179A	Samples
SN65LBC179ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL179A	Samples
SN65LBC179ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL179A	Samples
SN65LBC179AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65LBC179A	Samples
SN75LBC179AD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB179A	Samples
SN75LBC179ADG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB179A	Samples
SN75LBC179ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB179A	Samples
SN75LBC179ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB179A	Samples
SN75LBC179AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75LBC179A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

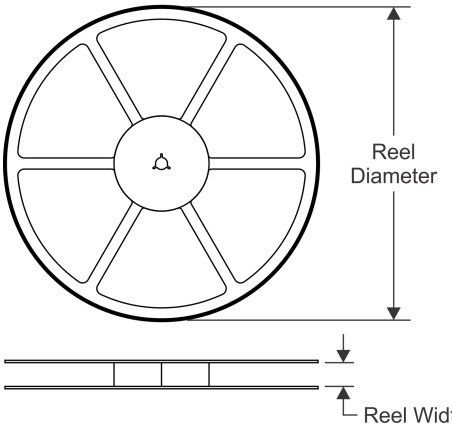
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

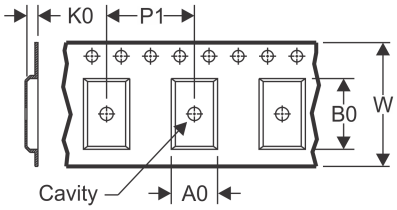
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

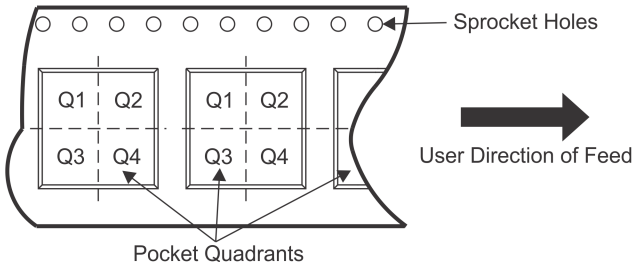


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

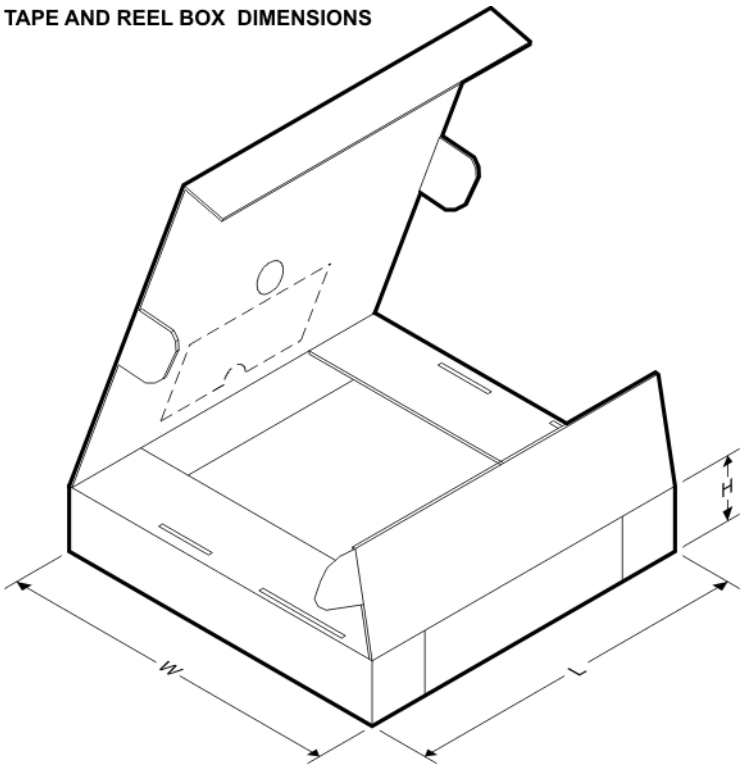
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC179ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC179ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

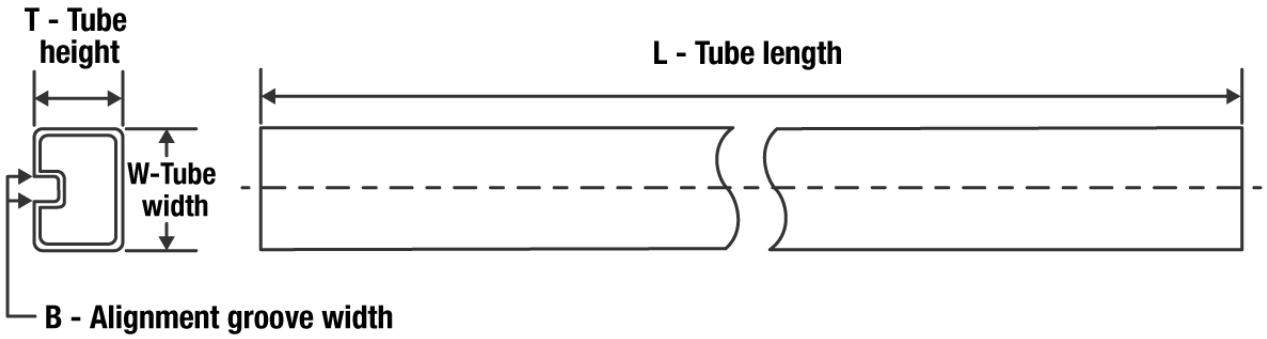
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

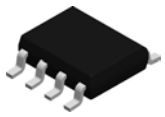
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC179ADR	SOIC	D	8	2500	340.5	336.1	25.0
SN75LBC179ADR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC179AD	D	SOIC	8	75	507	8	3940	4.32
SN65LBC179ADG4	D	SOIC	8	75	507	8	3940	4.32
SN65LBC179AP	P	PDIP	8	50	506	13.97	11230	4.32
SN75LBC179AD	D	SOIC	8	75	507	8	3940	4.32
SN75LBC179ADG4	D	SOIC	8	75	507	8	3940	4.32
SN75LBC179AP	P	PDIP	8	50	506	13.97	11230	4.32

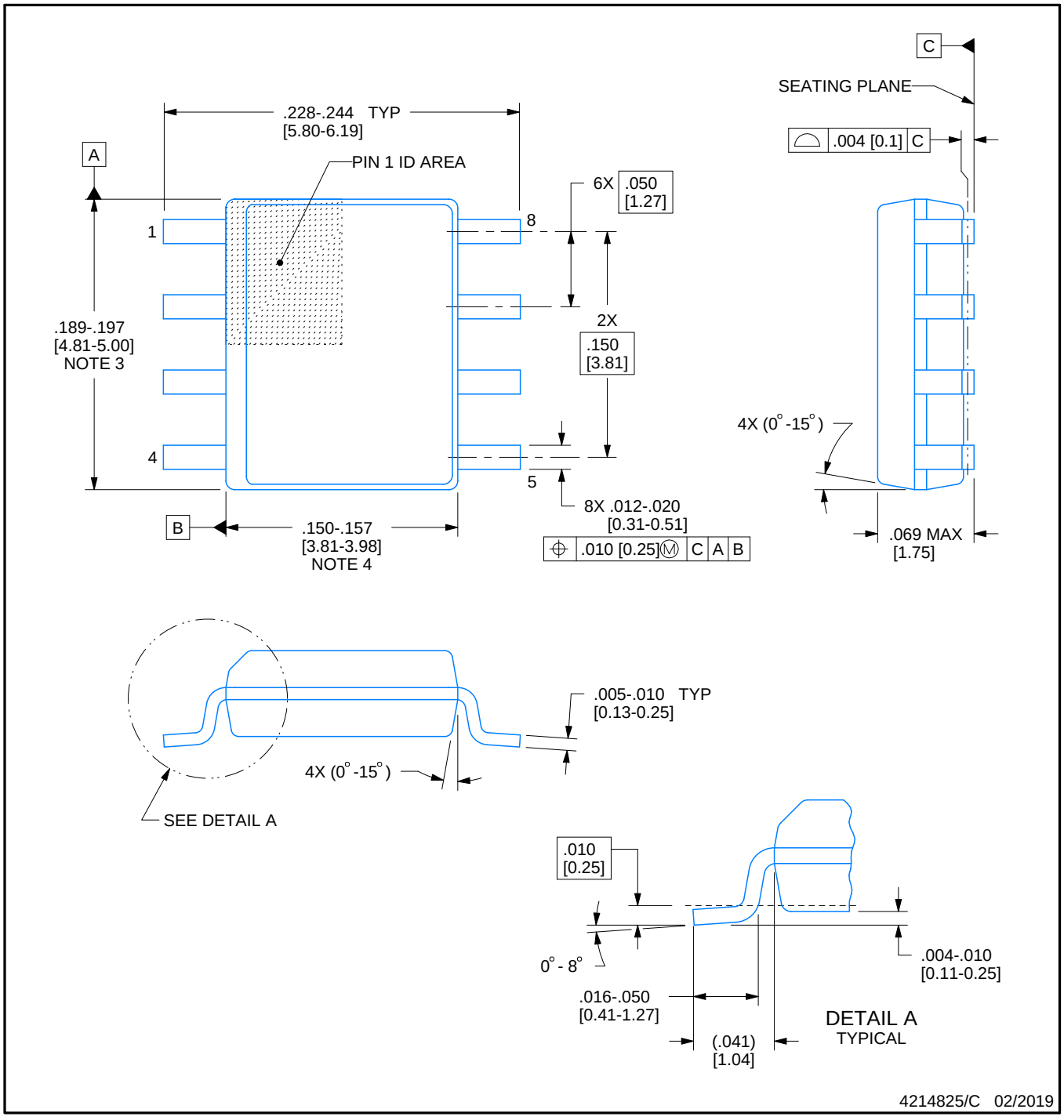


PACKAGE OUTLINE

D0008A

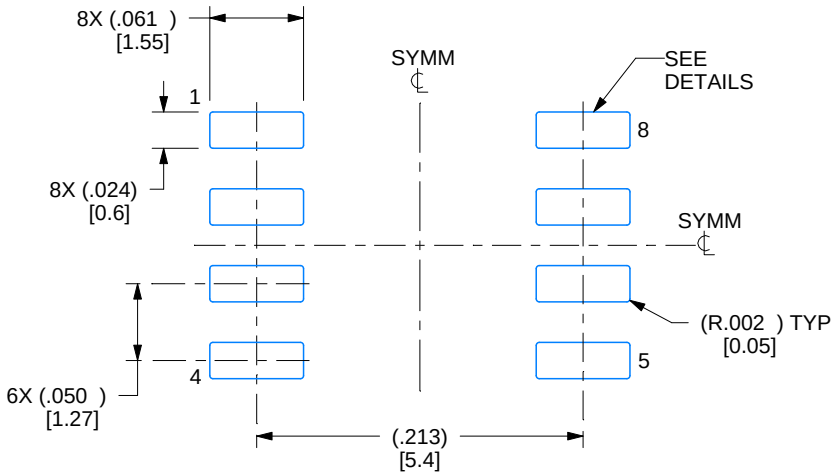
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

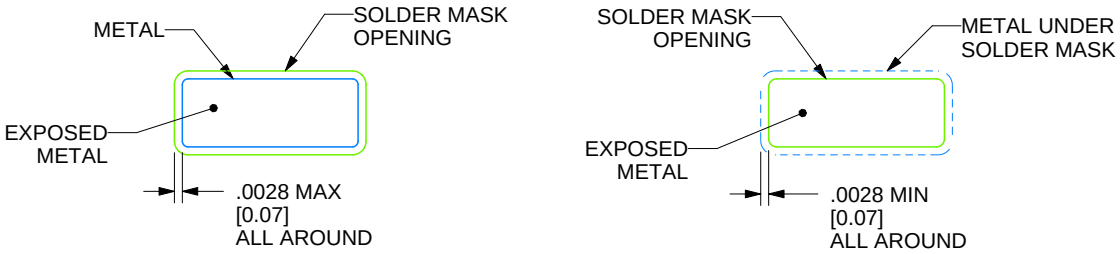


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

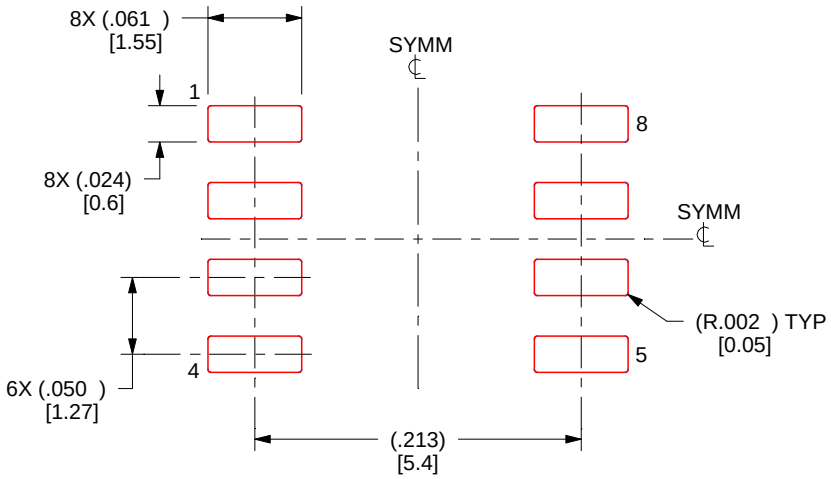
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



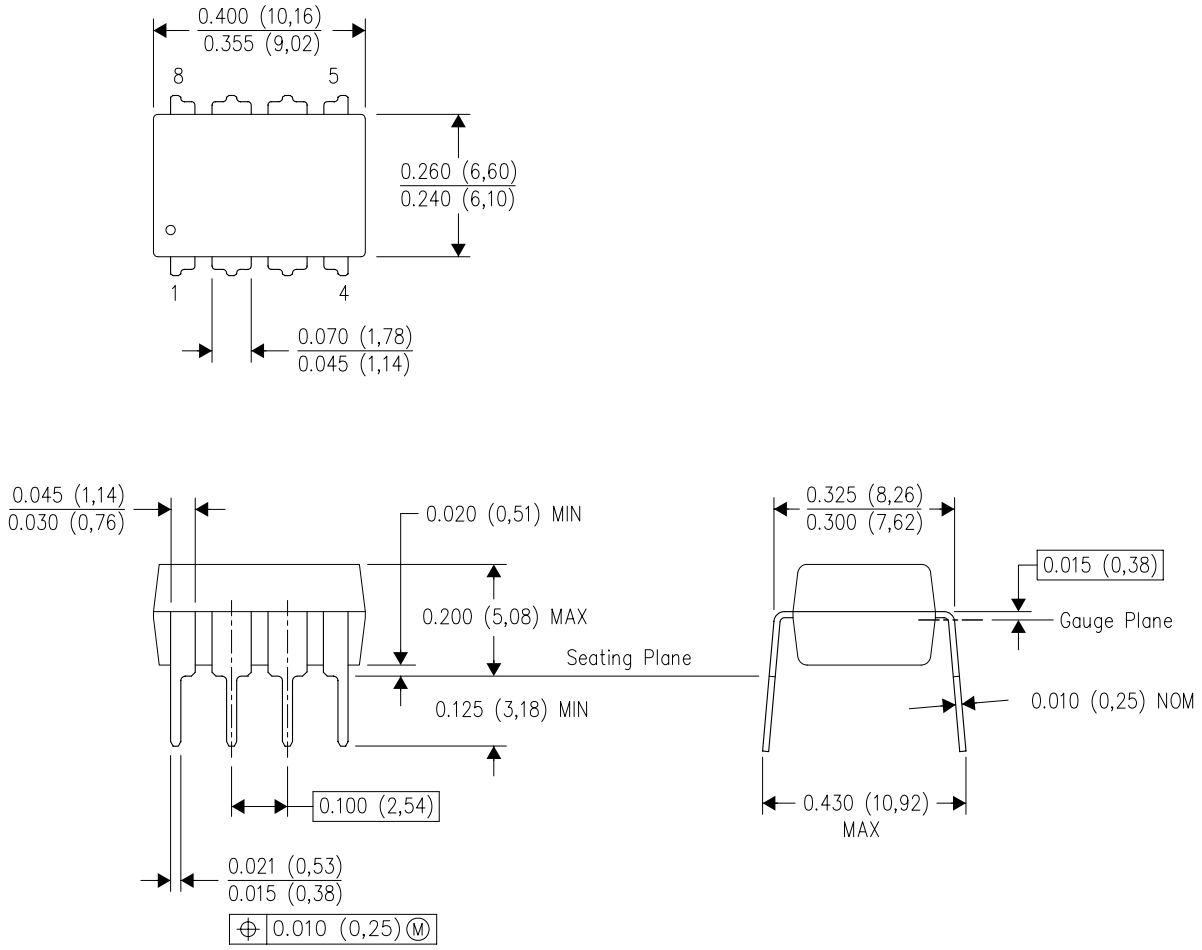
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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