

The TDS4 is a high voltage, high current disc pack SCR employing a high di/dt gate structure. This gate design allows the SCR to be reliably operated at high di/dt and dv/dt conditions in various phase control applications.

FEATURES:

- Low On-State Voltage
- High di/dt Capability
- High dv/dt Capability
- Hermetic Ceramic Package
- Excellent Surge and I²t Ratings

APPLICATIONS:

- DC Power Supplies
- Motor Controls

ORDERING INFORMATION

Select the complete 12 digit Part Number using the table below.
 EXAMPLE: TDS4443302DH is a4400V-3325A SCR with 300ma IGT and 12 inch gate and cathode potential leads.

PART	Voltage Rating $V_{DRM}-V_{RRM}$	Voltage Code	Current Rating I_{tavg}	Current Code	Turn-Off T_q	Gate I_{GT}	Leads
TDS4	4500	45	3325	33	0	2	DH
	4400	44					
	4200	42			600us	300ma	12"
	4000	40			(typ.)	(max)	

Absolute Maximum Ratings

Characteristic	Symbol	Rating	Units
Repetitive Peak Voltage	$V_{DRM}-V_{RRM}$	4000 - 4500	Volts
Average On-State Current, $T_C= 70\text{ }^\circ\text{C}$	$I_{T(Avg.)}$	3325	A
RMS On-State Current, $T_C= 70\text{ }^\circ\text{C}$	$I_{T(RMS)}$	5223	A
Average On-State Current, $T_C= 55\text{ }^\circ\text{C}$	$I_{T(Avg.)}$	3633	A
RMS On-State Current, $T_C= 55\text{ }^\circ\text{C}$	$I_{T(RMS)}$	5707	A
Peak One Cycle Surge Current, 60Hz, $V_R=0V$	I_{TSM}	56,000	A
Peak One Cycle Surge Current, 50Hz, $V_R=0V$	I_{TSM}	52,797	A
Fuse Coordination I^2t , 60Hz	I^2t	1.31E+07	A^2s
Fuse Coordination I^2t , 50Hz	I^2t	1.39E+07	A^2s
Critical Rate-of-Rise of On-State Current Repetitive from .67•VDRM	di/dt	100	A/us
Critical Rate-of-Rise of On-State Current Non-Repetitive from .67•VDRM	di/dt	150	A/us
Application Specific Repetitive di/dt Rate Linear Rate to 700A followed by 10A/us to Itavg.	di/dt	400	A/us
Peak Gate Power, 100us	P_{GM}	16	Watts
Average Gate Power	$P_{G(avg)}$	5	Watts
Operating Temperature	T_j	-40 to+125	$^\circ\text{C}$
Storage Temperature	$T_{Stg.}$	-50 to+150	$^\circ\text{C}$
Approximate Weight		5.0	lb
		2.27	Kg
Mounting Force		18,000 - 25,000	lbs
		80 - 110	KNewtons

Information presented is based upon manufacturers testing and projected capabilities. This information is subject to change without notice. The manufacturer makes no claim as to suitability for use, reliability, capability or future availability of this product.

Electrical Characteristics, Tj=25°C unless otherwise specified

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Repetitive Peak Forward Leakage Current	I_{DRM}	Tj=125°C, V_{DRM} =Rated			300	ma
Repetitive Peak Reverse Leakage Current	I_{RRM}	Tj=125°C, V_{RRM} =Rated			300	ma
Peak On-State Voltage	V_{TM}	Tj=125°C, I_{TM} = 4000 A			1.77	V
V_{TM} Model, Low Level	V_0	Tj=125°C			0.991	V
$V_{TM} = V_0 + r \cdot I_{TM}$	r	15% $I_{TM} - \pi \cdot I_{TM}$			0.196	mΩ
V_{TM} Model, High Level	V_0	Tj=125°C			0.772	V
$V_{TM} = V_0 + r \cdot I_{TM}$	r	$\pi \cdot I_{TM} - I_{TSM}$			0.218	mΩ
V_{TM} Model, 4-Term	A	Tj=125°C			0.132	
$V_{TM} = A + B \cdot \ln(I_{TM}) +$	B	15% $I_{TM} - I_{TSM}$			0.181	
$C \cdot (I_{TM}) + D \cdot (I_{TM})^{1/2}$	C				2.57E-04	
	D				-1.41E-02	
Turn-On Delay Time	t_d	$V_D = 0.5 \cdot V_{DRM}$ Gate Drive: 40V - 20Ω			3	us
Turn-Off Time (typ)	t_q	Tj=125°C $dv/dt = 20V/us$ to 80% V_{DRM}			600	us
$dv/dt_{(crit)}$	dv/dt	Tj=125°C Exp. Waveform $V_D = 67\%$ Rated			2000	V/us
Gate Trigger Current	I_{GT}	Tj=25°C $V_D = 12V$	40	100	300	ma
Gate Trigger Voltage	V_{GT}		0.8	2.0	4.0	V
Peak Reverse Gate Voltage	V_{GRM}				5	V

Thermal Characteristics

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Thermal Resistance						
Junction to Case	$R\theta_{jc}$	Double side cooled		0.0055	0.006	°C/Watt
Case to Sink	$R\theta_{cs}$	Double side cooled		0.001	0.0015	°C/Watt

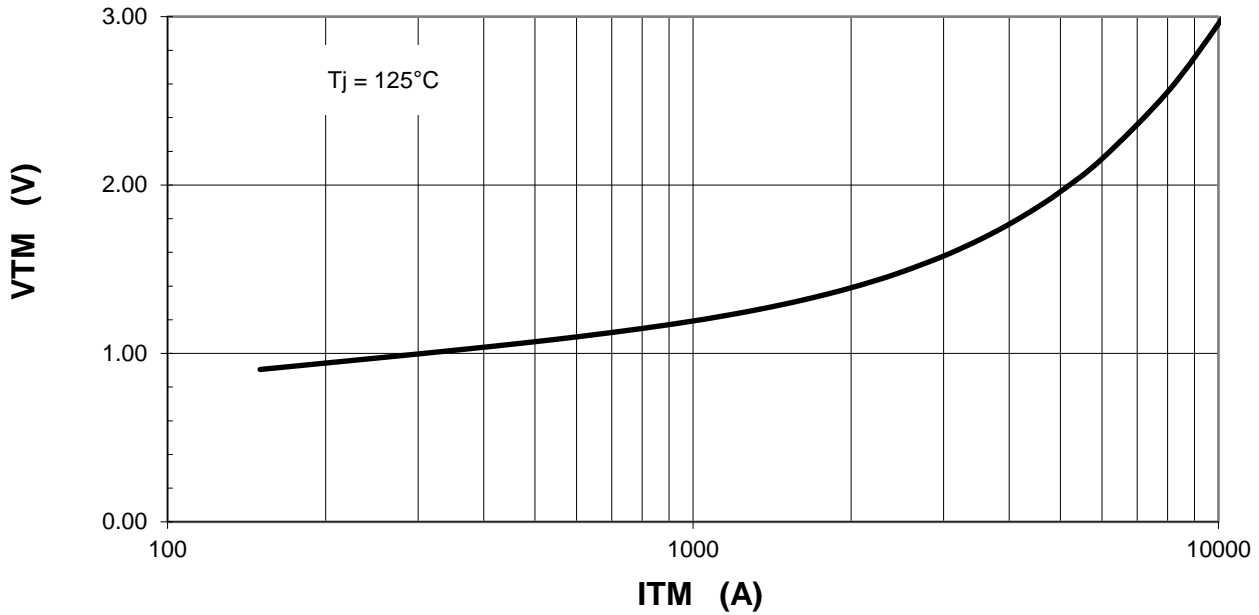
Thermal Impedance Model $Z\theta_{jc}$ Double side cooled

$$Z\theta_{jc}(t) = \sum(A(N) \cdot (1 - \exp(-t/Tau(N))))$$

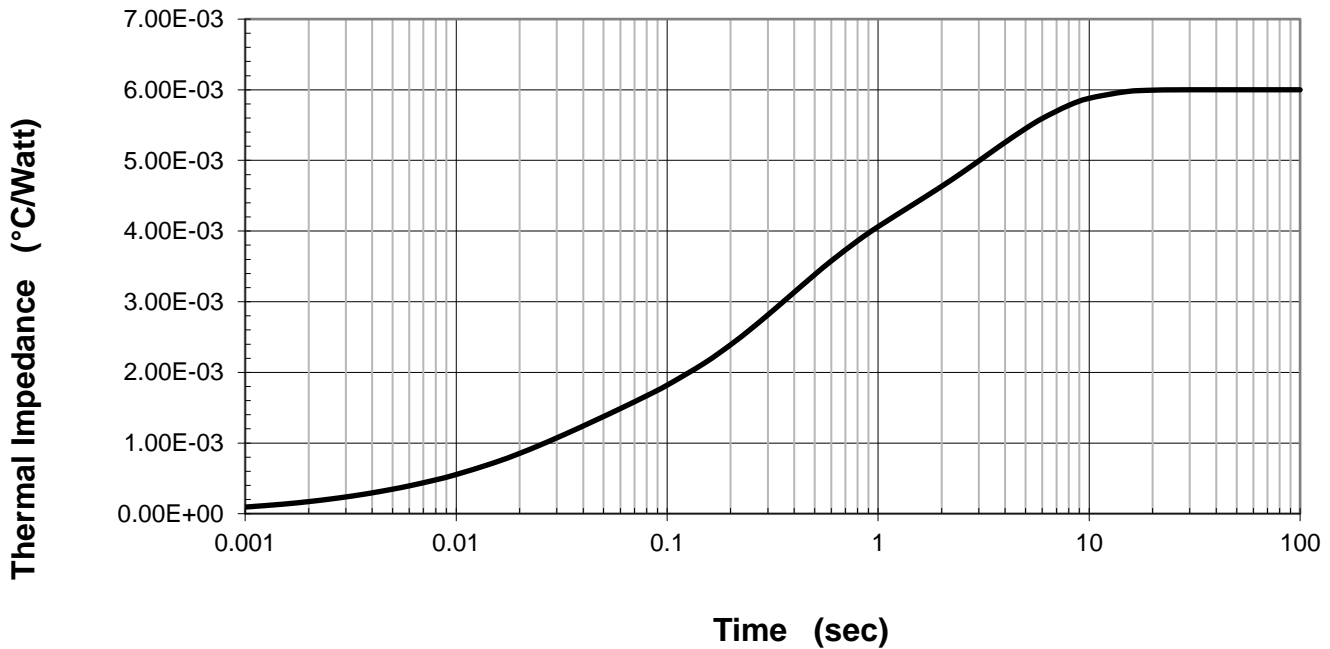
where: N = 1 2 3 4

A(N) =	1.43E-04	9.38E-04	2.42E-03	2.50E-03
Tau(N) =	2.62E-03	2.31E-02	3.05E-01	3.30E+00

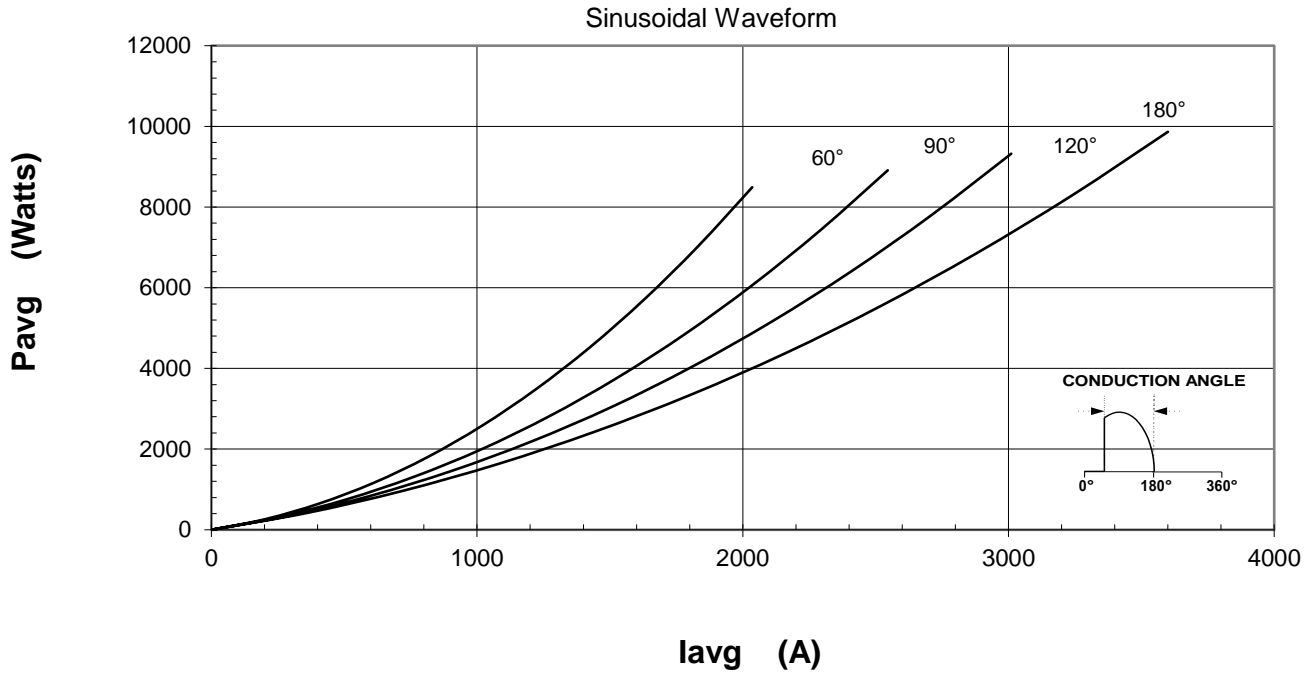
Maximum On-State Voltage Drop



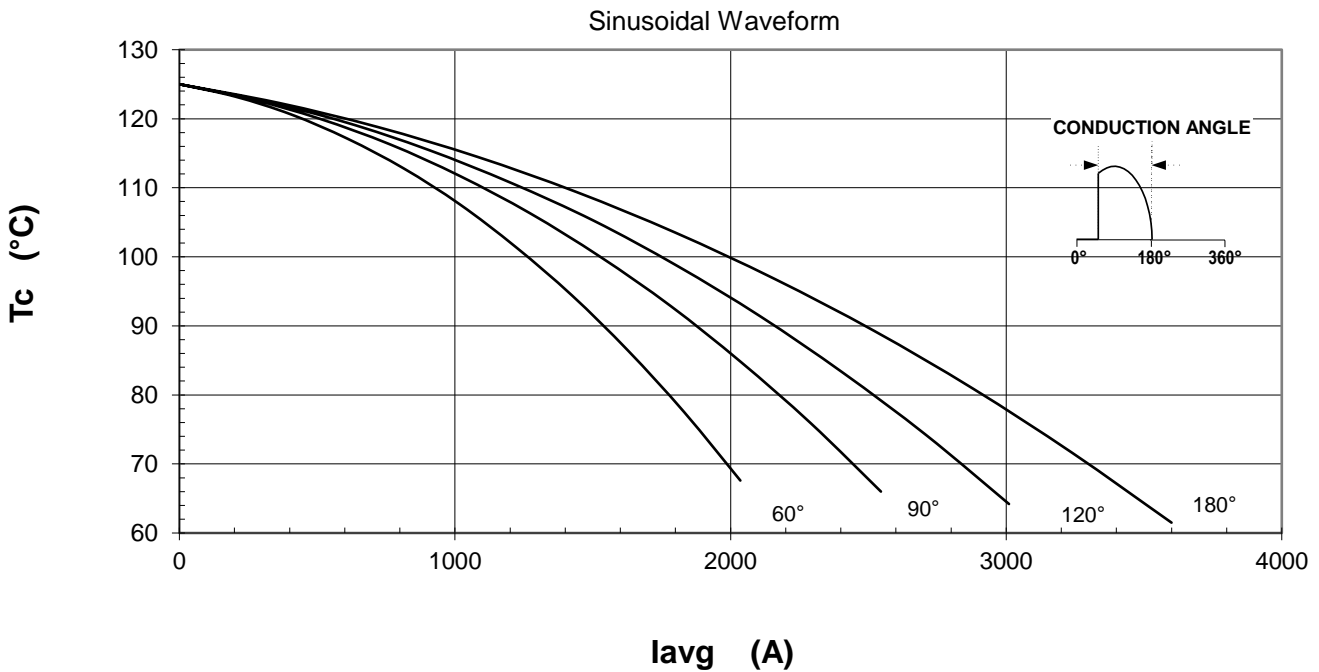
Maximum Transient Thermal Impedance



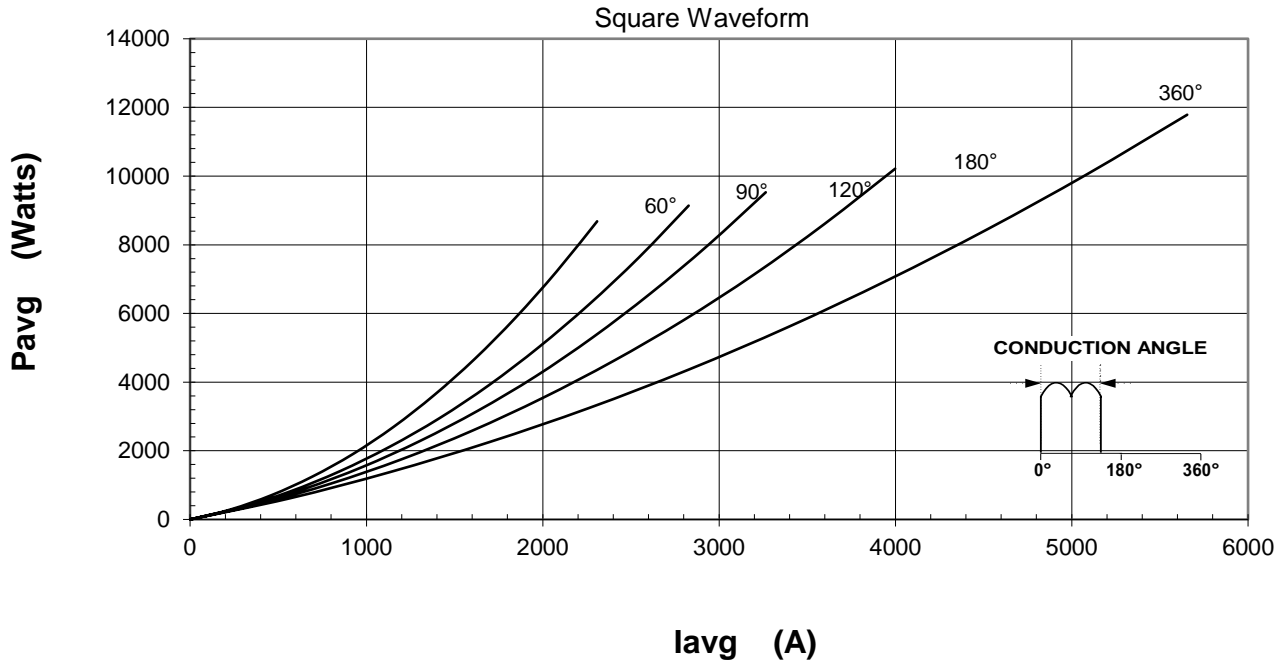
Maximum On-State Power Dissipation



Maximum Allowable Case Temperature



Maximum On-State Power Dissipation



Maximum Allowable Case Temperature

