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U_DDR3-RAM
DDR3-RAM.SchDoc

U_Ethernet
Ethernet.SchDoc

U_USB-PHY
USB-PHY.SchDoc

U_SOC
SOC.SchDoc

U_CPLD
CPLD.SchDoc

U_POWER2
POWER2.SchDoc

U_HyperFlash_RAM
HyperFlash_RAM.SchDoc

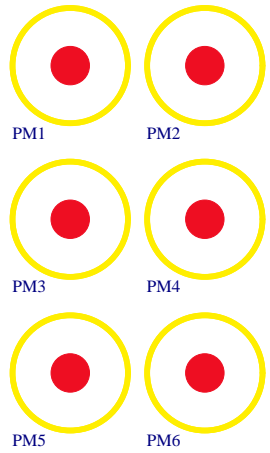
U_Clock
Clock.SchDoc

U_eMMC
eMMC.SchDoc

U_Connectors
Connectors.SchDoc

U_POWER
POWER.SchDoc

LOGO1
TE Logo PRINT Layer
LOGO PRINT



Serial
Serialnumber 6,3 x 6.3mm

Special notes:



Title: TE0782 - Overview		
A4	Number: TE0782 A2I33MA	Rev. 02
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Filename: TE0782.SchDoc		

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U_HSMC_CONN_J1
HSMC_CONN_J1.SchDoc



U_HSMC_CONN_J2
HSMC_CONN_J2.SchDoc



U_HSMC_CONN_J3
HSMC_CONN_J3.SchDoc



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		Title: TE0782 - Connectors	
		A4	Number: TE0782 A2I33MA
Date: 2015-05-27		Copyright: Trenz Electronic GmbH	
Filename: Connectors.SchDoc		Page2 of 31	

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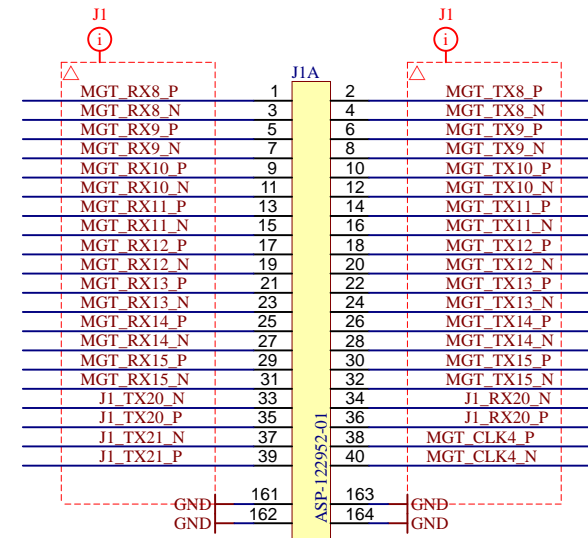
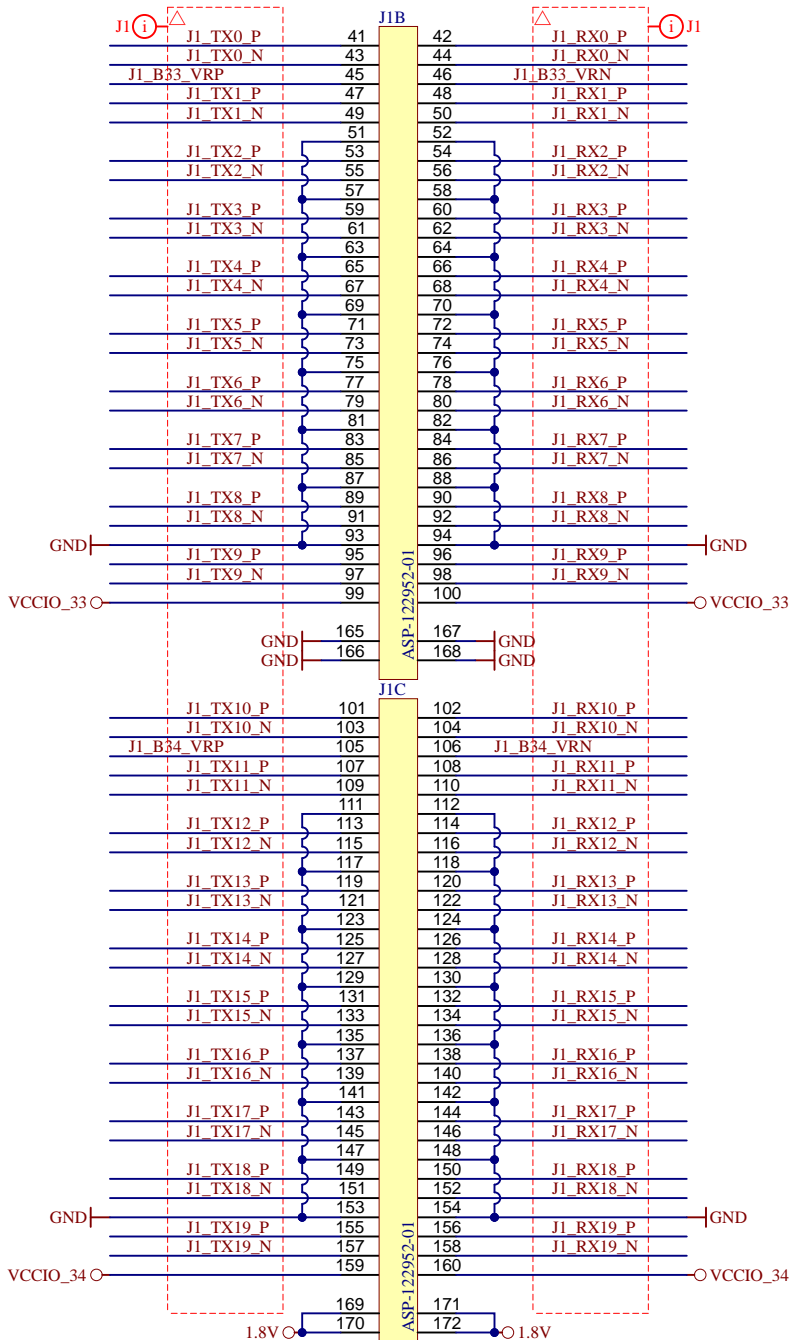
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Title: TE0782 - HSMC_Connector_J1

A4	Number: TE0782 A2I33MA	Rev. 02
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Filename: HSMC_CONN_J1.SchDoc		

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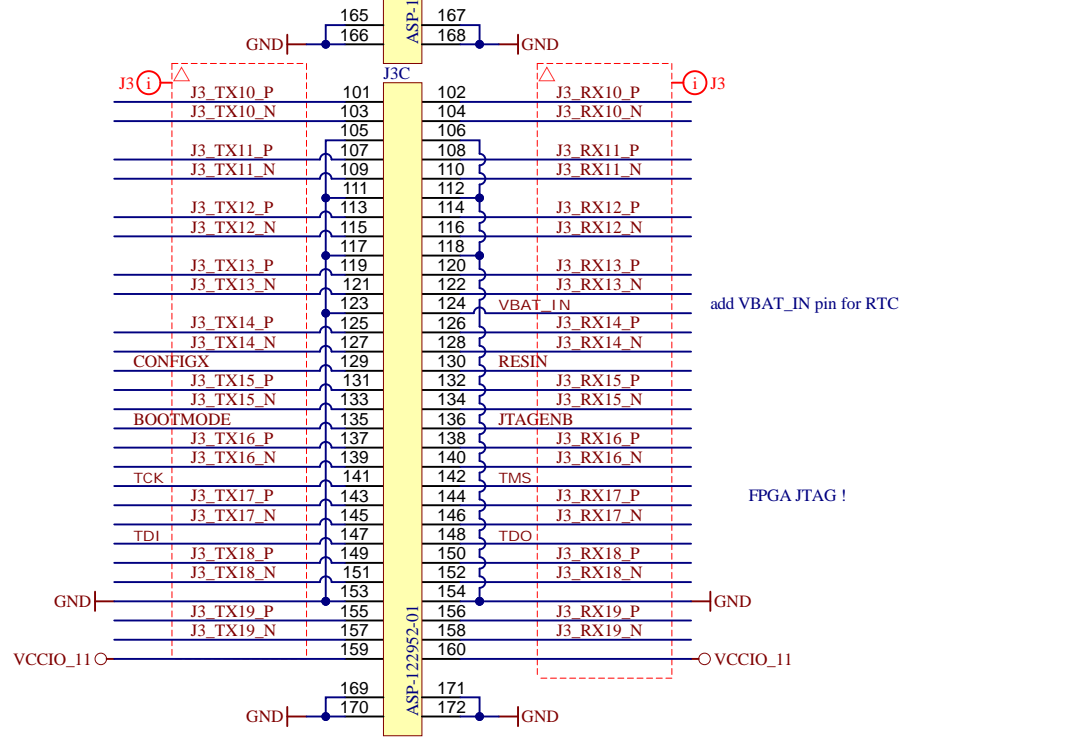
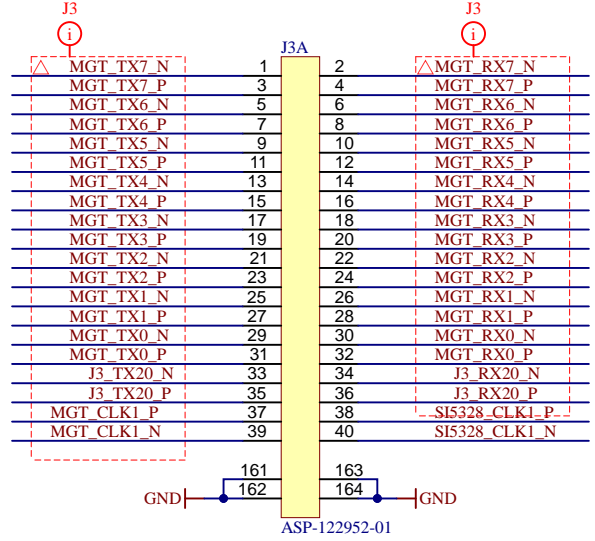
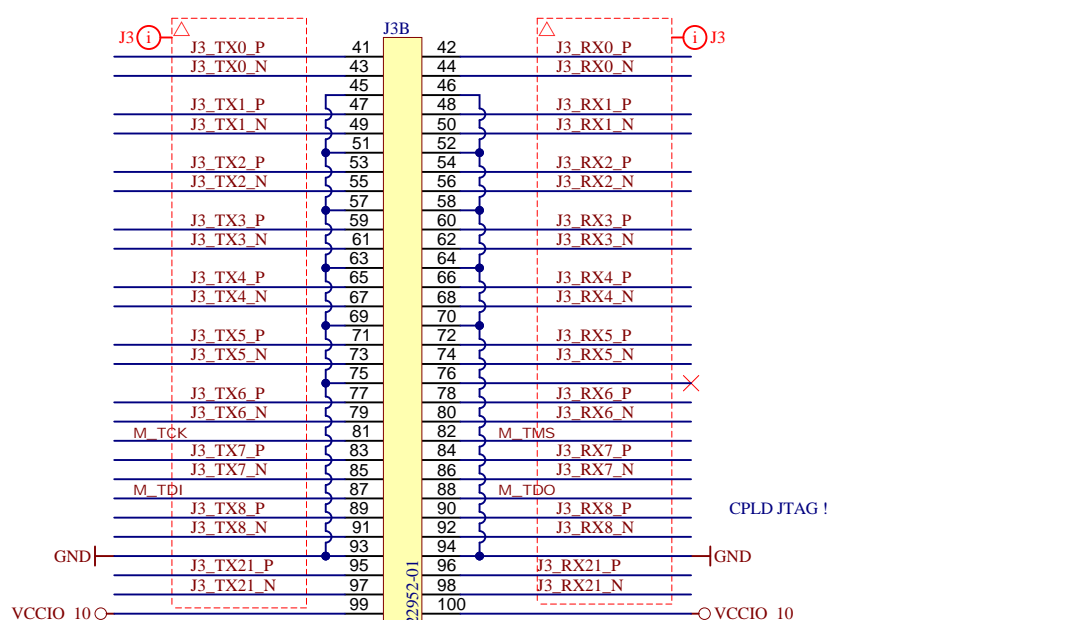
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Title: TE0782 - HSMC_Connector_J3		
A4	Number: TE0782 A2I33MA	Rev. 02
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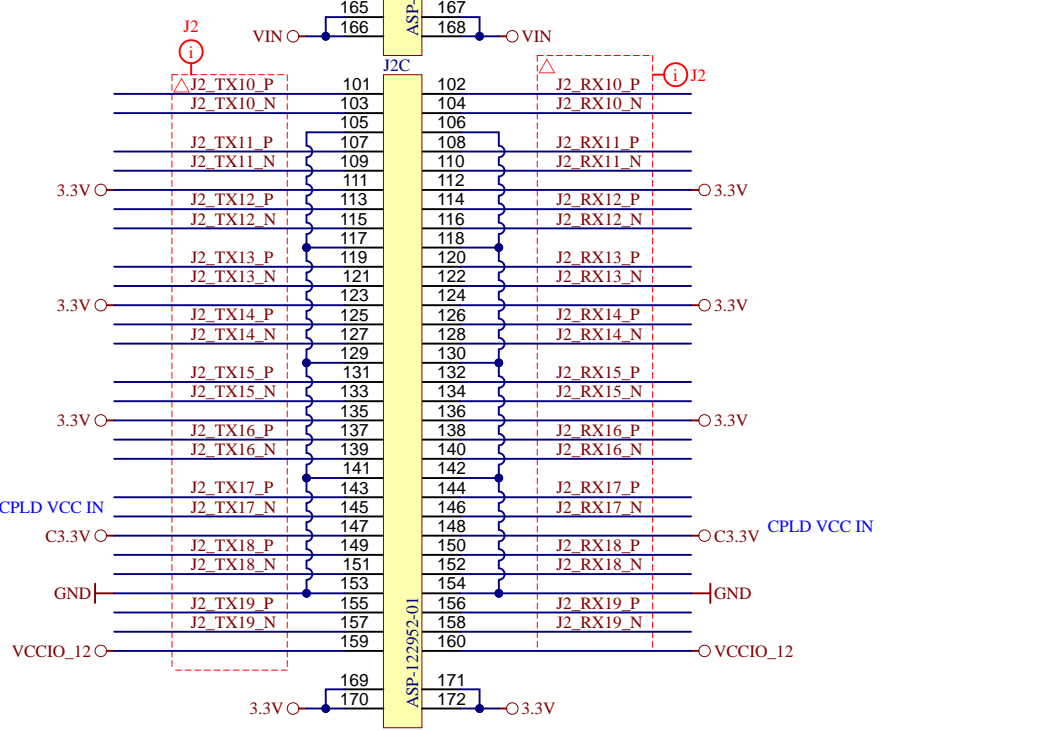
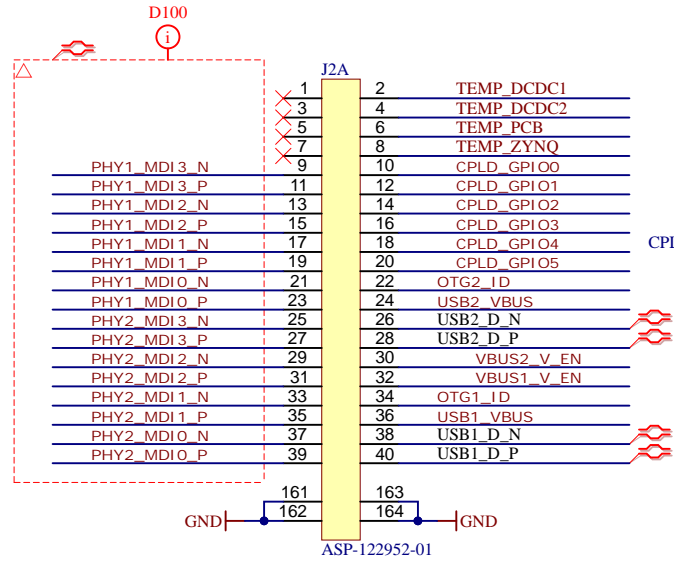
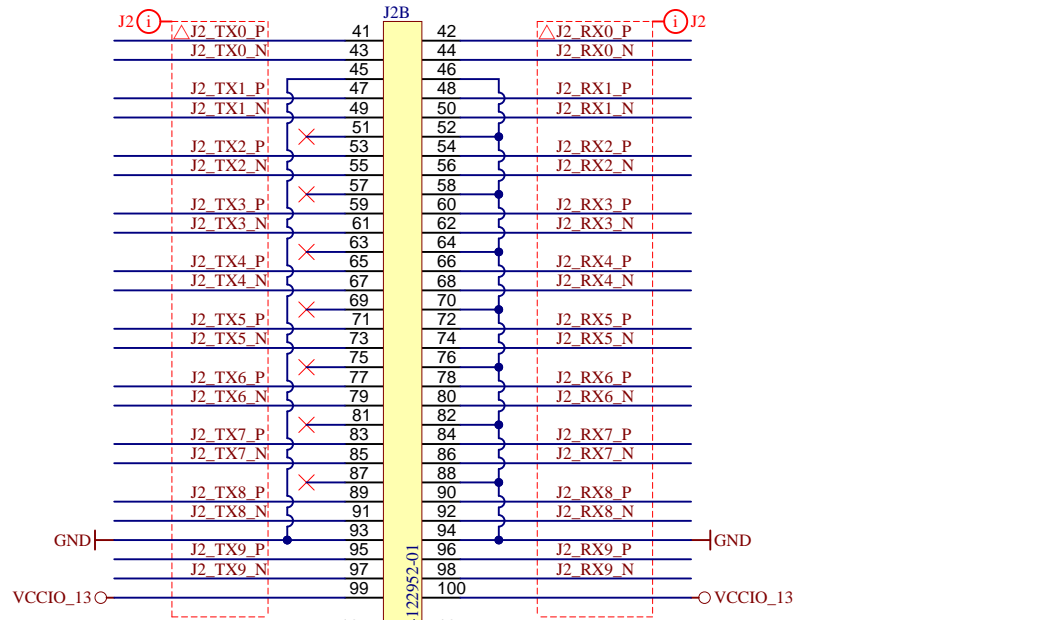
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Title: TE0782 - HSMC_Connector_J2		
A4	Number: TE0782 A2I33MA	Rev. 02
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U_PS-DDR
PS-DDR.SchDoc



U_B9
B9.SchDoc



U_MIO-BANKS
MIO-BANKS.SchDoc



U_B10
B10.SchDoc



U_HP-BANKS
HP-BANKS.SchDoc



U_B11
B11.SchDoc



B

B

U_FPGA-MGT
FPGA-MGT.SchDoc



U_B12
B12.SchDoc



U_FPGA-CFG
FPGA-CFG.SchDoc



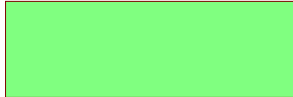
U_B13
B13.SchDoc



C


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U_FPGA-PWR
FPGA-PWR.SchDoc



D

D

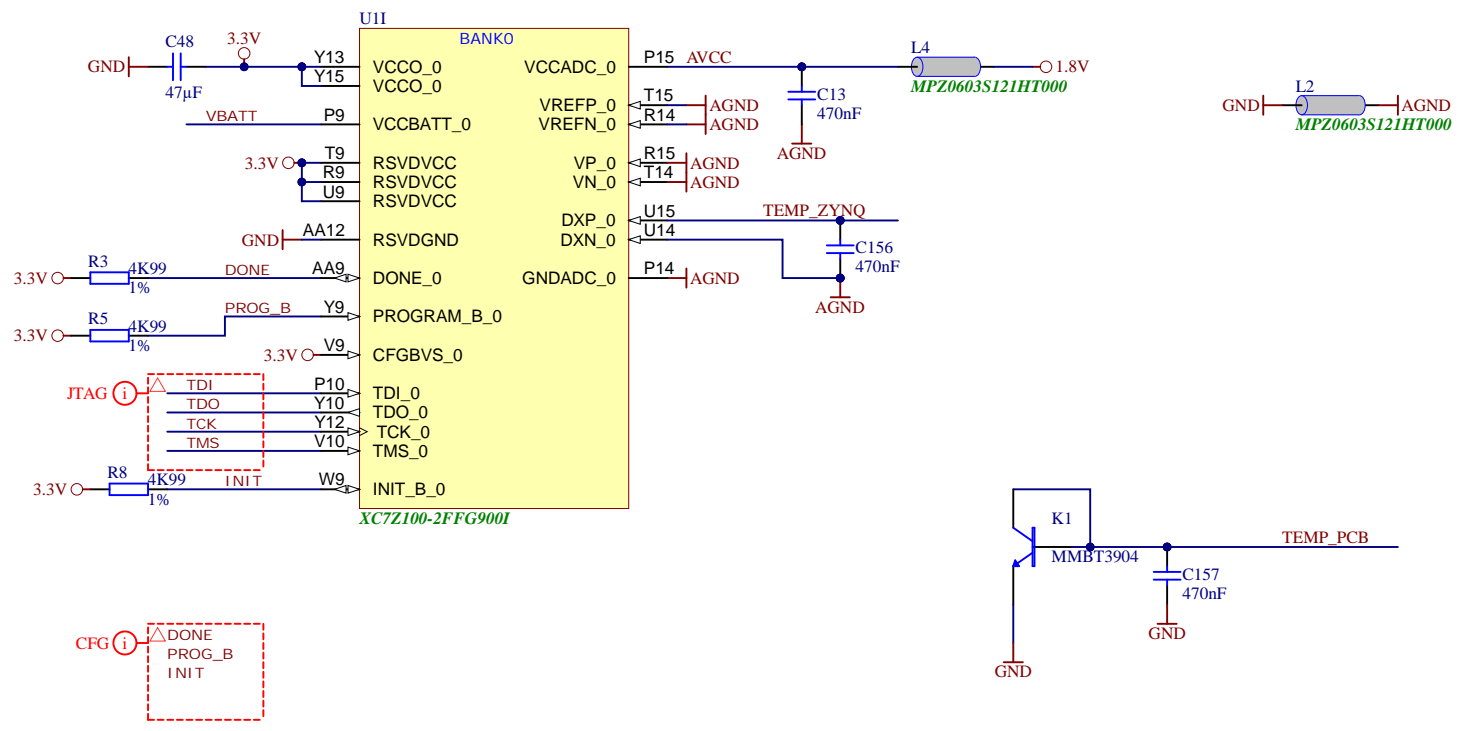
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		A4	Number: TE0782 A2I33MA
Date: 2015-05-27		Copyright: Trenz Electronic GmbH	
Filename: SOC.SchDoc		Page6 of 31	


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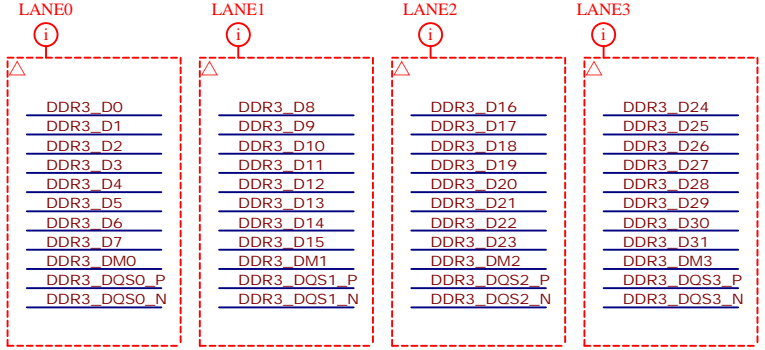
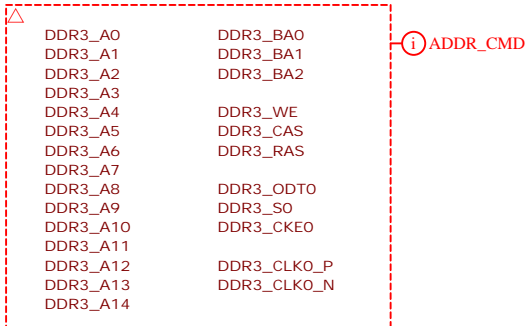
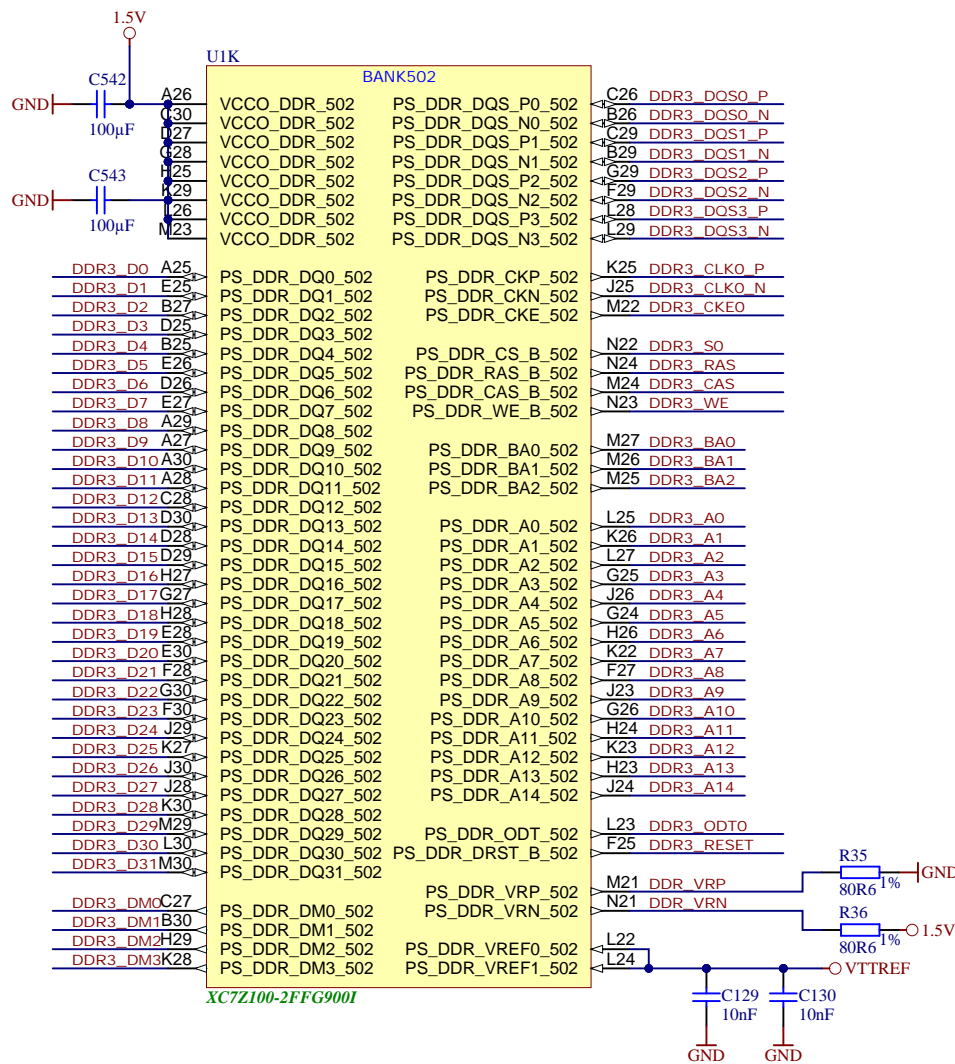
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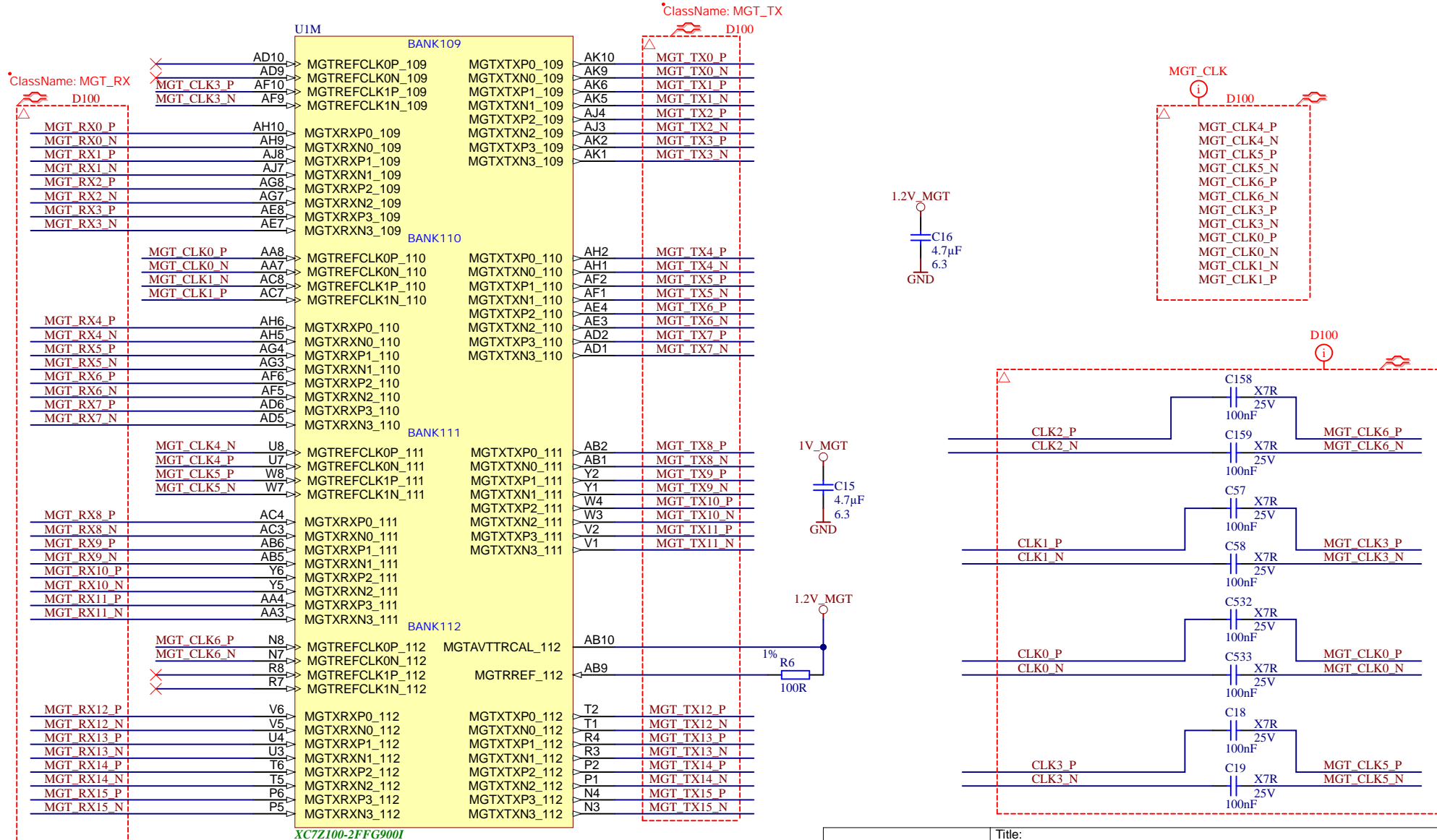
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		Title: TE0782 - FPGA Configuration	
		A4	Nummer: TE0782 A2I33MA
Datum: 2015-05-27		Zeichner: Trenz Electronic GmbH	
Filename: FPGA-CFG.SchDoc		Blatt 7 von 31	



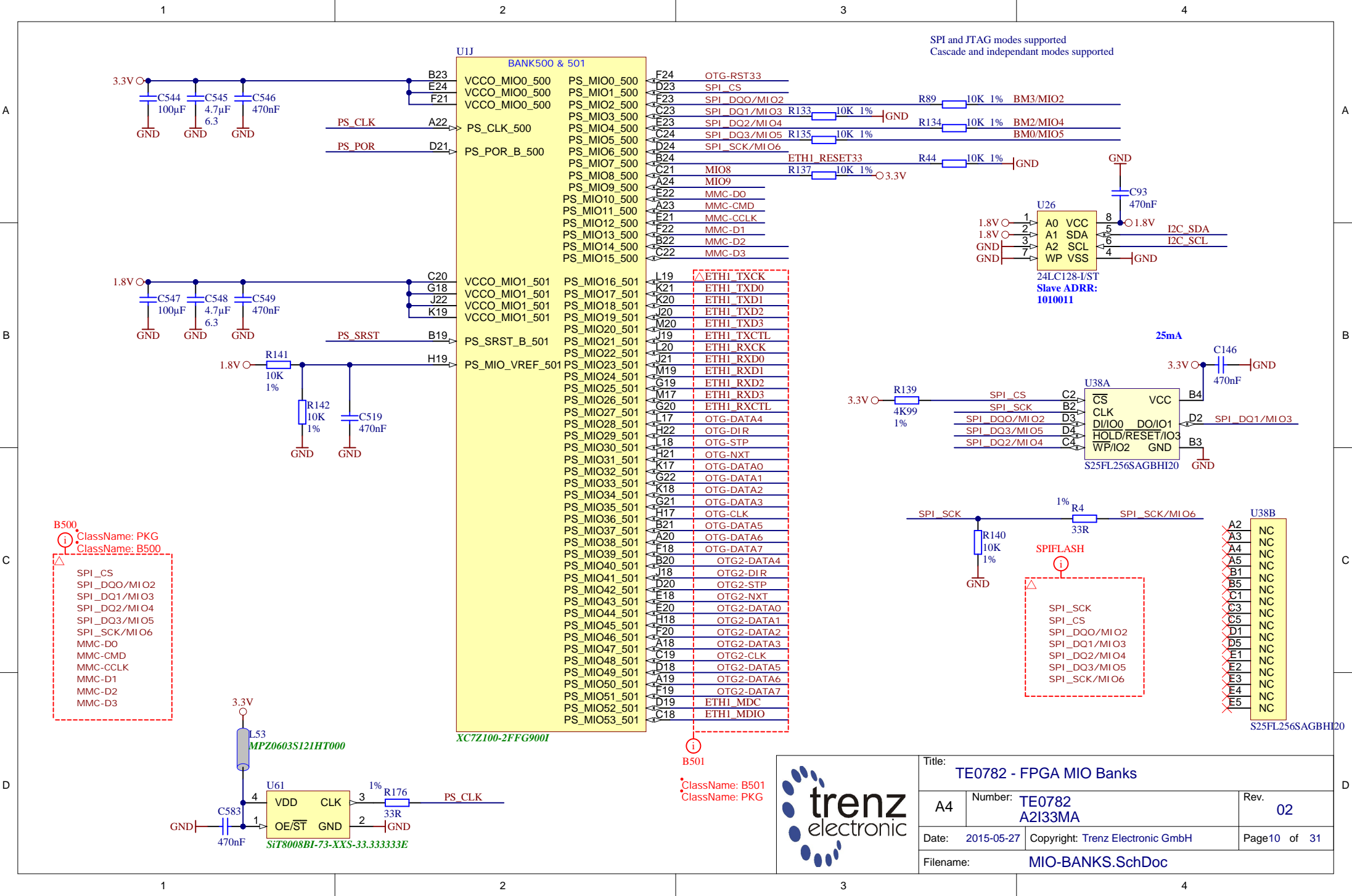
			Title: TE0782 - FPGA DDR Banks	
			A4	Number: TE0782 A2I33MA
Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page 8 of 31
Filename: PS-DDR.SchDoc				



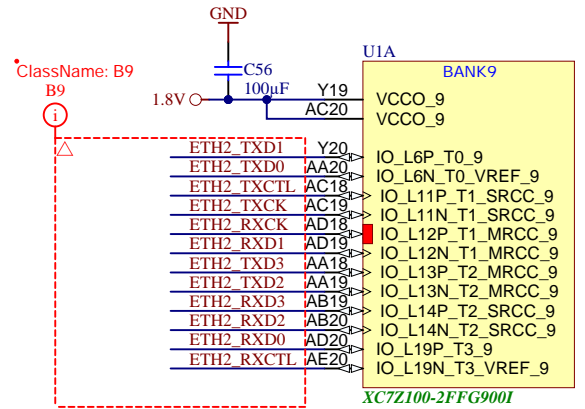
XC7Z100-2FFG900I



Title: TE0782 - FPGA MGT		
A4	Number: TE0782 A2I33MA	Rev. 02
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Filename: FPGA-MGT.SchDoc		



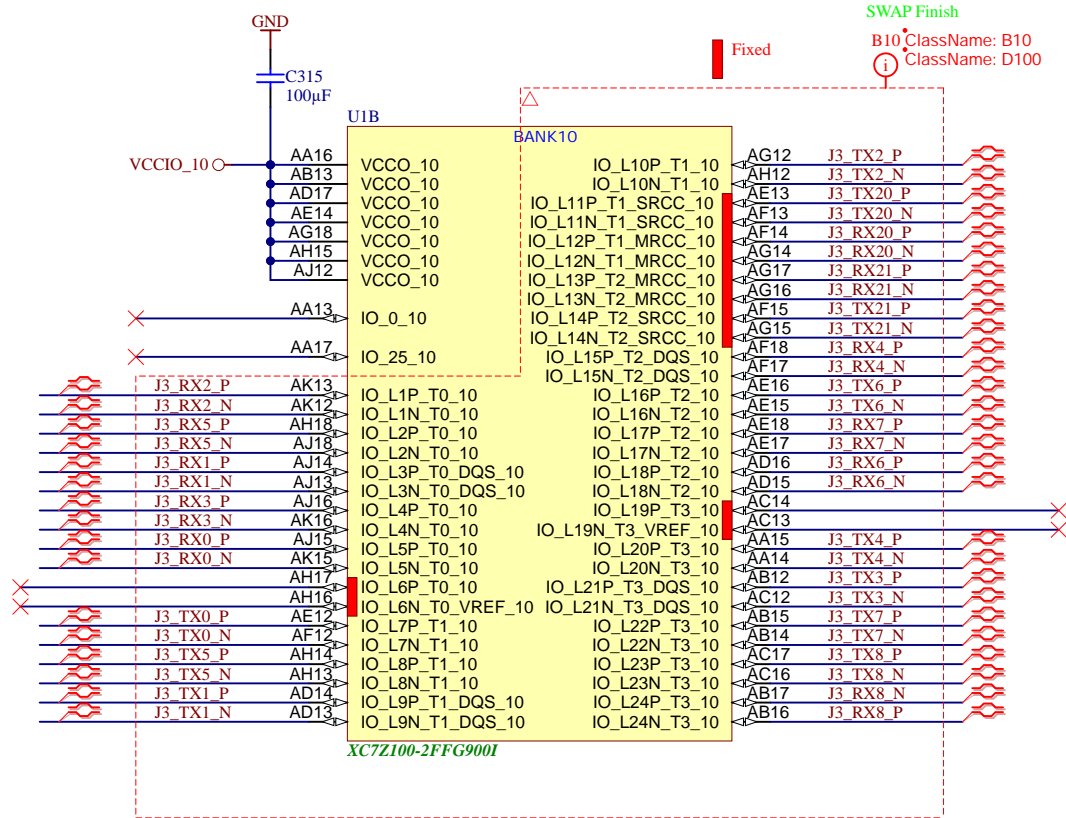
Title: TE0782 - FPGA MIO Banks		
A4	Number: TE0782 A2I33MA	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 10 of 31
Filename: MIO-BANKS.SchDoc		




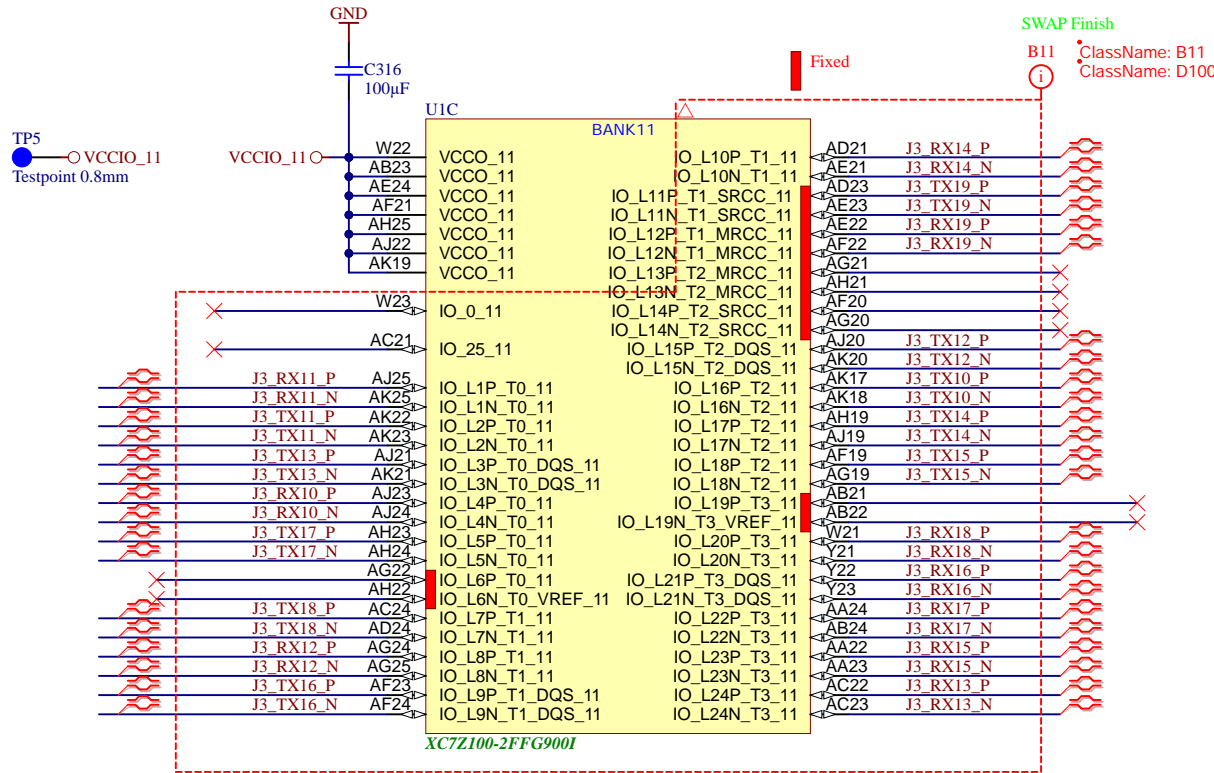
RXCK Fix to MRCCL
 Fixed

	Title: TE0782 - FPGA B9		
	A4	Number: TE0782 A2I33MA	Rev. 02
	Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 11 of 31
	Filename: B9.SchDoc		


TP4
 ● ○ VCCIO_10
 Testpoint 0.8mm

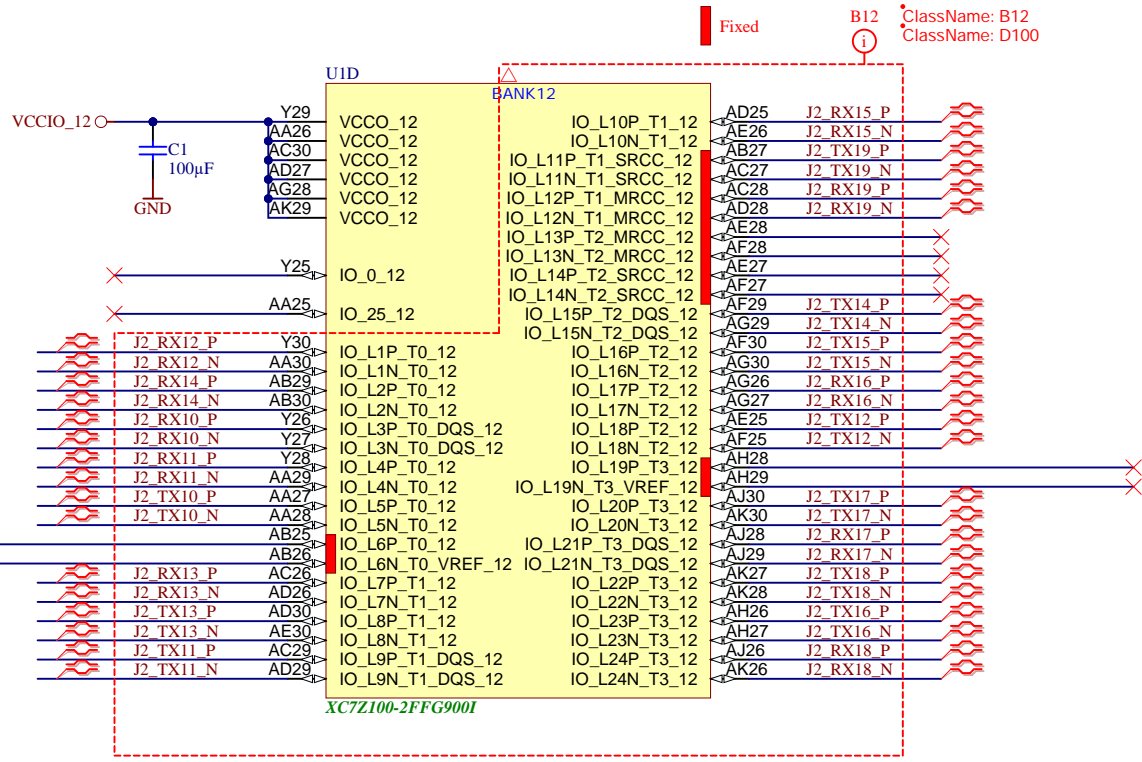


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	Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 12 of 31
	Filename: B10.SchDoc		

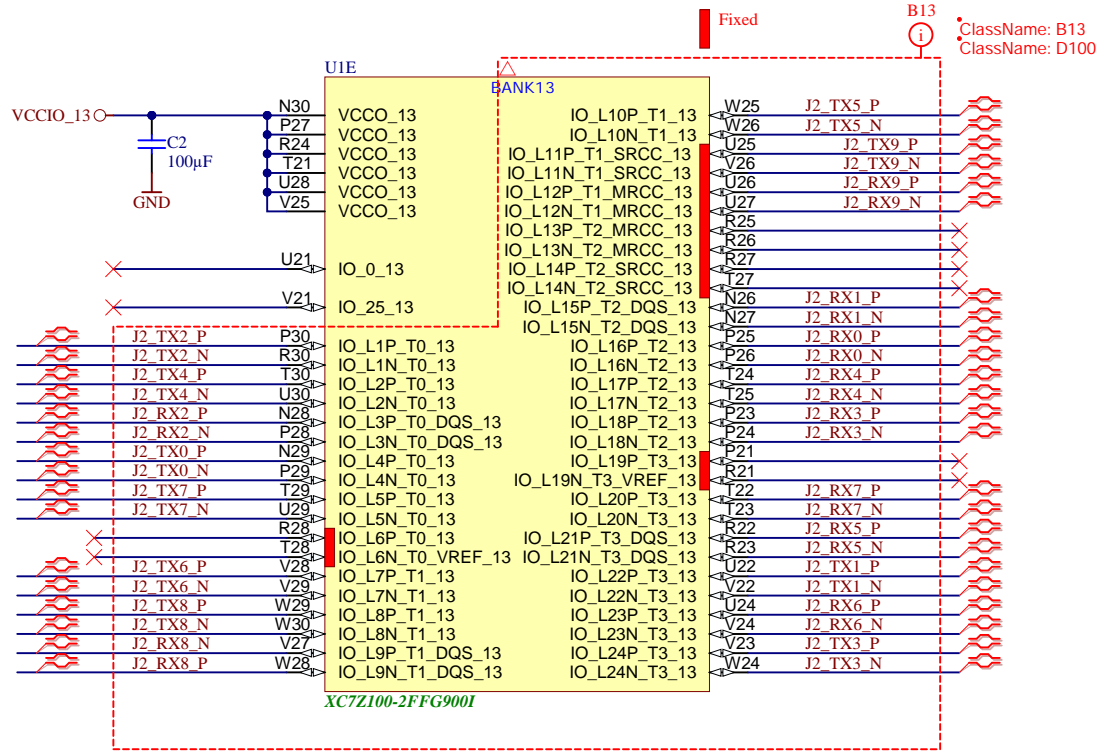
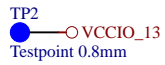



	Title: TE0782 - FPGA B11		
	A4	Number: TE0782 A2I33MA	Rev. 02
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	Filename: B11.SchDoc		

TP1
 VCCIO_12
 Testpoint 0.8mm



Title: TE0782 - FPGA B12		
A4	Number: TE0782 A2I33MA	Rev. 02
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			Title: TE0782 - FPGA B13	
			A4	Number: TE0782 A2I33MA
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Filename: B13.SchDoc				

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U_B33
B33.SchDoc



U_B34
B34.SchDoc



U_B35
B35.SchDoc



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		Title: TES0782 - FPGA HP Banks	
		A4	Number: TE0782 A2I33MA
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Filename: HP-BANKS.SchDoc		Page 16 of 31	

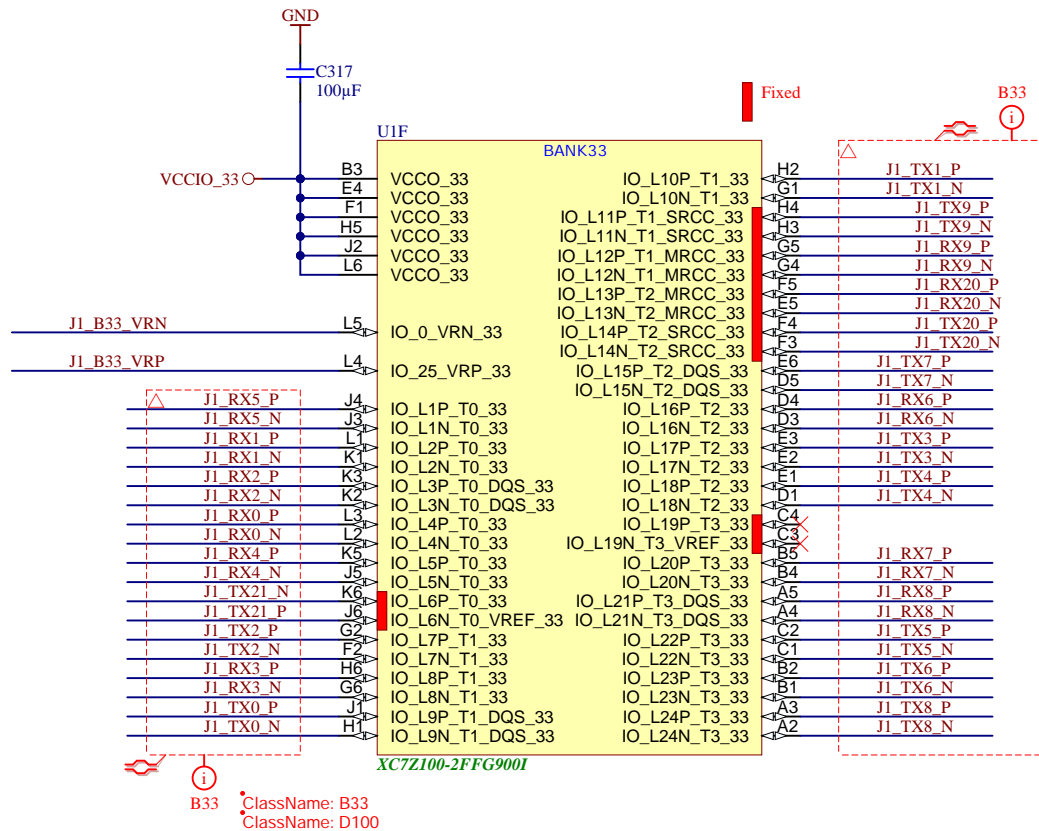
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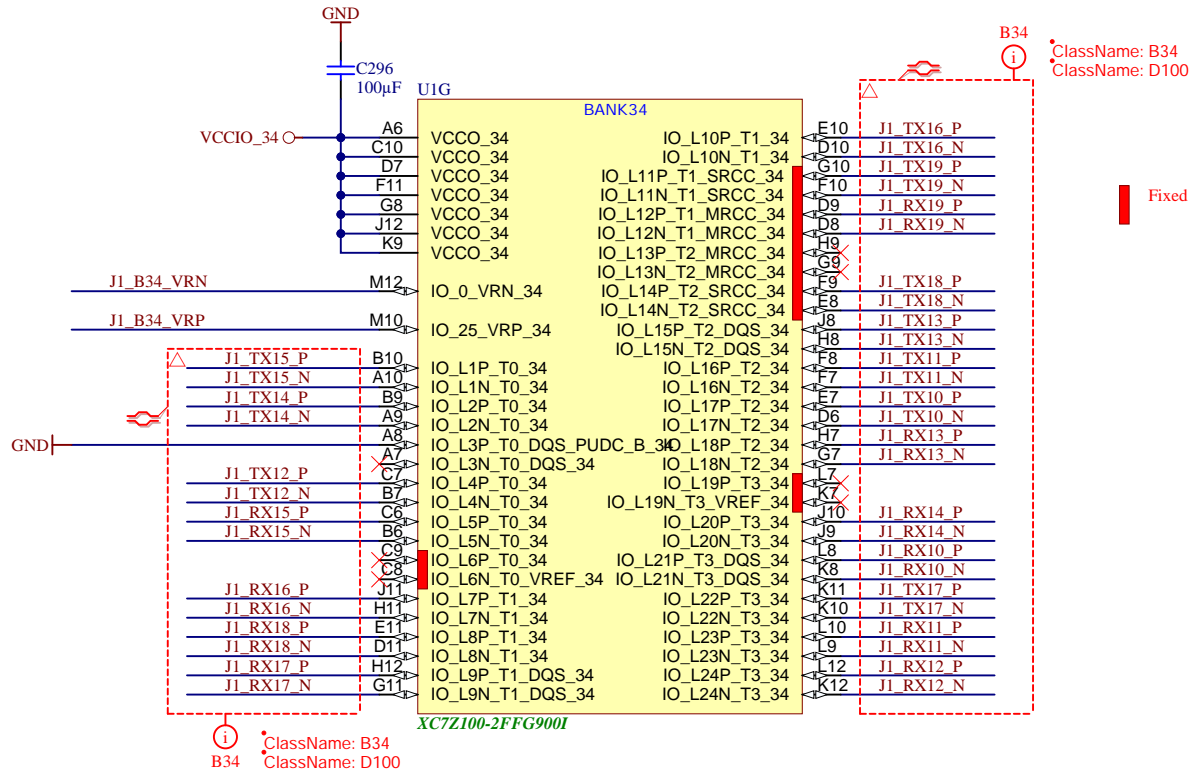
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TP6
 ● ○ VCCIO_33
 Testpoint 0.8mm

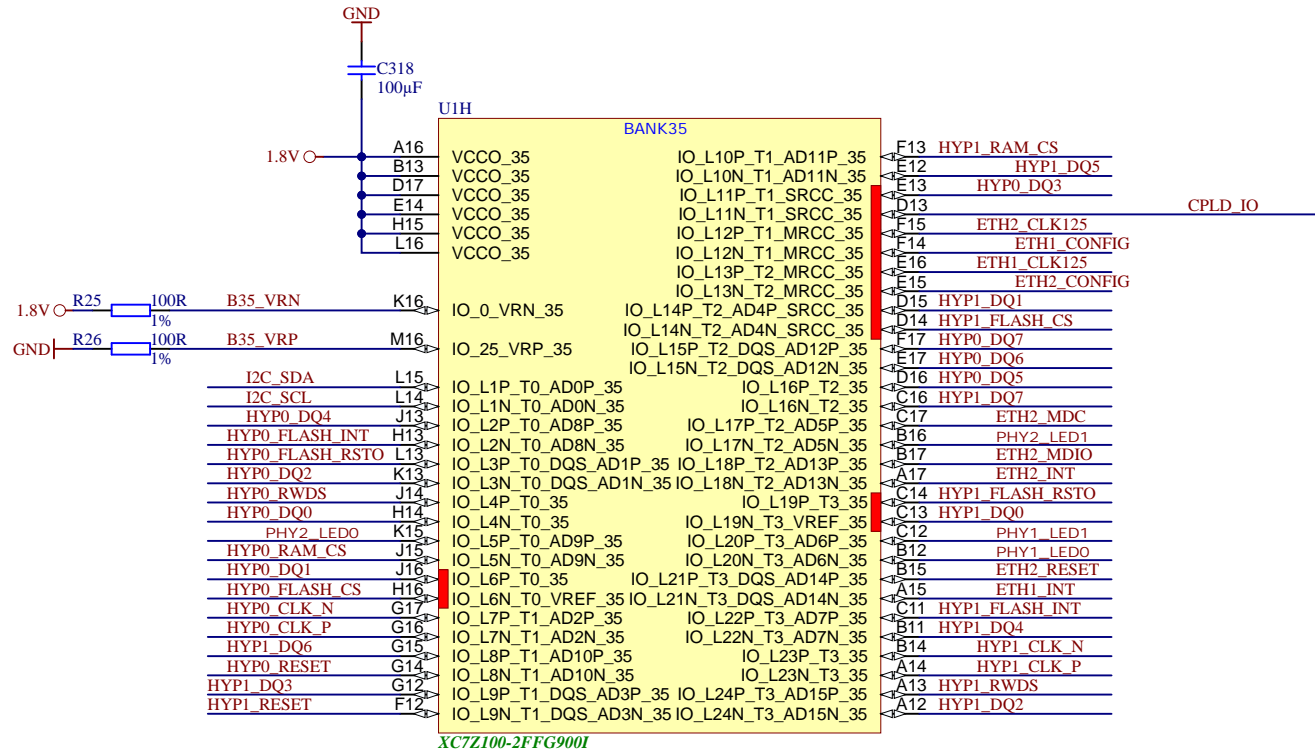


	Title: TE0782 - FPGA B33		
	A4	Number: TE0782 A2I33MA	Rev. 02
	Date: 2015-05-27	Copyright: Trenz Electronic GmbH	
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TP3
 VCCIO_34
 Testpoint 0.8mm

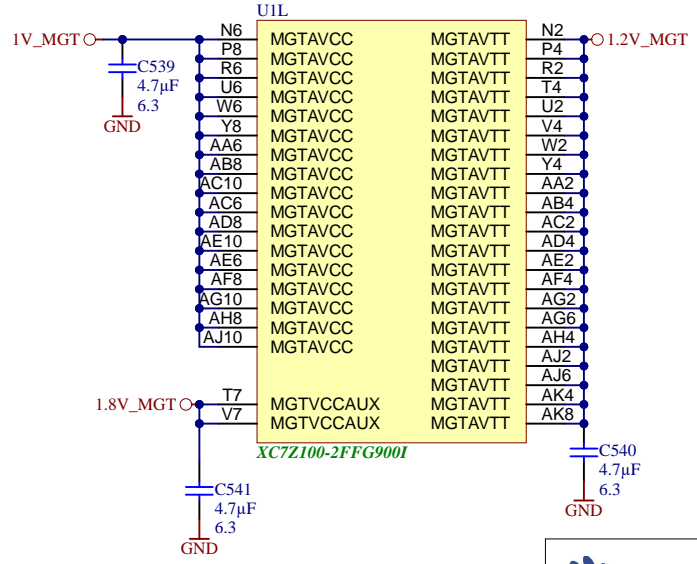
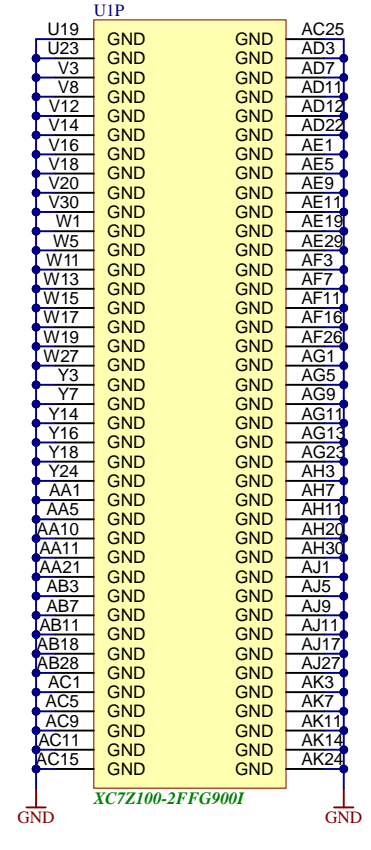
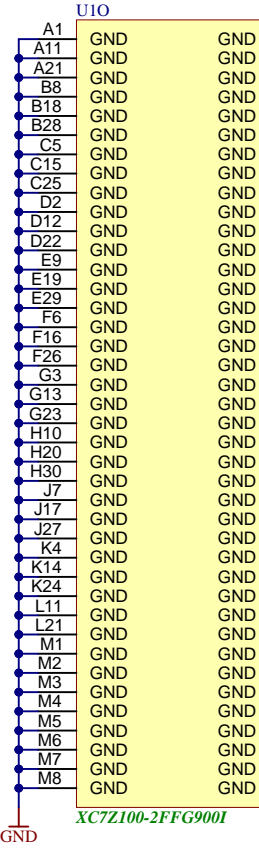
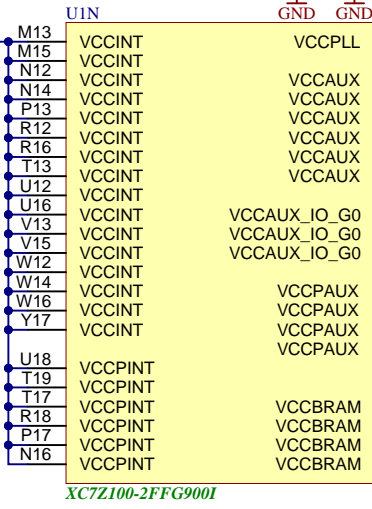
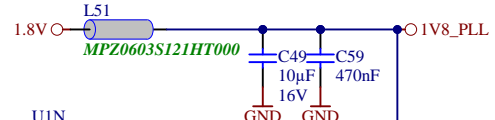
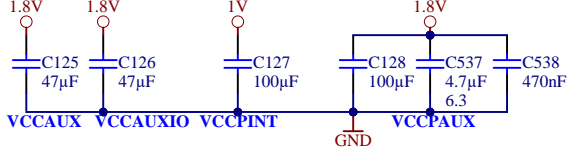
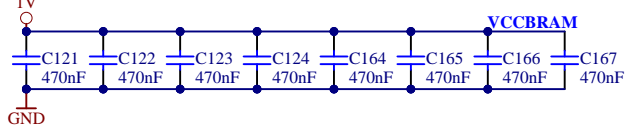
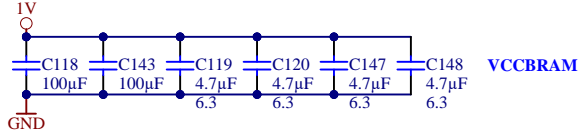
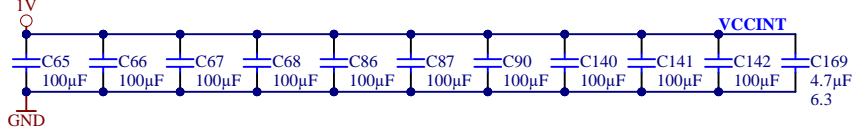
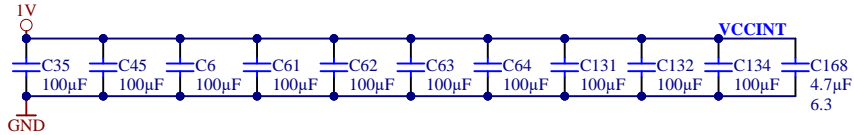


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A4	Number: TE0782 A2I33MA	Rev. 02
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Title: TE0782 - FPGA B35		
A4	Number: TE0782 A2I33MA	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 19 of 31
Filename: B35.SchDoc		

Capacitors suitable for XC7Z100



Title: TE0782 - ZYNQ POWER		
A4	Number: TE0782 A2I33MA	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	
Filename: FPGA-PWR.SchDoc		Page20 of 31

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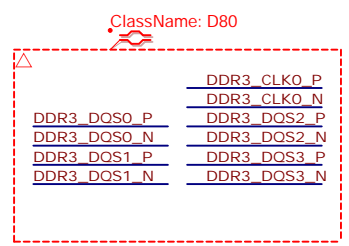
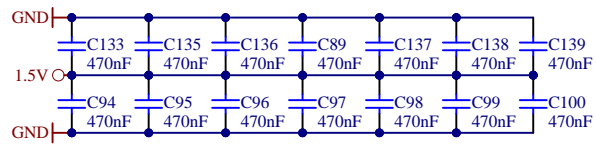
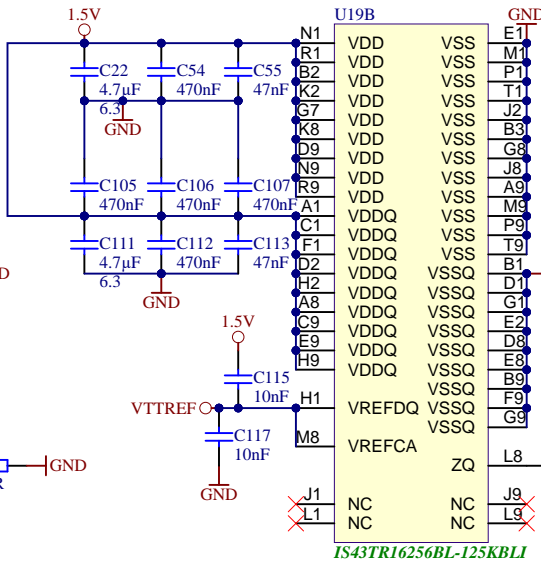
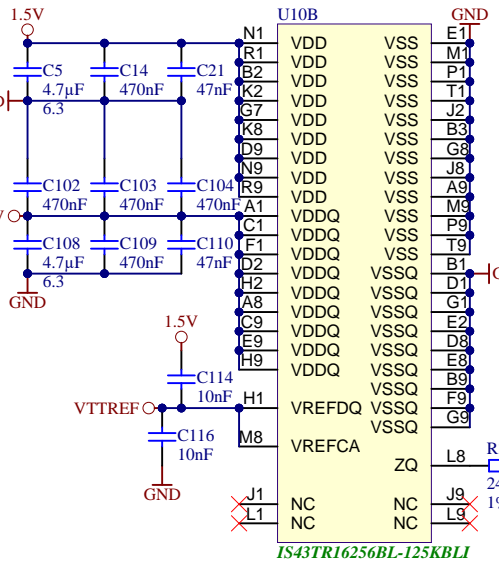
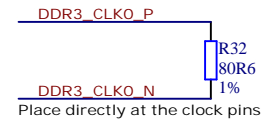
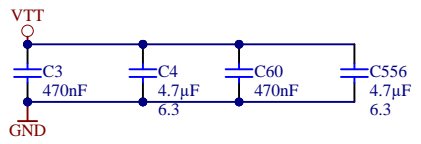
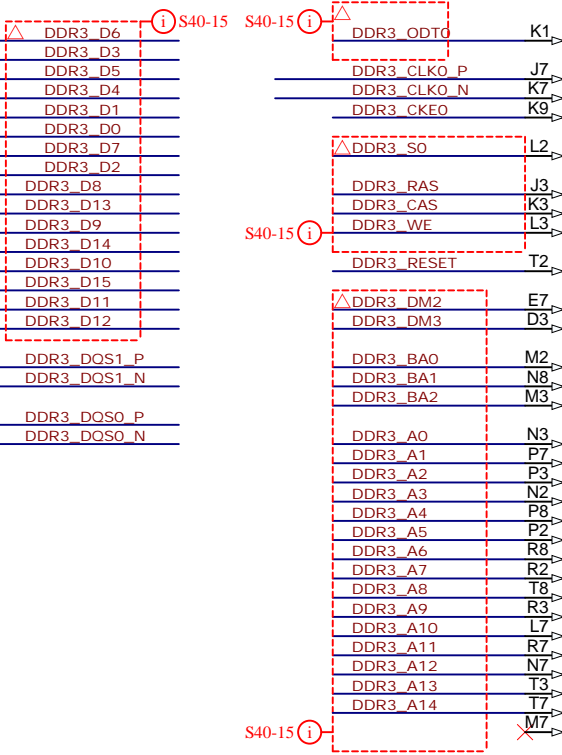
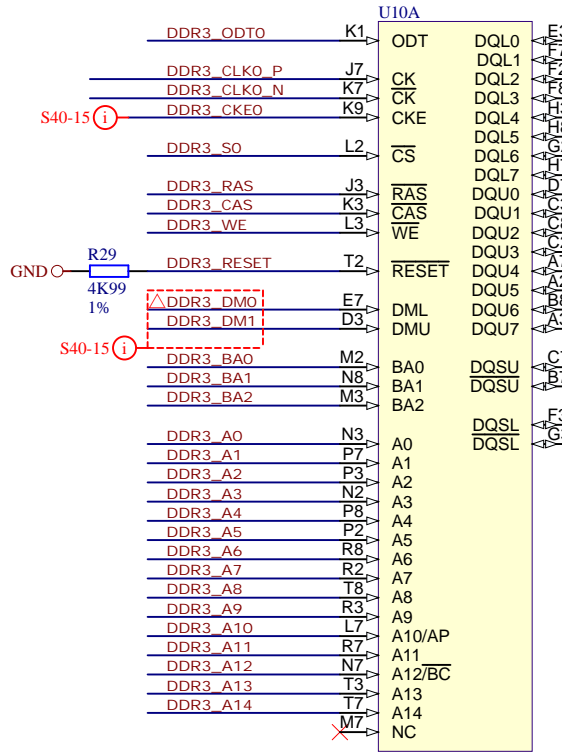
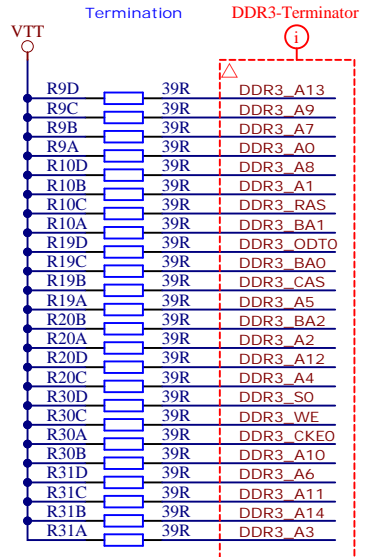
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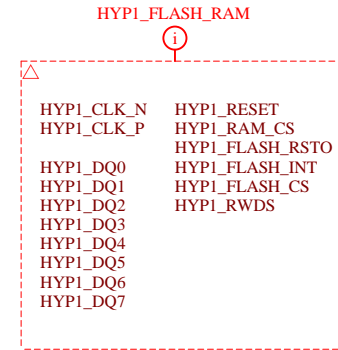
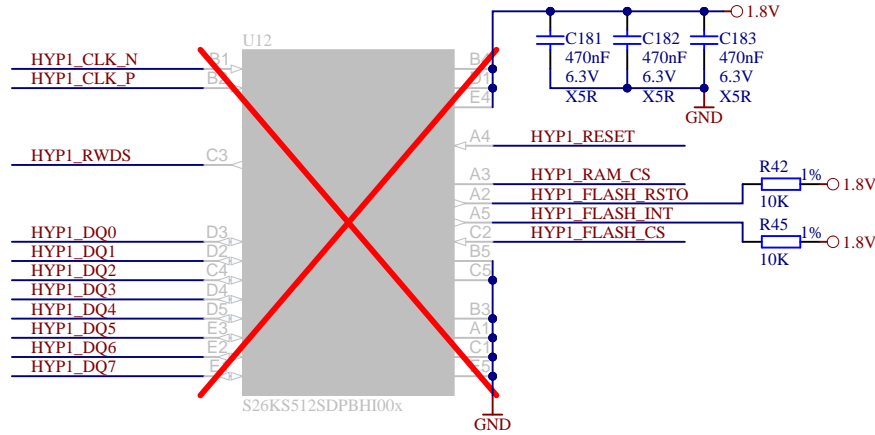
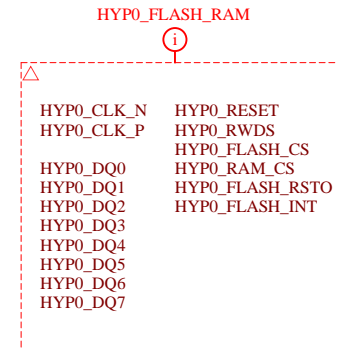
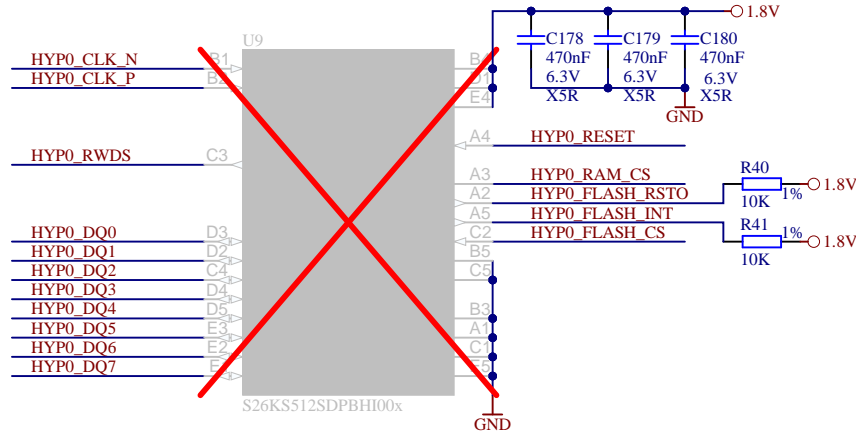
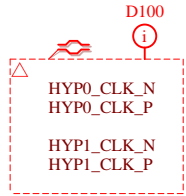

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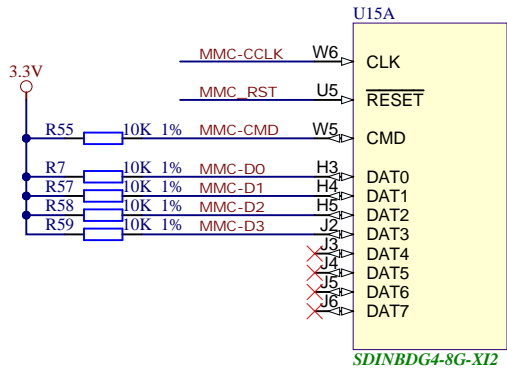


Title: TE0782 - DDR3 RAM		
A4	Number: TE0782 A2I33MA	Rev. 02
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Filename: DDR3-RAM.SchDoc		Page22 of 31

Title: TE0782 - HyperFlash_RAM		
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Filename: HyperFlash_RAM.SchDoc		

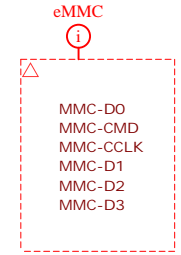
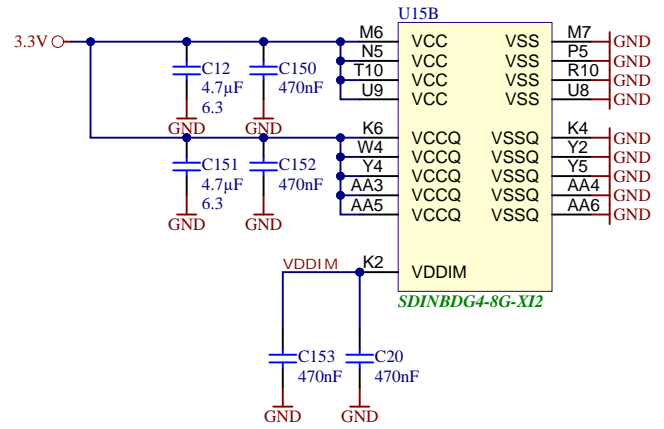
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A9	NC	NC	R12
A11	NC	NC	R13
B2	NC	NC	R14
B13	NC	NC	T1
D1	NC	NC	T2
D14	NC	NC	T3
H1	NC	NC	T12
H2	NC	NC	T13
H8	NC	NC	T14
H9	NC	NC	U1
H10	NC	NC	U2
H11	NC	NC	U3
H12	NC	NC	U12
H13	NC	NC	U13
H14	NC	NC	U14
J1	NC	NC	V1
J7	NC	NC	V2
J8	NC	NC	V3
J9	NC	NC	V12
J10	NC	NC	V13
J11	NC	NC	V14
J12	NC	NC	W1
J13	NC	NC	W2
J14	NC	NC	W3
K1	NC	NC	W7
K3	NC	NC	W8
K7	NC	NC	W9
K8	NC	NC	W10
K9	NC	NC	W11
K10	NC	NC	W12
K11	NC	NC	W13
K12	NC	NC	W14
K13	NC	NC	Y1
K14	NC	NC	Y3
L1	NC	NC	Y6
L2	NC	NC	Y7
L3	NC	NC	Y8
L4	NC	NC	Y9
L12	NC	NC	Y10
L13	NC	NC	Y11
L14	NC	NC	Y12
M1	NC	NC	Y13
M2	NC	NC	Y14
M3	NC	NC	AA1
M12	NC	NC	AA2
M13	NC	NC	AA8
M14	NC	NC	AA9
N1	NC	NC	AA11
N2	NC	NC	AA12
N3	NC	NC	AA13
N12	NC	NC	AA14
N13	NC	NC	AE1
N14	NC	NC	AE14
P1	NC	NC	AG2
P2	NC	NC	AG13
P12	NC	NC	AH4
P13	NC	NC	AH6
P14	NC	NC	AH9
R1	NC	NC	AH11
SDINBDG4-8G-XI2			



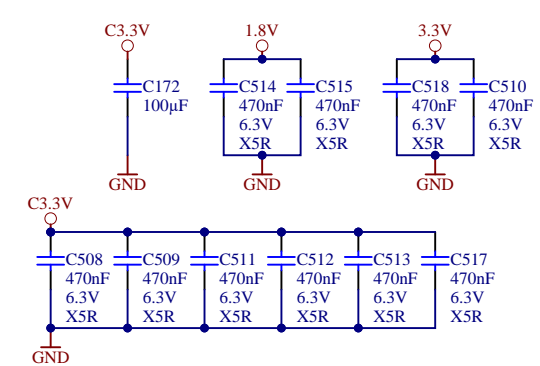
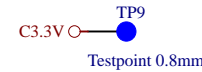
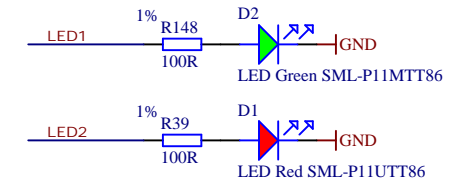
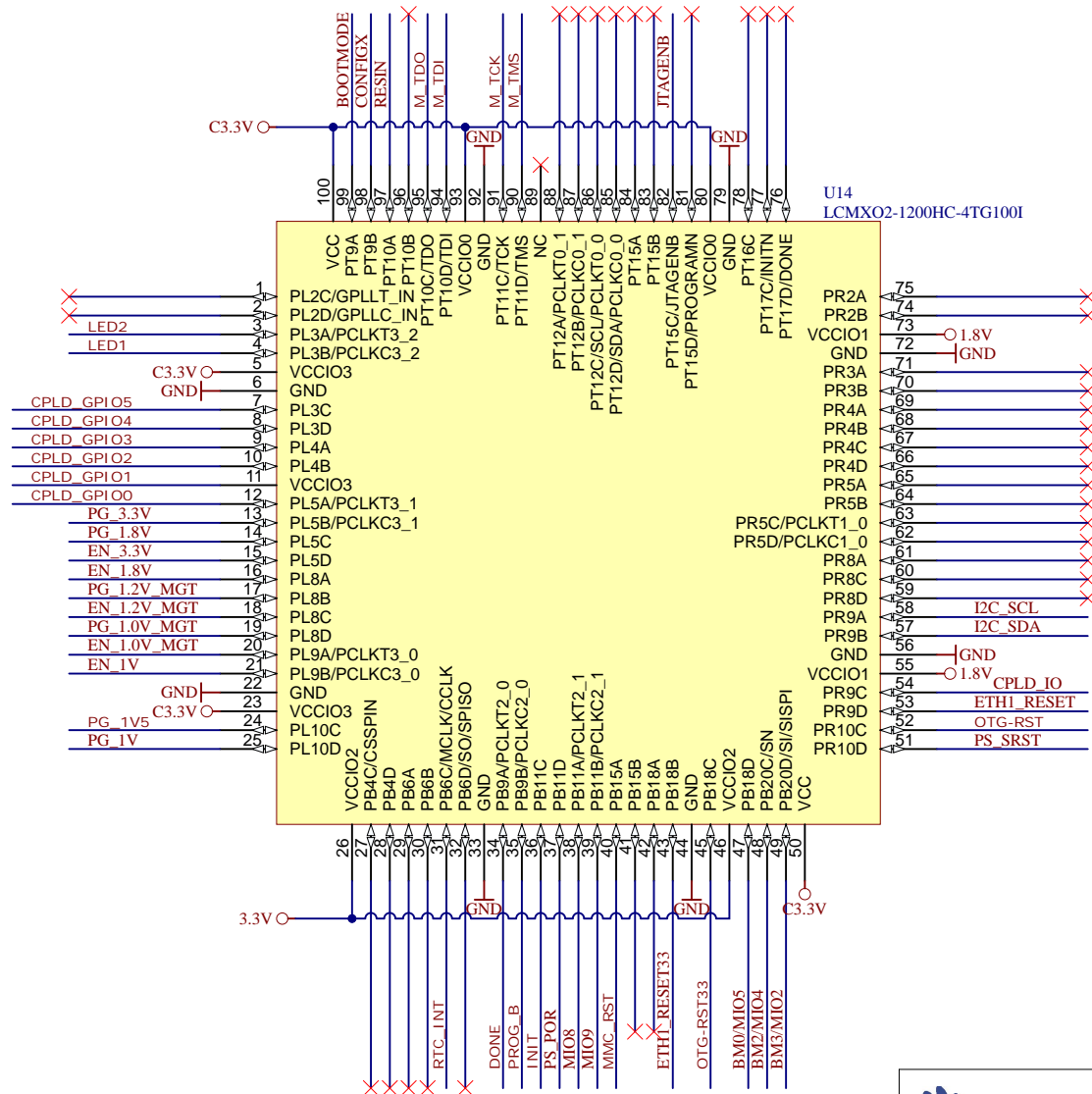
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U15C	
H6	RFU
H7	RFU
K5	RFU
M5	RFU
M8	RFU
M9	RFU
M10	RFU
N10	RFU
P3	RFU
P10	RFU
R5	RFU
T5	RFU
U6	RFU
U7	RFU
U10	RFU
AA7	RFU
AA10	RFU
SDINBDG4-8G-XI2	


MMC-D3

VDDIM



Title: TE0782 - eMMC			
A4	Number: TE0782 A2I33MA	Rev. 02	
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			Title: TE0782 - CPLD	
			A4	Number: TE0782 A2I33MA
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B

B

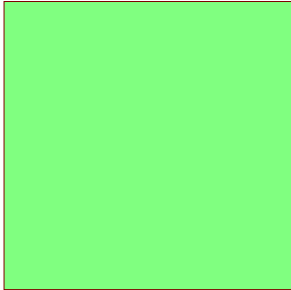
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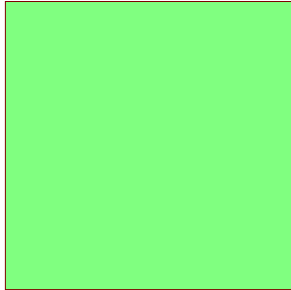
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D

U_ETH1
ETH1.SchDoc



U_ETH2
ETH2.SchDoc



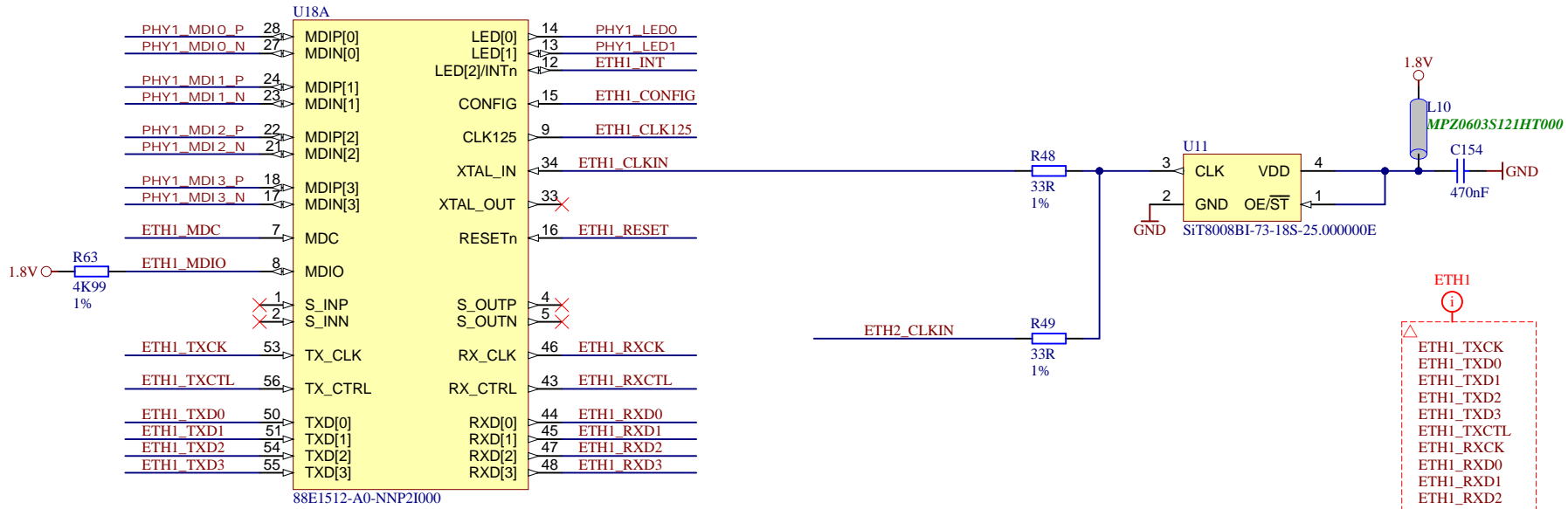
Title: TE0782 - Ethernet		
A4	Number: TE0782 A2I33MA	Rev. 02
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Filename: Ethernet.SchDoc		

1

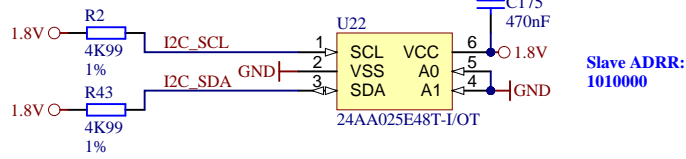
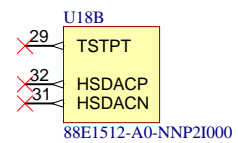
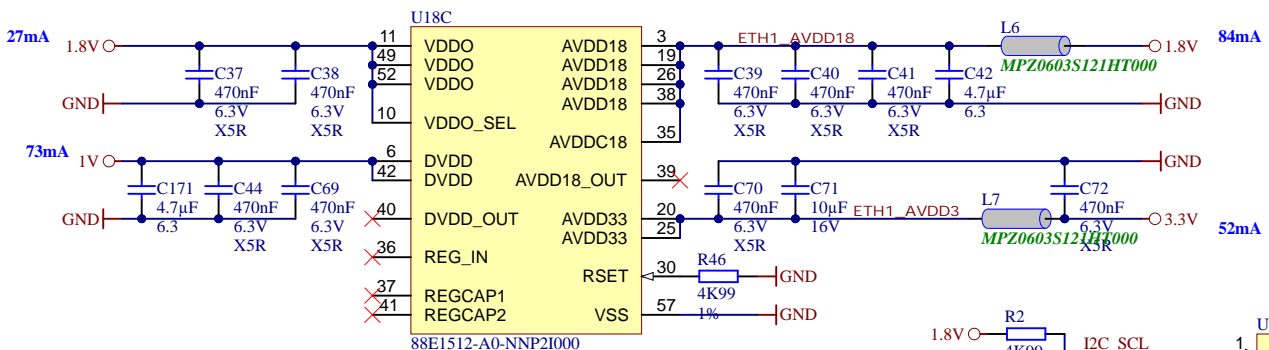
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3

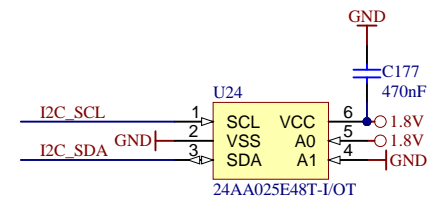
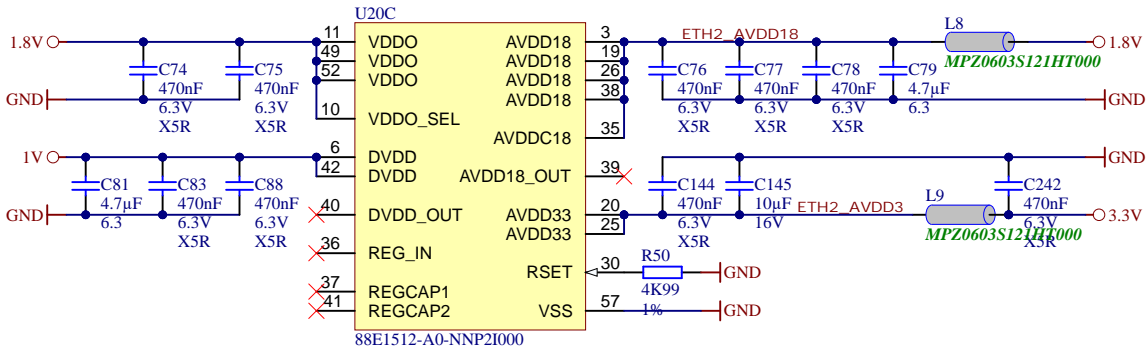
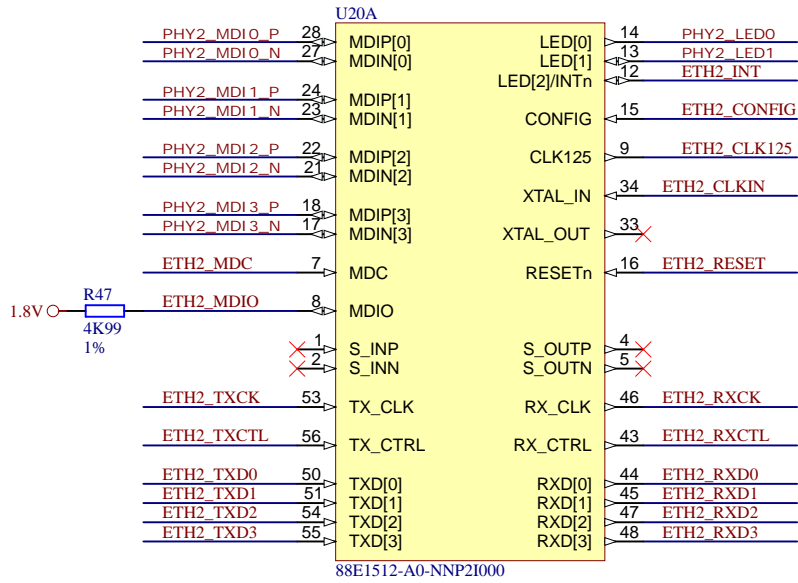
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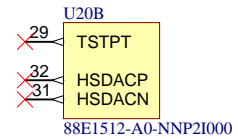
- ETH1**
- ETH1_TXCK
 - ETH1_TXD0
 - ETH1_TXD1
 - ETH1_TXD2
 - ETH1_TXD3
 - ETH1_TXCTL
 - ETH1_RXCK
 - ETH1_RXD0
 - ETH1_RXD1
 - ETH1_RXD2
 - ETH1_RXD3
 - ETH1_RXCTL
 - ETH1_MDC
 - ETH1_MDIO
- PHY1_LED0
PHY1_LED1
ETH1_INT
ETH1_CONFIG
ETH1_CLK125
ETH1_RESET



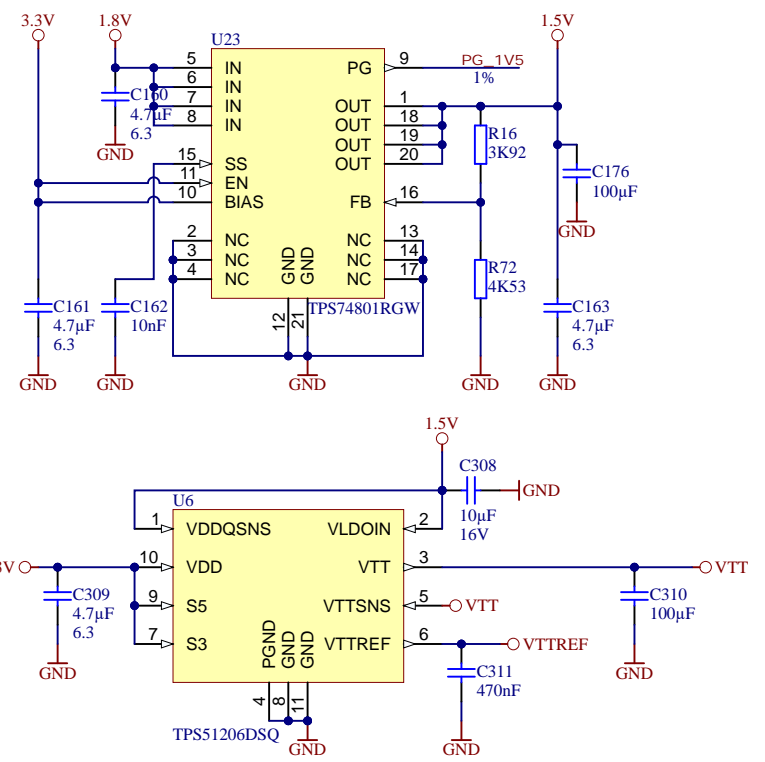
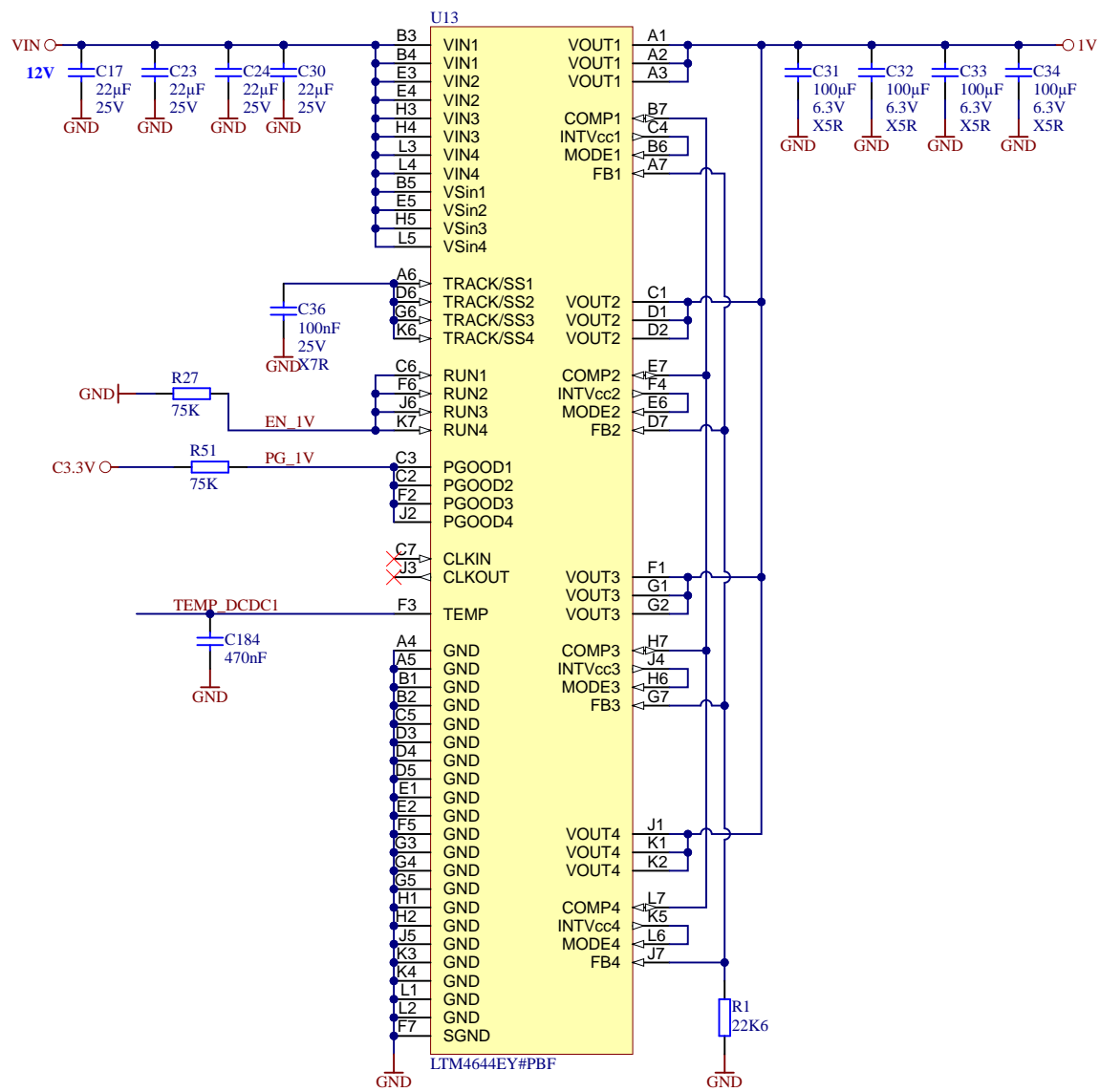
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Filename: ETH1.SchDoc				




Slave ADDR:
1010001



	Title: TE0782 - ETH_PHY2		
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	Filename: ETH2.SchDoc		



- TP7 1V Testpoint 0.8mm
- TP8 GND Testpoint 0.8mm
- TP10 1.5V Testpoint 0.8mm
- TP11 VTT Testpoint 0.8mm
- TP12 VTTREF0 Testpoint 0.8mm

			Title: TE0782 - POWER	
			A4	Number: TE0782 A2I33MA
Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page30 of 31
Filename: POWER.SchDoc				

