- **High-Speed Drive Controller for PNP Power Transistor**
- **Internal-Regulator Provides a Stable 1.5 V Reference Supply**
- **Low Start-Up Voltage 3.1 V**
- **Internal Short-Circuit Protection**
- **Internal Undervoltage Lockout Protection**
- **Internal Shut-Down Circuit by Channel**
- **Controllable Base Current of External Transistor**

description

The TL1464I incorporates on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, the TL1464I contains an on-chip 1.5 V regulator, four error amplifiers, an oscillator, two dead-time comparators, undervoltage lockout circuitry, short circuit protection, standby control circuitry, and output circuits.

The external speed-up capacitors provide exceptional rise and fall time performance for the PNP power transistor.

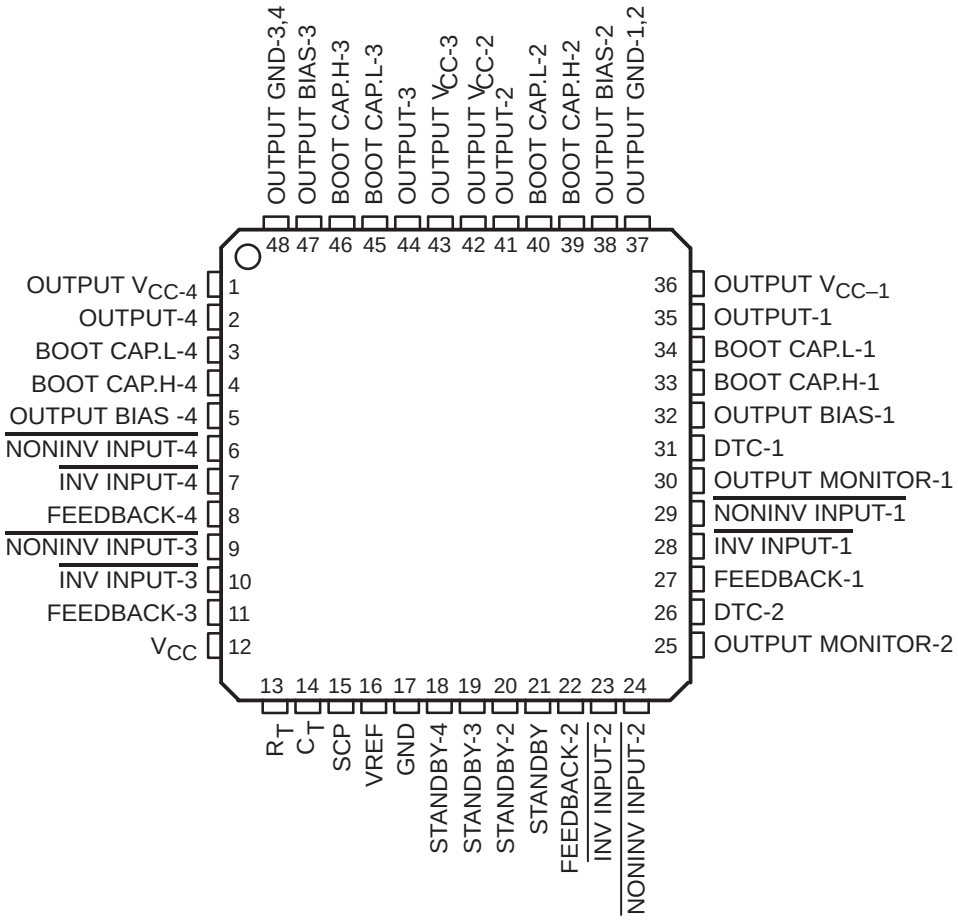
The TL1464I operates from 3.1 V supply voltage and 2 pair of four-outputs (CH-1/CH-3, CH-2/CH-4 the same period) at the inverse phase of each other. As a result, the TL1464I provides high-efficiency power supply.

FUNCTION TABLE

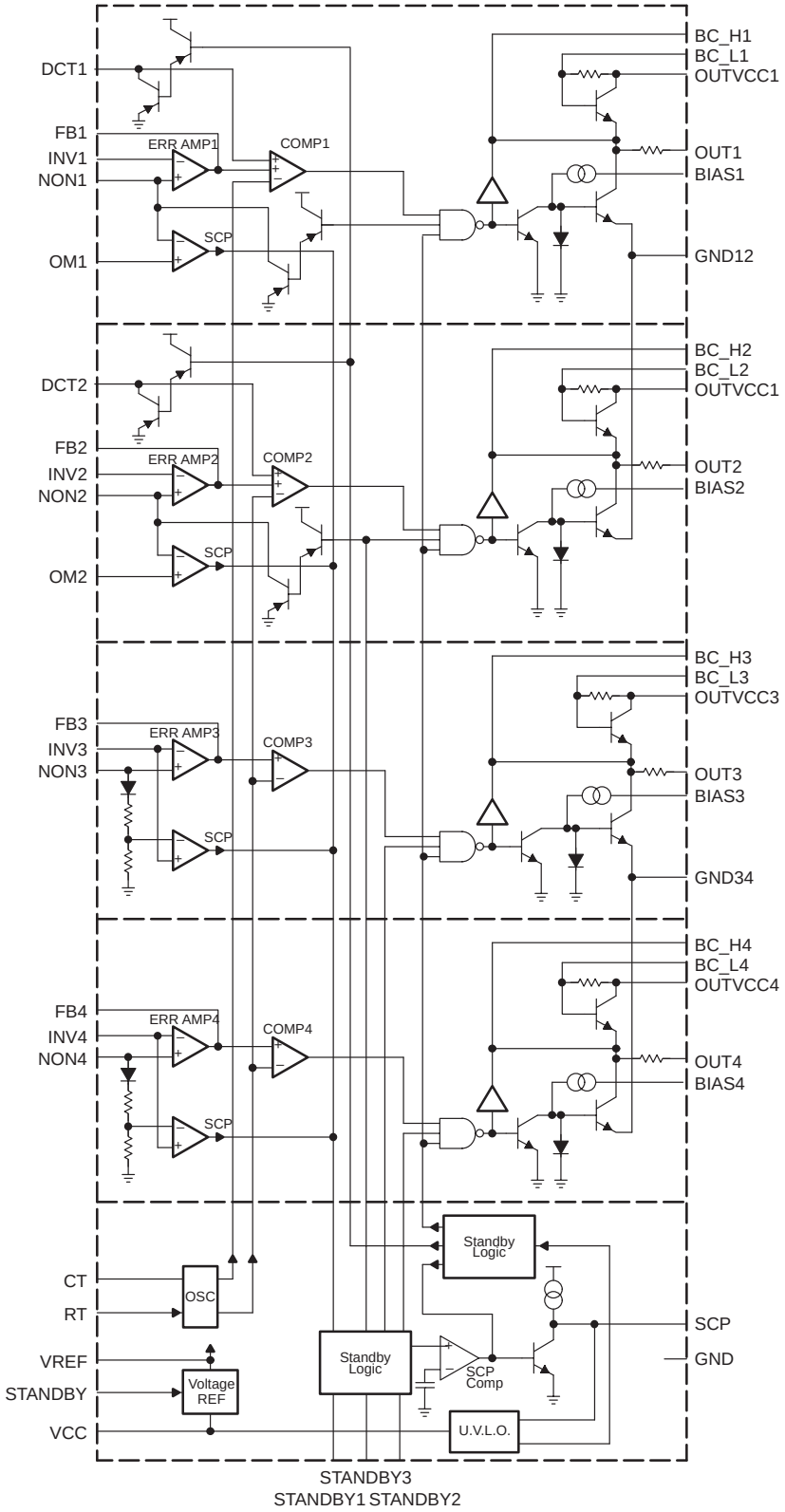
INPUTS		OUTPUT FUNCTIONS				
STANDBY	**STANDBY-2 TO4**	**VREF**	**OUTPUT-1**	**OUTPUT-2**	**OUTPUT-3**	**OUTPUT-4**
$V_I \le 0.4$ V	$V_I \le 0.4$ V, $V_I \ge 2.4$ V	L	OFF	OFF	OFF	OFF
$V_I \ge 2.4$ V	$V_I \ge 2.4$ V	H	ON	ON	ON	ON
	$V_I \ge 0.4$ V	H	ON	See Note	See Note	See Note

NOTE: When the STANDBY input is high (≥ 2.4 V), OUTPUT-2 to 4 are controlled individually. If STANDBY-2 input is low (≤ 0.4 V), OUTPUT-2 is turned off. When CH-2 standby mode is released, CH-2 can do the soft-start function.

PT PACKAGE
(TOP VIEW)



functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
BOOT CAP.H-1	33		Boot-strap capacitor connect pin (CH-1)
BOOT CAP.L-1	34		
BOOT CAP.H-2	39		Boot-strap capacitor connect pin (CH-2)
BOOT CAP.L-2	40		
BOOT CAP.H-3	46		Boot-strap capacitor connect pin (CH-3)
BOOT CAP.L-3	45		
BOOT CAP.H-4	4		Boot-strap capacitor connect pin (CH-4)
BOOT CAP.L-4	3		
C_T	14		Timing capacitor connect pin
DTC-1	31		Dead-time control input pin (CH-1)
DTC-2	26		Dead-time control input pin (CH-2)
FEEDBACK-1	27		Error amplifier output pin (CH-1)
FEEDBACK-2	22		Error amplifier output pin (CH-2)
FEEDBACK-3	11		Error amplifier output pin (CH-3)
FEEDBACK-4	8		Error amplifier output pin (CH-4)
GND	17		Ground pin
$\overline{\text{INV INPUT-1}}$	28		Error amplifier inverting input pin (CH-1)
$\overline{\text{INV INPUT-2}}$	23		Error amplifier inverting input pin (CH-2)
$\overline{\text{INV INPUT-3}}$	10		Error amplifier inverting input pin (CH-3)
$\overline{\text{INV INPUT-4}}$	7		Error amplifier inverting input pin (CH-4)
$\overline{\text{NONINV INPUT-1}}$	29		Error amplifier noninverting input pin (CH-1)
$\overline{\text{NONINV INPUT-2}}$	24		Error amplifier noninverting input pin (CH-2)
$\overline{\text{NONINV INPUT-3}}$	9		Error amplifier noninverting input pin (CH-3)
$\overline{\text{NONINV INPUT-4}}$	6		Error amplifier noninverting input pin (CH-4)
OUTPUT-1	35		Output pin (CH-1)
OUTPUT-2	41		Output pin (CH-2)
OUTPUT-3	44		Output pin (CH-3)
OUTPUT-4	2		Output pin (CH-4)
OUTPUT BIAS-1	32		Output ON current setup pin (CH-1)
OUTPUT BIAS-2	38		Output ON current setup pin (CH-2)
OUTPUT BIAS-3	47		Output ON current setup pin (CH-3)
OUTPUT BIAS-4	5		Output ON current setup pin (CH-4)
OUTPUT GND-1,2	37		Output ground pin (CH-1,2)
OUTPUT GND-3,4	48		Output ground pin (CH-3,4)
OUTPUT MONITOR-1	30		Output monitor comparator input pin (CH-1)
OUTPUT MONITOR-2	25		Output monitor comparator input pin (CH-2)
OUTPUT V_{CC-1}	36		Output supply pin (CH-1)
OUTPUT V_{CC-2}	42		Output supply pin (CH-2)
OUTPUT V_{CC-3}	43		Output supply pin (CH-3)
OUTPUT V_{CC-4}	1		Output supply pin (CH-4)
R_T	13		Timing resistor connect pin
SCP	15		Short-circuit protection capacitor connect pin

Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
STANDBY	21		Output-1 to 4 control pin. Input L level voltage (0.4 V max). All outputs function and VREF are shutdown.
STANDBY-2	20		Output-2 control pin. Input L level voltage (0.4 V max), output-2 function is shutdown.
STANDBY-3	19		Output-3 control pin. Input L level voltage (0.4 V max), output-3 function is shutdown.
STANDBY-4	18		Output-4 control pin. Input L level voltage (0.4 V max), output-4 function is shutdown.
V_{CC}	12		Power supply pin

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . 13 V
Amplifier input voltage, V_{IC} . . . . . 13 V
Output voltage, V_O . . . . . 13 V
Peak output current (sink), $I_{(SINK)}$ . . . . . 100 mA
Peak output current (source), I_{SOURCE} . . . . . 1 A
Continuous total dissipation at (or below) 25°C free-air temperature (unit), P_D . . . . . 695 mW
Continuous total dissipation at (or below) 25°C free-air temperature (using board), P_D
(see Note 2) . . . . . 1315 mW
Operating free-air temperature range, T_A . . . . . –20°C to 75°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage4 value are with respect to network ground terminal.
2. Using t1.6 × 50 × 50 mm glass epoxy resin.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3.1		12	V
Amplifier input voltage, V_{IC}	CH-1,2	–0.1		V_{CC}–1.8	V
	CH-3,4	0		V_{CC}–1.8	
Standby input voltage, V_I (pins 18, 19. 20. 21)	H level	2.4		V_{CC}	V
	L level			0.4	
Output voltage, V_O				12	V
Current into feedback terminal, $I_{(CAMP)}$				–45	µA
Feedback resistor, $R_{(NF)}$		100			kΩ
Boot-strap capacitor, $C_{(BOOT)}$		100	500		pF
Bias resistor, $R_{(BIAS)}$		1.2		20	
Bias capacitor, $C_{(BIAS)}$			30	200	pF
Timing resistor, $R_{(T)}$		7		50	kΩ
Timing capacitor, $C_{(T)}$		68		1000	pF
Oscillation frequency, $f_{(OSC)}$		0.05		2	MHz
Operating free-air temperature, T_A		–20		75	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 1 MHz (unless otherwise noted)

reference section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ref}	Output voltage (pin 16)	T_A = 25°C, $I_{(OR)}$ = –1 mA	1.485	1.50	1.515	V
$R_{(EGIN)}$	Input regulation	V_{OS} = 3.1 V to 12 V, $I_{(OR)}$ = –1 mA		2	12.5	mV
$R_{(EFL)}$	Output regulation	$I_{(OR)}$ = –0.1 mA to –1 mA		1	7.5	mV
$V_{(RTC1)}$	Output voltage change with temperature	T_A = 20°C to 25°C		–0.2%	±2%	
$R_{(RTC2)}$		T_A = 25°C to 75°C		–0.2%	±2%	
I_{OS}	Short-circuit output current	V_{ref} = 0 V	4	8		mA

undervoltage lockout section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Upper threshold voltage	T_A = 25°C		2.7		V
V_{IL}	Lower threshold voltage			2.5		V
V_{hys}	Hysteresis		0.1	0.2		V
V_R	Reset threshold voltage (V_{CC})		2.2	2.3		V

output voltage monitor section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IO(M)}$	Input offset voltage	T_A = 25°C (CH-1,2)		0		V
		V_I = 1.5 V (pins 6 and 9), T_A = 25°C (CH-3,4)		10.5		
$I_{(BOM)}$	Input bias current	V_I = 0 V		–200	–500	nA
$V_{(IOM)}$	Input voltage range	V_{CC} = 3.1 V ~ 12 V	0 to V_{CC}–1.8			V

protection control section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(tPC)}$	Input threshold voltage (pin 15)	T_A = 25°C	1.45	1.50	1.55	V
$V_{(stby)}$	Standby voltage (pin 15)		40	70	100	mV
V_I	Latched input voltage (pin 15)			10	30	mV
$I_{(bPC)}$	Input source current (pin 15)	T_A = 25°C	–1	–3	–6	µA

oscillator section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Frequency	C_t = 100 pF, R_t = 10 kΩ		1		MHz
$f_{(dev)}$	Standard deviation of frequency	All values are constant		7%		
$f_{(dV)}$	Frequency change with voltage	V_{CC} = 3 V ~ 12 V		1%		
$f_{(dT1)}$	Frequency change with temperature	T_A = 20°C to 25°C		–0.5%	±4%	
$f_{(dT2)}$		T_A = 25°C to 75°C		0.5%	±4%	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 1 MHz (unless otherwise noted) (continued)

dead-time control section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(Idt)}$	Input current			–1	–4	μA
$I_{(dt)}$	Latched mode sink current	T_A = 25°C	0.3	1	2	mA
$V_{(dt)}$	Latched input voltage	$I_{(dt)}$ = 100 μA			0.5	V
V_{IO}	Input threshold voltage	Zero duty cycle	0.6	0.7	0.8	V
$V_{(tt00)}$		100% duty cycle	1.3	1.4	1.5	

error-amplifier section

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		V_O = 1 V			±10	mV
I_{IO}	Input offset current		V_O = 1 V			±100	nA
I_{IB}	Input bias current		V_O = 1 V		–200	–500	nA
V_{ICR}	Common-mode input voltage	CH-1,2	V_{CC} = 3.1 V ~ 12 V	–0.1 to V_{CC}–1.8			V
		CH-3,4		0 to V_{CC}–1.8			
$A_{(v)}$	Open-loop voltage amplification		R_l = 200 kΩ	60	75		dB
B1	Unity-gain bandwidth				6		MHz
CMRR	Common-mode rejection ratio		V_{IC} = –0.1 V ~ V_{CC} – 1.8 V	60	80		dB
V_{OM+}	Maximum output voltage swing			V_{ref}–0.1			V
$V_{OM–}$						0.2	
$I_{O(vr+)}$	Output current (sink)		V_{ID} = –0.1 V, V_O = 1.25 V	0.5	1		mA
I_{I+}	Sink current (pin 24) (standby mode)		V_I = 0.3 V (pin 24) V_I = 0 V (pin 20)	0.1	0.5		mA
$I_{OM–}$	Output current (source)		V_{ID} = 0.1 V, V_O = 0.75 V	–45	–85		μA

output section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SINK)}$	Output current (sink)	$R_{(BIAS)}$ = 2.4 kΩ	15	20	25	mA
		$R_{(BIAS)}$ = 5.8 kΩ	7.5	10	12.5	

total device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{O(CS)}$	Standby supply current	Standby pin input voltage = 0 V		1	200	μA
$I_{O(CA)}$	Average supply current	R_t = 10 kΩ		4	7	mA

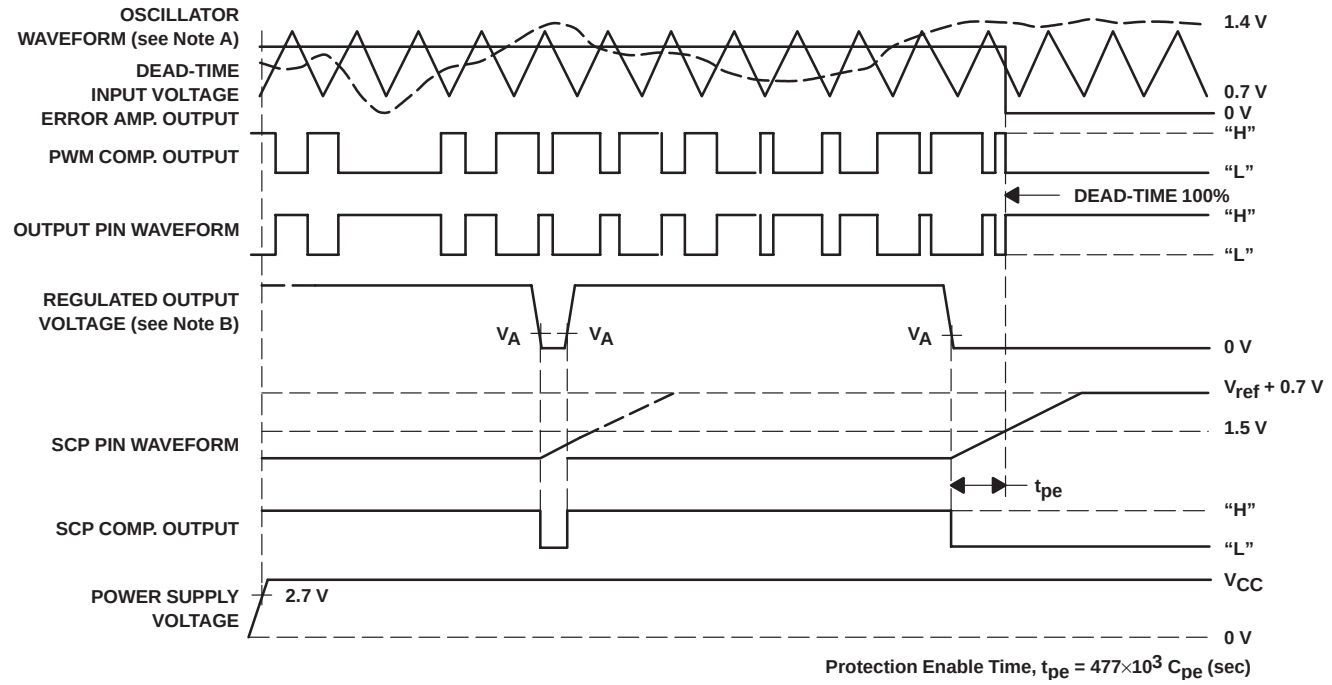


Figure 1. Timing Diagram (CH-1/CH-2)

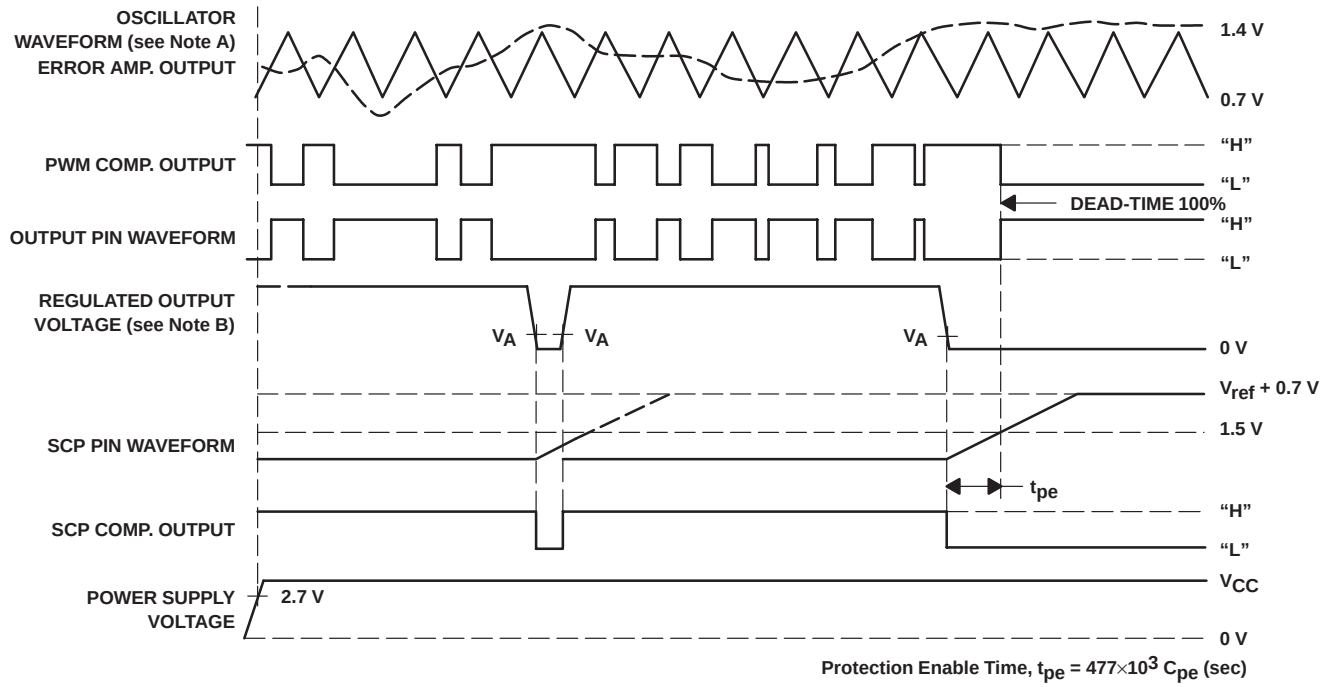
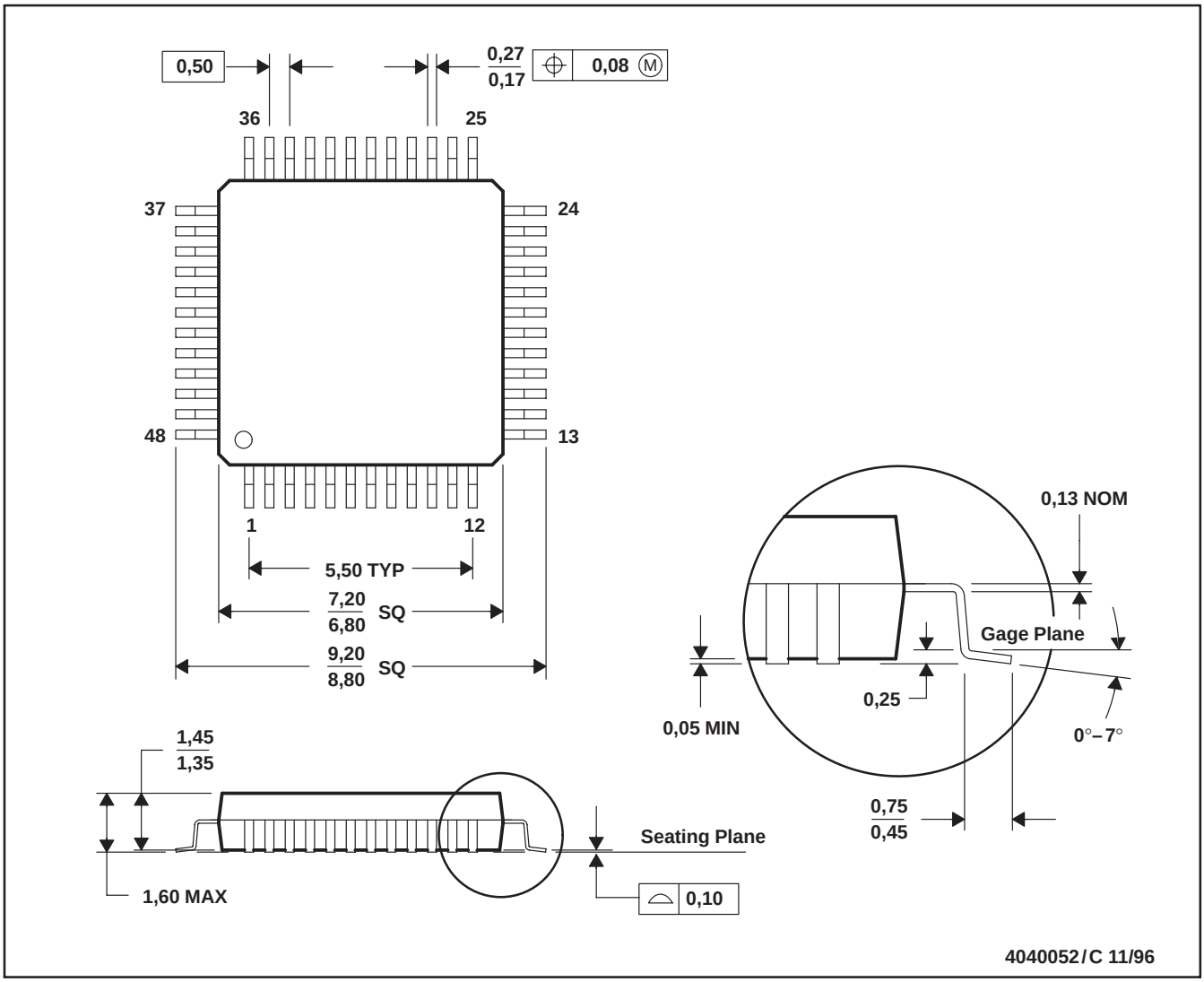


Figure 2. Timing Diagram (CH-3/CH-4)

NOTES: A. Oscillator waveform of CH-1 and CH-2 is inverting output each other.
B. Va = input voltage of pin 29 (pin 24)

MECHANICAL DATA

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL1464IPT	ACTIVE	LQFP	PT	48	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 75	Z1464	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

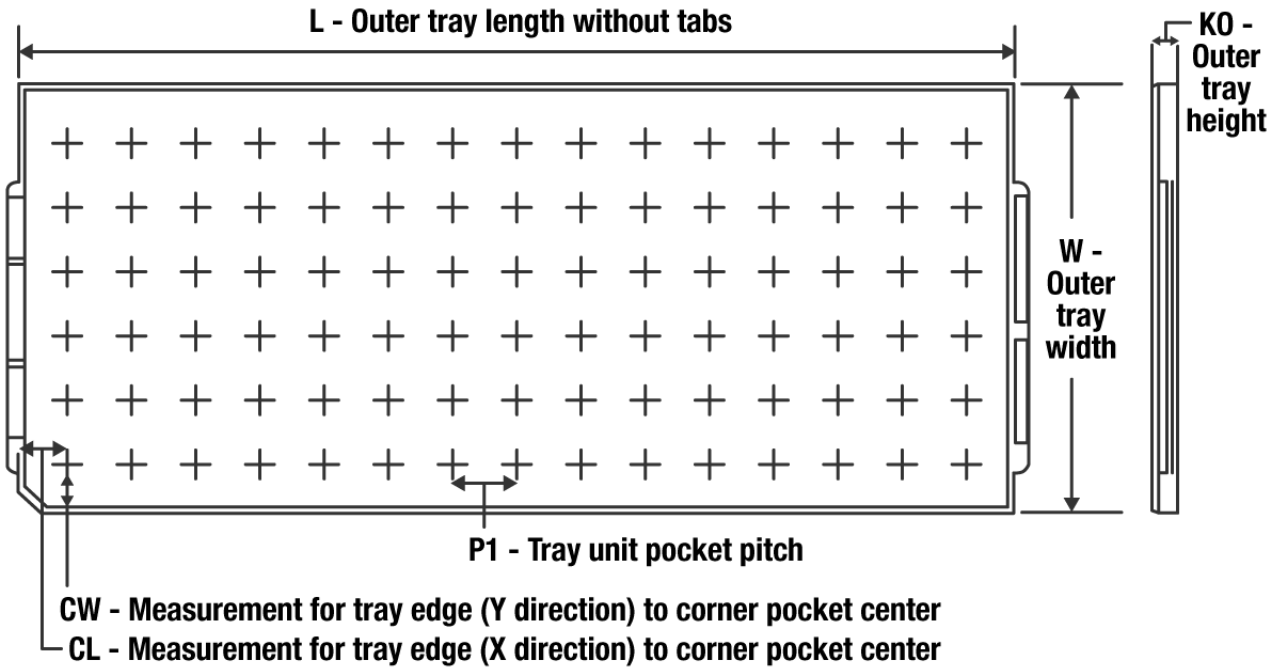
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TL1464IPT	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

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