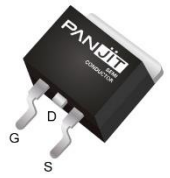
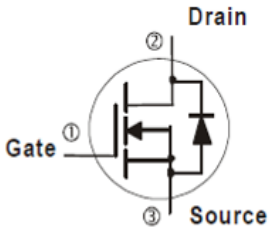
80V N-Channel Enhancement Mode MOSFET

Voltage	**80 V**	**R_{DSON}**	**3.4 mΩ**
Current	**161 A**	**$Q_{G\ (TYP)}$**	**103.5 nC**

TO-263





Feature:

- $R_{DS(ON)\ Max}$, V_{GS}@10V, I_D@50A<3.4mΩ
- $R_{DS(ON)\ Max}$, V_{GS}@7V, I_D@25A<5mΩ
- 100% Avalanche Tested
- 100% Rg Tested
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case: TO-263 package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 1.38 grams

Application

- BMS, BLDC. SMPS SR.

Absolute Maximum Ratings (T_A = 25 °C unless otherwise specified)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C=25°C (Note 3)	I_D	161	A
	T_C=100°C		102	
Pulsed Drain Current	T_C=25°C	I_{DM}	480	A
Single Pulse Avalanche Current (Note 5)		I_{AS}	38	A
Single Pulse Avalanche Energy (Note 5)		E_{AS}	722	mJ
Power Dissipation	T_C=25°C	P_D	156	W
	T_C=100°C		62.5	
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~150	°C

Thermal Characteristics

PARAMETER		SYMBOL	MAXIMUM	UNITS
Thermal Resistance	Junction-to-Case	$R_{\theta JC}$	0.8	°C/W
	Junction-to-Ambient (Note 4)	$R_{\theta JA}$	62.5	°C/W

Electrical Characteristics (T_A = 25 °C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS} (Note 7)	V_{GS}=0V, I_D=250uA	80	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	2.25	3.2	3.75	
Drain-Source On-State Resistance (Note 1)	$R_{DS(on)}$	V_{GS}=10V, I_D=50A	-	3	3.4	mΩ
		V_{GS}=7V, I_D=25A	-	3.5	5	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V, V_{GS}=0V	-	-	1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Dynamic (Note 6)						
Total Gate Charge	Q_g	V_{DS}=40V, I_D=50A, V_{GS}=7V	-	76	-	nC
		V_{DS}=40V, I_D=50A, V_{GS}=10V	-	103.5	-	
Gate-Source Charge	Q_{gs}		-	34.1	-	
Gate-Drain Charge	Q_{gd}		-	20.9	-	
Input Capacitance	Ciss	V_{DS}=40V, V_{GS}=0V, F=1MHz	-	7430	-	pF
Output Capacitance	Coss		-	1483	-	
Reverse Transfer Capacitance	Crss		-	89	-	
Turn-On Delay Time	$td_{(on)}$	V_{DD}=40V, I_D=50A, V_{GS}=10V, R_G=2Ω (Note 2)	-	70.6	-	ns
Turn-On Rise Time	t_r		-	103	-	
Turn-Off Delay Time	$td_{(off)}$		-	122	-	
Turn-Off Fall Time	t_f		-	48.5	-	
Gate Resistance	Rg	f=1.0MHz	-	3.2	-	Ω
Drain-Source Diode						
Diode Forward Voltage	V_{SD}	I_S=50A, V_{GS}=0V	-	0.88	1.2	V
Reverse Recovery Charge	Q_{rr}	I_S=50A di/dt=100A/μs	-	114	-	nC
Reverse Recovery Time	T_{rr}		-	69	-	ns

NOTES :

1. Pulse width<580us,
2. Essentially independent of operating temperature typical characteristics.
3. The maximum current rating is silicon limited.
4. RθJA is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 $inch^2$ with 2oz.square pad of copper.
5. The test condition is L=1mH, I_{AS}=38A, V_{DD}=40V, V_{GS}=10V, R_G=25ohm, Starting T_J=25℃
6. Guaranteed by design, not subject to production testing.
7. BVDSS is over 85V during mass production.

TYPICAL CHARACTERISTIC CURVES

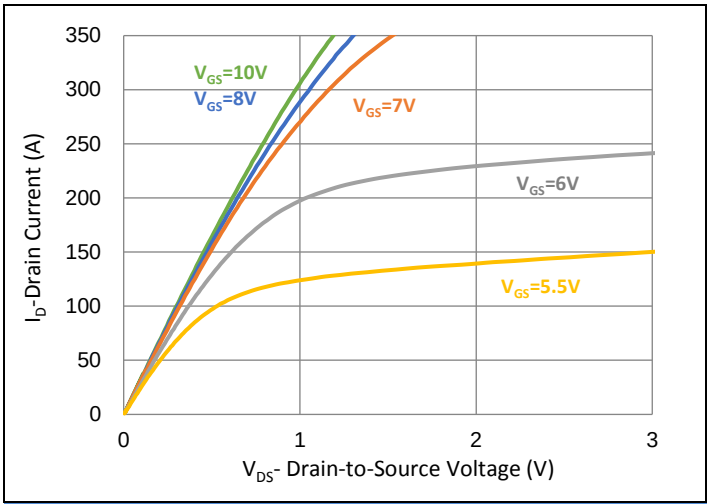


Fig.1 Output Characteristics

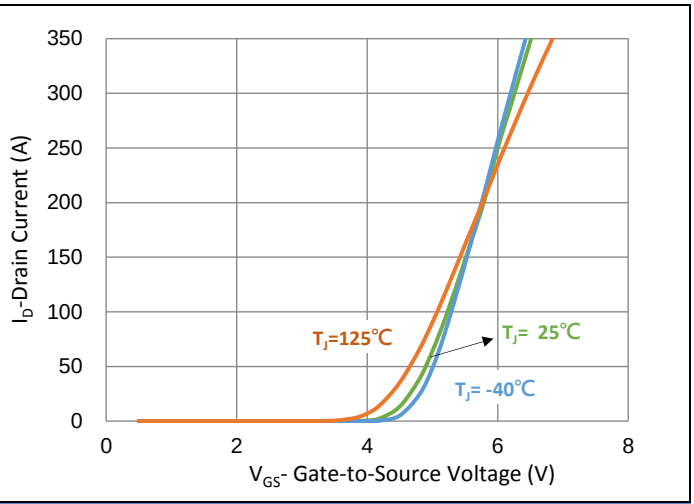


Fig.2 Transfer Characteristics

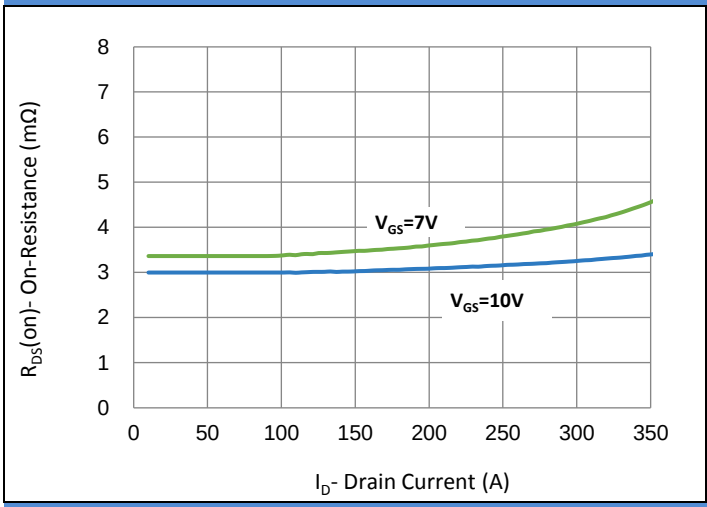


Fig.3 On-Resistance vs. Drain Current

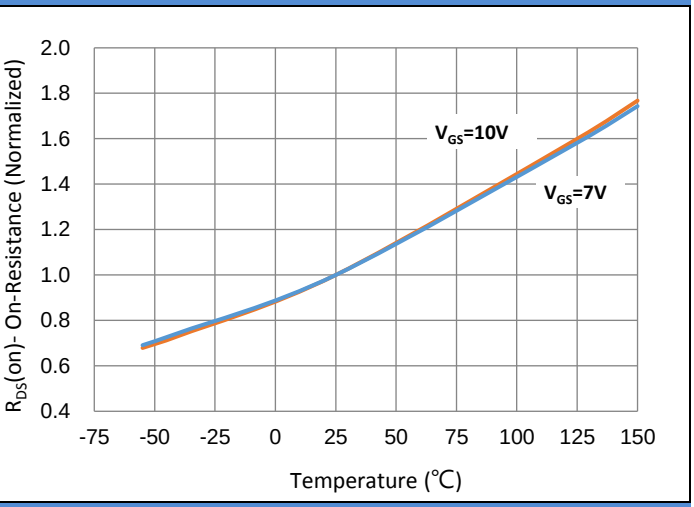


Fig.4 On-Resistance vs. Junction Temperature

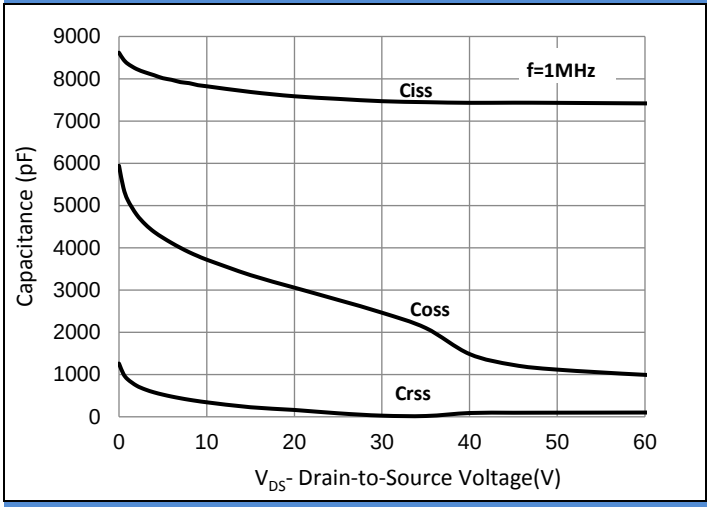


Fig.5 Capacitance vs. Drain-Source Voltage

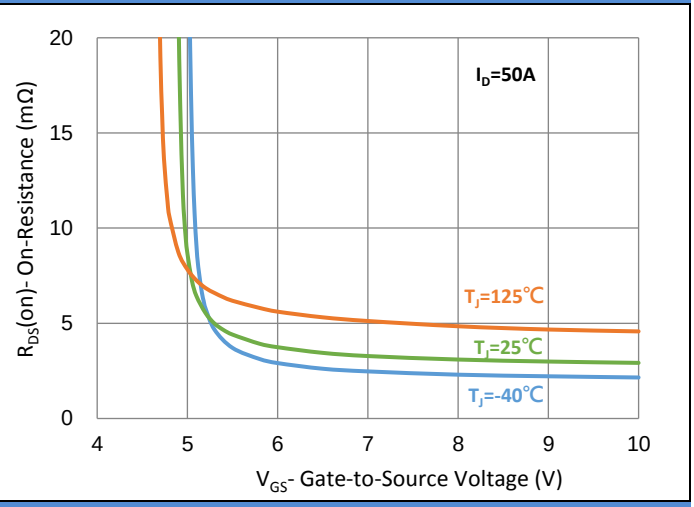


Fig.6 On-Resistance vs. Gate-Source Voltage

TYPICAL CHARACTERISTIC CURVES

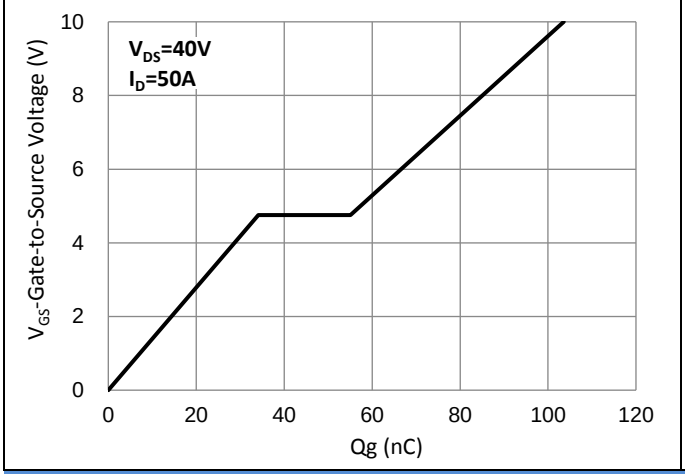


Fig.7 Gate-Charge Characteristics

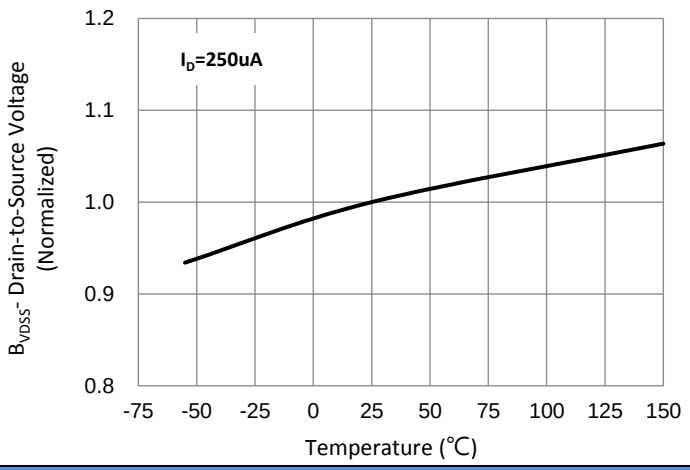


Fig.8 Breakdown Voltage Variation vs. Temperature

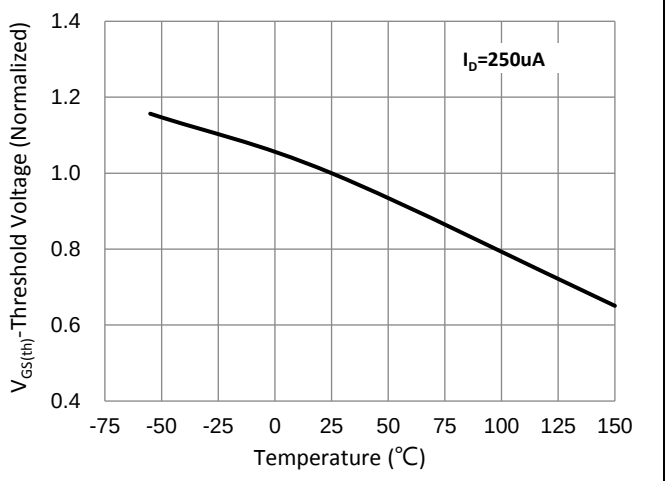


Fig.9 Threshold Voltage Variation with Temperature

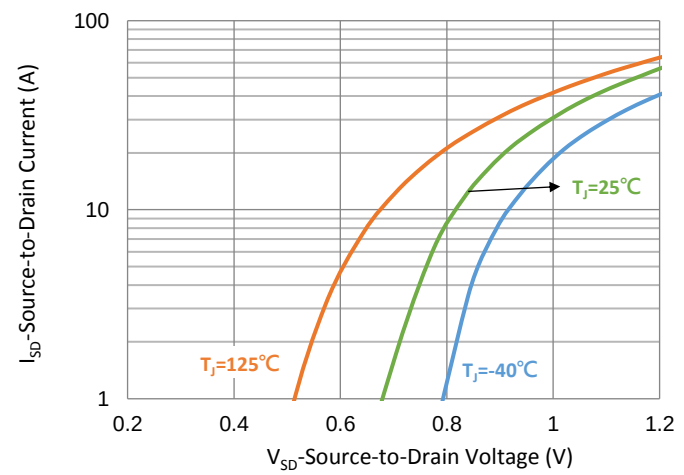


Fig.10 Source-Drain Diode Forward Voltage

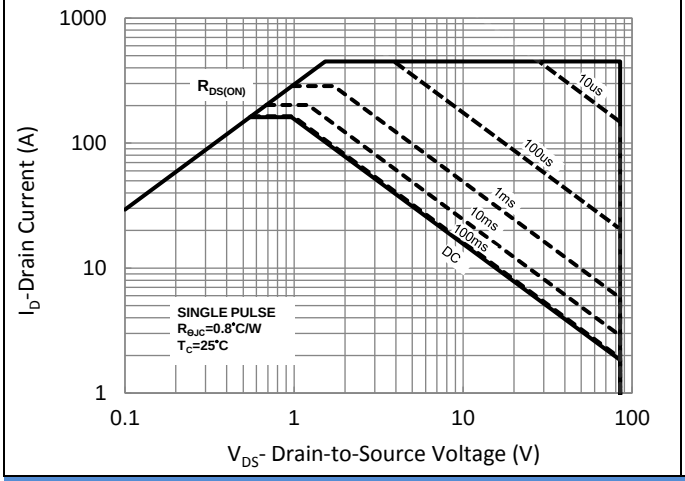


Fig.11 Maximum Safe Operating Area

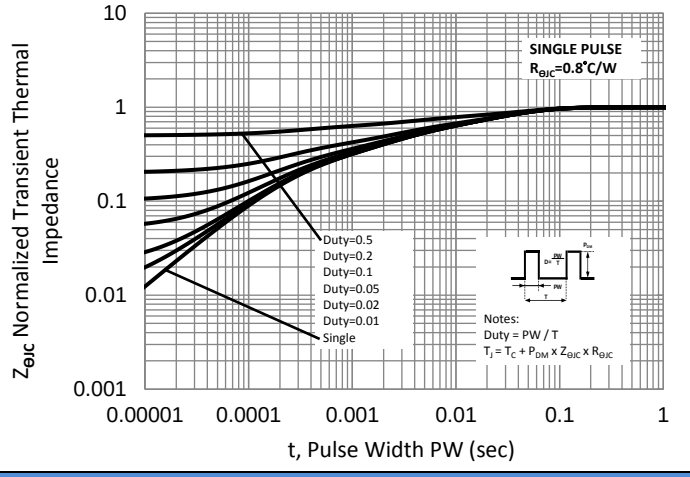


Fig.12 Normalized Transient Thermal Impedance

TYPICAL CHARACTERISTIC CURVES

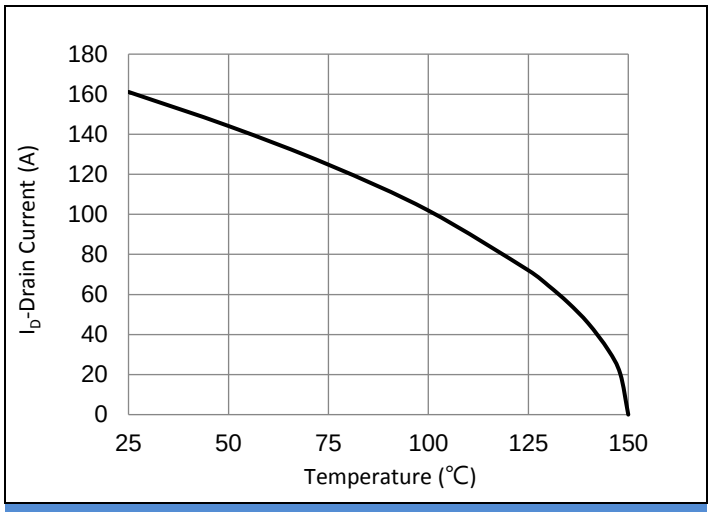


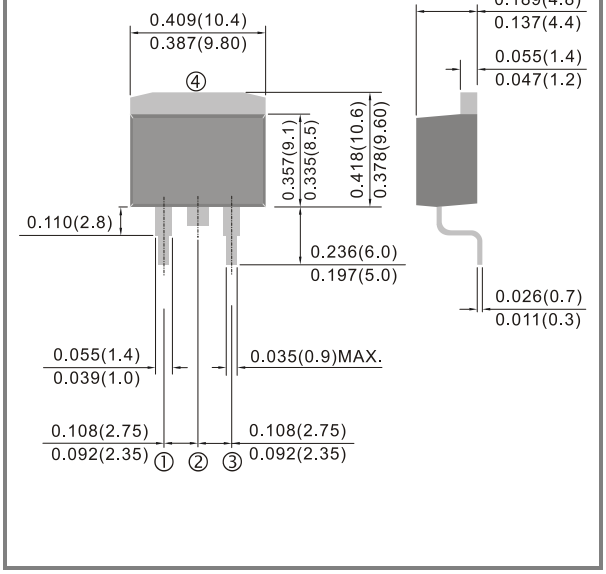
Fig.13 Drain Current vs. Case Temperature

Product and Packing Information

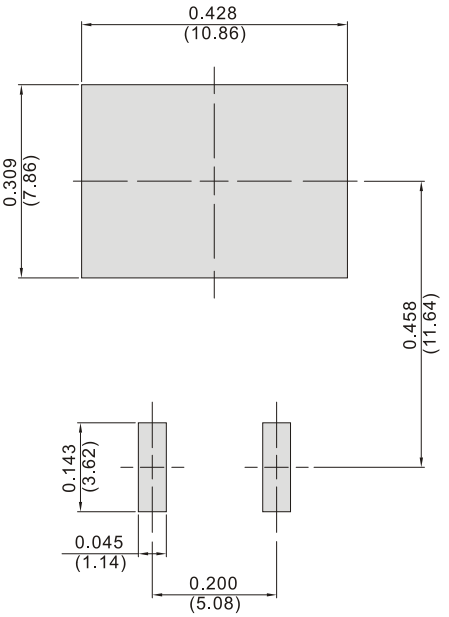
Part No.	Package Type	Packing Type	Marking
PSMB032N08NS1	TO-263	50pcs / Tube 800pcs / Reel	032N08NS

Packaging Information & Mounting Pad Layout

TO-263 Dimension — Unit: inch(mm)



TO-263 Pad Layout — Unit: inch(mm)



Marking Diagram

PJ 032N08NS YWLL x

Y = Year Code
W = Week Code (A~Z)
LL = Lot Code (00~99)
x = Production Line Code

Disclaimer

- Reproducing and modifying information of the document is prohibited without permission from Panjit International Inc..
- Panjit International Inc. reserves the rights to make changes of the content herein the document anytime without notification. Please refer to our website for the latest document.
- Panjit International Inc. disclaims any and all liability arising out of the application or use of any product including damages incidentally and consequentially occurred.
- Panjit International Inc. does not assume any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.
- Applications shown on the herein document are examples of standard use and operation. Customers are responsible in comprehending the suitable use in particular applications. Panjit International Inc. makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.
- The products shown herein are not designed and authorized for equipments requiring high level of reliability or relating to human life and for any applications concerning life-saving or life-sustaining, such as medical instruments, transportation equipment, aerospace machinery et cetera. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Panjit International Inc. for any damages resulting from such improper use or sale.
- Since Panjit uses lot number as the tracking base, please provide the lot number for tracking when complaining.