Quasi-Resonant type AC/DC converter IC

BD768xFJ-LB series Quasi-Resonant converter Technical Design **24V / 1A (SIC TO-3PFM SCT2H12NZ)**

This application note describes the design of Quasi-Resonant converters using ROHM's AC/DC converter IC BD768xFJ-LB series devices. It explains the selection of external components and PCB layout guidelines.

● Description

The BD768xFJ-LB series are Quasi-Resonant switching AC/DC converter for driving SiC (Silicon Carbide)–MOSFET. Using external switching MOSFET and current detection resistors provides a lot of flexibility in the design. Power efficiency is improved by the burst function and the reduction of switching frequency under light load conditions. This is the product that guarantees long time support in the Industrial market.

● Key features

Quasi-resonant method(Maximum frequency control 120kHz)/Current mode Low power when load is light (Burst operation) / Frequency reduction function VCC pin : under voltage protection / over voltage protection Leading-Edge-Blanking function Over-current protection (cycle-by-cycle) ZT trigger mask function ZT Over voltage protection AC voltage correction function Soft start Brown IN/OUT function Gate Clamp circuit MASK Function

● Basic specifications

(*) Product structure:Silicon monolithic integrated circuit This product has no designed protection against radioactive rays (*) Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

● BD768xFJ-LB Series line-up

● Applications

Industrial equipment, AC Adaptor, Household appliances

● Block Diagram

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1.**Design of Isolated Fly-buck Quasi-Resonant convertor**

Quasi-resonant converter is self-excited fly-back converter power supply system using the voltage resonance of the transformer primary winding inductor and resonant capacitor.

Generally, Quasi-resonant converter is possible to reduce the loss and noise than the PWM fly-back converter.

Quasi-Resonant Converter becomes DCM (Discontinuous Conduction Mode) under light load, and switching frequency increases with the load increasing. When the load increased further, Quasi-Resonant Converter becomes BCM (Boundary Conduction Mode), and switching frequency decreases with the load increasing.

The relation of switching Frequency and output load characteristics is shown in Figure 1-2. The Switching waveform at DCM and CCM is shown in Figure 1-2.

Figure 1-1.Switching Frequency – Output Load Characteristics

Figure 1-2.Switching waveform (MOSFET Vds,Ids)

1-1.**Transformer T1 design (24V1A, Vin(DC)=300V**~**900V)**

1-1-1. Determination of fly-back voltage VOR

 Turns-ratio Np:Ns and duty-ratio is determined along with Fly-back voltage VOR

$$
VOR = VO \times \frac{Np}{Ns} = \frac{ton}{toff} \times VIN
$$

$$
\Rightarrow \frac{Np}{Ns} = \frac{VOR}{VO}
$$

$$
\Rightarrow Duty = \frac{VOR}{VIN + VOR}
$$

When VIN(MIN)=300V, VOR=204V, Vf=1.5V:

$$
\frac{Np}{Ns} = \frac{VOR}{VO} = \frac{VOR}{Vout + Vf} = \frac{204V}{24V + 1.5V} = 8.0
$$

Duty(max) =
$$
\frac{VOR}{VIN(min) + VOR} = \frac{204V}{300V + 204V} = 0.405
$$

Figure1-3.MOSFET Vds

(*) VOR is adjusted to set it below 0.5 in consideration of MOSFET's loss.

1-1-2. Determination of Minimum frequency fsw and calculation of primary side winding inductance Lp The primary side maximum current Ippk and the primary side winding inductance Lp is determined from the minimum input voltage(VIN=300V) and the minimum frequency (Fsw=92kHz).

Other's parameter is following:

Po=24V × 1A=24W, Po (max)=30W(de-rating 0.8) in consideration of over current protection.

Transformer efficiency: η =85%

Resonance capacitor: Cv=100pF

$$
L_p = \left[\frac{VIN \text{ (min)} \times Duty \text{ (max)}}{\sqrt{\frac{2 \times \text{Po}(\text{max}) \times \text{fsw}}{\eta}} + \text{VIN}(\text{min}) \times Duty \text{ (max)} \times \text{fsw} \times \pi \times \sqrt{C_V}} \right]^2 = 1755 uH
$$

$$
Ippk = \sqrt{\frac{2 \times Po(\text{max})}{\eta \times Lp \times fsw}} = 0.662 A
$$

1-1-3. Determination of transformer size

Core size of the transformer is determined to EFD30 by the condition of Po(max)=30W.

(*) The above is guideline values. For details, check with the transformer manufacturer, etc.

1-1-4.Calculation of primary-side turn count Np

Generally, the maximum magnetic flux density $B(T)$ for an ordinary ferrite core is 0.4T @100°C, so Bsat = 0.3T.

$$
Np > \frac{Lp \times lppk}{Ae \times Bsat} = \frac{1750uH \times 0.66A}{68mm^2 \times 0.3T} = 57turns
$$

 In order not to cause a magnetic saturation, the IC must be used in areas that do not saturate from AL-Value-NI characteristics. In the case of Np=50 turns:

$$
AL-Value = \frac{Lp}{Np^2} = \frac{1750uH}{50turns^2} = 700nH/turns^2
$$

$$
NI = Np \times Ippk = 50 \text{turns} \times 0.66A = 33A \cdot \text{turns}
$$

Transformer is saturated based on the AL-value-NI characteristics.

Set the number of primary winding so as not to be saturation region. In the case of Np=64 turns:

$$
AL-Value = \frac{Lp}{Np^2} = \frac{1750uH}{64turns^2} = 427nH / turns^2
$$

$$
NI = Np \times Ippk = 64 \text{turns} \times 0.66A = 42.2A \cdot \text{turns}
$$

 In this case, this point is within the tolerance range Np = 64 turns is determined

1-1-5. Calculation of secondary-side turn count Ns

$$
\frac{\text{Np}}{\text{Ns}} = 8 \quad \rightarrow \quad \text{Ns} = \frac{64}{8} = 8 \text{ turns}
$$

1-1-6.Calculation of VCC turn count Nd

When VCC=24V, Vf_vcc=1V,

$$
Nd = Ns \times \frac{VCC + Vf_vcc}{Vout + V f} = 8turns \times \frac{24V + 1.0V}{24V + 1.5V} = 7.8turns
$$

(*)In the case of driving SiC-MOSFET, since it is necessary to control the Gate voltage, VCC is required more than 22V.

As a result, the transformer specifications are as follows.

Table 1-2. Transformer Specifications

Core	EFD30 compatible
٠D	1750uH
Np	64 turns
Ns	8 turns
Nd	8 turns

NI limit vs. AL-value (Typ.)

Reference Characteristics

1-1-7. Transformer design

1-2.**Selection of main components**

1-2-1.MOSFET:Q1

 For MOSFET selection, it must be considered maximum voltage between the drain and source, peak current, losses due to Ron, maximum power dissipation of the package.

 At low input voltage, the ON time of the MOSFET becomes long and the heat generated by Ron loss is bigger. Be sure to confirm the state incorporated in the product and execute the heat dissipation of the heat sink as needed. Current rating should be selected twice about Ippk.

 $Vds(\text{max}) = VIN(\text{max}) + VOR + Vspike = VIN(\text{max}) + (Vout + Vf) \times \frac{Np}{Ns} + Vspike = DC900V + (24V + 1.5V) \times \frac{64turns}{8turns} + Vspike$ $= 1104V + Vspike$

Calculation of Vspike is difficult. MOSFET breakdown voltage is 1700V by using a snubber circuit. In this design example, ROHM's MOSFET SCT2H12NZ(1700V 4A 1.15Ω) is selected .

Below show the typical characteristics of SCT2H12NY. Please refer to the SCT2H12NY data sheet for formal data.

1-2-2.Input capacitor: C2,C3,C4 Balance resistance: R1,R2,R3,R4,R5,R6 Use Table 1-3 to select the capacitance of the input capacitor.

Since Pout=24Vx1.1A≒25W Cmain:1x25=25 → 33uF

(*)When selecting, also consider other specifications such as the retention-time.

The breakdown voltage of the capacitor is required above the maximum input voltage.

VIN(MAX)/de-rating=900V/0.8=1125V

Using three 450V breakdown voltage capacitors in series, the breakdown voltage of the capacitor is 450V × 3 = 1350V. As noted, when connecting the capacitors in series, the balanced resistance is required for a constant voltage applied to all capacitors. Since the resistance is in loss, it is recommended to use more resistance 470kohm.

R1,R2,R3,R4,R5,R6's loss is below.

P11_12_13_14_15_16=VN(MAX)×VIN(MAX)/R=900V×900V/2.82Mohm=0.287W It is shown in Figure 1-5.

Figure 1-5. Input capacitor and Balance resistance

1-2-3.Current-sensing resistor: R19 Resistance for noise protection of CS terminal:R22

The current-sensing resistor limits the current that flows on the primary side to provide protection against output overload.

$$
R19 = \frac{Vcs}{Ippk} = \frac{1.0V}{0.66A} = 1.515\Omega
$$

Sensing resistor loss P_R19:

$$
P_R19(peak) = Ippk^2 \times R19 = 0.66A^2 \times 1.5\Omega = 0.6534W
$$

$$
P_R19(rms) = Iprms^2 \times R19 = \left(Ippk \times \sqrt{\frac{Duty(max)}{3}}\right)^2 \times R19 = \left(0.66A \times \sqrt{\frac{0.404}{3}}\right)^2 \times 1.0 = 0.0586W
$$

Set the value 1W or above in consideration of pulse resistance.

The structure of the resistance may vary the pulse resistance even with the same power rating. Check with the resistor manufacturers for details.

1-2-4. Overload protection correction setting resistor: R20

BD768xFJ-LB series has overload protection correction function in the input voltage. After the IC detects overload, there is a delay time to stop the switching operation. This delay is to increase the overload protection point with an increase input voltage. Correction function reduces the current detection level when it equals or exceeds an input voltage value. This function corrects the overload.

Since the input voltage range is DC300V ~ DC900V, switching voltage is set to DC400V. Izt is the current flowing from the IC to the transformer Nd winding in time of the switching ON.

Izt lower the current detection level at the top than 1mA, overload protection point is lowered.

$$
R20 = VIN(change) \times \frac{Nd}{Np} \times \frac{1}{Izt} = 500V \times \frac{8turns}{64turns} \times \frac{1}{1mA} = 62.5k\Omega
$$

Check whether the rating load can be taken after the point of over load protection is switched.

When the IC switches CS over current voltage level, it is changed from 1.0V to 0.7V.

$$
VIN(change) = R20 \times \frac{Np}{Nd} \times Izt = 56k \Omega \times \frac{64turns}{8turns} \times 1mA = 448V
$$

\n
$$
Ippk' = \frac{Vcs}{R19} = \frac{0.70V}{1.5\Omega} = 0.466A
$$

\n
$$
ton' = \frac{Lp \times Ippk'}{VIN(change)} = \frac{1750uH \times 0.466A}{496V} = 1.64us
$$

\n
$$
Ispk' = \frac{Np}{Ns} \times Ippk' = \frac{64turns}{8turns} \times 0.466A = 3.728A
$$

\n
$$
Ls = Lp \times \left(\frac{Ns}{Np}\right)^2 = 1750uH \times \left(\frac{8turns}{64turns}\right)^2 = 27.34uH
$$

\n
$$
toff' = \frac{Ls \times Ispk'}{Vout + Vf} = \frac{27.34uH \times 3.728A}{24V + 1.5V} = 3.997us
$$

\n
$$
tdelay = \pi \times \sqrt{Lp \times Cv} = 3.14 \times \sqrt{1750uH \times 100pF} = 1.31us
$$

\n
$$
fsw' = \frac{1}{ton' + toff' + tdelay} = \frac{1}{1.64us + 3.997us + 1.31us} = 143kHz
$$

$$
\begin{array}{c}\n\hline\n\text{tdelay.} \\
\hline\n\text{toff.} \\
\hline\n\end{array}
$$

 $Po' = \frac{1}{2} \times Lp \times Ippk^{2} \times fsw \times \eta = \frac{1}{2} \times 1750uH \times 0.466A^{2} \times 120kHz \times 0.85 = 19.38W$ $Po' = \frac{1}{2} \times Lp \times Ippk'^2 \times fsw' \times \eta = \frac{1}{2} \times 1750uH \times 0.466A^2 \times 120kHz \times 0.85 = 19.38W$ Transformer efficiency: $\eta = 0.85$

When Po' is under the rated output power, R19 has to be adjusted. In this board, furthermore, if the over load point is adjusted by a resistor of 100 kHz, the point is changed to 816V

because the maximum frequency of the IC is restricted to 120 kHz. Regarding the over load protection point, please check in an actual product.

Figure 1-7. Input voltage correction circuit of overcurrent detection (reference value)

1-2-5. Setting resistor for ZT terminal voltage: R21

The ZT bottom detected voltage is Vzt1=100mV(typ)(ZT fall), Vzt2=200mV(typ)(ZT rise), and ZT OVP(min) is 3.30V, so as a guide, set Vzt to 1V to 3V.

$$
Vzt = (Vout + Vf) \times \frac{Nd}{Ns} \times \frac{R21}{R20 + R21} = 2.7V - \text{R21} = 11.84k\Omega
$$

1-2-6.ZT terminal capacitor: C11

 C11 is a capacitor for stability of ZT voltage and timing adjustment of the bottom detection. Check the waveform of ZT terminal and the timing of bottom detection, and adjust it as necessary.

1-2-7.VCC-diode: D18

A high-speed diode is recommended as the VCC-diode.

When D13_Vf=1V, reverse voltage applied to the VCC-diode:

$$
Vdr = VCC(max) + Vf + VINmax \times \frac{Nd}{Np}
$$

This IC has VCC OVP function, VCC OVP (max) = 31.5V.

Reverse voltage of the diode is set so as not to exceed the Vr of diode in conditions of VCC OVP (max).

$$
Vdr = 31.5V + 1.0V + 900V \times \frac{8 \text{turns}}{64 \text{turns}} = 145V
$$

With a design-margin taken into account, $145V/0.7 \div 200V \rightarrow 200V$ component is selected. (Example: ROHM's RF05VAM2S 200V 0.5A)

1-2-8.VCC winding surge-voltage limiting resistor: Rvcc1

Based on the transformer's leakage inductance (Lleak), a large surge-voltage (spike noise) may occur during the instant when the MOSFET is switched from ON to OFF. This surge-voltage is induced in the VCC winding, and as the VCC voltage increases the IC's VCC overvoltage protection may be triggered.

A limiting resistor R16 (approximately 5Ω to 22Ω) is inserted to reduce the surge-voltage that is induced in the VCC winding. Confirm the rise in VCC voltage while the resistor is assembled in the product.

1-2-9. VCC starter resistance ; R11,R12,R13,R14 capacitance; C5,C6 and Rectifier diode; D18, D19

Start resistance R_{START} is the resistance required to start the IC.

When the start resistance R_{START} value is reduced, the standby power is increased and the startup time is shortened. Conversely, when the start resistance R_{START} value is increased, the standby power is reduced and the startup time is lengthened. When BD768xFJ is in standby mode, current I_{OFF} becomes 40 μ A (Max) However, this is the minimum current required to start the IC. In this case current I_{OFF} is 40µA(Max) with margin. Input voltage VIN_start=180V: VCCUVLO(max)=20V: lvcc-protected(min)=0.3mA:

 $Rstart < (Vec_{{\text{start}}}-VCCuvl\alpha(\text{min}))/Istart(\text{max}) = (180V - 20V)/40uA = 4000kohm$

Rstart (*Vin*_max*Vcc*_ *ovp*(max))/ *Icc*_ *protect* (900*V* 31.5*V*)/ 0.3*mA* 2895*kohm*

2895kohm Rstart 4000*kohm*

From the above results, set Rstart = 2940kohm (1Mohm \times 2 + 470kohm \times 2 series).

Start-up time is shown in Figure 1-8.

Figure 1-8. Start up time

A VCC capacitor is needed to stabilize the IC's VCC voltage.

Capacitance of 2.2μF or above is recommended.

This example is recommended circuit of Figure 1-9 for the start-up time and stability.

At startup, only the C6 works for fast start. After starting, after the output voltage is above a certain voltage, C5 operates. D18 is recommended Low IR Switching diode. (Example Rohm 1SS355VM)

Figure1-9. resistance of Starter and VCC capacitor

1-2-10.Brown IN/OUT resistance: R7,R8,R9,R10,R15 and BO capacitor: C8

When the input VH value is low, the brown out function stops the DC/DC operations (The IC itself continues to operate).

In the following example, V_{HON} is the operation start V_H voltage (L to H), and V_{HOFF} is the operation stop V_H voltage (H to L). IC operation start (OFF => ON) $(V_{HON}-1.0) / R_H = 1.0 / R_L + 15*10e-6$

IC operation stop (ON => OFF) $(V_{\text{HOFF}}-1.0) / R_{\text{H}} = 1.0 / R_{\text{L}}$

Based on the above, R_H and R_L can be calculated as follows. $R_{H} = (V_{HON} - V_{HOFF}) / (15 * 10e - 6)$, $R_{L} = 1.0 / (V_{HOFF} - 1.0) * R_{H}$

V_{HON}=90V, V_{HOFF}=60V: It becomes the circuit shown in Figure 1-10.

It should be noted that the BO terminal is required capacitor C8.

Figure 1-10. Broun IN/OUT setting

1-2-11.Snubber circuits: C snubber 1, R snubber1, D13,D14, D15,D16

Based on the transformer's leakage inductance (Lleak), a large surge-voltage (spike noise) may occur during the instant when the MOSFET is switched from ON to OFF. This surge-voltage is applied between the MOSFET's Drain and Source, so in the worst case damage to MOSFET might occur. RCD snubber circuits are recommended to suppress this surge-voltage.

(1) Determination of clamp voltage (Vclamp) and clamp ripple-voltage (Vripple)

The clamp voltage is determined by the MOSFET's withstand voltage considering a design margin. Vclamp = 1700V × 0.8 = 1360V

The clamp ripple-voltage (Vripple) is set about 50V.

(2) Determination of R snubber 1

R snubber 1 is selected according to the following conditions.

R snubber $1 < 2 \times Vclamp \times \frac{Vclamp - VOR}{Lleak \times Ip^2 \times fsw(max)}$

 Lleak = Lp x 10% = 1750uH x 10% = 175uH In the case of Po=25W, VIN(max)=900V, Ip、fsw is calculated

$$
Po = \frac{1}{2} \times Lp \times Ip^2 \times fsw \times \eta
$$

\n
$$
Ip = \frac{Vcs}{Rcs}
$$
\n
$$
fsw = \frac{1}{\tan + \text{toff} + \text{tdelay}} = \frac{1}{\left(\frac{Lp}{VIN} \times Ip\right) + \left(\frac{Ls}{Vo + Vf} \times \frac{Np}{Ns} \times lp\right) + \pi \times \sqrt{Lp \times Cv}}
$$

⇒ Vcs=0.7V, Ip=0.466A, fsw=161kHz

Rsnubber $1 < 2 \times 1360V \times \frac{1360V - 204V}{175uH \times 0.466^2 \times 120kHz} = 253k \Omega$

R snubber 1 loss P_ R snubber 1 is expressed as

$$
P_R \text{ subber } 1 = \frac{(\text{Vclamp } - \text{VIN })^2}{R \text{ subber } 1} = \frac{(1360 - 900)^2}{200 \text{k } \Omega} = 1.05 \text{W}
$$

A more than 2W component is determined with consideration for design margin.

(3) Determination of C snubber 1

 $\frac{1360 \text{V}}{50 \text{V} \times 120 \text{kHz}} \times 200 \text{k} \quad \Omega = 1607 \text{pF}$ Csnubber $1 > \frac{Vclamp}{Vripple \times fsw(min) \times Rsnubber} = \frac{1360V}{50V \times 120kHz \times 200k \Omega} =$

The voltage applied to C snubber 1 is 1360V-900=460V.

C snubber 1 is set 600V or above with design margin.

(4) Determination of D13,D14

Choose a fast recovery diode as the diode, with a withstand voltage that is at or above the MOSFET's Vds (max) value. The surge-voltage affects not only the transformer's leakage inductance but also the PCB substrate's pattern. Confirm the Vds voltage while assembled in the product, and adjust the snubber circuit as necessary.

(5) TVS: D15, D16

 For excellent protection performance, it is possible to cramp the transient noises. Please determine after checking the withstand voltage and operation waveform.

1-2-12.FB terminal capacitor: C12

C12 is a capacitor for stability of FB voltage (approximately 1000pF to 0.01uF).

1-2-13.MOSFET gate circuit: R16,R17,R18,D17

 The MOSFET's gate circuits affect the MOSFET's loss and the generation of noise. The Switching speed for turn-on is adjusted using R16+R17, and for turn-off is adjusted using R16, via the drawing diode D17. (Example: R16:10Ω 0.25W、R17:150Ω、D17:SBD 60V 1A)

In the case of Quasi-Resonant converters, switching-loss basically does not occur during turn-on, but it occurs predominantly during turn-off. To reduce switching-loss when the IC turned off, turn-off speed can be increased by reducing R16 value, but sharp changes in current will occur, which increases the switching-noise. Since there is a trade-off relation between loss (heat generation) and noise, measure the MOSFET's temperature rise and noise while it is assembled in the product, and adjust it as necessary.

Also, since a pulse current flows to R16, check the pulse resistance of the resistors being used. R18 is the resistance to pull down the gate of the MOSFET. The recommended value is 10kohm ~ 100kohm.

1-2-14.Output rectification diode: DN1

Choose a high-speed diode (Schottky barrier diode or fast recovery diode) as the output rectification diode. When Vf=1.5V, reverse voltage applied to output diode is

 $Vdr = Vout(max) + Vf + VINmax \times \frac{Ns}{Np}$

When Vout(max)=24.0V+5%=25.2V:

 $Vdr = 25.2V + 1.5V + 900V \times \frac{8}{64} = 139.2V$

139.2V/0.7=198V \rightarrow 200V component is determined with consideration for design margin.

 Also, diode loss (approximate value) becomes Pd=Vf x Iout=1.5V x 1.0A=1.5W (Example: ROHM's RFN10T2D:200V 10A, TO-220FN package)

Using a voltage margin of 70% or less and current of 50% or less is recommended. Check the rise in temperature while assembled in the product. If necessary, reconsider the component and radiate heat by a heat sink or similar to dissipate the heat.

1-2-15.Output capacitors: C out 1,C out 2,C out 3, C out 4

Determine the output capacitors based on the output load's allowable peak-to-peak ripple voltage (∆Vpp) and ripple-current. When the MOSFET is ON, the output diode is OFF. At that time, current is supplied to the load from the output capacitors. When the MOSFET is OFF, the output diode is ON. At that time, the output capacitors are charged and a load current is also supplied.

When ∆Vpp = 200mV,

$$
Z_C < \frac{\Delta Vpp}{Ispk} = \frac{\Delta Vpp}{\frac{Np}{Ns} \times Ippk} = \frac{0.2V}{\frac{64}{8} \times 0.66A} = 0.0379 \text{ }\Omega \qquad \text{at} \quad 60 \text{kHz (fsw min)}
$$

With an ordinary switching power supply electrolytic-capacitor (low-impedance component), impedance is rated at 100 kHz, so it is converted to 100kHz.

$$
Z_C < 0.0379 \quad \Omega \times \frac{60}{100} = 0.02274 \quad \Omega \quad \text{at} \quad 100kHz
$$

Ripple-current Is (rms):

Is(rms) = Ispk ×
$$
\sqrt{\frac{1 - Duty}{3}}
$$
 = $\frac{64}{8}$ × 0.66A × $\sqrt{\frac{1 - 0.261}{3}}$ = 2.62A

The capacitor's withstand voltage should be set to about twice the output voltage.

Vout x 2 = 24V x 2 = 48V \rightarrow 50V over

Select an electrolytic capacitor that is suitable for these conditions.

(Example: low impedance type 50V, 470 μF × 3 parallel for switching power supply)

(*) Use the actual equipment to confirm the actual ripple-voltage and ripple-current.

1-2-16. Output voltage setting resistors: R25,R26,R28

When Shunt regulator IC2:Vref=2.495V,

$$
Vo = \left(1 + \frac{R25 + R26}{R28}\right) \times Vref = \left(1 + \frac{82 k\Omega + 4.3 k\Omega}{10 k\Omega}\right) \times 2.495 V = 24.02 V
$$

1-2-17.Parts for adjustment of control circuit: R24,R27,R32,C15

R27 and C15 are parts for phase compensation. Approximately R27=1k~30kΩ, C15=0.1uF, and adjust them while they are assembled in the product.

R32 is a resistor which limits a control circuit current. Approximately R32:300 to 2kΩ, and adjust it while it assembled in the product.R24 is a resistor for adjustment of minimum operating current of shunt regulator IC2.

In case of IC2: TL431, minimum operating current is 1mA. And when Optocoupler:PC1_Vf is 1V, $R24 = 1V / 1mA = 1kΩ$

1-3.**EMI countermeasures**

Confirm the following with regard to EMI countermeasures.

(*) Constants are reference values. Need to be adjusted based on noise effects.

- Addition of filter to input block
- Addition of capacitor between primary-side and secondary-side (approximately CY1,CY2+CY3: Y-Cap 2200pF)
- Addition of RC snubber to secondary diode

1-4.**Output noise countermeasures**

As an output noise countermeasure, add an LC filter (approximately L:10μH, C: 10μF to 100μF) to the output.

(*) Constants are reference values.

Need to be adjusted based on noise effects.

Figure1-11. LC Filter Circuit

1-5.**Proposed PCB layout**

A proposed layout (example) for these circuits is shown in Figure 1-12.

・Double-sided board, lead component view

Figure 1-13. Evaluation board

2. Evaluation result

2.1. Evaluation circuit and parts list

The evaluation circuit is shown in Figure 2-1, parts list is shown in Table 2-1.

Figure 2-1. Isolated Fly-buck Quasi-Resonant convertor (24V1A=24W)

Table 2-1. Isolated Fly-buck Quasi-Resonant convertor (24V1A=24W)

Application Note

2.2. Evaluation Result (Efficiency, switching frequency)

Figure 2-2. Efficiency vs Output Power

Figure 2-3 Switching Frequency vs Output Power

2.3. Evaluation Result (Waveform)

VIN(DC)=300V VIN(DC)=600V VIN(DC)=900V Figure 2-4. Drain Voltage and Drain current waveform (VO=24V,IO=1.0A, PO=24W) **CH1: Vdrain (200V/div), CH4: Idrain (200mA/div)**

VIN(DC)=300V VIN(DC)=600V VIN(DC)=900V Figure 2-5. Drain Voltage and Drain current waveform (VO=24V,IO=2.1A, PO=50W) **CH1: Vdrain (200V/div), CH4: Idrain (500mA/div)**

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