BTS50010-1TAE

Smart High-Side Power Switch

1 Overview

Quality Requirement Category: Automotive

Features

- One high-side power output
- Output peak current up to 250 A
- Wide range logic input signal (3.3 V, 5 V, 12 V)
- Embedded diagnostic and protection features
- Current mirror for load current measurement
- Electrostatic discharge protection (ESD)
- Low standby current and very low output leakage current
- Green Product (RoHS compliant)
- AEC Qualified

Applications

- Suitable for inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for 12V applications with very high inrush current (<250 A), such as small engine starter motors

Description

The BTS50010-1TAE is a 1.0 mΩ single channel Smart High-Side Power Switch, embedded in a PG-TO-263-7-10 package, providing protective functions and diagnosis. The power transistor is built by a N-channel power MOSFET with charge pump. It is specially designed to drive loads with up to 250 A peak current, and low wire harness inductance.

Overview

Table 1 Product Summary

Parameter	Symbol	Values
Operating voltage range	$V_{S(OP)}$	8 V … 18 V
Extended supply voltage	$V_{S(DYN)}$	5.5 V … 28 V
Typical ON-state resistance (T_J = 25°C)	$R_{DS(ON)}$	1 mΩ
Maximum ON-state resistance (T_J = 150°C)	$R_{DS(ON)}$	2.1 mΩ
Typical load current (T_A = 85°C)	$I_{L(NOM)}$	40 A
Typical current sense differential ratio	dk_{ILIS}	52100
Minimum short circuit current threshold	$I_{CL(0)}$	250 A
Maximum stand-by current for the whole device with load (T_A = T_J = 85°C)	$I_{VS\ (OFF)}$	18 µA
Maximum reverse battery voltage (T_A = 25°C for 2 min)	$-V_{S(REV)}$	16 V

Embedded Diagnostic Functions

- Proportional load current sense
- Short circuit / Overtemperature detection
- Latched status signal after short circuit or overtemperature detection

Embedded Protection Functions

- Undervoltage shutdown with latch at low supply voltages
- Infineon® ReverSave™: Reverse battery protection by self turn ON of power MOSFET
- Infineon® Inversave: Inverse operation robustness capability
- Secure load turn-OFF while device loss of GND connection
- Overtemperature protection with latch
- Short circuit protection with latch
- Overvoltage protection with external components
- Enhanced short circuit operation
- Infineon® SMART CLAMPING

Type	Package	Marking
BTS50010-1TAE	PG-TO-263-7-10	S50010E

Table of Contents

2 Block Diagram

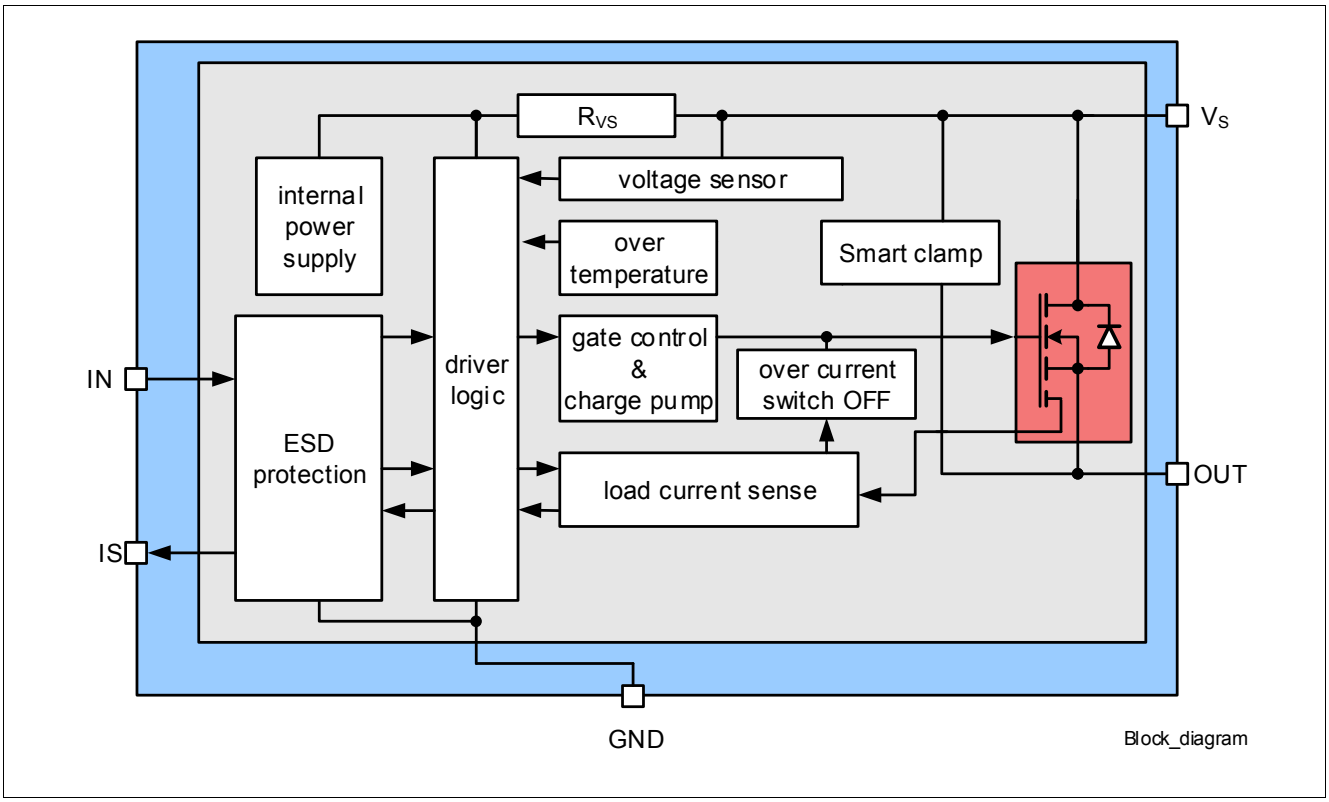


Figure 1 Block Diagram for the BTS50010-1TAE

3 Pin Configuration

3.1 Pin Assignment

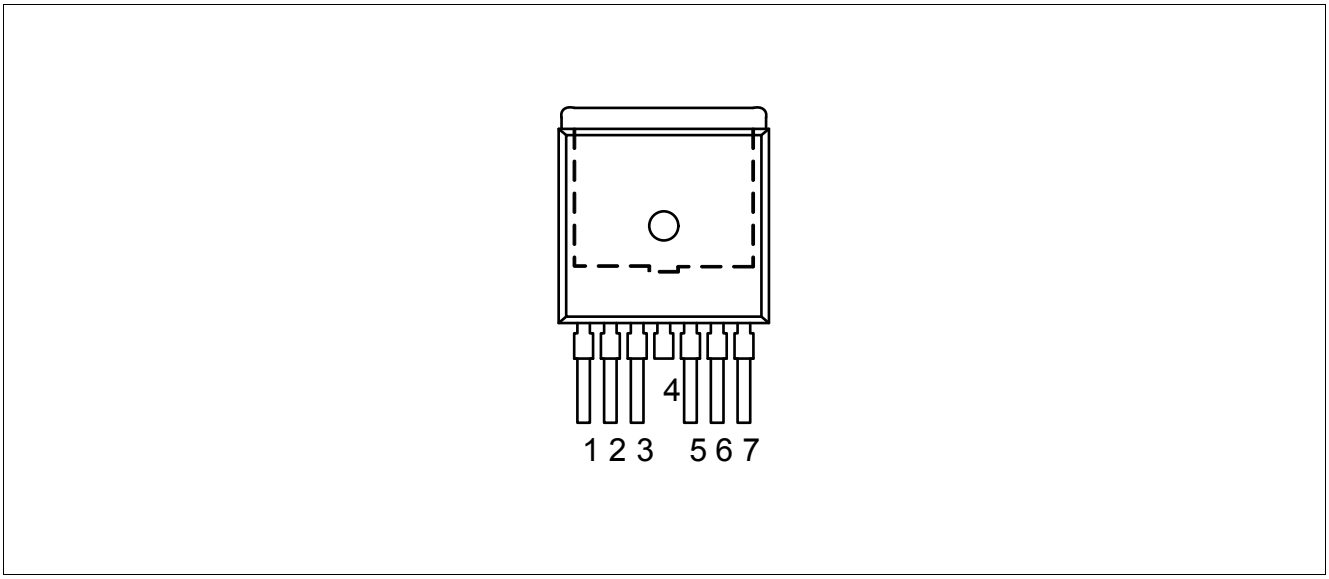


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	**GrouND;** Signal Ground
2	IN	**INput;** Digital signal to switch ON channel (“high” active)
3	IS	**Sense;** Analog/Digital signal for diagnosis, if not used: left open
4, Cooling tab	VS	**Supply Voltage;** Battery voltage
5, 6, 7	OUT	**OUTput;** Protected high side power output channel[1)]

1) All output pins are internally shorted. All output pins have to be shorted on PCB, too. Not shorting all outputs on PCB will considerably increase the ON-state resistance and decrease the current sense / overcurrent tripping accuracy. PCB traces have to be designed to withstand the maximum current.

3.3 Voltage and Current Definition

Figure 3 shows all terms used in this Data Sheet, with associated convention for positive values.

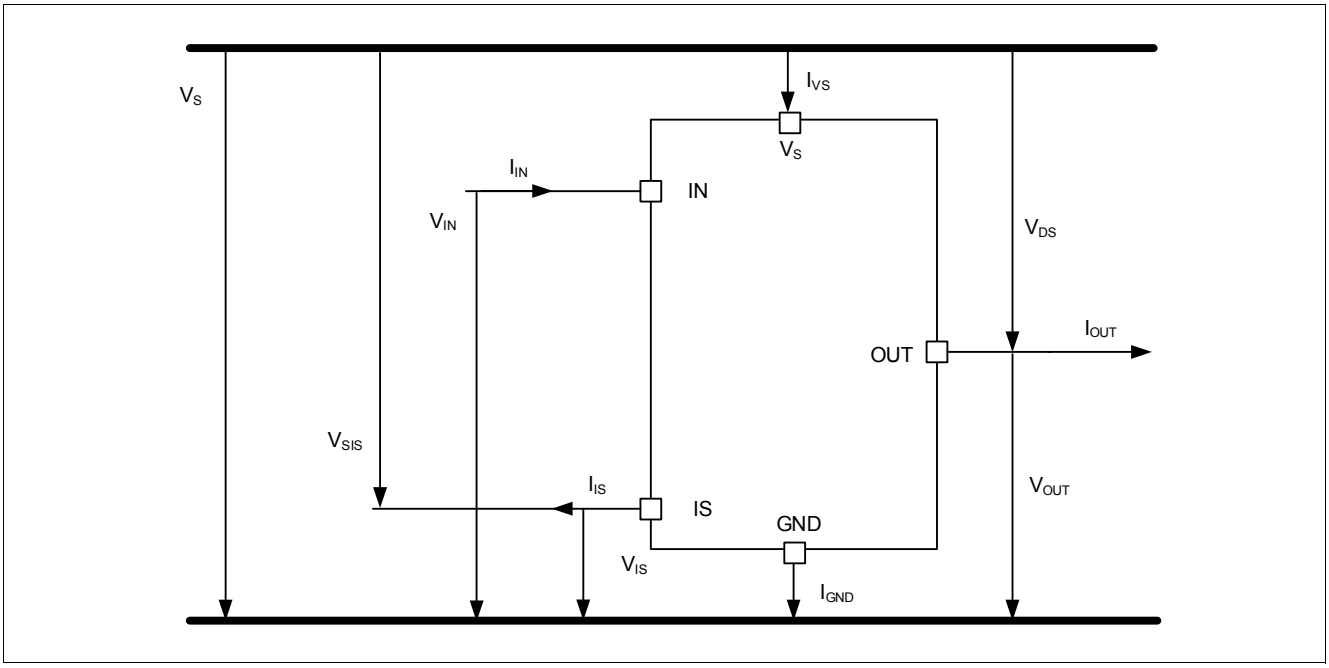


Figure 3 Voltage and Current Definition

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings[1)]

T_J = -40°C to +150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Supply Voltage	V_S	-0.3	–	28	V	–	P_4.1.1
Reverse Polarity Voltage	$-V_{S(REV)}$	0	–	16	V	[2)] $t < 2$ min T_A = 25°C $R_L \geq 0.5\ \Omega$	P_4.1.2
Load Dump Voltage	$V_{BAT(LD)}$	–	–	45	V	[3)] $R_I = 2\ \Omega$ $R_L = 2.2\ \Omega$ $R_{IS} = 1\ k\Omega$ $R_{IN} = 4.7\ k\Omega$	P_4.1.5
Short Circuit Capability							
Supply Voltage for Short Circuit Protection	$V_{BAT(SC)}$	5	–	16	V	[4)] $T_{J(0)} \leq 85°C$ $R_{SUPPLY} + R_{CABLE}$= 20 mΩ ... 35 mΩ $L_{SUPPLY} + L_{CABLE}$ = 1 µH ... 2.5 µH See **Figure 24** + **Chapter 5.3.6**	P_4.1.3
GND Pin							
Current through GND pin	I_{GND}	-15 –[5)]	– –	10[6)] 15	mA	– $t \leq 2$ min	P_4.1.6
Input Pin							
Voltage at IN pin	V_{IN}	-0.3	–	V_S	V	–	P_4.1.7
Current through IN pin	I_{IN}	-5 -5	– –	5 50[5)]	mA	– $t \leq 2$ min	P_4.1.8
Maximum Retry Frequency in Fault Condition	f_{fault}	–	–	1	Hz	–	P_4.1.9
Sense Pin							
Voltage at IS pin	V_{IS}	-0.3	–	V_S	V	–	P_4.1.10
Current through IS Pin	I_{IS}	-15 –[5)]	– –	10[6)] 15	mA	– $t \leq 2$ min	P_4.1.11

Table 2 Absolute Maximum Ratings[1)] (cont'd)

T_J = -40°C to +150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power Stage							
Maximum Energy Dissipation by Switching Off Inductive Load Single Pulse over Lifetime	E_{AS}	–	–	450	mJ	V_S = 13.5 V I_L = 250A $T_{J(0)} \leq$ 150°C See **Figure 5**	P_4.1.12
Maximum Energy Dissipation Repetitive Pulse	E_{AR}	–	–	460	mJ	[7)] V_S = 13.5 V $I_L = I_{L(NOM)}$ = 40A $T_{J(0)} \leq$ 105°C See **Figure 5**	P_4.1.13
Maximum Energy Dissipation Repetitive Pulse	E_{AR}	–	–	235	mJ	[7)] V_S = 13.5 V I_L = 80A $T_{J(0)} \leq$ 105°C See **Figure 5**	P_4.1.14
Average Power Dissipation	P_{TOT}	–	–	200	W	T_C = -40°C to 150°C	P_4.1.15
Voltage at OUT Pin	V_{OUT}	-64	–	–	V	–	P_4.1.21
Temperatures							
Junction Temperature	T_J	-40	–	150	°C	–	P_4.1.16
Dynamic Temperature Increase while Switching	ΔT_J	–	–	60	K	See **Chapter 5.3**	P_4.1.17
Storage Temperature	T_{STG}	-55	–	150	°C	–	P_4.1.18
ESD Susceptibility							
ESD Susceptibility (all Pins)	$V_{ESD(HBM)}$	-2	–	2	kV	HBM[8)]	P_4.1.19
ESD Susceptibility OUT Pin vs. GND / V_S	$V_{ESD(HBM)}$	-4	–	4	kV	HBM[8)]	P_4.1.20

1) Not subject to production test, specified by design.
2) The device is mounted on a FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection.
3) $V_{S(LD)}$ is setup without DUT connected to the generator per ISO 7637-1.
4) Not in accordance to AEC Q100-012 "short circuit reliability characterization of smart power devices for 12V systems".
5) The total reverse current (sum of I_{GND}, I_{IS} and $-I_{IN}$) is limited by $-V_{S(REV)\_max}$ and R_{VS}.
6) $T_C \leq$ 125°C
7) Setup for EAR equivalent to short circuit test AEC Q100-012: Grade A (exceeding 10^6 cycles, parameter deviations are possible)
8) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the Data Sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

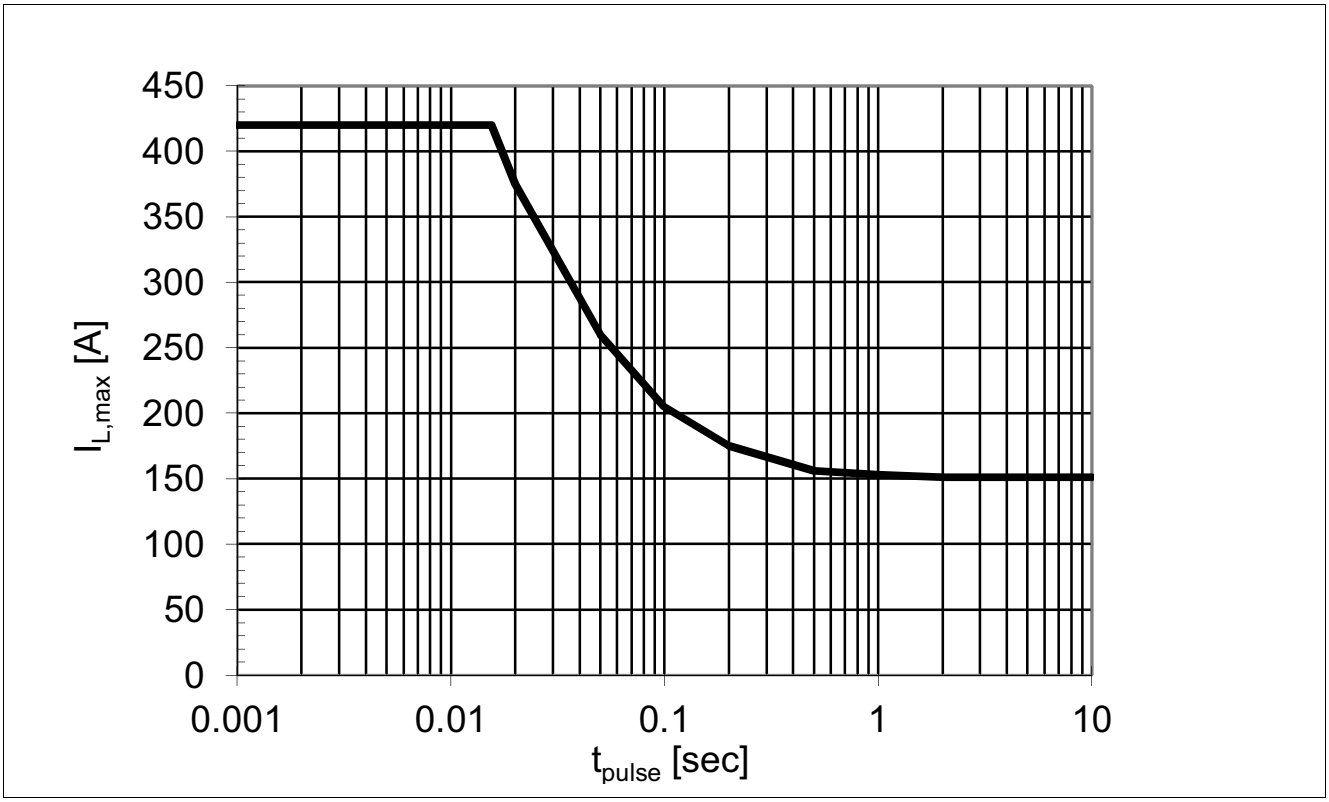


Figure 4 Maximum Single Pulse Current vs. Pulse Time, $T_J \leq 150°C$, $T_{PIN} = 85°C$

Note: Above diagram shows the maximum single pulse current that can be maintained by the internal power stage bond wires for a given pulse time t_{pulse}. The maximum reachable current may be smaller depending on the device current limitation level. The maximum reachable pulse time may be shorter due to thermal protection of the device. T_{PIN} is the temperature of pins 5, 6 and 7.

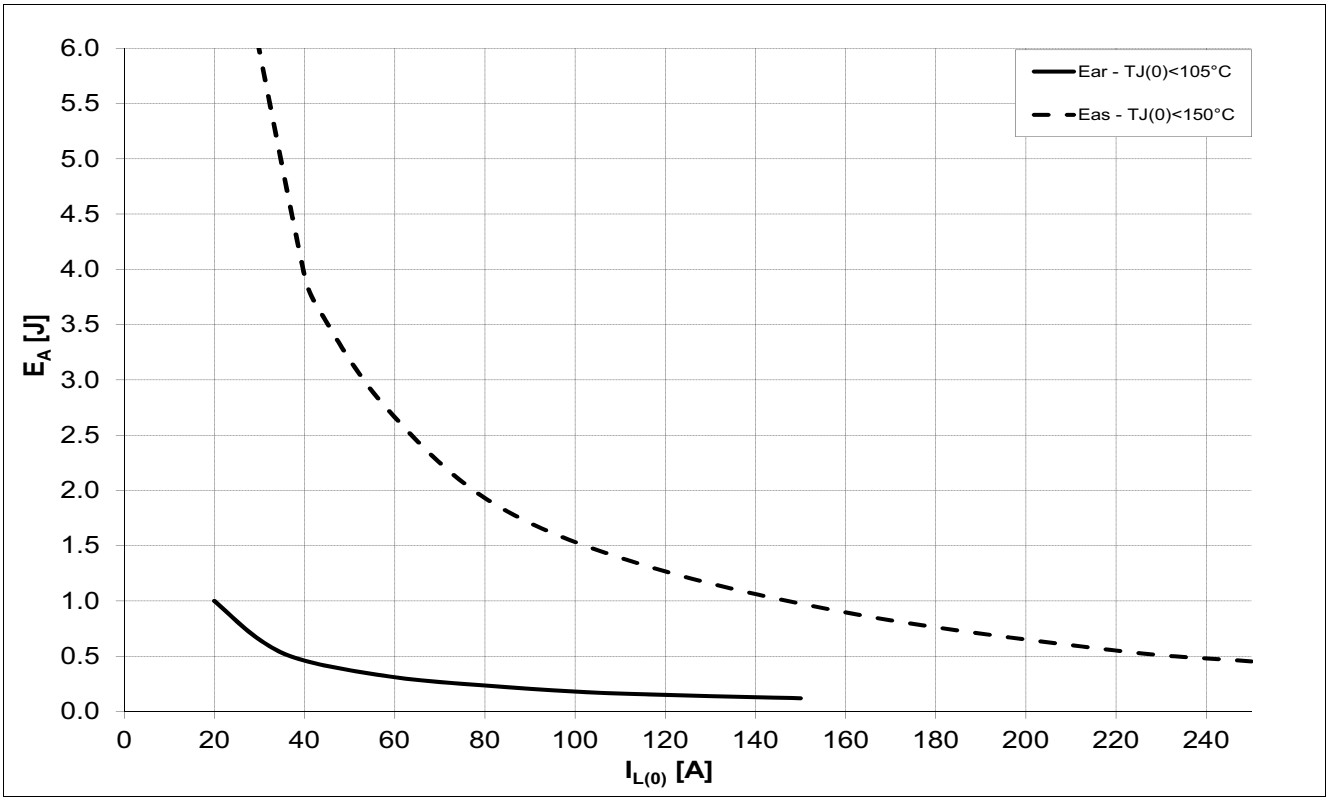


Figure 5 Maximum Energy Dissipation for Inductive Switch OFF, E_A vs. I_L at V_S = 13.5 V

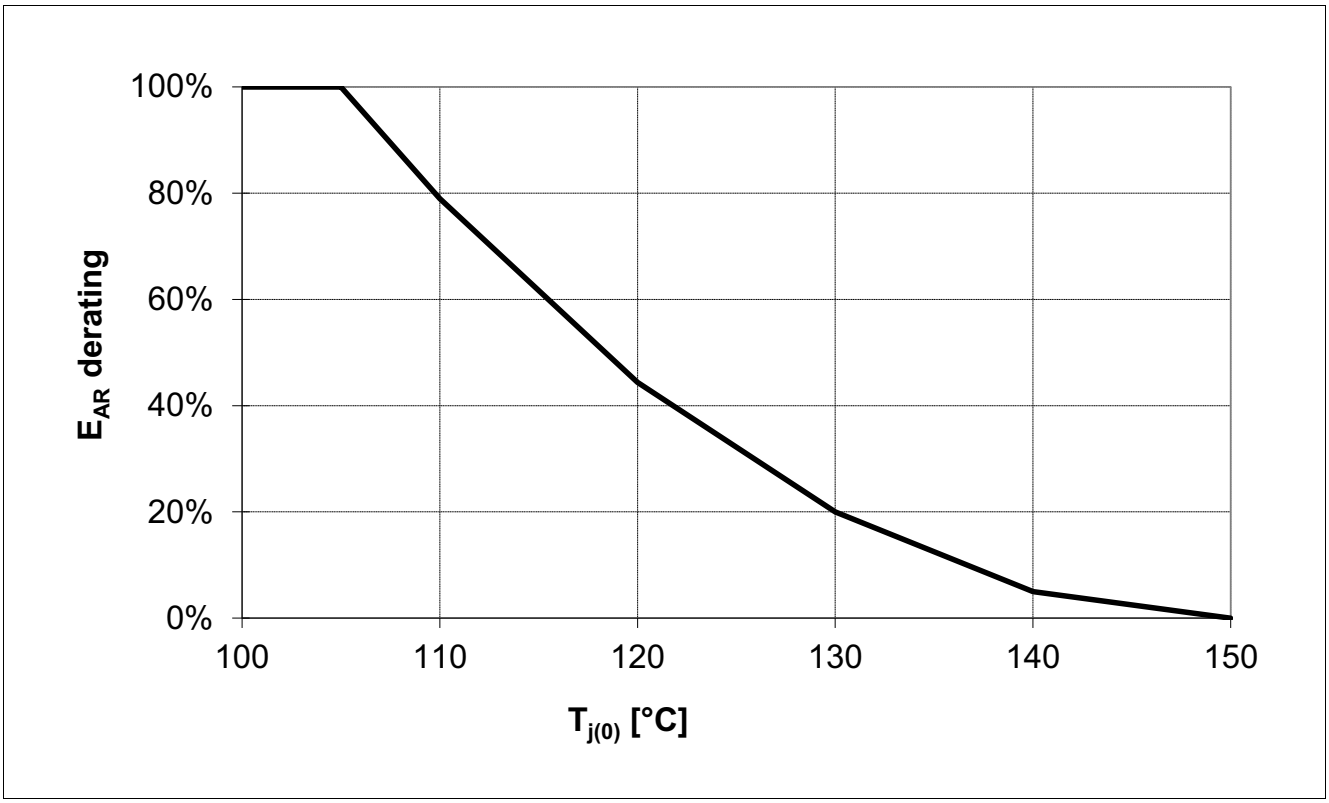


Figure 6 Maximum Energy Dissipation Repetitive Pulse temperature derating

4.2 Functional Range

Table 3 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage Range for Nominal Operation	$V_{S(NOM)}$	8	–	18	V	–	P_4.2.1
Supply Voltage Range for Extended Operation	$V_{S(EXT)}$	$V_{S(UV)}$	–	28	V	1) $V_{IN} \geq 2.2$ V $I_L \leq I_{L(NOM)}$ Parameter deviations possible	P_4.2.2
Slewrate at OUT	$\lvert dV_{DS}/dt \rvert$	–	–	10	V/µs	1) $\lvert V_{DS} \rvert < 3$V See **Chapter 5.1.4**	P_4.2.7
Slewrate at OUT	$\lvert dV_{DS}/dt \rvert$	–	–	0.2	V/µs	1) $V_{S(EXT)} < V_S < 8$ V $0 < V_{DS} < 1$ V $t < t_{ON(DELAY)}$ See **Chapter 5.1.4**	P_4.2.8

1) Not subject to production test. Specified by design

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal Resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	–	0.5	K/W	1)	P_4.3.1
Junction to Ambient	$R_{thJA(2s2p)}$	–	20	–	K/W	1)2)	P_4.3.2
Junction to Ambient	R_{thJA}	–	70	–	K/W	1)3)	P_4.3.3

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. T_A = 25°C. Device is dissipating 2 W power.

3) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 1s0p board; the Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with only one top copper layer 1 × 70 µm. T_A = 25°C. Device is dissipating 2 W power.

Figure 7 is showing the typical thermal impedance of BTS50010-1TAE mounted according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 1s0p and 2s2p boards.

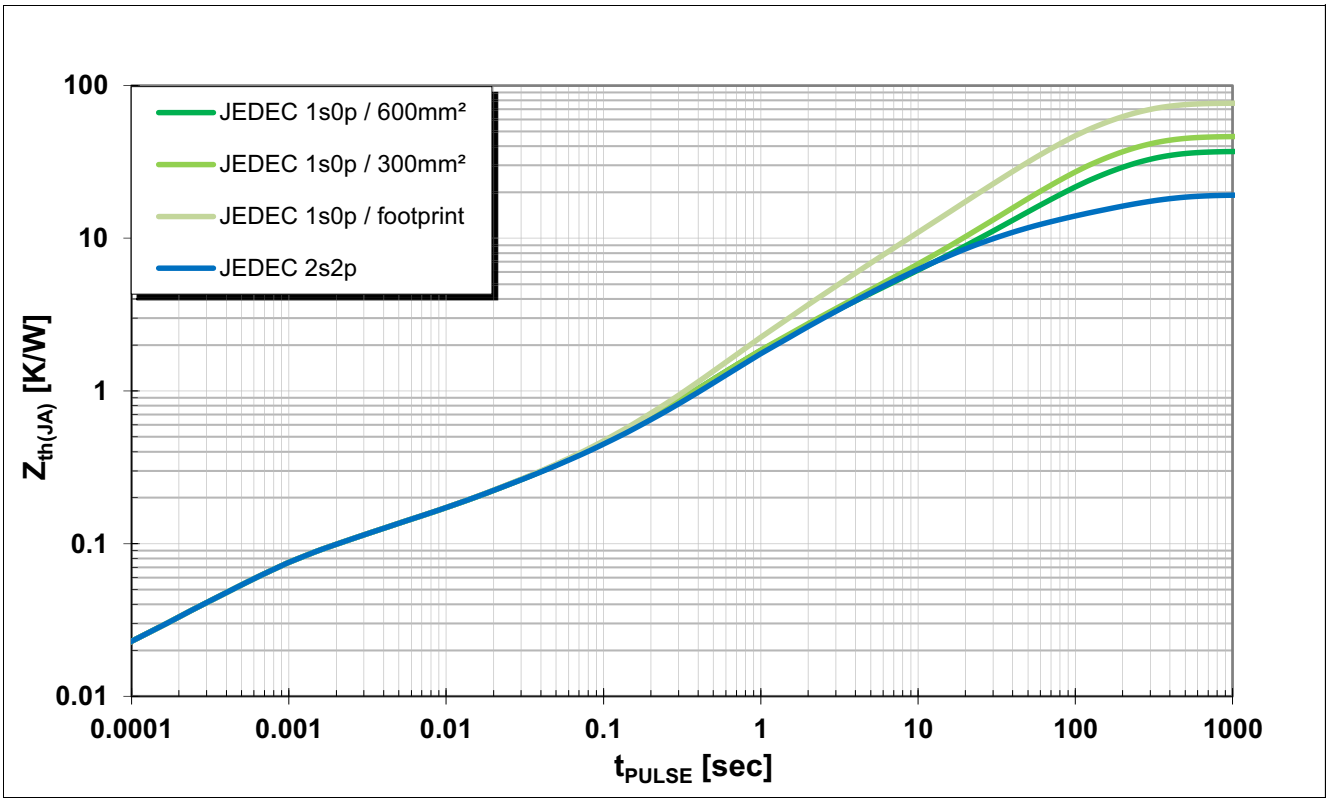


Figure 7 Typical Transient Thermal Impedance $Z_{th(JA)}$ = f(time) for Different PCB Conditions

5 Functional Description

5.1 Power Stage

The power stage is built by a N-channel power MOSFET (DMOS) with charge pump.

5.1.1 Output ON-State Resistance

The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature T_J. **Page 36** shows the dependencies in terms of temperature and supply voltage, for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 5.3.5**.

A HIGH signal (see **Chapter 5.2**) at the input pin causes the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission.

5.1.2 Switching Resistive Loads

Figure 8 shows the typical timing when switching a resistive load. The power stage has a defined switching behavior. Defined slew rates results in lowest EMC emission at minimum switching losses.

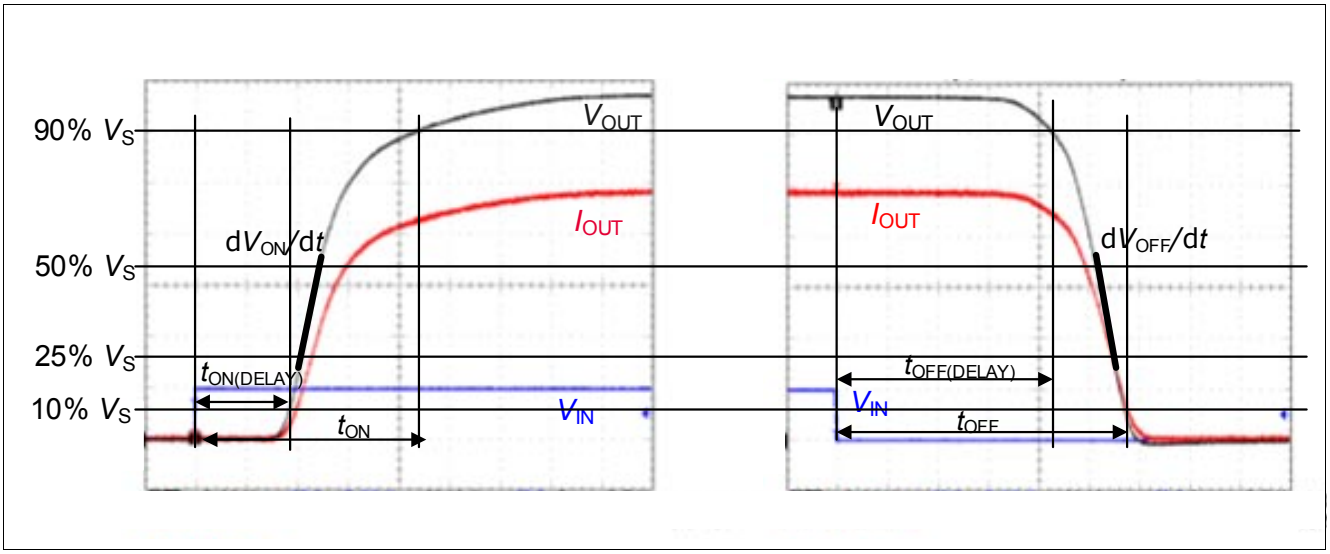


Figure 8 Switching a Resistive Load: Timing

5.1.3 Switching Inductive Loads

5.1.3.1 Output Clamping

When switching OFF inductive loads with high side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to high voltages, there is a Infineon® SMART CLAMPING mechanism implemented that keeps negative output voltage to a certain level (V_S - $V_{DS(CL)}$). Please refer to **Figure 9** and **Figure 10** for details. Nevertheless, the maximum allowed load inductance remains limited.

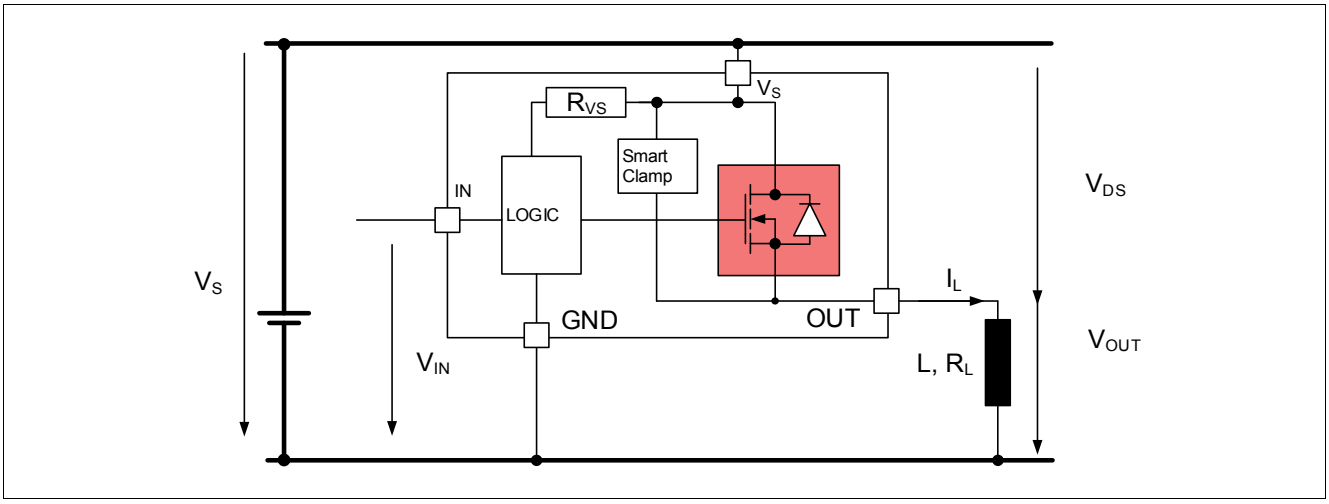


Figure 9 Output Clamp

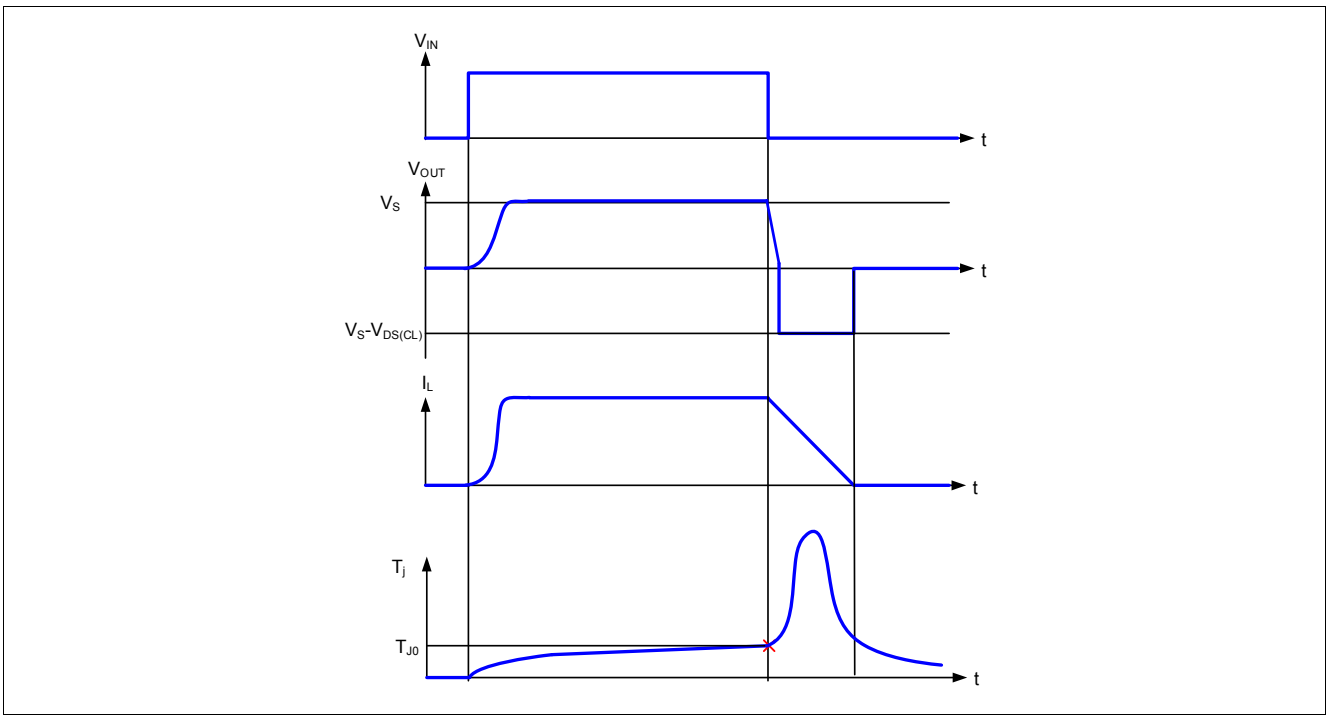


Figure 10 Switching an Inductance

The BTS50010-1TAE provides Infineon® SMART CLAMPING functionality. To increase the energy capability, the clamp voltage $V_{DS(CL)}$ increases with junction temperature T_J and with load current I_L. Refer to **Page 38**.

5.1.3.2 Maximum Load Inductance

During demagnetization of inductive loads, energy must be dissipated in the BTS50010-1TAE. This energy can be calculated with following equation:

$$E = V_{DS(CL)} \times \frac{L}{R_L} \times \left[\frac{V_S - V_{DS(CL)}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_S - V_{DS(CL)}}\right) + I_L \right] \quad (5.1)$$

For simplification, equation (5.2) can be used if R_L = 0 Ω.

$$E = \frac{1}{2} \times L \times I_L^2 \times \left(1 - \frac{V_S}{V_S - V_{DS(CL)}}\right) \quad (5.2)$$

The energy, which is converted into heat, is limited by the thermal design of the component. See **Figure 5** for the maximum allowed energy dissipation as function of the load current.

5.1.4 Switching Active Loads

When switching generative or electronic loads such as motors or secondary ECUs which have the ability to feed back voltage disturbances to the OUT pins, special attention is required about the resulting absolute and dynamic voltage V_{DS} between VS pin and OUT pins.

To maintain device functionality it is required to limit the maximum positive or negative slew rate of $V_{DS} = V_S - V_{OUT}$ below $|dV_{DS}/dt|$ (parameter P_4.2.7) .

To ensure turn-ON in normal operation at low battery voltage ($V_{bat} < 8$ V), during turn ON delay $t_{ON(DELAY)}$ (maxium 150 µs after turn-on command), $V_{DS} \geq 2$V has to be ensured. If these conditions are not met, the device may not turn on, and a fault signal will be present on IS pin.

For loads that generate steady or dynamic voltage at the OUT pins which is higher than voltage at VS pin please consider **Chapter 5.1.5**.

5.1.5 Inverse Current Capability

In case of inverse current, meaning a voltage $V_{OUT(INV)}$ at the output higher than the supply voltage V_S, an inverse (negative) load current $I_{L(INV)}$ will flow from output to V_S pin via the body diode of the power transistor (please refer to **Figure 11** and **Figure 13**). In case the IN pin is HIGH, the power DMOS is already activated and will continue to remain in ON state during the inverse event. In case, the input goes from “L” to “H”, the DMOS will be activated even during an inverse event. Under inverse condition, the device is not overtemperature / overload protected. During inverse mode at ON the sense pin will provide a leakage current of less or equal to I_{IS0}. Due to the limited speed of INV comparator, the inverse duration needs to be limited.

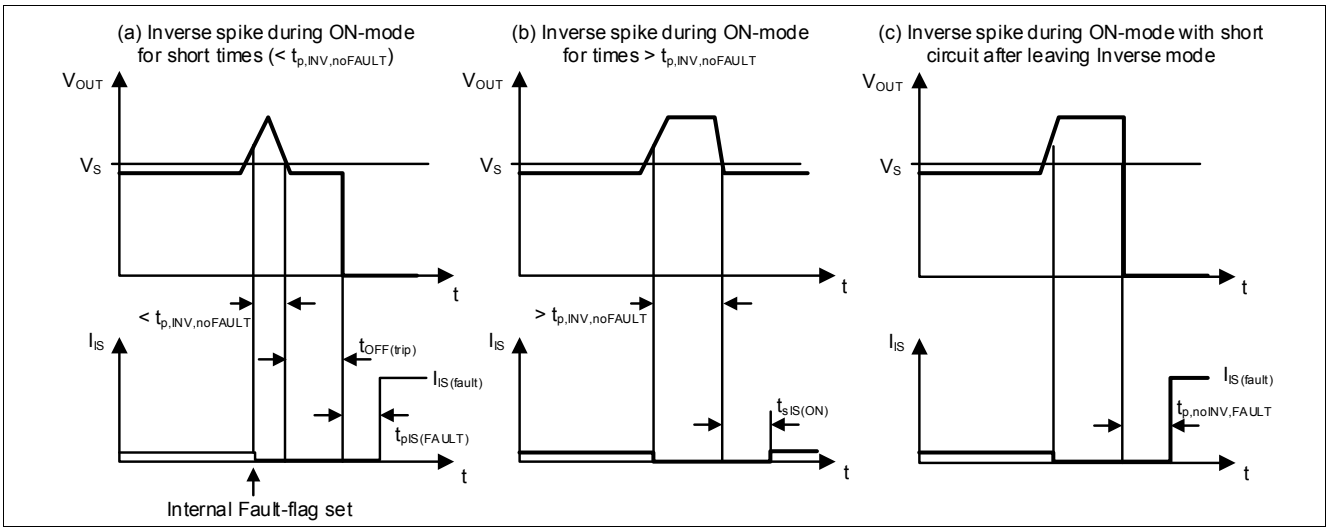


Figure 11 Inverse Behavior - Timing Diagram

5.2 Input Pins

5.2.1 Input Circuitry

The input circuitry is compatible with 3.3 V and 5 V microcontrollers or can be directly driven by V_S. The concept of the input pin is to react to voltage threshold. With the Schmitt trigger, the output is either ON or OFF. **Figure 12** shows the electrical equivalent input circuitry.

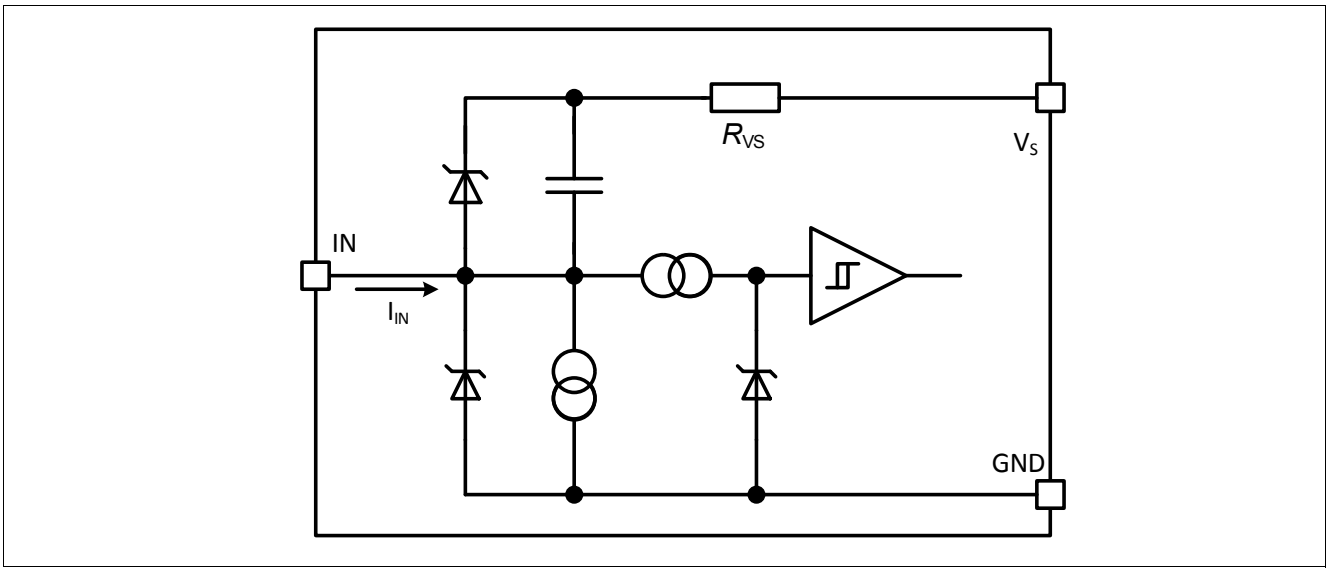


Figure 12 Input Pin Circuitry

5.2.2 Input Pin Voltage

The IN uses a comparator with hysteresis. The switching ON / OFF takes place in a defined region, set by the threshold $V_{IN(L)\ Max}$ and $V_{IN(H)\ Min.}$ The exact value where ON and OFF take place depends on the process, as well as the temperature. To avoid cross talk and parasitic turn ON and OFF, an hysteresis is implemented. This ensures immunity to noise.

5.3 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent the destruction of the IC from fault conditions described in the Data Sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are designed neither for continuous nor for repetitive operation.

Figure 13 describes the typical functionality of the diagnosis and protection block.

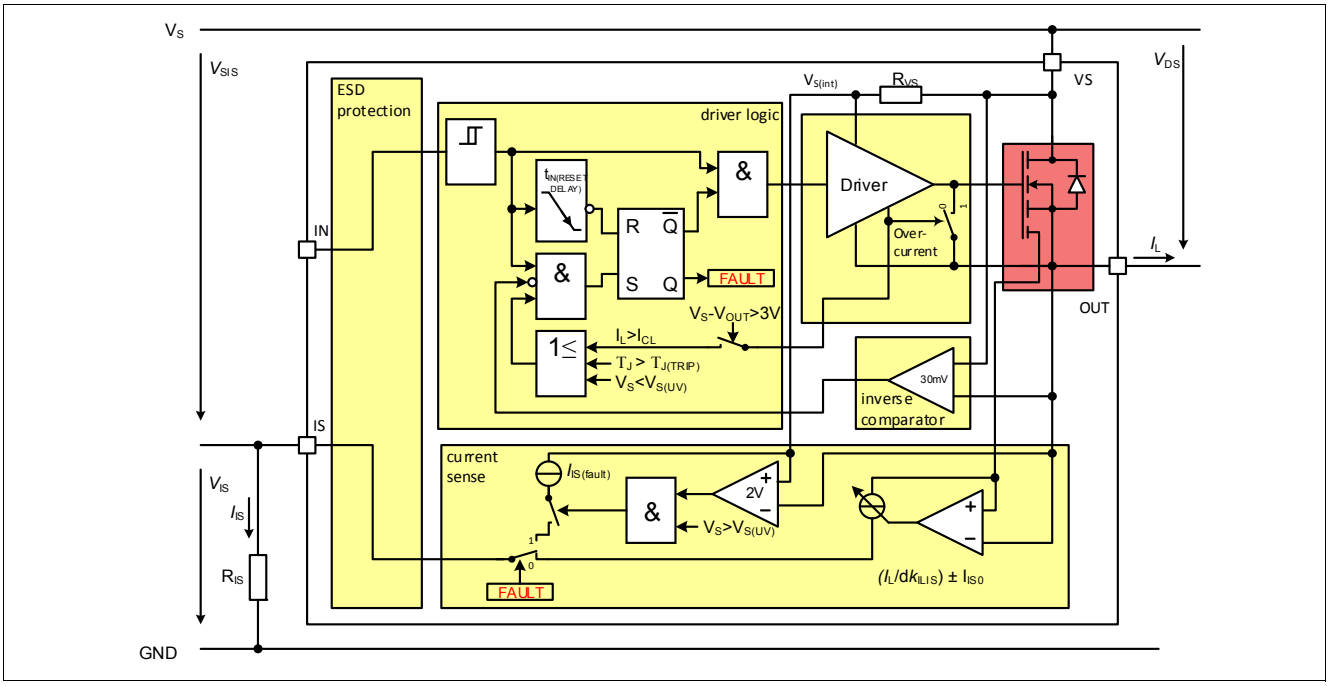


Figure 13 Diagram of Diagnosis & Protection Block

5.3.1 Loss of Ground Protection

In case of loss of module or device ground, where the load remains connected to ground, the device protects itself by automatically turning OFF (when it was previously ON) or remains OFF, regardless of the voltage applied at IN pin. It is recommended to use input resistors between the microcontroller and the BTS50010-1TAE to ensure switching OFF of channel. In case of loss of module or device ground, a current ($I_{OUT(GND)}$) can flow out of the DMOS. **Figure 14** sketches the situation.

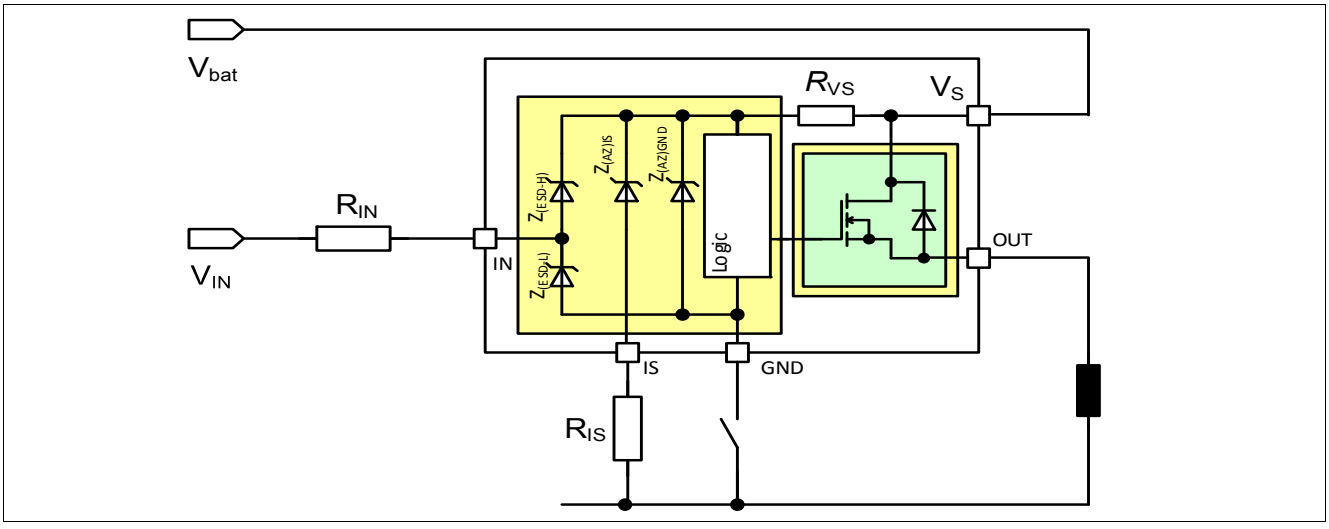


Figure 14 Loss of Ground Protection with External Components

5.3.2 Protection during Loss of Load or Loss of V_S Condition

In case of loss of load with charged primary inductances the supply voltage transient has to be limited. It is recommended to use a Zener diode, a varistor or V_S clamping power switches with connected loads in parallel. The voltage must be limited according to the minimum value of the parameter 6.1.33 indicated in **Table 6**.

In case of loss of V_S connection with charged inductive loads, a current path with sufficient load current capability has to be provided, to demagnetize the charged inductances. It is recommended to protect the device using a Zener diode together with a diode ($V_{Z1} + V_{D1} < 16$ V), with path (A) or path (B) as shown in **Figure 15**.

For a proper restart of the device after loss of V_S, the input voltage must be delayed compared to the supply voltage ramp up. This can be realized by a capacitor between IN and GND (see **Figure 24**).

For higher clamp voltages, currents through all pins have to be limited according to the maximum ratings. Please see **Figure 15** and **Figure 16** for details.

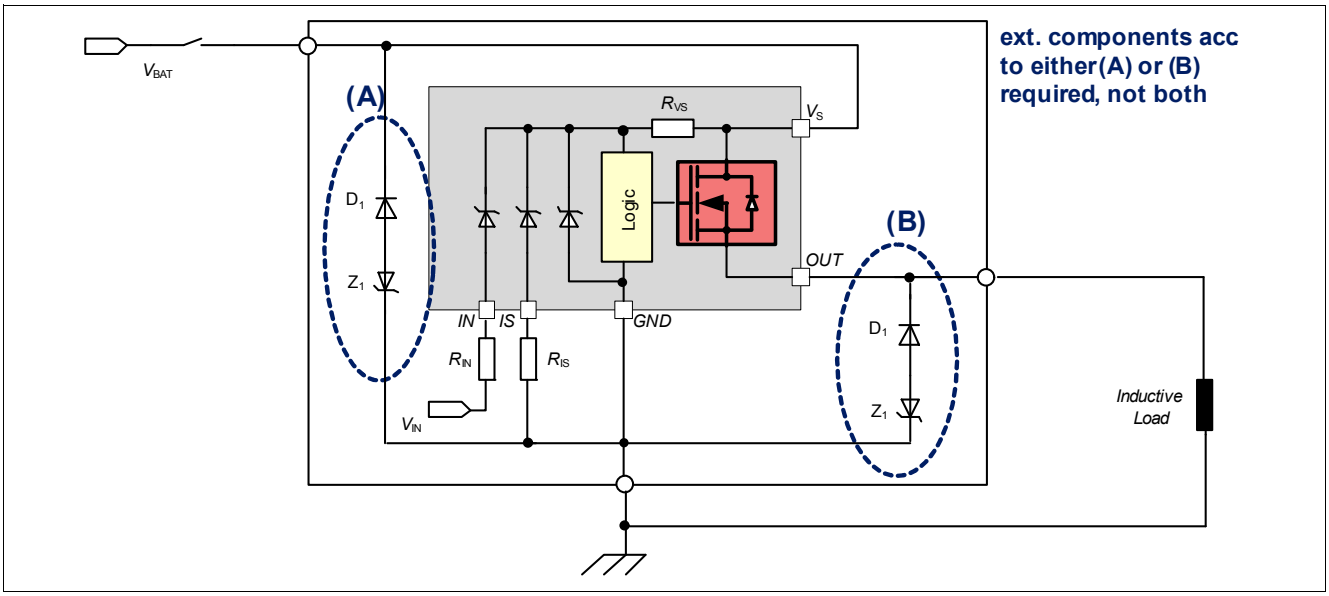


Figure 15 Loss of V_S

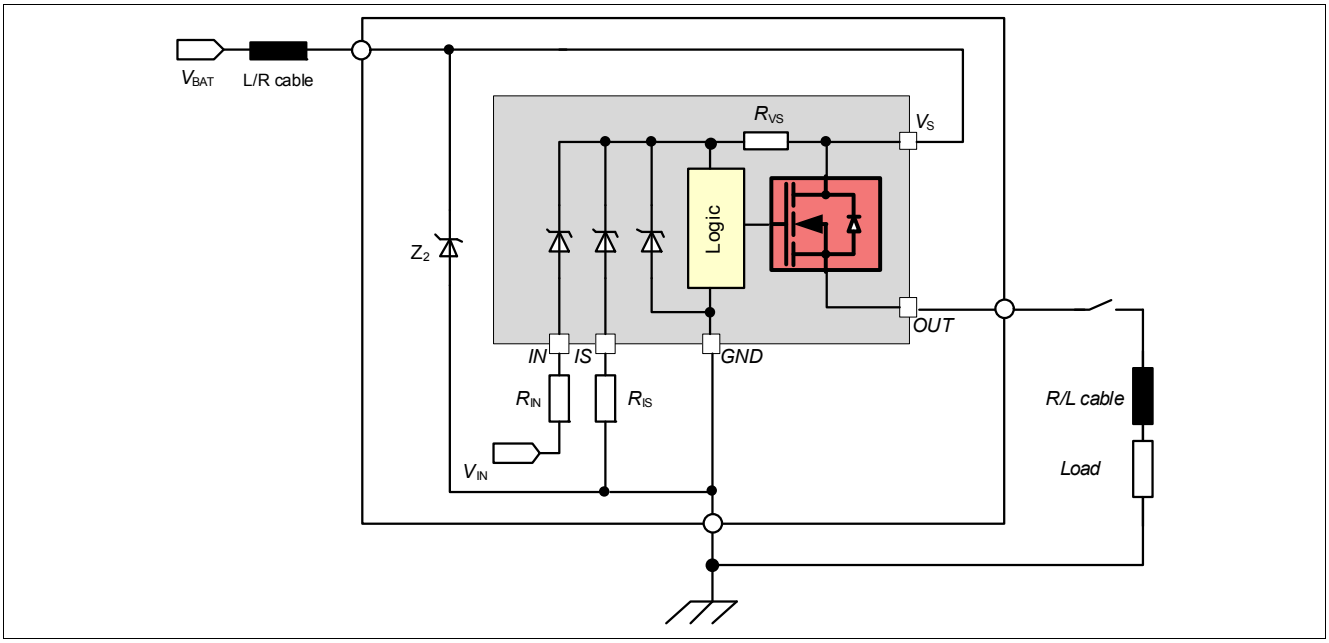


Figure 16 Loss of Load

5.3.3 Undervoltage Behavior

If the device is already ON and the power supply decreases but remains above the $V_{S(UV)}$, no effect is observed and the device keeps on working normally.

If the power supply falls below $V_{S(UV)}$, for more than $t_{FLTR(UV)}$, the devices turns off (undervoltage shutdown). Undervoltage shutdown is latched. When the supply voltage rises higher than the undervoltage restart threshold ($V_{S(UV)} + V_{S(UV)\_HYS}$) after more than $t_{FLTR(UV)}$, the device stays off and provides a FAULT signal on IS pin until the device is reset via pin IN (IN = LOW for $t > t_{IN(RESETDELAY)}$).

*Note: For negative load currents, undervoltage detection is blocked by inverse comparator (see **Chapter 5.1.5**). At low load currents, together with C_{OUT} this may effect undervoltage behavior of the device.*

5.3.4 Overvoltage Protection

In case $V_{S(SC)\_max} < V_S < V_{DS(CL)}$, the device will switch ON/OFF normally as in the nominal voltage range.

Parameters may deviate from the specified limits and lifetime is reduced. This specially impacts the short circuit robustness, as well as the maximum energy E_{AS} and E_{AR} the device can handle.

The BTS50010-1TAE provides Infineon® SMART CLAMPING functionality, which suppresses excessive transient overvoltage by actively clamping the overvoltage across the power stage and the load. This is achieved by controlling the clamp voltage $V_{DS(CL)}$ depending on the junction temperature T_J and the load current I_L (see **Figure 17** for details).

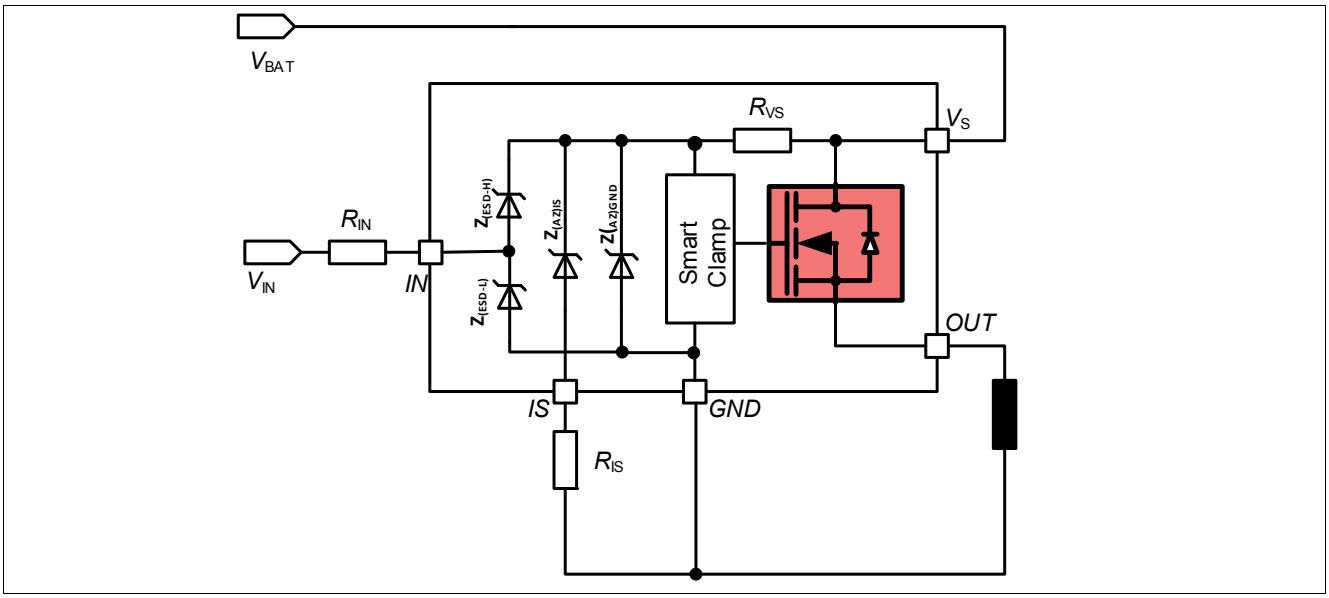


Figure 17 Overvoltage Protection with External Components

5.3.5 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diode of the power DMOS causes power dissipation. To limit the risk of overtemperature, the device provides Infineon® ReverSave™ functionality. The power in this intrinsic body diode is limited by turning the DMOS ON. The DMOS resistance is then equal to $R_{DS(REV)}$.

Additionally, the current into the logic has to be limited. The device includes a R_{VS} resistor which limits the current in the diodes. To avoid overcurrent in the R_{VS} resistor, it is nevertheless recommended to use a R_{IN} resistor. Please refer to maximum current described in **Chapter 4.1**.

Figure 18 shows a typical application.

R_{IS} is used to limit the current in the sense transistor, which behaves as a diode.

The recommended typical value for R_{IN} is 4.7 kΩ and for R_{IS} 1 kΩ.

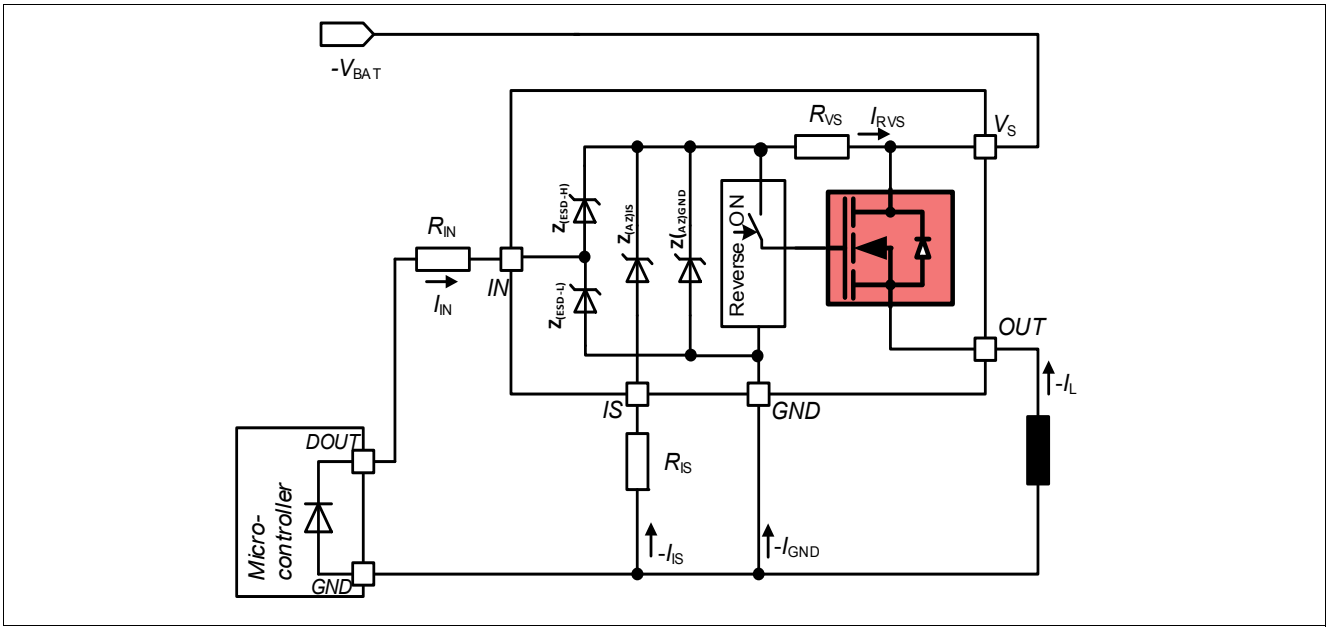


Figure 18 Reverse Polarity Protection with External Components

5.3.6 Overload Protection by Short Circuit Shutdown

In case of overload, high inrush current or short circuit to ground, the BTS50010-1TAE offers several protection mechanisms. Any protective switch OFF latches the output. To restart the device, it is necessary to set IN = LOW for $t > t_{IN(RESETDELAY)}$. This behavior is known as latch behavior. **Figure 19** gives a sketch of the situation.

For overload (short circuit or overtemperature), the maximum retry frequency (f_{fault}) under fault condition must be considered.

When the switch is activated into short circuit (short circuity type1, SC1), the current will raise until reaching the $I_{CL(0)}$ value (SC1). After $t_{OFF(TRIP)}$, the device will turn OFF.

When the device is already in ON state and a short circuit to ground appears at the output (short circuit type 2, SC2) with an overcurrent higher than $I_{CL(0)}$ for a time longer than $t_{OFF(TRIP)}$, the device automatically turns OFF, too.

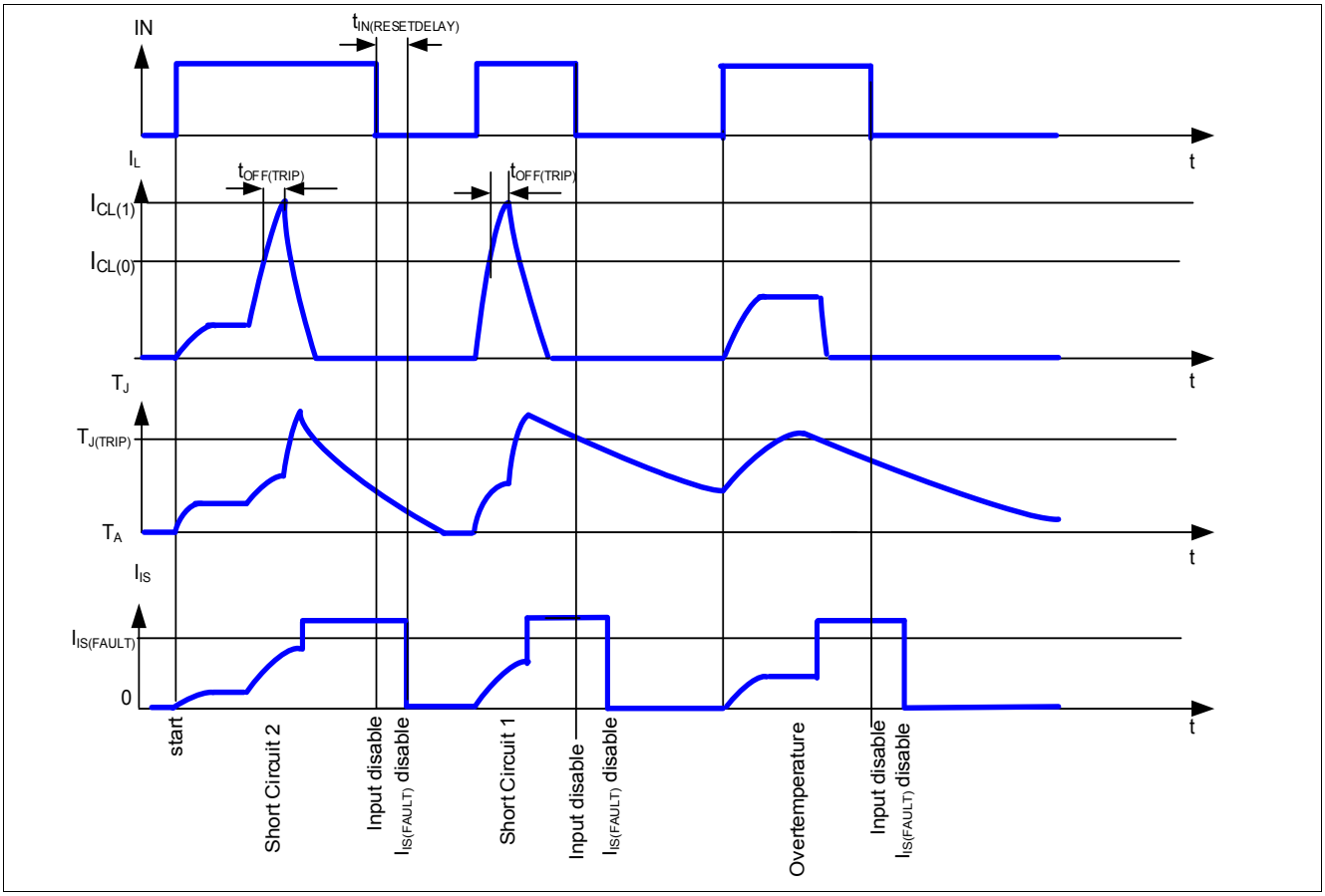


Figure 19 Overload Protection

The capability of the BTS50010-1TAE to handle single short circuit events depends on the battery voltage as well as on the impedance of the remaining circuit connected to the device (see **Chapter 4.1** for maximum ratings and **Figure 24** for R_{supply}, L_{supply}, R_{cable}, L_{cable}).

5.3.7 Temperature Limitation in the Power DMOS

The BTS50010-1TAE incorporates an absolute ($T_{J(TRIP)}$) temperature sensor. Activation of the sensor will cause an overheated channel to switch OFF to prevent destruction. The device restarts when the IN pin is set to low for $t > t_{IN(RESETDELAY)}$ and the temperature has decreased below $T_{J(TRIP)} - \Delta T_{J(TRIP)}$.

The current sense exact signal timing can be found in the **Chapter 5.4**. It is represented here only for device's behavior understanding.

In order to allow the device to detect overtemperature conditions and react effectively, it is recommended to limit the power dissipation below P_{TOT} (parameter 4.1.15).

5.4 Diagnostic Functions

For diagnosis purposes, the BTS50010-1TAE provides a combination of digital and analog signal at pin IS.

5.4.1 IS Pin

The BTS50010-1TAE provides an enhanced current sense signal called I_{IS} at pin IS. As long as no "hard" failure mode occurs (short circuit to GND / overcurrent / overtemperature / undervoltage) and the condition $V_{IS} \leq V_{OUT} - 5\,V$ is fulfilled, a proportional signal to the load current is provided. The complete IS pin and diagnostic mechanism is described in **Figure 20**. The accuracy of the sense current depends on temperature

and load current. In case of failure, a fixed $I_{IS(FAULT)}$ is provided. In order to enable the fault current reporting, the condition V_S - V_{OUT} > 2 V must be fulfilled. In order to get the fault current in the specified range, the condition V_S - V_{IS} ≥ 5 V must be fulfilled.

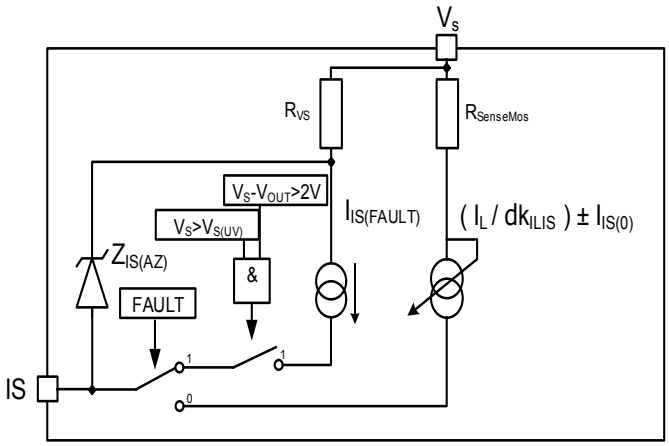


Figure 20 Diagnostic Block Diagram

5.4.2 SENSE Signal in Different Operation Modes

Table 5 Sense Signal, Function of Operation Mode[1)]

Operation mode	Input Level	Output Level V_{OUT}	Diagnostic Output (IS)[2)]
Normal operation	LOW (OFF)	~ GND	$I_{IS(OFF)}$
Short circuit to GND		GND	$I_{IS(OFF)}$
Overtemperature		~ GND	$I_{IS(OFF)}$
Short circuit to VS		V_S	$I_{IS(OFF)}$
Open Load		Z	$I_{IS(OFF)}$
Inverse current		> V_S	$I_{IS(OFF)}$
Normal operation	HIGH (ON)	~ V_S	$I_{IS} = (I_L / dk_{ILIS}) \pm I_{IS0}$
Overcurrent condition		< V_S	$I_{IS} = (I_L / dk_{ILIS}) \pm I_{IS0}$ or $I_{IS(FAULT)}$
Short circuit to GND		GND	$I_{IS(FAULT)}$
Overtemperature (after the event)		~ GND	$I_{IS(FAULT)}$
Short circuit to VS		V_S	$I_{IS} < I_L / dk_{ILIS} \pm I_{IS0}$
Open Load		V_S	I_{IS0}
Inverse current		> V_S	$<I_{IS0}$
Undervoltage		~ GND	$I_{IS(OFF)}$
After undervoltage shutdown		~ GND	$I_{IS(FAULT)}$

1) Z = High Impedance

2) See **Chapter 5.4.3** for Current Sense Range and Improved Current Sense Accuracy.

5.4.3 SENSE Signal in the Nominal Current Range

Figure 21 and **Figure 22** show the current sense as function of the load current in the power DMOS. Usually, a pull-down resistor R_{IS} is connected to the current sense pin IS. A typical value is 1 kΩ. The dotted curve

represents the typical sense current, assuming a typical dk_{ILIS} factor value. The range between the two solid curves shows the sense accuracy range that the device is able to provide, at a defined current.

$$I_{IS} = \frac{I_L}{dk_{ILIS}} + I_{IS0} \text{ with } (I_{IS} \geq 0) \tag{5.3}$$

where the definition of dk_{ILIS} is:

$$dk_{ILIS} = \frac{I_{L4} - I_{L1}}{I_{IS4} - I_{IS1}} \tag{5.4}$$

and the definition of I_{IS0} is:

$$I_{IS0} = I_{IS1} - \frac{I_{L1}}{dk_{ILIS}} \tag{5.5}$$

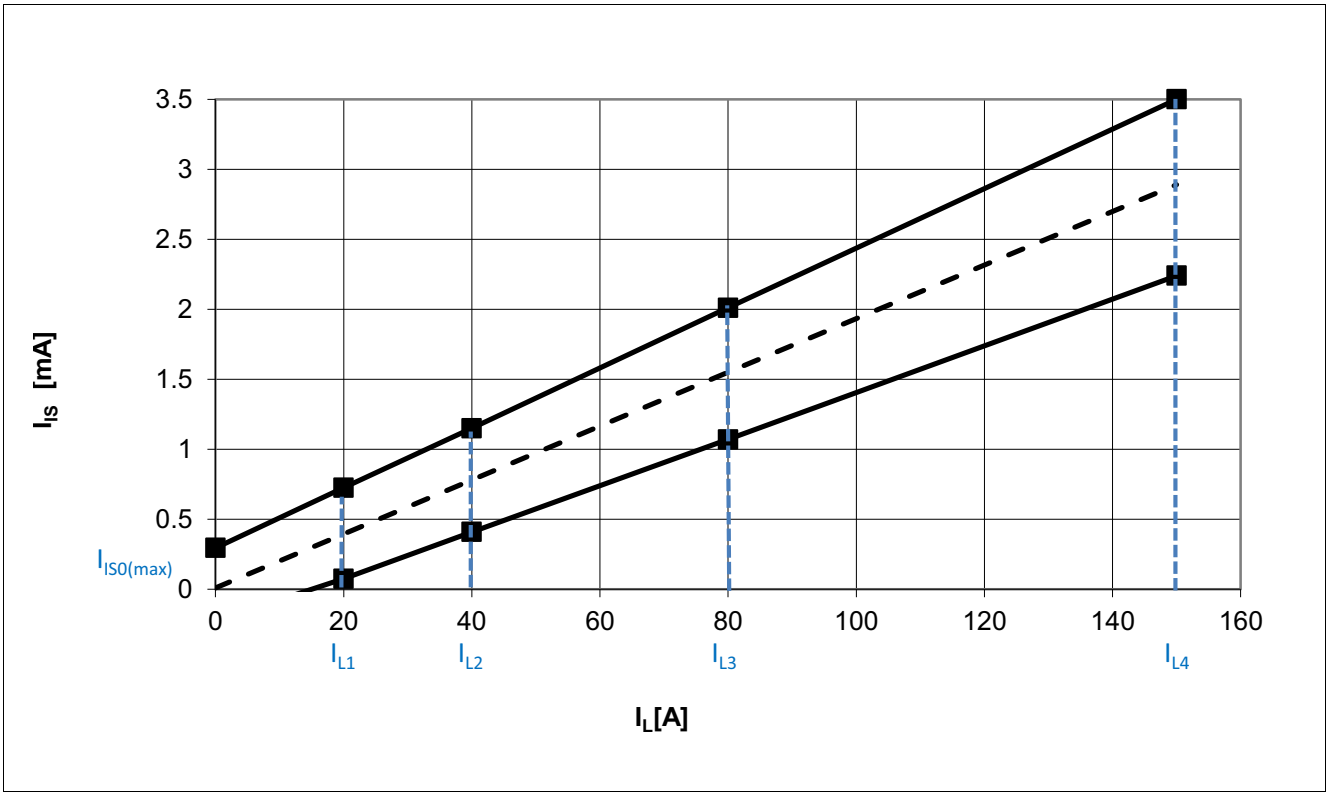


Figure 21 Current Sense for Nominal and Overload Condition

5.4.3.1 SENSE Signal Variation and Calibration

In some applications, an enhanced accuracy is required around the device nominal current range $I_{L(NOM)}$. To achieve this accuracy requirement, a calibration on the application is possible. After two point calibration, the BTS50010-1TAE will have a limited I_{IS} value spread at different load currents and temperature conditions. The I_{IS} variation can be described with the parameters $\Delta(dk_{ILIS(cal)})$ and the $\Delta I_{IS0(cal)}$. The blue solid line in **Figure 22**

is the current sense ratio after the two point calibration at a given temperature. The slope of this line is defined as follows:

$$\frac{1}{dk_{ILIS(cal)}} = \frac{I_{IS(cal)2} - I_{IS(cal)1}}{I_{L(cal)2} - I_{L(cal)1}} \tag{5.6}$$

The offset is defined as follows:

$$I_{IS0(cal)} = I_{IS(cal)1} - \frac{I_{L(cal)1}}{dk_{ILIS(cal)}} = I_{IS(cal)2} - \frac{I_{L(cal)2}}{dk_{ILIS(cal)}} \tag{5.7}$$

The bluish area in **Figure 22** is the range where the current sense ratio can vary across temperature and load current after performing the calibration. The accuracy of the load current sensing is improved and, given a sense current value I_{IS} (measured in the application), the load current can be calculated as follow, using the absolute value for $\Delta(dk_{ILIS(cal)})$ instead of % values:

$$I_L = dk_{ILIS(cal)} \times \left(1 + \Delta(dk_{ILIS(cal)})\right) \times \left(I_{IS} - I_{IS0(cal)} - \Delta I_{IS0(cal)}\right) \tag{5.8}$$

where $dk_{ILIS(cal)}$ is the current sense ratio measured after two-points calibration (defined in **Equation (5.6)**), $I_{IS0(cal)}$ is the current sense offset (calculated after two points calibration, see **Equation (5.7)**), and $\Delta I_{IS0(cal)}$ is the additional variation of the individual offset over life time and temperature. For a calibration at 25°C $\Delta I_{IS0(cal)}$ varies over temperature and life time for all positive $\Delta I_{IS0(cal)}$ within the differences of the temperature dependent Max. limits. All negative $\Delta I_{IS0(cal)}$ vary within the differences of the temperature dependent Min. limits.

For positive $I_{IS0(cal)}$ values ($I_{IS0(cal)} > 0$):

$$\text{Max } I_{IS0}\ (@T_J = 150°C) - \text{Max } I_{IS0}\ (@T_J = 25°C) \le \Delta I_{IS0(cal)} \le \text{Max } I_{IS0}\ (@T_J = -40°C) - \text{Max } I_{IS0}\ (@T_J = 25°C) \tag{5.9}$$

For negative $I_{IS0(cal)}$ values ($I_{IS0(cal)} < 0$):

$$\text{Min } I_{IS0}\ (@T_J = 150°C) - \text{Min } I_{IS0}\ (@T_J = 25°C) \ge \Delta I_{IS0(cal)} \ge \text{Min } I_{IS0}\ (@T_J = -40°C) - \text{Min } I_{IS0}\ (@T_J = 25°C) \tag{5.10}$$

Equation (5.8) actually provides four solutions for load current, considering that $\Delta(dk_{ILIS(cal)})$ and $\Delta I_{IS0(cal)}$ can be both positive and negative. The load current I_L for any sense current I_{IS} will spread between a minimum I_L value resulting from the combination of lowest $\Delta(dk_{ILIS(cal)})$ value and highest $\Delta I_{IS0(cal)}$ and a maximum I_L value resulting from the combination of highest $\Delta(dk_{ILIS(cal)})$ value and lowest $\Delta I_{IS0(cal)}$.

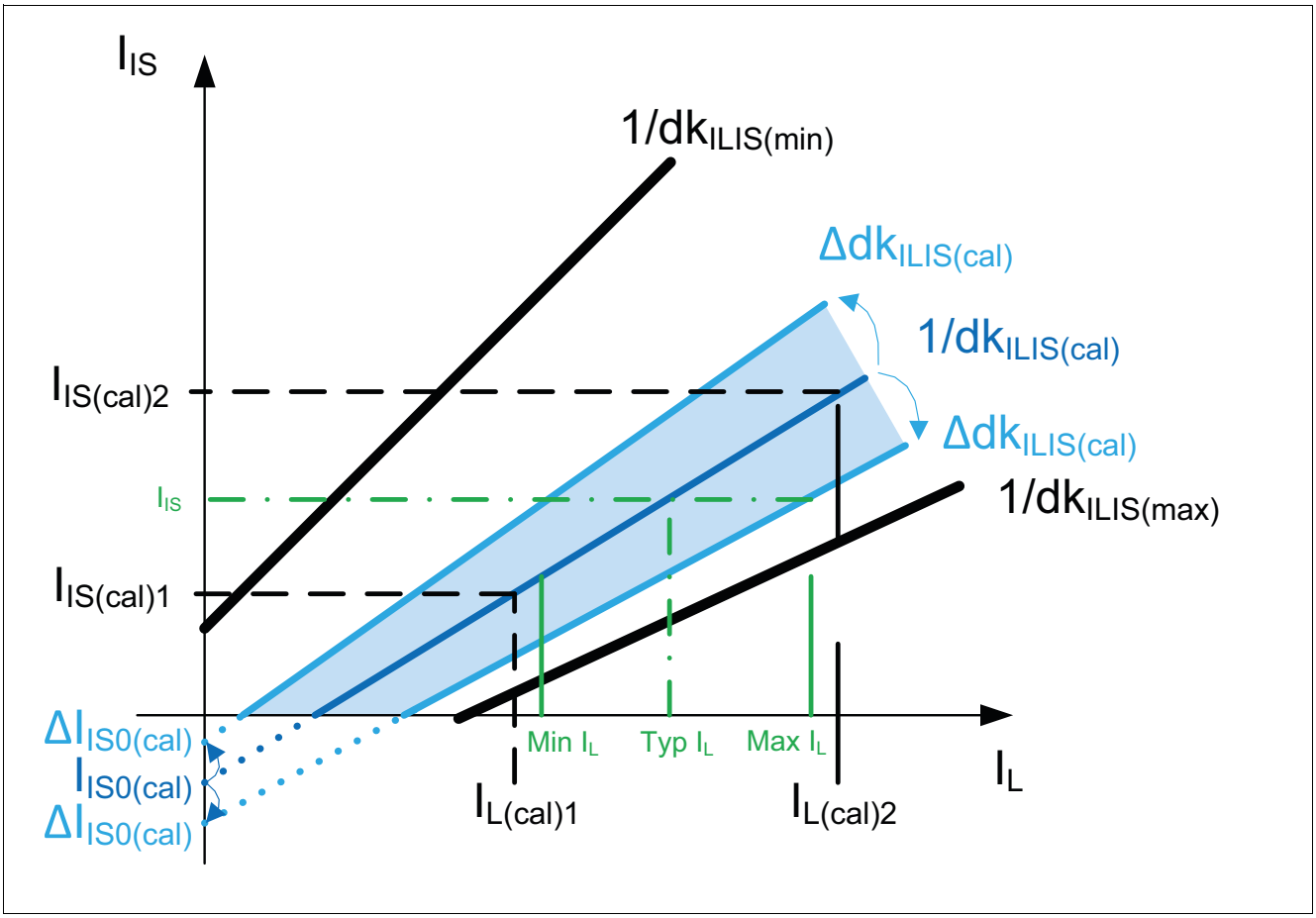


Figure 22 Improved Current Sense Accuracy after 2-Point Calibration

5.4.3.2 SENSE Signal Timing

Figure 23 shows the timing during settling and disabling of the sense.

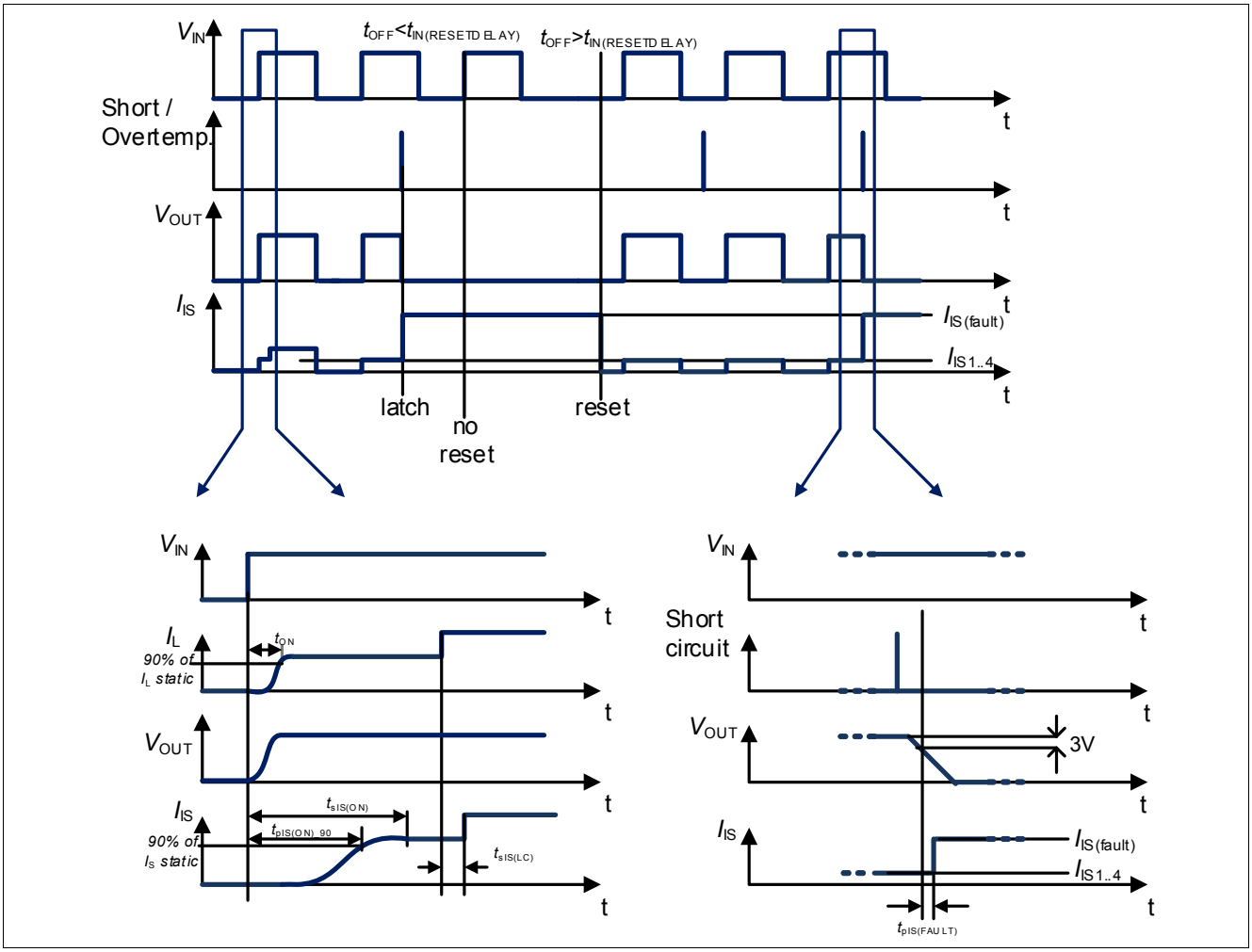


Figure 23 Fault Acknowledgement

5.4.3.3 SENSE Signal in Case of Short Circuit to V_S

In case of a short circuit between OUT and VS, a major part of the load current will flow through the short circuit. As a result, a lower current compared to the nominal operation will flow through the DMOS of the BTS50010-1TAE, which can be recognized at the current sense signal.

5.4.3.4 SENSE Signal in Case of Over Load

An over load condition is defined by a current flowing out of the DMOS reaching the current over load I_{CL} or the junction temperature reaches the thermal shutdown temperature $T_{J(TRIP)}$. Please refer to **Chapter 5.3.6** for details. In that case, the SENSE signal will be in the range of $I_{IS(FAULT)}$ when the IN pin stays HIGH.

This is a device with latch functionality. The state of the device will remain and the sense signal will remain on $I_{IS(FAULT)}$ until a reset signal comes from the IN pin. For example, when a thermal shutdown occurs, even when the over temperature condition has disappeared, the DMOS can only be reactivated when a reset signal is sent to the IN pin.

6 Electrical Characteristics BTS50010-1TAE

6.1 Electrical Characteristics Table

Table 6 Electrical Characteristics: BTS50010-1TAE

V_S = 8 V to 18 V, T_J = -40°C to +150°C (unless otherwise specified)
For a given temperature or voltage range, typical values are specified at V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Operating and Standby Currents							
Operating Current (Channel Active)	$I_{GND(ACTIVE)}$	–	1.2	3	mA	$V_{IN} \geq$ 2.2 V	P_6.1.1
Standby Current for Whole Device with Load	$I_{VS(OFF)}$	–	8	18	µA	[1] V_S = 18 V V_{OUT} = 0 V $V_{IN} \leq$ 0.8 V $T_J \leq$ 85°C See **Page 35**	P_6.1.2
Maximum Standby Current for Whole Device with Load	$I_{VS(OFF)}$	–	22	130	µA	V_S = 18 V V_{OUT} = 0 V $V_{IN} \leq$ 0.8 V $T_J \leq$ 150°C See **Page 35**	P_6.1.3
Power Stage							
ON-State Resistance in Forward Condition	$R_{DS(ON)}$	–	1.6	2.1	mΩ	I_L = 150 A $V_{IN} \geq$ 2.2 V T_J = 150°C See **Page 36**	P_6.1.4
ON-State Resistance in Forward Condition, Low Battery Voltage	$R_{DS(ON)}$	–	2	3.2	mΩ	I_L = 20 A $V_{IN} \geq$ 2.2 V V_S = 5.5 V T_J = 150°C See **Page 36**	P_6.1.5
ON-State Resistance in Forward Condition	$R_{DS(ON)}$	–	1.0	–	mΩ	[1] I_L = 150 A $V_{IN} \geq$ 2.2 V T_J = 25°C See **Page 36**	P_6.1.6
ON-State Resistance in Inverse Condition	$R_{DS(INV)}$	–	1.6	2.1	mΩ	I_L = -150 A $V_{IN} \geq$ 2.2 V T_J = 150°C See **Figure 13**	P_6.1.7
ON-State Resistance in Inverse Condition	$R_{DS(INV)}$	–	1.0	–	mΩ	[1] I_L = -150 A $V_{IN} \geq$ 2.2 V T_J = 25°C See **Figure 20**	P_6.1.8

Table 6 Electrical Characteristics: BTS50010-1TAE (cont'd)

V_S = 8 V to 18 V, T_J = -40°C to +150°C (unless otherwise specified)
For a given temperature or voltage range, typical values are specified at V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Nominal Load Current	$I_{L(NOM)}$	40	48	–	A	T_A = 85°C[2)] $T_J \leq$ 150°C	P_6.1.9
Drain to Source Smart Clamp Voltage $V_{DS(CL)} = V_S - V_{OUT}$	$V_{DS(CL)}$	28	–	46	V	I_{DS} = 50 mA See **Page 38**	P_6.1.11
Output Leakage Current	$I_{L(OFF)}$	–	3	15	µA	[1)]$V_{IN} \leq$ 0.8 V V_{OUT} = 0 V $T_J \leq$ 85°C	P_6.1.13
Output Leakage Current	$I_{L(OFF)}$	–	20	110	µA	$V_{IN} \leq$ 0.8 V V_{OUT} = 0 V T_J = 150°C	P_6.1.14
Turn ON Slew Rate V_{OUT} = 25% to 50% V_S	dV_{ON}/dt	0.05	0.23	0.5	V/µs	R_L = 0.5 Ω V_S = 13.5 V See **Figure 8** See **Page 36**	P_6.1.15
Turn OFF Slew Rate V_{OUT} = 50% to 25% V_S	$-dV_{OFF}/dt$[1)]	–	10	–	V/µs		P_6.1.16
Turn ON Time to V_{OUT} = 90% V_S	t_{ON}	–	175	700	µs		P_6.1.17
Turn OFF Time to V_{OUT} = 10% V_S	t_{OFF}	–	260	735	µs		P_6.1.18
Turn ON Time to V_{OUT} = 10% V_S	$t_{ON(DELAY)}$	–	60	150	µs		P_6.1.19
Turn OFF Time to V_{OUT} = 90% V_S	$t_{OFF(DELAY)}$	–	230	520	µs	R_L = 0.5 Ω V_S = 13.5 V See **Figure 8** See **Page 36**	P_6.1.20
Input Pin							
LOW Level Input Voltage	$V_{IN(L)}$	–	–	0.8	V	See **Page 38**	P_6.1.23
HIGH Level Input Voltage	$V_{IN(H)}$	2.2	–	–	V		P_6.1.24
Input Voltage Hysteresis	$V_{IN(HYS)}$[1)]	–	200	–	mV		P_6.1.25
LOW Level Input Current	$I_{IN(L)}$	8	–	–	µA	V_{IN} = 0.8 V	P_6.1.26
HIGH Level Input Current	$I_{IN(H)}$	–	–	80	µA	$V_{IN} \geq$ 2.2 V	P_6.1.27
Protection							
Output Leakage Current while Module GND Disconnected	$I_{OUT(GND\_M)}$	0	20	110	µA	[1)3)]V_S = 18 V V_{OUT} = 0 V IS, IN and GND pin open T_J = 150°C See **Figure 14**	P_6.1.28

Table 6 Electrical Characteristics: BTS50010-1TAE (cont'd)

V_S = 8 V to 18 V, T_J = -40°C to +150°C (unless otherwise specified)
For a given temperature or voltage range, typical values are specified at V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Leakage Current While Device GND Disconnected	$I_{OUT(GND)}$	0	20	110	µA	V_S = 18 V GND pin open V_{IN} ≥ 2.2 V 1 kΩ pull down from IS to GND 4.7 kΩ to IN pin T_J = 150°C See **Figure 14** See **Page 39**	P_6.1.29
ON-State Resistance in Reverse Polarity	$R_{DS(REV)}$	–	–	2.2	mΩ	V_S = 0 V V_{GND} = V_{IN} = 16 V I_L = -20 A T_J = 150°C See **Figure 18**	P_6.1.30
ON-State Resistance in Reverse Polarity	$R_{DS(REV)}$	–	1.1	–	mΩ	[1] V_S = 0 V V_{GND} = V_{IN} = 16 V I_L = -20 A T_J = 25°C See **Page 39**	P_6.1.31
Integrated Resistor	R_{VS}	–	60	90	Ω	T_J = 25°C	P_6.1.32
Overvoltage Protection V_S to GND Pin	$V_{S(AZ)\_GND}$	64	70	80	V	See **Figure 17** See **Page 38**	P_6.1.33
Overvoltage Protection V_S to IS Pin	$V_{S(AZ)\_IS}$	64	70	80	V	GND and IN pin open See **Figure 17** See **Page 38**	P_6.1.34
Undervoltage shutdown V_S to GND Pin	$V_{S(UV)}$	4.5	5	5.5	V	I_L ≥ 6 A	P_6.1.10
Undervoltage shutdown hysteresis	$V_{S(UV)\_HYS}$	–	0.2	–	V	–	P_6.1.54
Undervoltage shutdown filter time	$t_{FLTR(UV)}$	–	20	–	µs	[1]	P_6.1.59
Current Trip Detection Level	$I_{CL(0)}$	250	285	–	A	V_S = 13.5 V, static T_J = 150°C See **Figure 19**	P_6.1.35
	$I_{CL(0)}$	250	315	–	A	V_S = 13.5 V, static T_J = -40 ... 25°C See **Figure 19**	
Current Trip Peak Level	$I_{CL(1)}$	–	335	425	A	[1] V_S = 13.5 V dI_L/dt = 1 A/µs See **Page 39**	

Table 6 Electrical Characteristics: BTS50010-1TAE (cont'd)

V_S = 8 V to 18 V, T_J = -40°C to +150°C (unless otherwise specified)
For a given temperature or voltage range, typical values are specified at V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overload Shutdown Delay Time	$t_{OFF(TRIP)}$	–	20	–	µs	1)	P_6.1.36
Thermal Shutdown Temperature	$T_{J(TRIP)}$	150	170[1)]	200[1)]	°C	See **Figure 19**	P_6.1.37
Thermal Shutdown Hysteresis	$\Delta T_{J(TRIP)}$	–	10	–	K	1)	P_6.1.38
Diagnostic Functions							
Sense Signal Current in Fault Condition	$I_{IS(FAULT)}$	3.5	6	8	mA	1) V_{IN} = 4.5 V V_S - V_{IS} ≥ 5 V	P_6.1.40
Sense Signal Saturation Current	$I_{IS(LIM)}$	3.5	6	8	mA	1) V_{IN} = 4.5 V V_S - V_{IS} ≥ 5 V	P_6.1.57
Current Sense Differential Ratio	dk_{ILIS}	44500	52100	59100	–	I_{L4} = 150 A I_{L1} = 20 A See **Equation (5.4)**	P_6.1.41
Calculated Sense Offset Current $I_L = I_{L0}$ = 0 A	I_{IS0}	-235	20	274	µA	4) V_{IN} ≥ 2.2 V V_S - V_{IS} ≥ 5 V T_J = -40°C See **Figure 21**	P_6.1.42
	I_{IS0}	-162	8	180	µA	1)4) V_{IN} ≥ 2.2 V V_S - V_{IS} ≥ 5 V T_J = 25°C See **Figure 21**	
	I_{IS0}	-88	-4	80	µA	4) V_{IN} ≥ 2.2 V V_S - V_{IS} ≥ 5 V T_J = 150°C See **Figure 21**	
Sense Current $I_L = I_{L1}$ = 20 A	I_{IS1}	103	392	702	µA	V_{IN} ≥ 2.2 V V_S - V_{IS} ≥ 5 V See **Figure 21**	P_6.1.43
Sense Current $I_L = I_{L2}$ = 40 A	I_{IS2}	442	776	1131	µA	1) V_{IN} ≥ 2.2 V V_S - V_{IS} ≥ 5 V See **Figure 21**	P_6.1.44
Sense Current $I_L = I_{L3}$ = 80 A	I_{IS3}	1.12	1.54	1.99	mA	1) V_{IN} ≥ 2.2 V V_S - V_{IS} ≥ 5 V See **Figure 21**	P_6.1.45
Sense Current $I_L = I_{L4}$ = 150 A	I_{IS4}	2.30	2.89	3.49	mA	V_{IN} ≥ 2.2 V V_S - V_{IS} ≥ 5 V See **Figure 21**	P_6.1.46

Table 6 Electrical Characteristics: BTS50010-1TAE (cont'd)

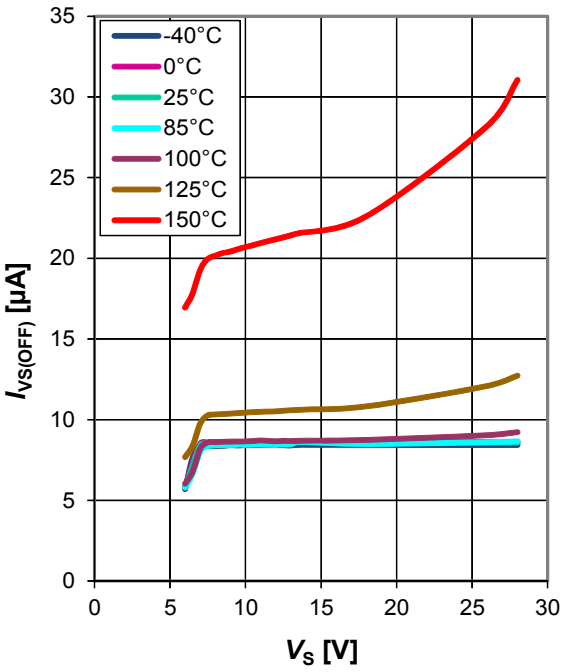
V_S = 8 V to 18 V, T_J = -40°C to +150°C (unless otherwise specified)
For a given temperature or voltage range, typical values are specified at V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Sense Ratio Spread between -40°C and 25°C for Repetitive Operation	$\Delta(dk_{ILIS(cal)(-40°C)})$	-3	–	4.5	%	1) $dk_{ILIS(cal)(-40°C)}/dk_{ILIS(cal)(25°C)}$) See **Figure 22** See **Page 40**	P_6.1.12
Current Sense Ratio Spread between 150°C and 25°C for Repetitive Operation	$\Delta(dk_{ILIS(cal)(150°C)})$	-8.5	–	-3	%	1) $dk_{ILIS(cal)(150°C)}/dk_{ILIS(cal)(25°C)}$) See **Figure 22** See **Page 40**	P_6.1.39
Current Sense Propagation Time until 90% of I_{IS} Stable After Positive Input Slope on IN Pin	$t_{pIS(ON)\_90}$	0	–	700	µs	$V_{IN} \geq 2.2$ V V_S = 13.5 V R_L = 0.5 Ω See **Figure 23**	P_6.1.48
Current Sense Settling Time to I_{IS} Stable after Positive Input Slope on IN Pin	$t_{sIS(ON)}$	–	–	3000	µs	$V_{IN} \geq 2.2$ V V_S = 13.5 V R_L = 0.5 Ω See **Figure 23**	P_6.1.49
I_{IS} Leakage Current when IN Disabled	$I_{IS(OFF)}$	0	0.05	1	µA	$V_{IN} \leq 0.8$ V R_{IS} = 1k Ω	P_6.1.50
Current Sense Settling Time after Load Change	$t_{sIS(LC)}$	–	50	–	µs	1) $V_{IN} \geq 2.2$ V dI_L/dt = 0.4 A/µs	P_6.1.51
Current Sense Propagation Time for Short Circuit Detection	$t_{pIS(FAULT)}$	0	–	100	µs	1) $V_{IN} \geq 2.2$ V from $V_{OUT} = V_S$ - 3 V to $I_{IS(FAULT)\_min}$ See **Figure 23**	P_6.1.52
Delay Time to Reset Fault Signal at IS Pin after Turning OFF V_{IN}	$t_{IN(RESETDELAY)}$	250	1000	1500	µs	1)	P_6.1.53
Timing: Inverse Behavior							
Propagation Time From $V_{OUT} > V_S$ to Fault Disable	$t_{p,INV,noFAULT}$	–	4	–	µs	1) See **Figure 11**	P_6.1.55
Propagation Time from $V_{OUT} < V_S$ to Fault Enable	$t_{p,noINV,FAULT}$	–	10	–	µs	1) See **Figure 11**	P_6.1.56

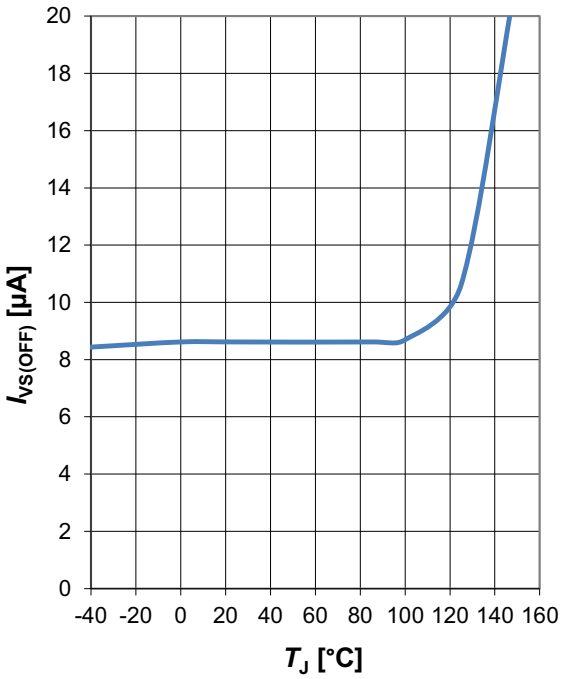
1) Not subject to production test, specified by design.
2) Value is calculated from the parameters typ. $R_{thJA(2s2p)}$, with 65 K temperature increase, typ. and max. $R_{DS(ON)}$.
3) All pins are disconnected except V_S and OUT.
4) Value is calculated from the parameters dk_{ILIS} and I_{IS1}.

6.2 Typical Performance Characteristics

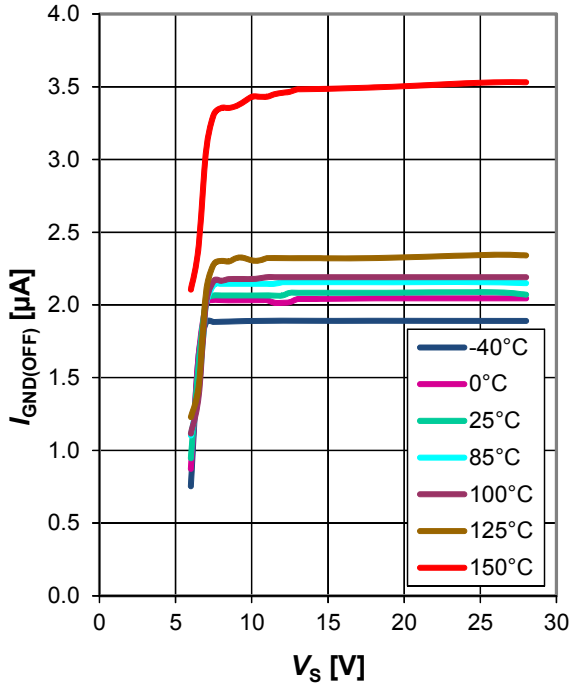
Standby Current for Whole Device with Load, $I_{VS(OFF)} = f(V_S, T_J)$



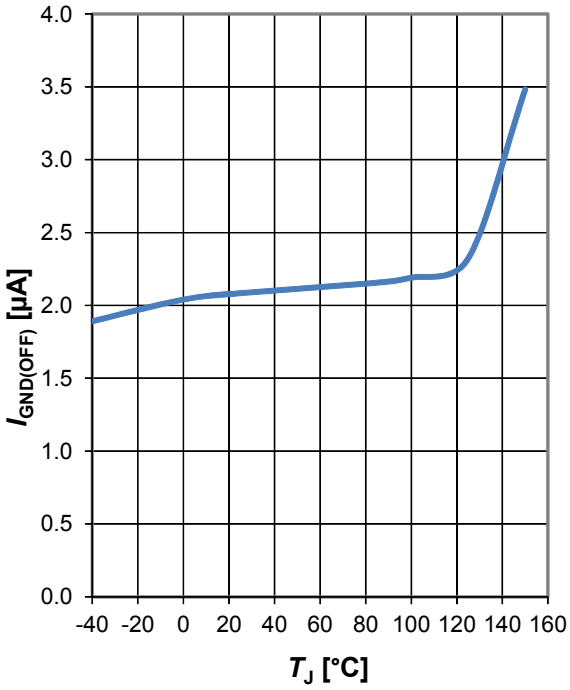
Standby Current for Whole Device with Load, $I_{VS(OFF)} = f(T_J)$ at V_S = 13.5 V



GND Leakage Current $I_{GND(OFF)} = f(V_S, T_J)$

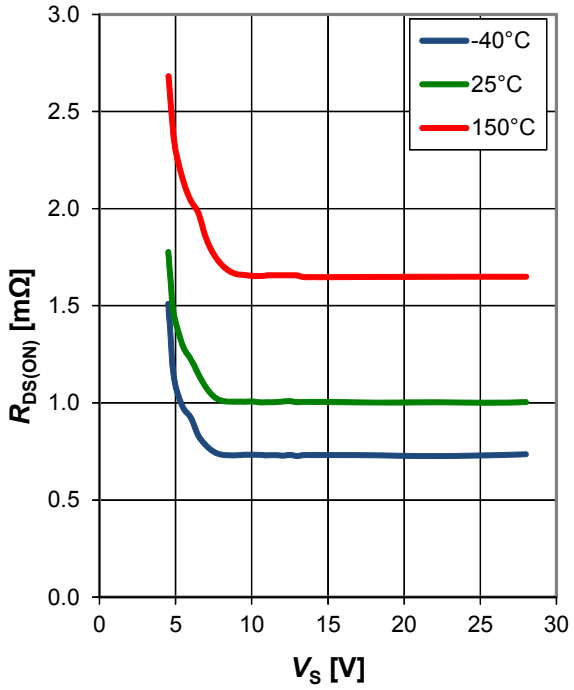


GND Leakage Current $I_{GND(OFF)} = f(T_J)$ at V_S = 13.5 V



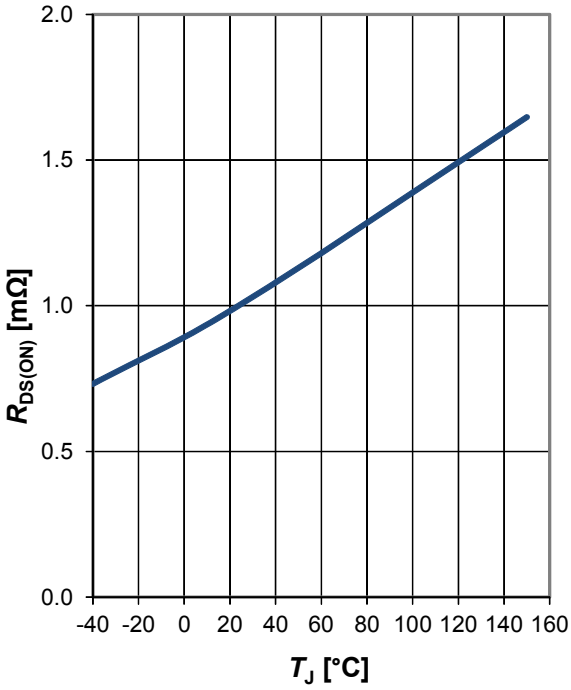
ON State Resistance

$R_{DS(ON)} = f(V_S, T_J)$, I_L = 20 A ... 150 A



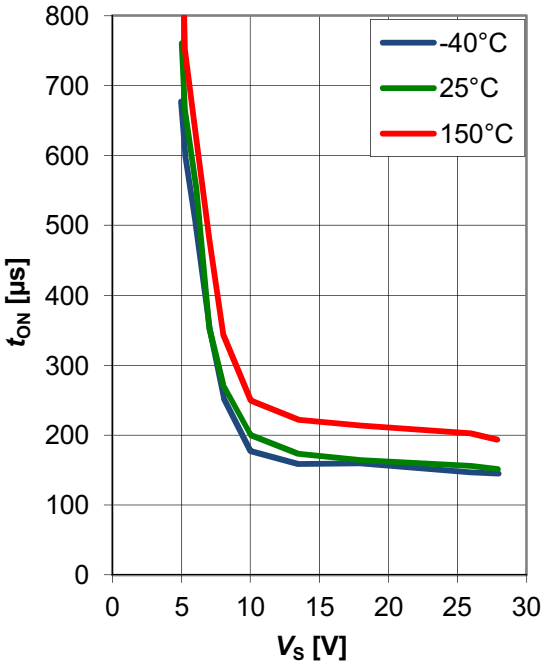
ON State Resistance

$R_{DS(ON)} = f(T_J)$, V_S = 13.5 V, I_L = 20 A ... 150 A



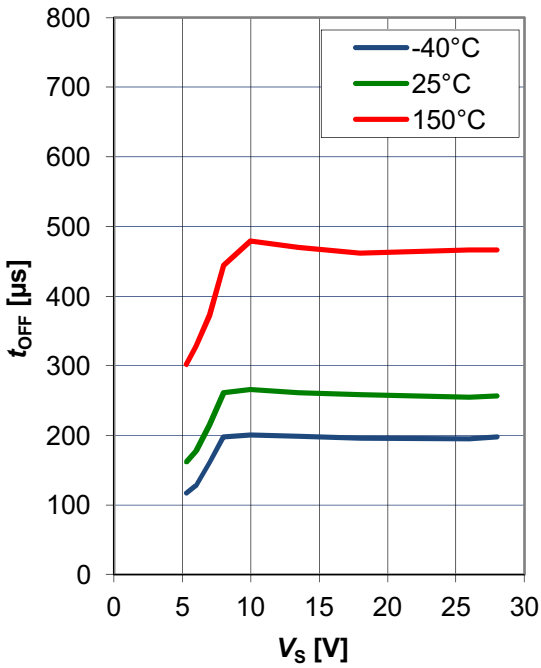
Turn ON Time

$t_{ON} = f(V_S, T_J)$, R_L = 0.5 Ω

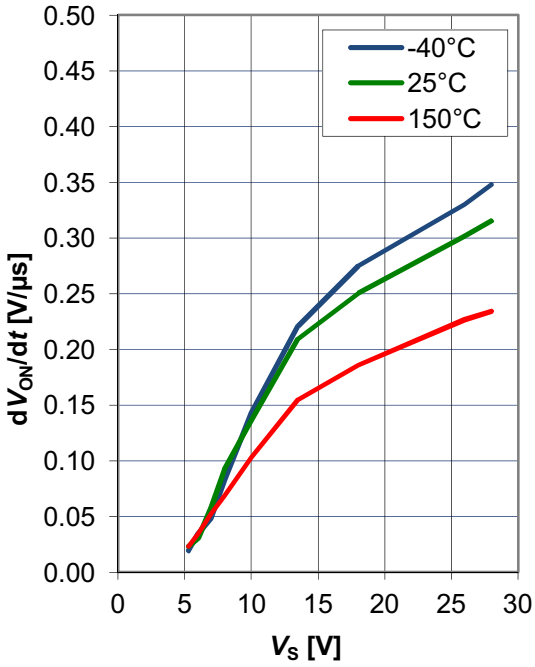


Turn OFF Time

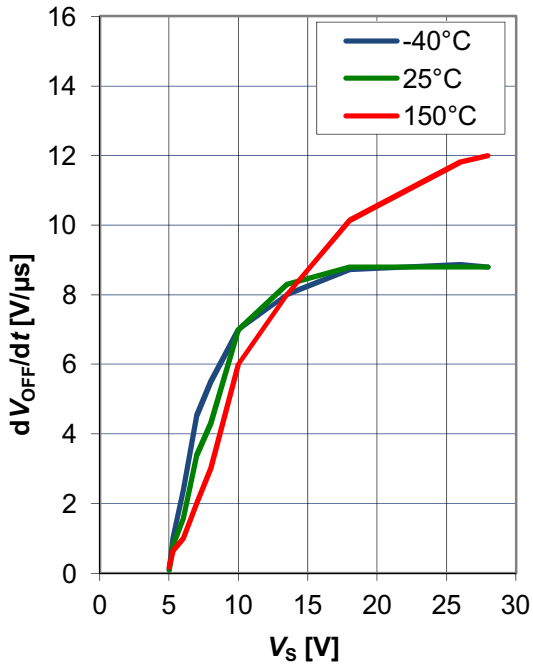
$t_{OFF} = f(V_S, T_J)$, R_L = 0.5 Ω



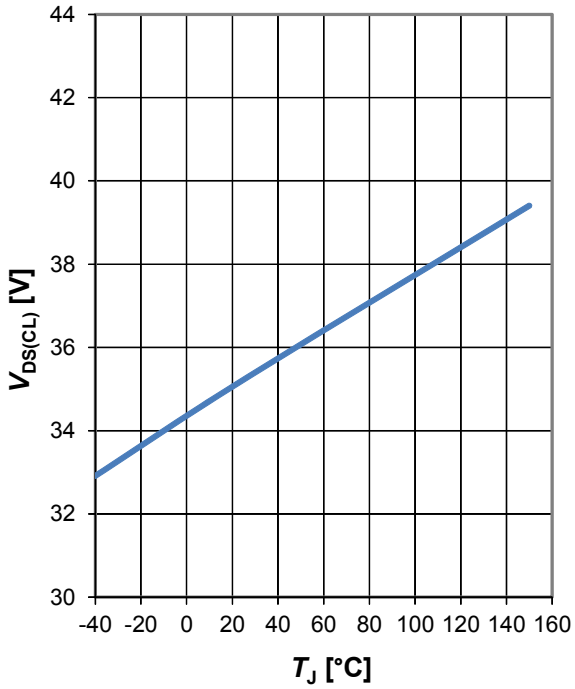
Slew Rate at Turn ON
$dV_{ON} / dt = f(V_S, T_J)$, $R_L = 0.5\ \Omega$



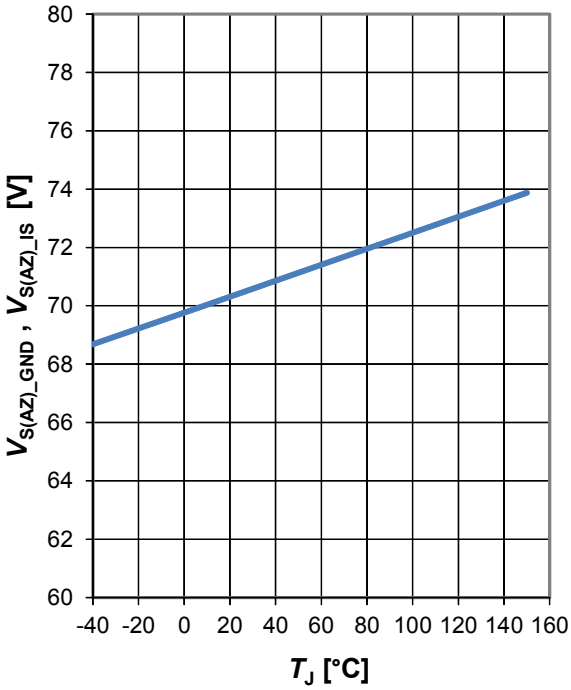
Slew Rate at Turn OFF
$dV_{OFF} / dt = f(V_S, T_J)$, $R_L = 0.5\ \Omega$



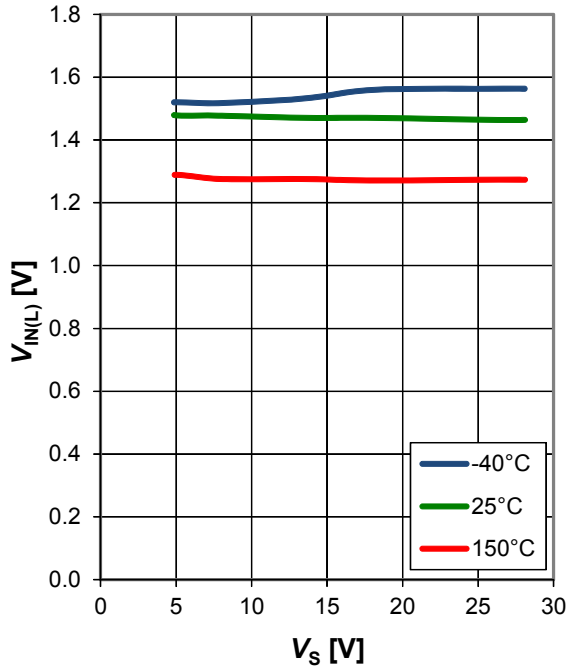
Drain to Source Clamp Voltage
$V_{DS(CL)} = f(T_J)$, I_L = 50 mA



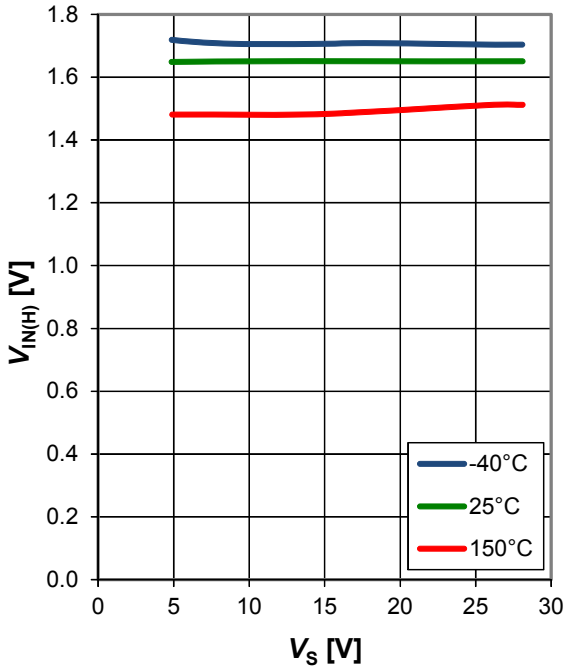
Overvoltage Protection
$V_{S(AZ)\_GND} = f(T_J)$, $V_{S(AZ)\_IS} = f(T_J)$



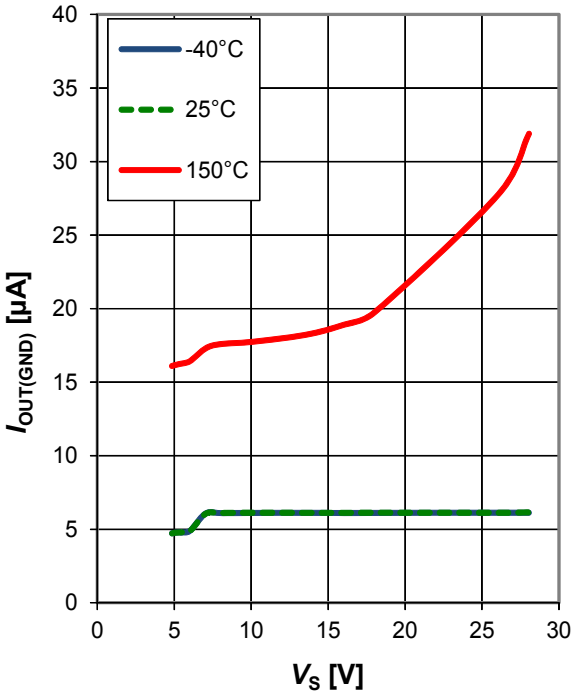
LOW Level Input Voltage
$V_{IN(L)} = f(V_S, T_J)$



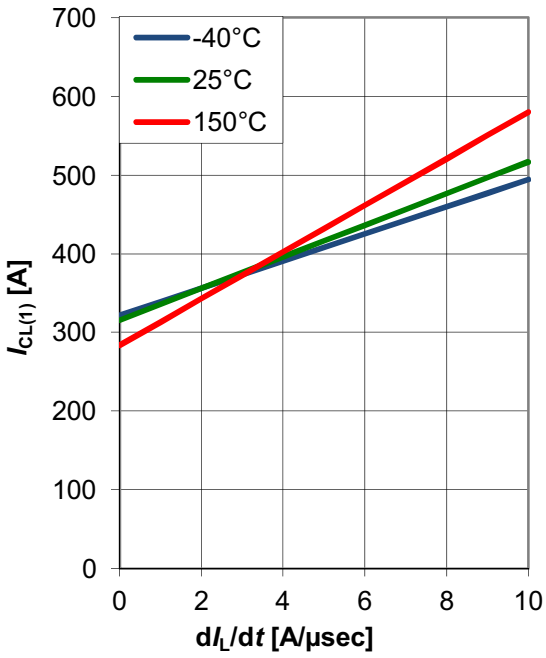
HIGH Level Input Voltage
$V_{IN(H)} = f(V_S, T_J)$



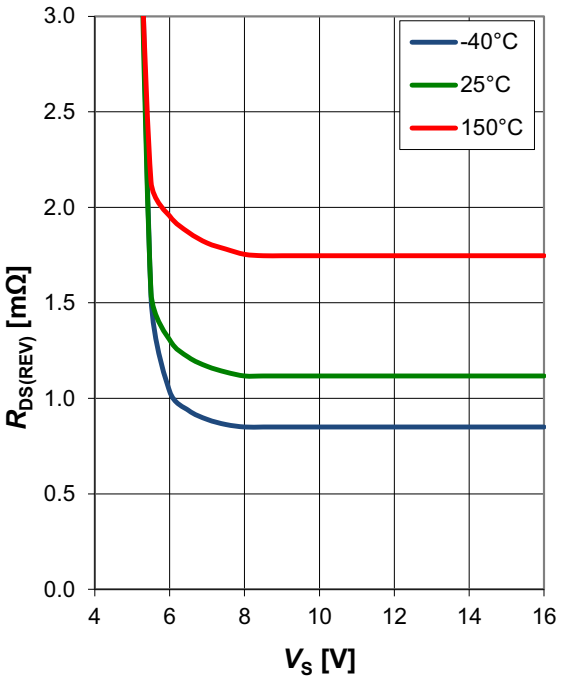
Output Leakage Current while Device GND Disconnected, $I_{OUT(GND)} = f(V_S, T_J)$



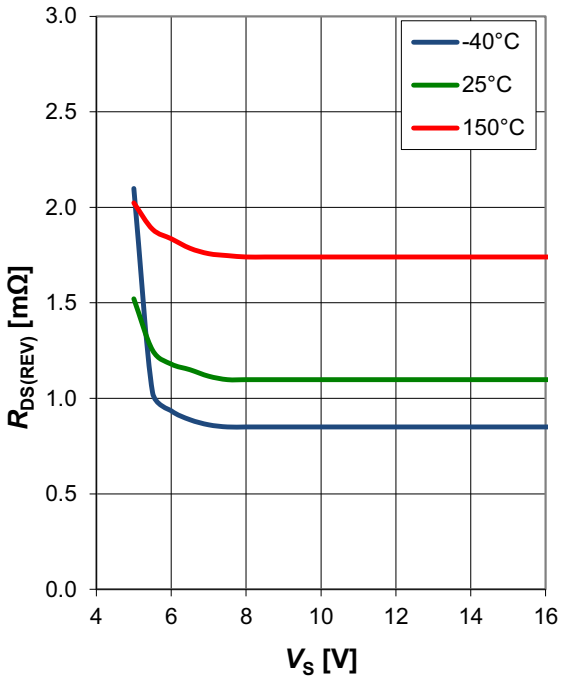
Current Trip Peak Level $I_{CL(1)} = f(dI_L/dt, T_J)$, V_S = 13.5 V



Resistance in ReverSave™ $R_{DS(REV)} = f(V_S, T_J)$, I_L = -150 A



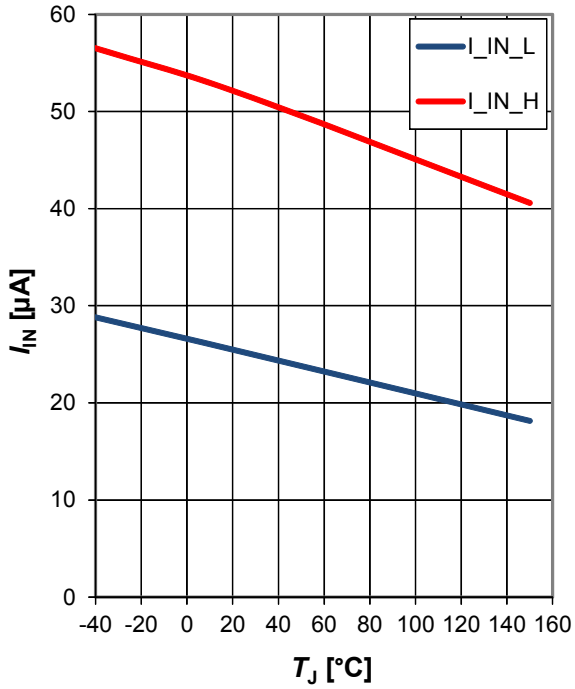
Resistance in ReverSave™ $R_{DS(REV)} = f(V_S, T_J)$, I_L = -20 A



Electrical Characteristics BTS50010-1TAE

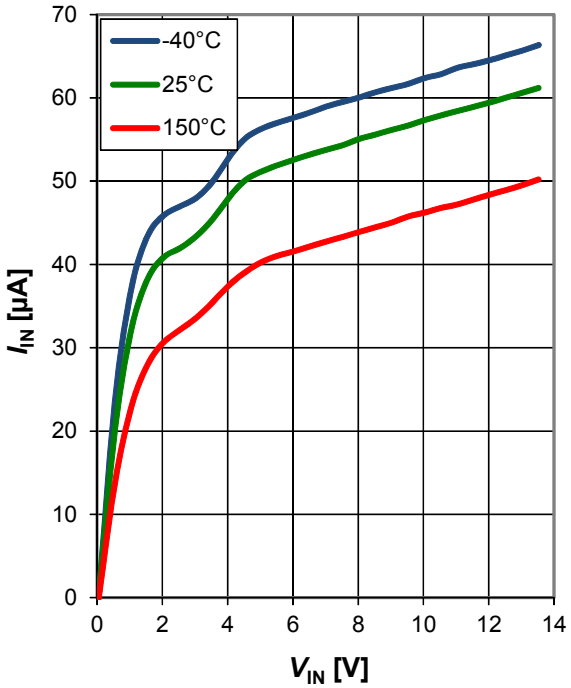
Input Current

$I_{IN} = f(T_J)$; V_S = 13.5 V; $V_{IN(L)}$ = 0.8V; $V_{IN(H)}$ = 5.0 V



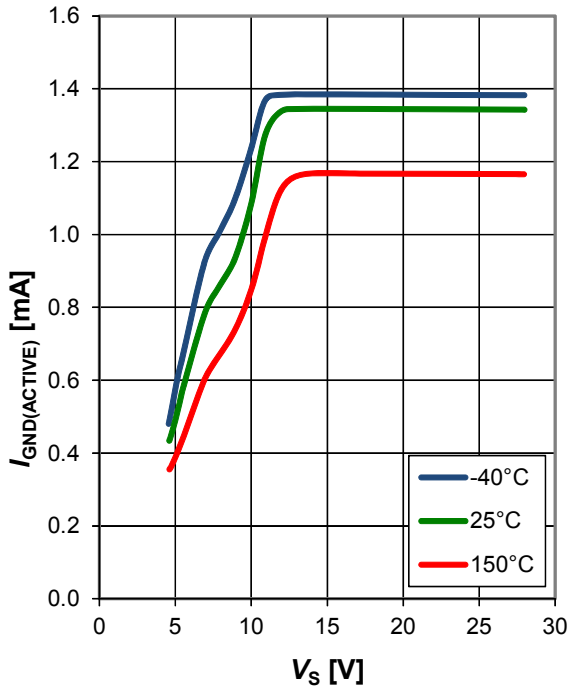
Input Current

$I_{IN(H)} = f(V_{IN}, T_J)$; V_S = 13.5 V



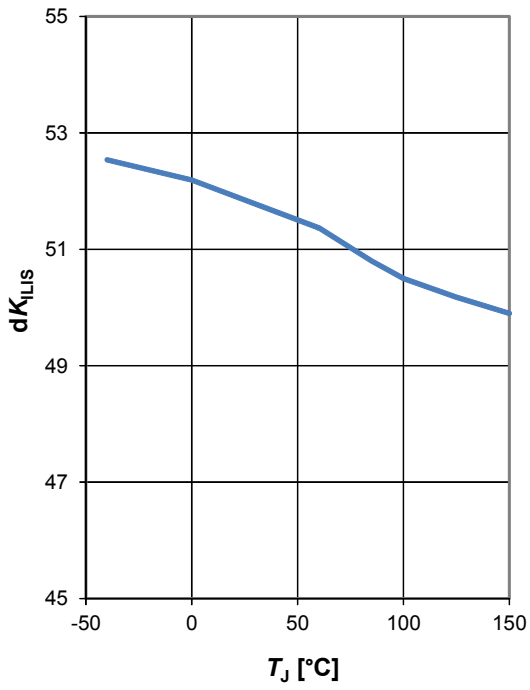
GND current

$I_{GND(ACTIVE)} = f(V_S, T_J)$; V_{IN} = 2.2 V



Current Sense Differential Ratio

$dk_{ILIS} = f(T_J)$



7 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

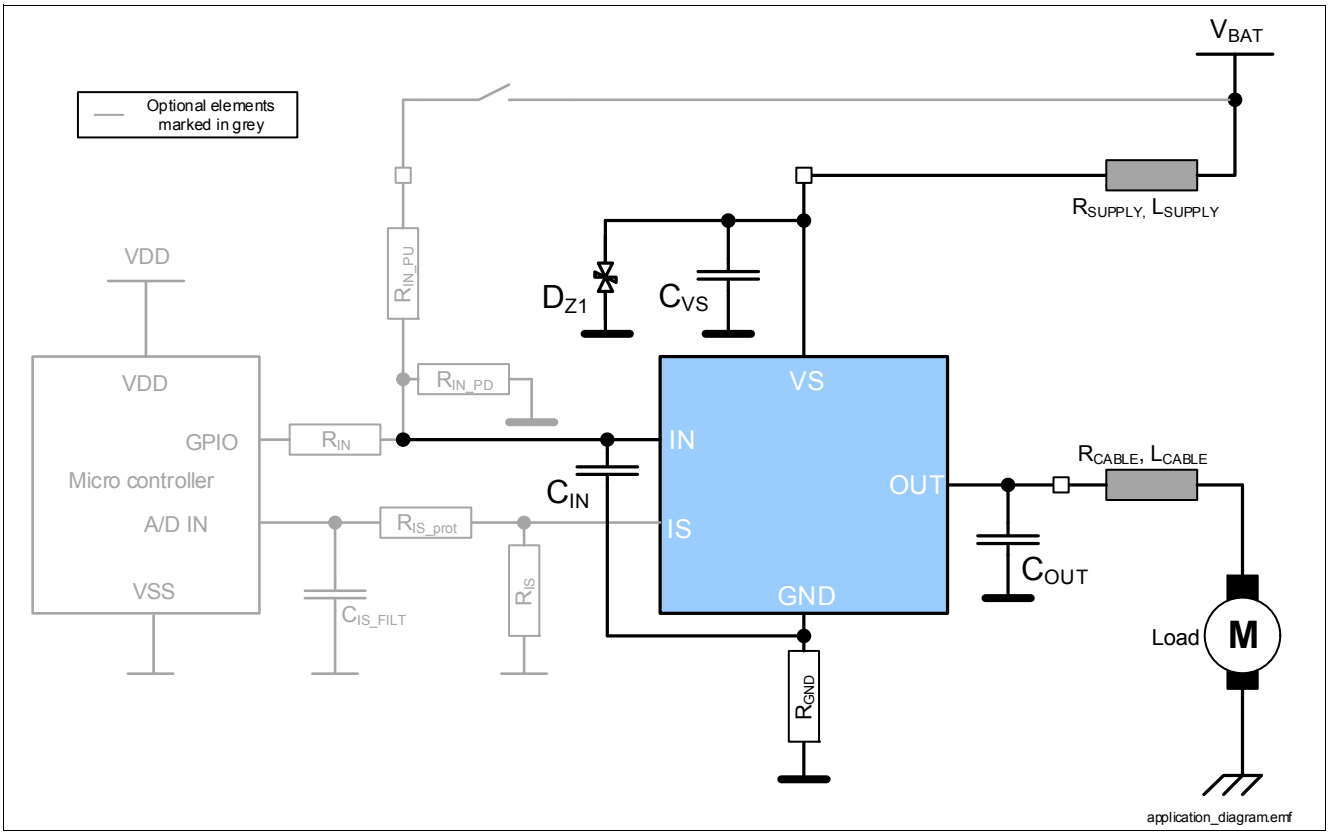


Figure 24 Application Diagram with BTS50010-1TAE

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

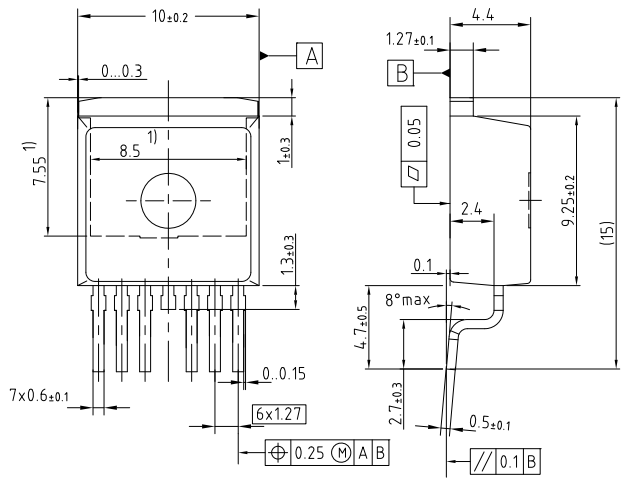
Table 7 Bill of material

Reference	Value	Purpose
R_{GND}	10 Ω	Protection in case of Overvoltage and Loss of Battery while driving inductive loads
D_{Z1}	40 V Z-Diode	Suppressor diode Protection during Overvoltage and in case of Loss of Battery, see **Chapter 5.3.2**
C_{VS}	100 nF	Improved EMC behavior (in layout, pls. place close to the pins)
C_{OUT}	10 nF	Improved EMC behavior (in layout, pls. place close to the pins)
C_{IN}	150 nF	BTS50010-1TAE tends to latched switch-off due to short negative transients on supply pin; C_{IN} automatically resets the device (for an 3.3V or 5V input signal)
R_{SUPPLY}, L_{SUPPLY}	intrinsic	Supply line impedance (battery, connectors, cable)
R_{CABLE}, L_{CABLE}	intrinsic	Output line impedance (connectors, cable)
Controlling BTS50010-1TAE with a microcontroller		
R_{IN}	4.7 kΩ	Protection of the microcontroller during overvoltage, reverse polarity allows BTS50010-1TAE channels OFF during loss of ground
R_{IS}	1 kΩ	Sense resistor; if IS signal is not used, leave IS pin open
R_{IS_PROT}	4.7 kΩ	Protection of the microcontroller during overvoltage Protection of the BTS50010-1TAE during reverse polarity
C_{IS_FILT}	10 nF	Sense signal filtering
Controlling BTS50010-1TAE with a mechanical button		
R_{IN_PU}	4.7 kΩ	Protection of the IN pin during overvoltage, reverse polarity signal debouncing
R_{IN_PD}	4.7 kΩ	fast discharging of C_{IN}

7.1 Further Application Information

- Please contact us for information regarding the pin FMEA
- For further information you may contact **http://www.infineon.com/**

8 Package Outlines



Dimensions in

Figure 25 PG-TO-263-7-10 (RoHS-Compliant)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Table 8 Handling Information

Parameter	Symbol	Values
Moisture sensitivity level acc. J-STD-020-D	*MSL*	1
Jedec classification temperature acc. J-STD-020-D	T_{peak}	245 °C

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

9 Revision History

Revision	Date	Changes
1.0	2018-06-08	Initial version of Datasheet

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Do you have a question about any aspect of this document?
Email: erratum@infineon.com