



LD6915 series

Dual low-dropout regulators, low noise, 150 mA

Rev. 1 — 8 July 2013

Objective data sheet

1. Product profile

1.1 General description

The LD6915 series consists of small-size dual Low DropOut regulators (LDO). Each device delivers two times 150 mA with a typical voltage drop of 120 mV at 150 mA for each LDO. The system offers two individual fixed nominal output voltages ($V_{O(nom)}$) from 1.2 V to 3.6 V with high Power Supply Rejection Ratio (PSRR) of 80 dB.

The LDO has an integrated Soft start to control the inrush current during start-up. The output mode, when disabled, can be high-ohmic 3-state or auto discharge. Optionally a delayed output circuit is available for the second output. The devices are available in DFN1212-6 (SOT1229) package with a maximum height of 0.4 mm.

1.2 Features and benefits

- Extremely low standby current in shutdown mode ($\leq 0.1 \mu\text{A}$)
- Low quiescent current
- Fast turn-on time
- Safety features (temperature watchdog, current limiter and foldback circuit)
- Delayed output circuit for second LDO (optional)
- High PSRR
- Auto discharge or high-ohmic mode for output when disabled
- DFN1212-6 (SOT1229) with 0.4 mm pitch and package size of $1.2 \times 1.2 \times 0.4 \text{ mm}$
- Pb-free, Restriction of Hazardous Substances (RoHS) compliant, free of halogen and antimony (Dark Green compliant)

1.3 Applications

- Smartphones
- Mobile handsets
- Digital still cameras
- Tablet PCs
- Mobile internet devices
- Portable media players

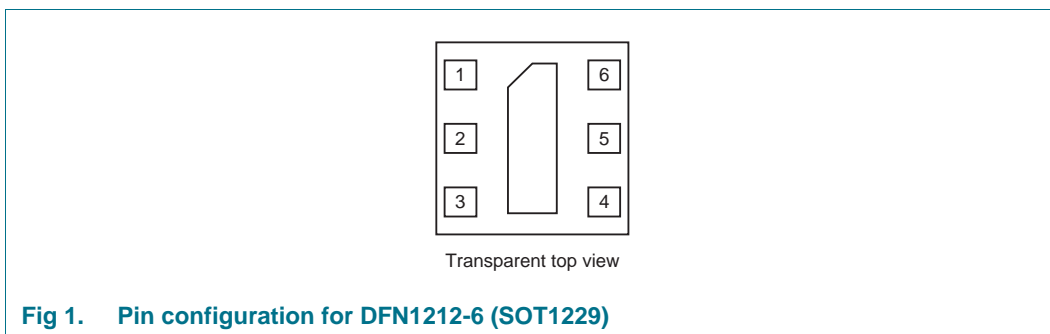
1.4 Quick reference data

- $I_O = 150 \text{ mA}$ for each LDO
- PSRR = 80 dB at 1 kHz
- RMS noise $V_{n(o)RMS} = 60 \mu\text{V}$ at 10 Hz to 100 kHz
- $t_{startup(reg)} = 150 \mu\text{s}$
- $V_I = 1.75 \text{ V}$ to 5.5 V
- $V_O = 1.2 \text{ V}$ to 3.6 V (fixed value)
- Dropout voltage $V_{do} = 120 \text{ mV}$ at $I_O = 150 \text{ mA}$ for each LDO
- Quiescent current $I_q = 2 \times 35 \mu\text{A}$ at $I_O = 0 \text{ mA}$



2. Pinning information

2.1 Pinning



2.2 Pin description

Table 1. Pin description for DFN1212-6 (SOT1229)

Symbol	Pin	Description
OUT1	1	regulator 1 output voltage
OUT2	2	regulator 2 output voltage
GND	3	supply ground
EN2	4	regulator 2 enable input
IN	5	supply voltage input
EN1	6	regulator 1 enable input
i.c.	TAB	internal connected [1]

[1] The TAB is GND level (it is placed on the reverse side of the IC). It is recommended to connect the TAB to GND. Leaving it unconnected is also allowed but it may result in lower thermal performance.

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
LD6915LX	DFN1212-6	plastic extremely thin small outline package; no leads; 6 terminals; body 1.2 × 1.2 × 0.4 mm	SOT1229

3.1 Ordering options

Further output voltage versions are available on request; see [Section 19 “Contact information”](#)

Table 3. Type number and nominal output voltage of high-ohmic output

Type number	Nominal output voltage $V_{O(nom)}$	
	OUT1	OUT2
LD6915LX/3028H	3.0 V	2.8 V
LD6915LX/3328H	3.3 V	2.8 V

Table 4. Type number and nominal output voltage of auto discharge

Type number	Nominal output voltage $V_{O(nom)}$	
	OUT1	OUT2
LD6915LX/1815P	1.8 V	1.5 V
LD6915LX/1828P	1.8 V	2.8 V
LD6915LX/2818P	2.8 V	1.8 V
LD6915LX/3018P	3.0 V	1.8 V
LD6915LX/3028P	3.0 V	2.8 V
LD6915LX/3318P	3.3 V	1.8 V
LD6915LX/3328P	3.3 V	2.8 V
LD6915LX/3333P	3.3 V	3.3 V
LD6915LX/3612P	3.6 V	1.2 V

Table 5. Type number and nominal output voltage of high-ohmic output with delay circuit

Type number	Nominal output voltage $V_{O(nom)}$	
	OUT1	OUT2
LD6915LX/3328HD	3.3 V	2.8 V

Table 6. Type number and nominal output voltage of auto discharge with delay circuit

Type number	Nominal output voltage $V_{O(nom)}$	
	OUT1	OUT2
LD6915LX/2818PD	2.8 V	1.8 V

4. Block diagram

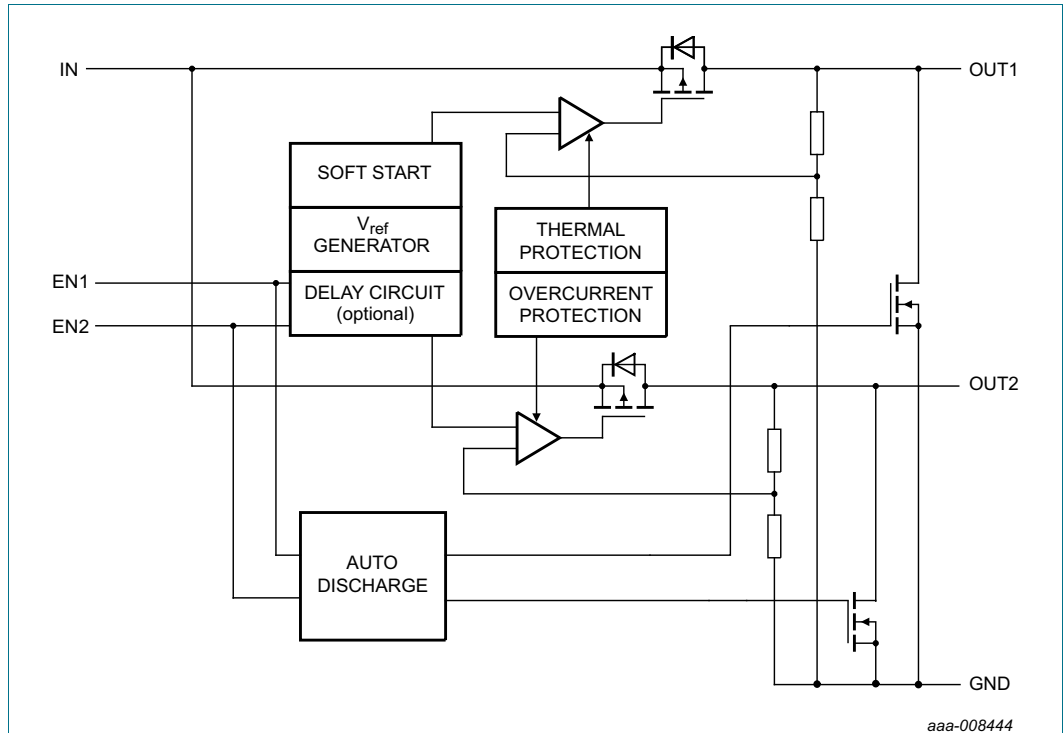


Fig 2. Block diagram dual LDO with auto discharge function (-P and -PD versions)

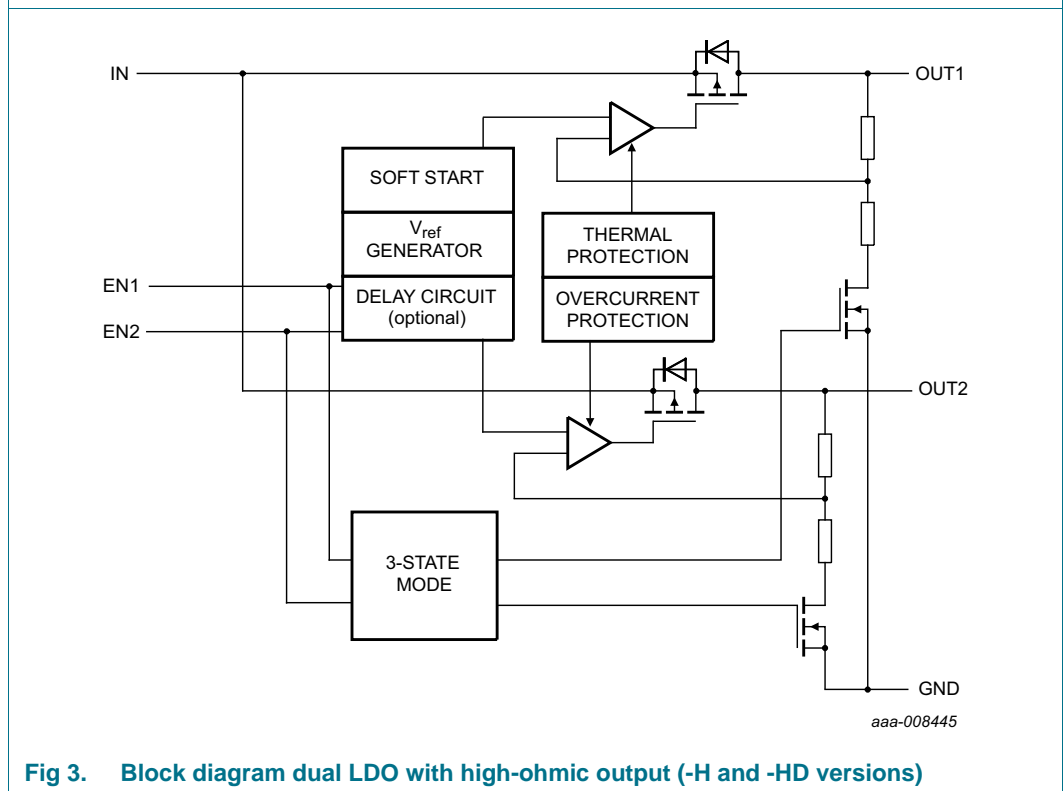


Fig 3. Block diagram dual LDO with high-ohmic output (-H and -HD versions)

5. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
Pin IN, EN1 and EN2					
V_I	input voltage	4 ms transient	-0.5	+6.0	V
V_{EN}	voltage on pin EN	4 ms transient	-0.5	+6.0	V
Pin OUT1 and OUT2					
V_O	output voltage	4 ms transient	-0.5	+6.0	V
Per device					
P_{tot}	total power dissipation		[1] -	670	mW
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-40	+125	°C
T_{amb}	ambient temperature		-40	+85	°C
V_{ESD}	electrostatic discharge voltage	human body model	[2]	±2	kV
		machine model	[3] -	±200	V

[1] The (absolute) maximum power dissipation depends on the junction temperature T_j . Higher power dissipation is allowed with lower ambient temperatures. The conditions to determine the specified values are $T_{amb} = 25\text{ °C}$ and the use of a two-layer Printed-Circuit Board (PCB).

[2] According to JESD22-A114F.

[3] According to JESD22-A115C.

6. Recommended operating conditions

Table 8. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{amb}	ambient temperature		-40	+85	°C
T_j	junction temperature		-	+125	°C
Pin IN					
V_I	input voltage		1.75	5.5	V
$C_{ext(IN)}$	external capacitance on pin IN		[1] 1.0	-	μF
Pin EN1 and EN2					
V_{EN}	voltage on pin EN		0	5.5	V
Pin OUT1 and OUT2					
V_O	output voltage		0	$V_I + 0.3$	V
$C_{L(ext)}$	external load capacitance		[1] 1.0	-	μF

[1] See [Section 10.1 "Input and output capacitor values"](#).

7. Thermal characteristics

Table 9. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1][2] 150	K/W

- [1] The overall $R_{th(j-a)}$ can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$, all pins must have a solid connection to larger Cu layer areas for example to the power and ground layer. In multilayer PCB applications, the second layer should be used to create a large heat spreader area directly below the LDO. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply. Avoid the use of solder-stop varnish under the chip.
- [2] Use the measurement data given for a rough estimation of the $R_{th(j-a)}$ in your application. The actual $R_{th(j-a)}$ value can vary in applications using different layer stacks and layouts.

8. Characteristics

Table 10. Electrical characteristics

At recommended input voltages and $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$; voltages are referenced to GND (ground = 0 V); $V_I = V_{O(nom)} + 1\text{ V}$; $C_{ext(IN)} = 1\text{ }\mu\text{F}$; $C_{L(ext)} = 1\text{ }\mu\text{F}$ at pin OUT1 and OUT2; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output voltage (pin OUT1, pin OUT2) per LDO						
V_{do}	dropout voltage	$I_O = 150\text{ mA}$; $V_I \leq V_{O(nom)}$	[2] -	120	-	mV
ΔV_O	output voltage variation	$V_O \geq 1.8\text{ V}$; $I_O = 1\text{ mA}$				
		$T_{amb} = +25\text{ °C}$	-2	-	+2	%
		$-30\text{ °C} \leq T_{amb} \leq +85\text{ °C}$	[2] -3	-	+3	%
		$V_O < 1.8\text{ V}$; $I_O = 1\text{ mA}$				
		$T_{amb} = +25\text{ °C}$	-3	-	+3	%
		$-30\text{ °C} \leq T_{amb} \leq +85\text{ °C}$	[2] -4	-	+4	%
Line regulation error per LDO						
$\Delta V_O / (V_O \times \Delta V_I)$	relative output voltage variation with input voltage	$V_I = (V_{O(nom)} + 1\text{ V})$ to 5 V; $I_O = 1\text{ mA}$	[2] -0.1	-	+0.1	%/V
Load regulation error per LDO						
$\Delta V_O / (V_O \times \Delta I_O)$	relative output voltage variation with output current	$1\text{ mA} \leq I_O \leq 150\text{ mA}$	[2] -0.01	0.0025	0.01	%/mA
Output current (pin OUT1, pin OUT2) per LDO						
I_O	output current		150	-	-	mA
$I_{act(fold)}$	foldback activation current		[2] -	750	-	mA
I_{sc}	short-circuit current	$V_O = 0\text{ V}$	[2] -	100	-	mA
Regulator input current (pin IN) per LDO						
$I_{inrush(lim)}$	inrush current limit	$(V_{EN1} \text{ or } V_{EN2}) > 1.1\text{ V}$	[2] -	-	400	mA
I_q	quiescent current	$(V_{EN1} = V_{EN2}) > 1.1\text{ V}$; $I_O = 0\text{ mA}$ at OUT1 and OUT2	-	35	50	μA
		$(V_{EN1} = V_{EN2}) > 1.1\text{ V}$; $1\text{ mA} \leq I_O \leq 150\text{ mA}$ at OUT1 and OUT2	[2] -	400	-	μA
		$(V_{EN1} = V_{EN2}) \leq 0.4\text{ V}$	-	0.1	1.0	μA

Table 10. Electrical characteristics ...continued

At recommended input voltages and $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$; voltages are referenced to GND (ground = 0 V);
 $V_I = V_{O(nom)} + 1\text{ V}$; $C_{ext(IN)} = 1\text{ }\mu\text{F}$; $C_{L(ext)} = 1\text{ }\mu\text{F}$ at pin OUT1 and OUT2; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Ripple rejection and output noise per LDO						
PSRR	power supply rejection ratio	$I_O = 30\text{ mA}$; $f_{ripple} = 1\text{ kHz}$	[2]	-	80	- dB
$V_{n(o)(RMS)}$	RMS output noise voltage	bandwidth = 10 Hz to 100 kHz; $V_O = 1.8\text{ V}$	[2]	-	60	- μV
Enable input and timing (pin EN1, pin EN2) per LDO						
V_{IL}	LOW-level input voltage		0	-	0.4	V
V_{IH}	HIGH-level input voltage		1.1	-	5.5	V
I_{en}	enable current		-	400	-	nA
$t_{startup(reg)}$	regulator start-up time	$V_O = 0.95 \times V_{O(nom)}$; $I_O = 150\text{ mA}$	[1][2]	-	150	- μs
t_d	delay time	for LDO2; -PD or -HD version	[2]	-	100	- μs
Auto discharge function (-P or -PD version) per LDO						
R_{pd}	pull-down resistance		[2]	-	100	- Ω
$t_{sd(reg)}$	regulator shutdown time	$I_O = 0\text{ A}$; $V_O = 0.1 \times V_{O(nom)}$	[1][2]	-	300	- μs
Thermal protection						
T_{sd}	shutdown temperature		[2]	-	160	- $^{\circ}\text{C}$
$T_{sd(hys)}$	shutdown temperature hysteresis		[1][2]	-	20	- K

[1] After T_{sd} was reached and after the device was disabled, the junction temperature must decrease by $T_{sd(hys)}$ to enable the device.

[2] The parameter was verified and is guaranteed by design.

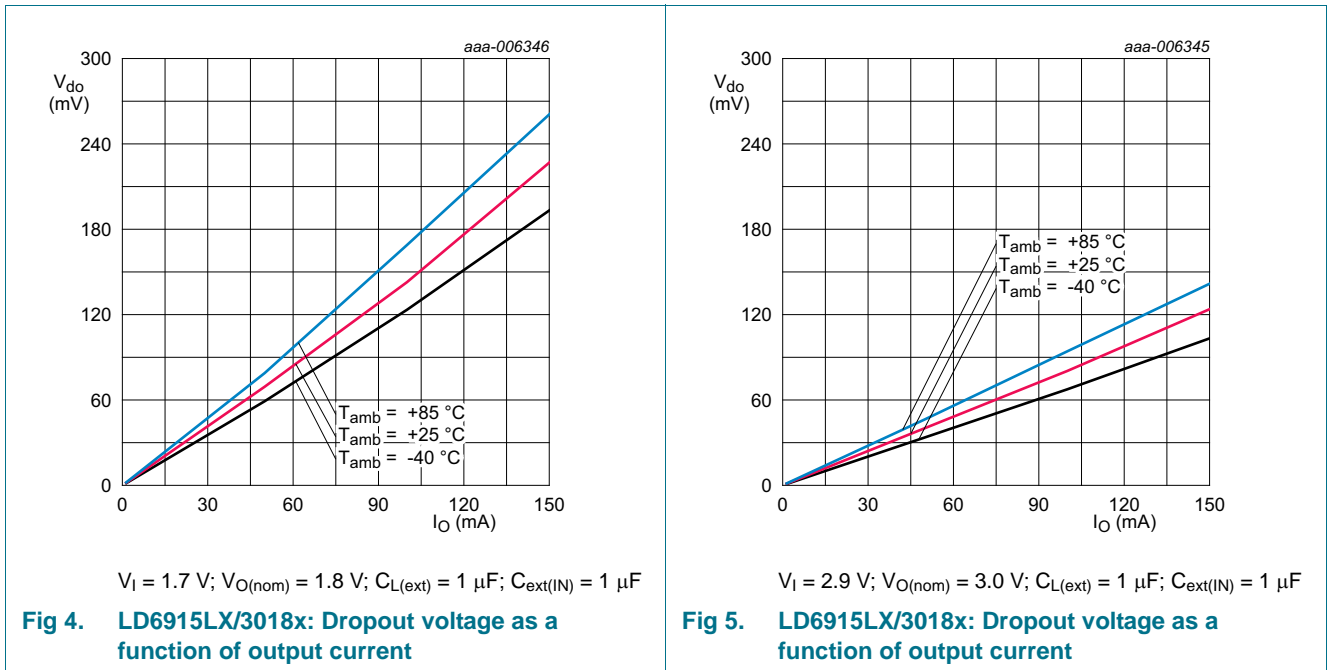
9. Dynamic behavior

All results described in [Section 9](#) are based on measurements of types from the LD6915 product series.

9.1 Dropout

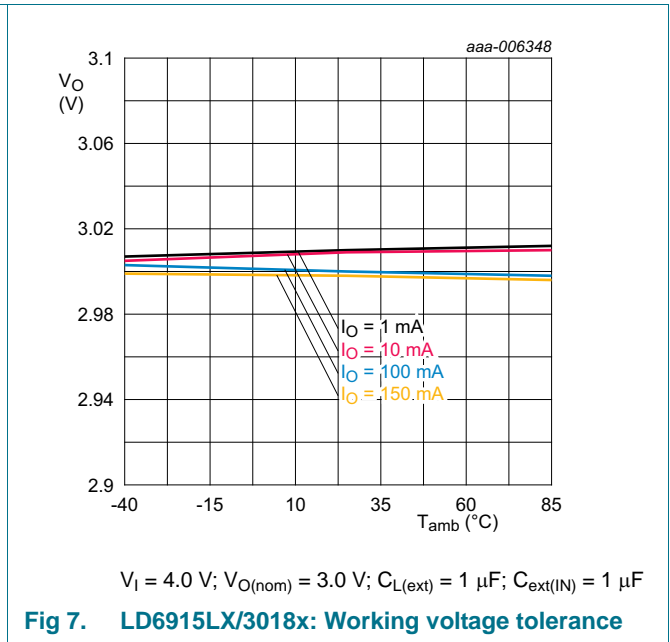
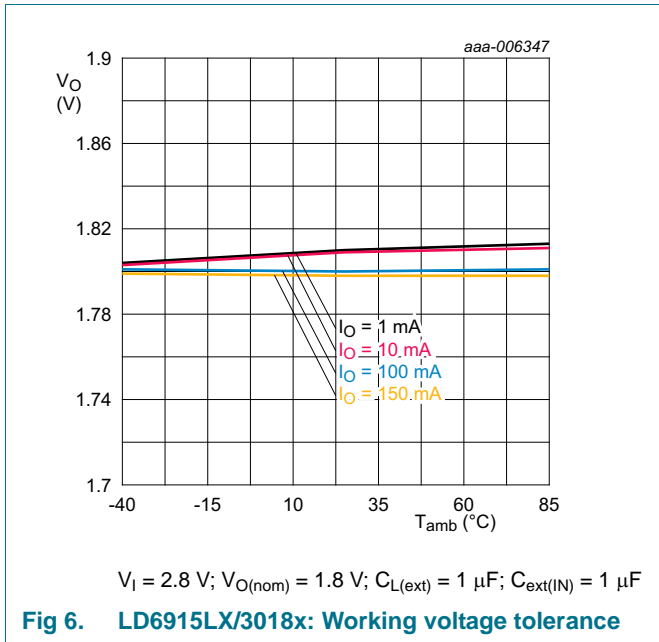
The dropout voltage is defined as the smallest input-to-output voltage difference at a specified load current when the regulator operates within its linear region with the pass transistor functioning simply as a resistor. This means that the input voltage is below the nominal output voltage value.

A small dropout voltage guarantees lower power consumption and maximizes efficiency.



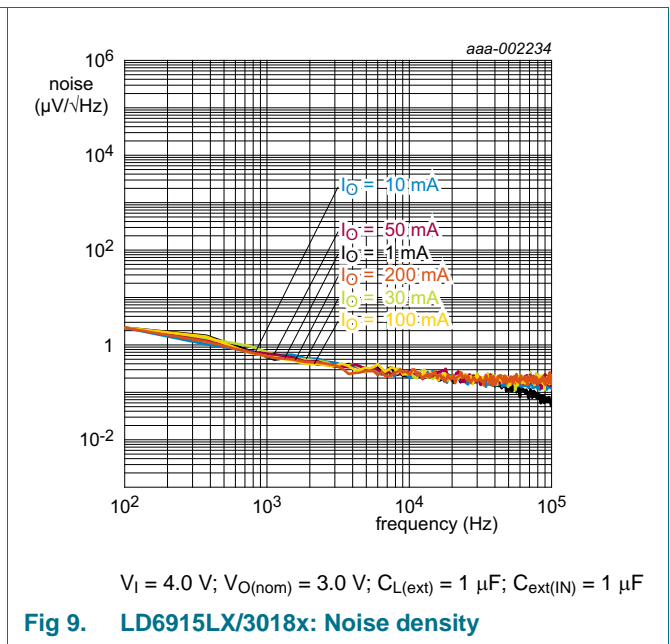
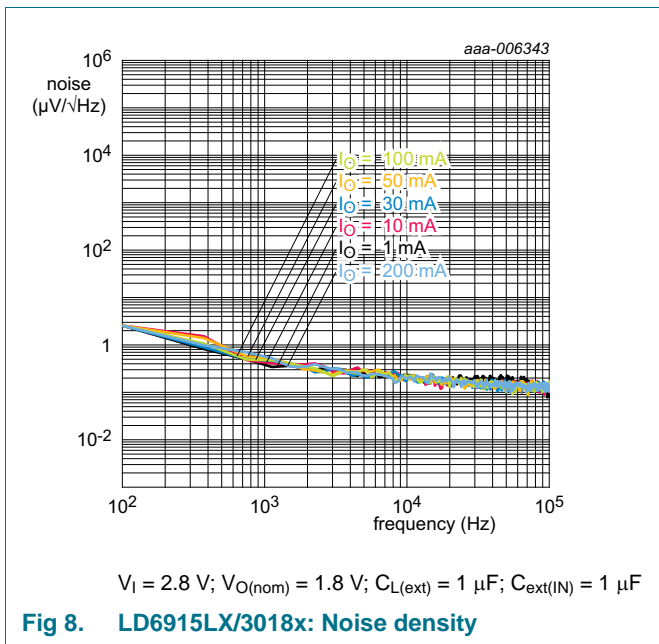
9.2 Working voltage tolerance

The guaranteed output voltages are specified in [Table 10](#).



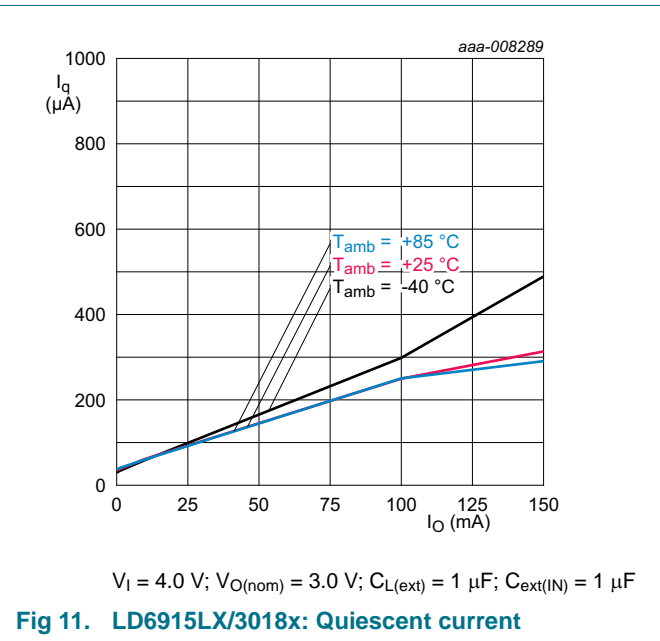
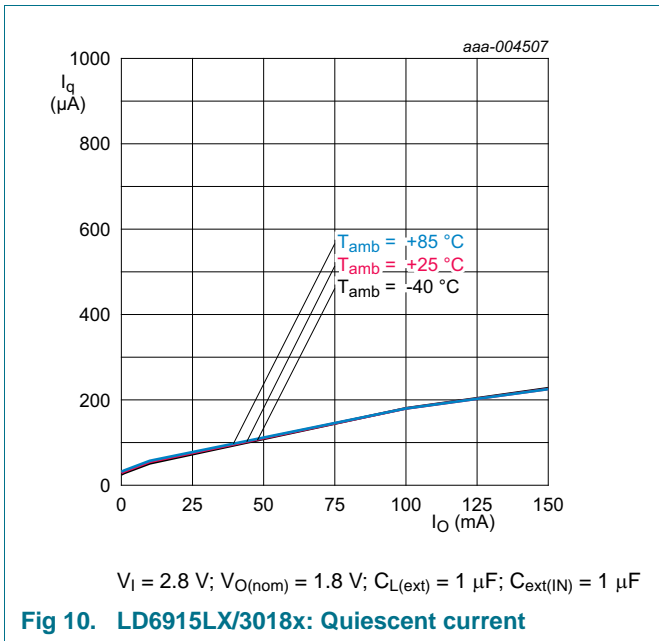
9.3 Noise

Output noise voltage of an LDO circuit is given as noise density or RMS output noise voltage over a defined range of frequencies (10 Hz to 100 kHz). Permanent conditions are a constant output current and a ripple-free input voltage. The output noise voltage is generated by the LDO regulator.



9.4 Quiescent current

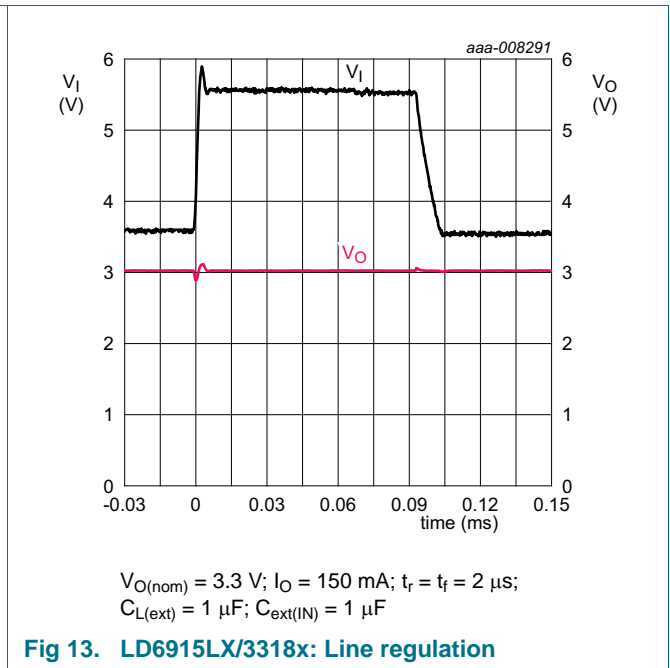
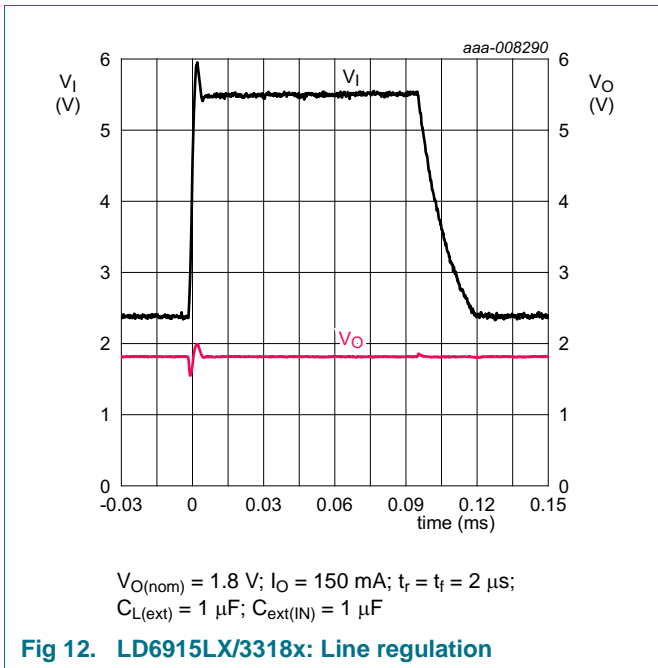
Quiescent or ground current is the difference between the input and the output current of the regulator.



9.5 Line regulation

Line regulation response is the capability of the circuit to maintain the nominal output voltage while varying the input voltage.

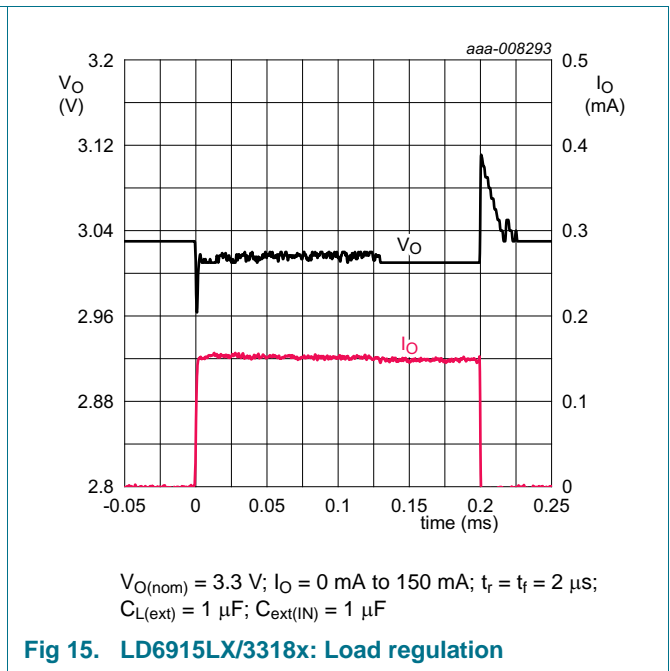
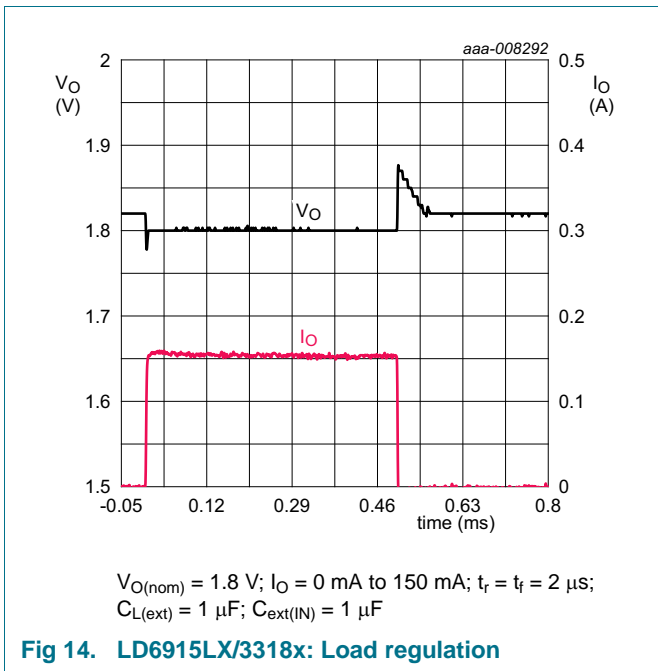
$$\text{Line regulation (\%/V)} = \frac{\Delta V_O}{\Delta V_I} \times \frac{100}{V_O} \tag{1}$$



9.6 Load regulation

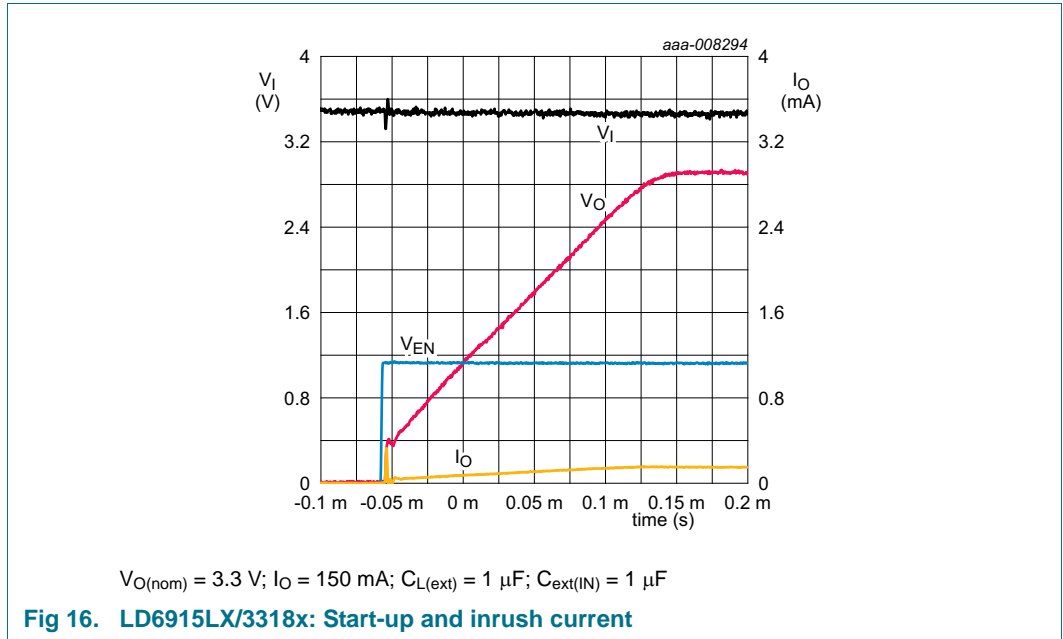
Load regulation is the capability of the circuit to maintain the nominal output voltage while varying the output load current.

$$\text{Load regulation (\%/mA)} = \frac{\frac{\Delta V_O}{V_{O(nom)}} \times 100}{\Delta I_O} \tag{2}$$



9.7 Start-up, inrush current

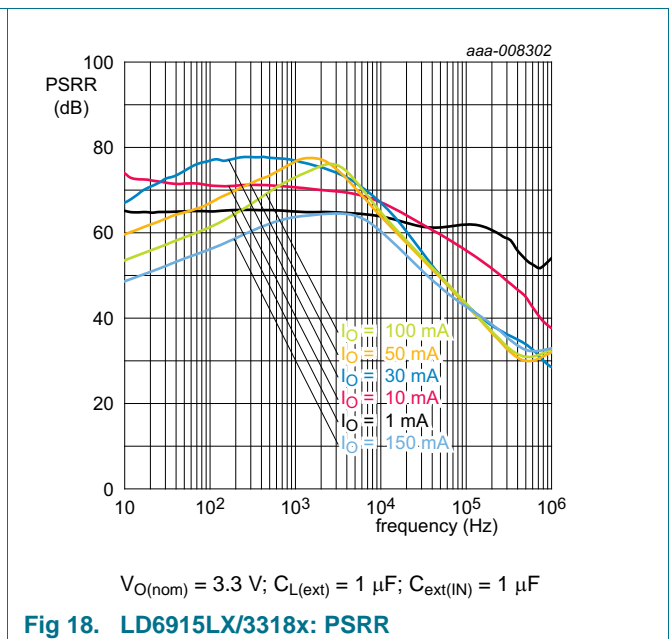
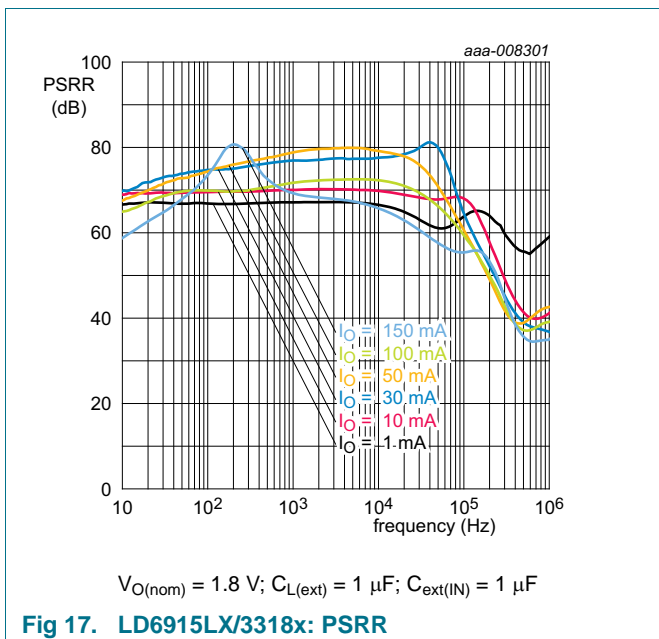
Start-up time defines the time needed for the LDO to achieve 95 % of its typical output voltage level after activation via the enable pin.



9.8 Power Supply Rejection Ratio (PSRR)

PSRR stands for the capability of the regulator to suppress unwanted signals on the input voltage like noise or ripples.

$$PSRR\ (dB) = (-20)\log\frac{V_{O(ripple)}}{V_{I(ripple)}}\ \text{for all frequencies.}$$



10. Application information

10.1 Input and output capacitor values

The devices require external capacitors at the output to guarantee a stable regulator behavior. Also an input capacitor is recommended to keep the input voltage stable. These capacitors should not under-run the specified minimum Equivalent Series Resistance (ESR).

The absolute value of the total capacitance attached to the output pin OUT influences the shutdown time ($t_{sd(Reg)}$) of the devices.

Table 11. External load capacitor

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{ext(IN)}$	external capacitance on pin IN		0.7	1.0	-	μF
$C_{L(ext)}$	external load capacitance	[1]	0.7	1.0	-	μF
ESR	equivalent series resistance		5	-	500	$\text{m}\Omega$

[1] The minimum value of capacitance for stability and correct operation is 0.7 μF . The capacitor tolerance should be $\pm 30\%$ or better over the temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure that this minimum capacitance specification is met. The recommended capacitor type is X7R to meet the full device temperature specification of $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$.

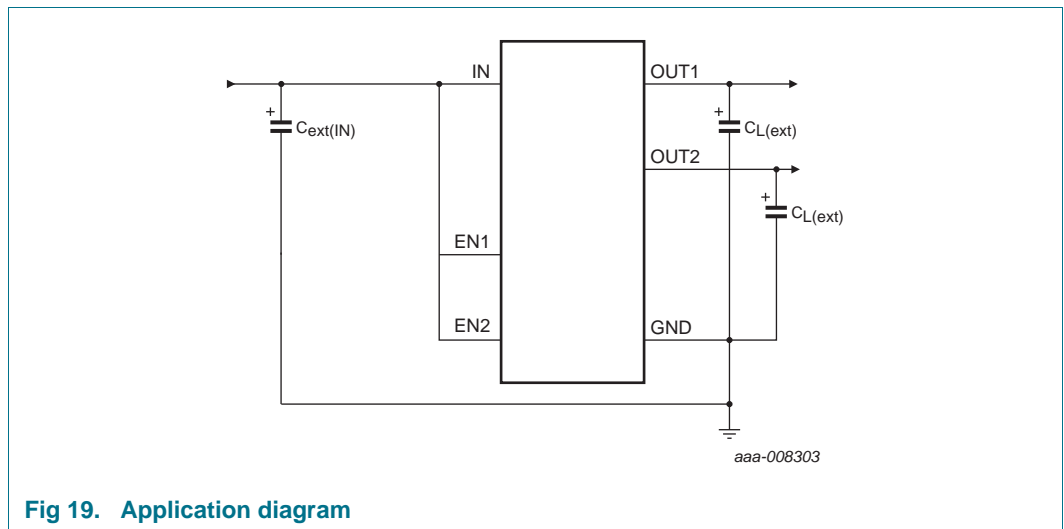


Fig 19. Application diagram

10.2 Optional delay circuit

The two enable input pins EN1 and EN2 allow a control of both LDOs. In case the availability of General-Purpose Input/Output (GPIO) pins is limited, the optional delay circuit of -HD or -PD version can be used to control both LDOs at once without the drawback of doubled inrush current. When both enable signals EN1 and EN2 are activated simultaneously, the delay circuit delays the activation of LDO2 and postpones the associated inrush current. The LDO2 is only active when LDO1 is set to HIGH.

Table 12. Truth table output mode with delay circuit

EN1	EN2	LDO1 output	LDO2 output
LOW	LOW	OFF	OFF
HIGH	LOW	ON	OFF
LOW	HIGH	OFF	OFF
HIGH	HIGH	ON	ON

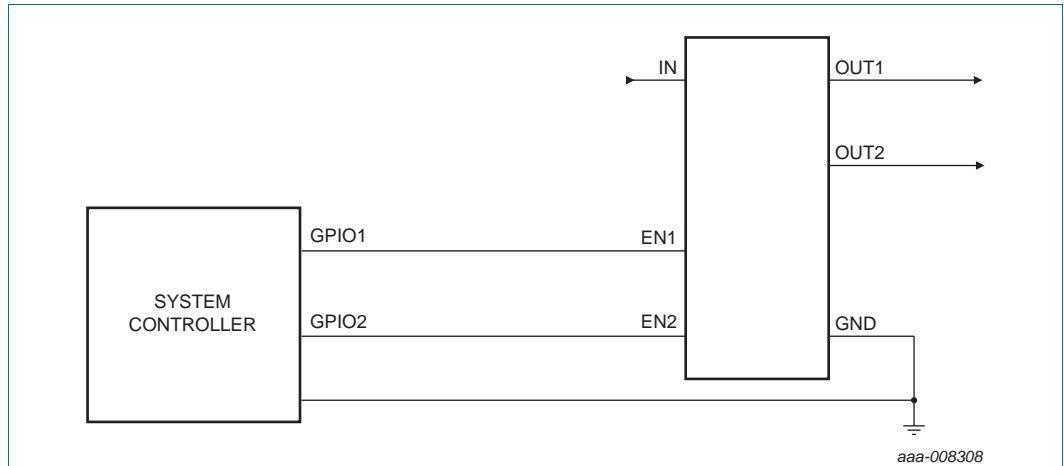


Fig 20. Flexible control with two separate GPIO signals

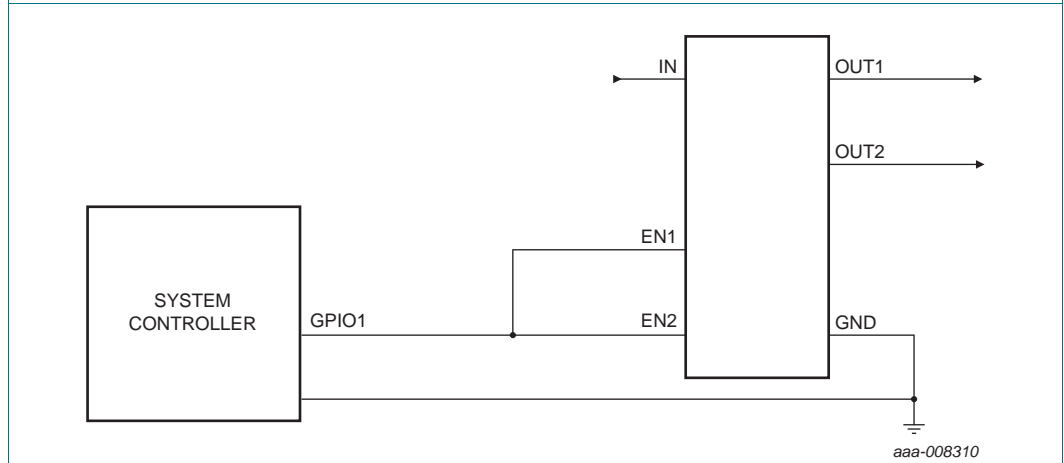


Fig 21. Control with one GPIO signal and delay circuit of -PD or -HD version

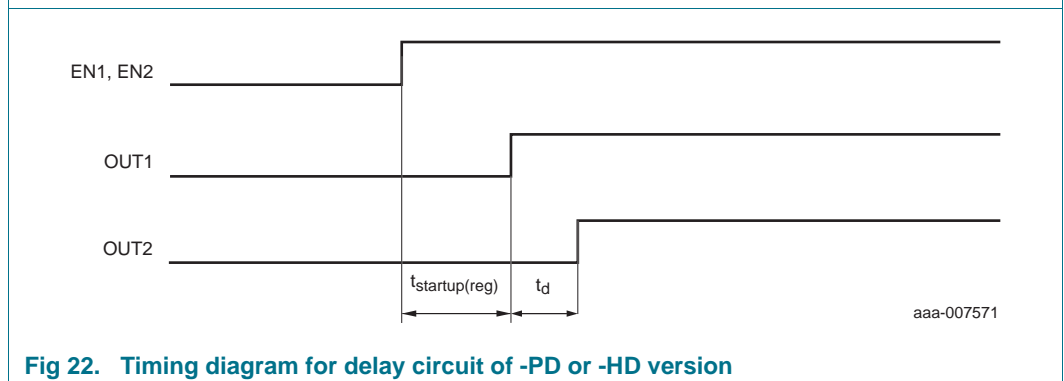


Fig 22. Timing diagram for delay circuit of -PD or -HD version

11. Test information

11.1 Quality information

This product has been qualified in accordance with *NX1-00023 NXP Semiconductors Quality and Reliability Specification* and is suitable for use in consumer applications.

12. Marking

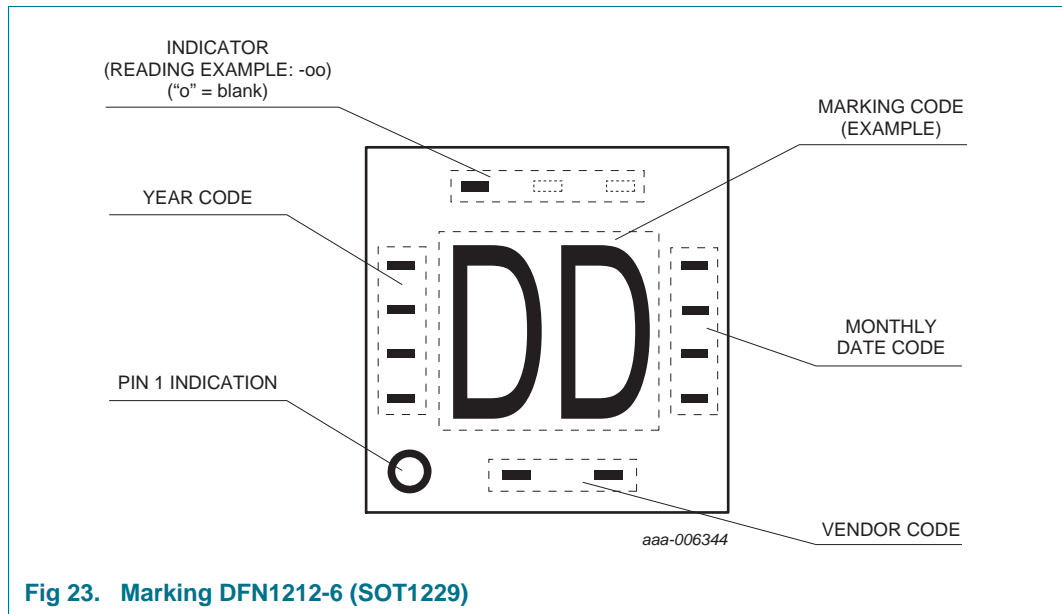


Fig 23. Marking DFN1212-6 (SOT1229)

Table 13. Marking code and indicator of high-ohmic output

Type number	V _{O(nom)}	Marking code	Indicator
LD6915LX/3028H	3.0 V / 2.8 V	<td>	oo-
LD6915LX/3328H	3.3 V / 2.8 V	<td>	oo-

Table 14. Marking code and indicator of auto discharge

Type number	V _{O(nom)}	Marking code	Indicator
LD6915LX/1815P	1.8 V / 1.5 V	<td>	-oo
LD6915LX/1828P	1.8 V / 2.8 V	AP	-oo
LD6915LX/2818P	2.8 V / 1.8 V	<td>	-oo
LD6915LX/3018P	3.0 V / 1.8 V	<td>	-oo
LD6915LX/3028P	3.0 V / 2.8 V	<td>	-oo
LD6915LX/3318P	3.3 V / 1.8 V	<td>	-oo
LD6915LX/3328P	3.3 V / 2.8 V	<td>	-oo
LD6915LX/3333P	3.3 V / 3.3 V	<td>	-oo
LD6915LX/3612P	3.6 V / 1.2 V	<td>	-oo

Table 15. Marking code and indicator of high-ohmic output with delay circuit

Type number	V _{O(nom)}	Marking code	Indicator
LD6915LX/3328HD	3.3 V / 2.8 V	<td>	-o-

Table 16. Marking code and indicator of auto discharge with delay circuit

Type number	V _{O(nom)}	Marking code	Indicator
LD6915LX/2818PD	2.8 V / 1.8 V	<td>	o-o

13. Package outline

DFN1212-6 plastic extremely thin small outline package; no leads; 6 terminals; body 1.2 x 1.2 x 0.4 mm.

SOT1229

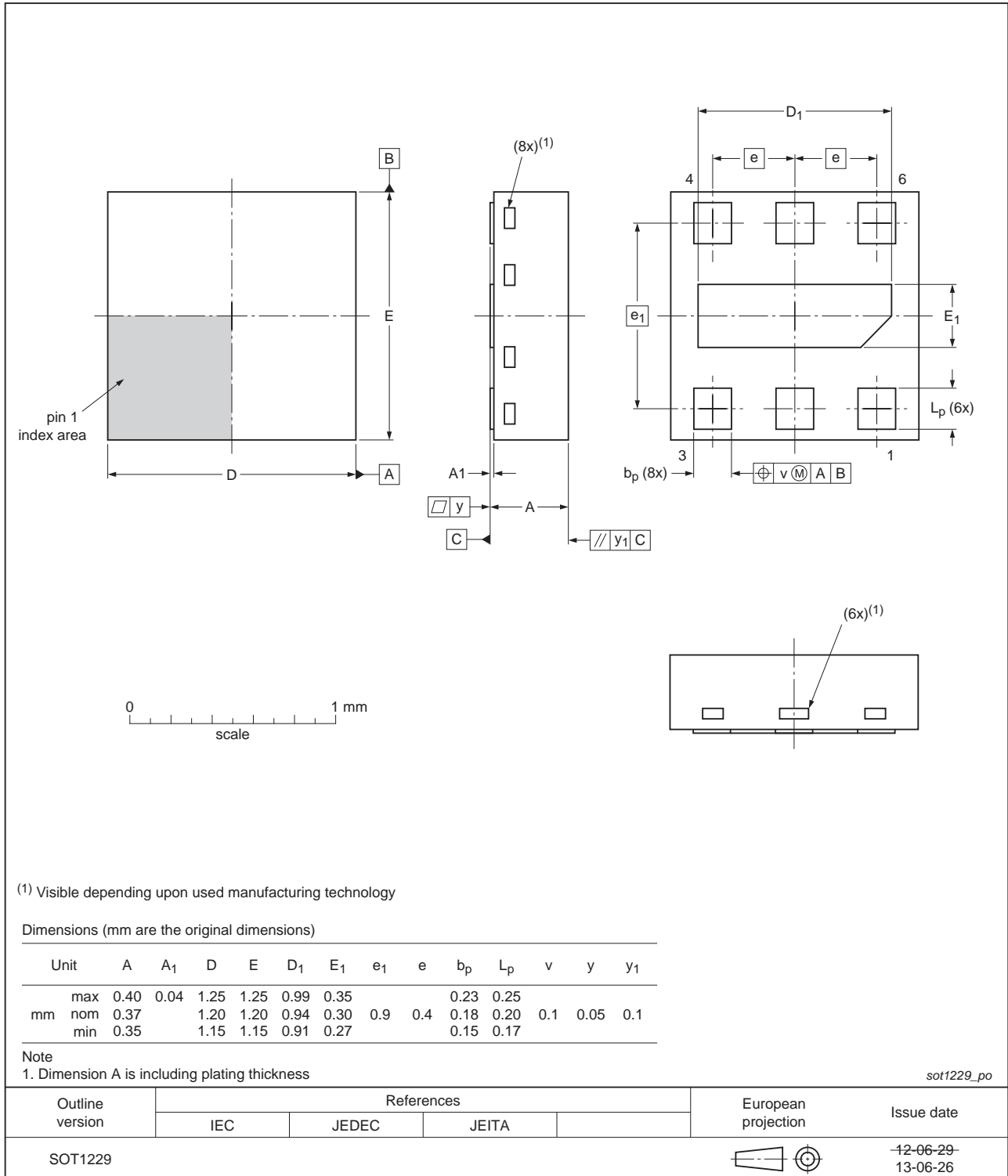


Fig 24. Package outline DFN1212-6 (SOT1229)

14. Packing information

14.1 Packing methods

Table 17. Packing methods

Type number	Package	Description	Orientation [1]	12NC ending	Packing quantity
LD6915LX	SOT1229	<td> mm pitch, <td> mm tape and reel	Q3	125	<td>

[1] For further information about orientation, see [Section 14.2](#).

14.2 Carrier tape information

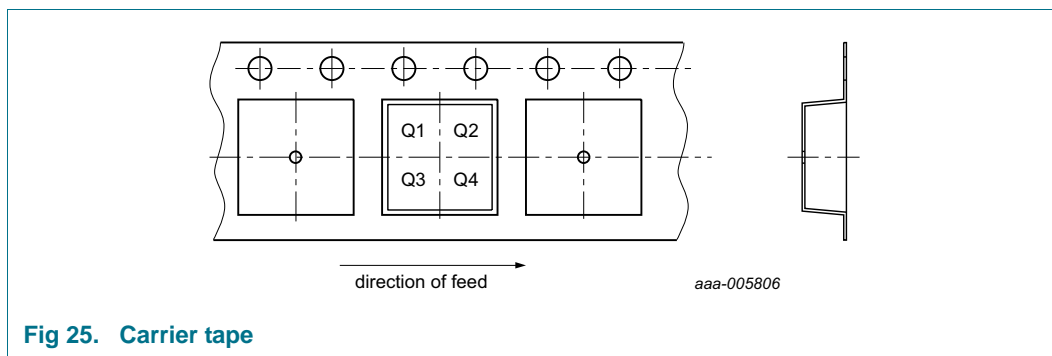


Fig 25. Carrier tape

Table 18. Orientations

Orientation	Meaning	Pin 1 location
Q1	quadrant 1	upper left
Q2	quadrant 2	upper right
Q3	quadrant 3	lower left
Q4	quadrant 4	lower right

15. Soldering

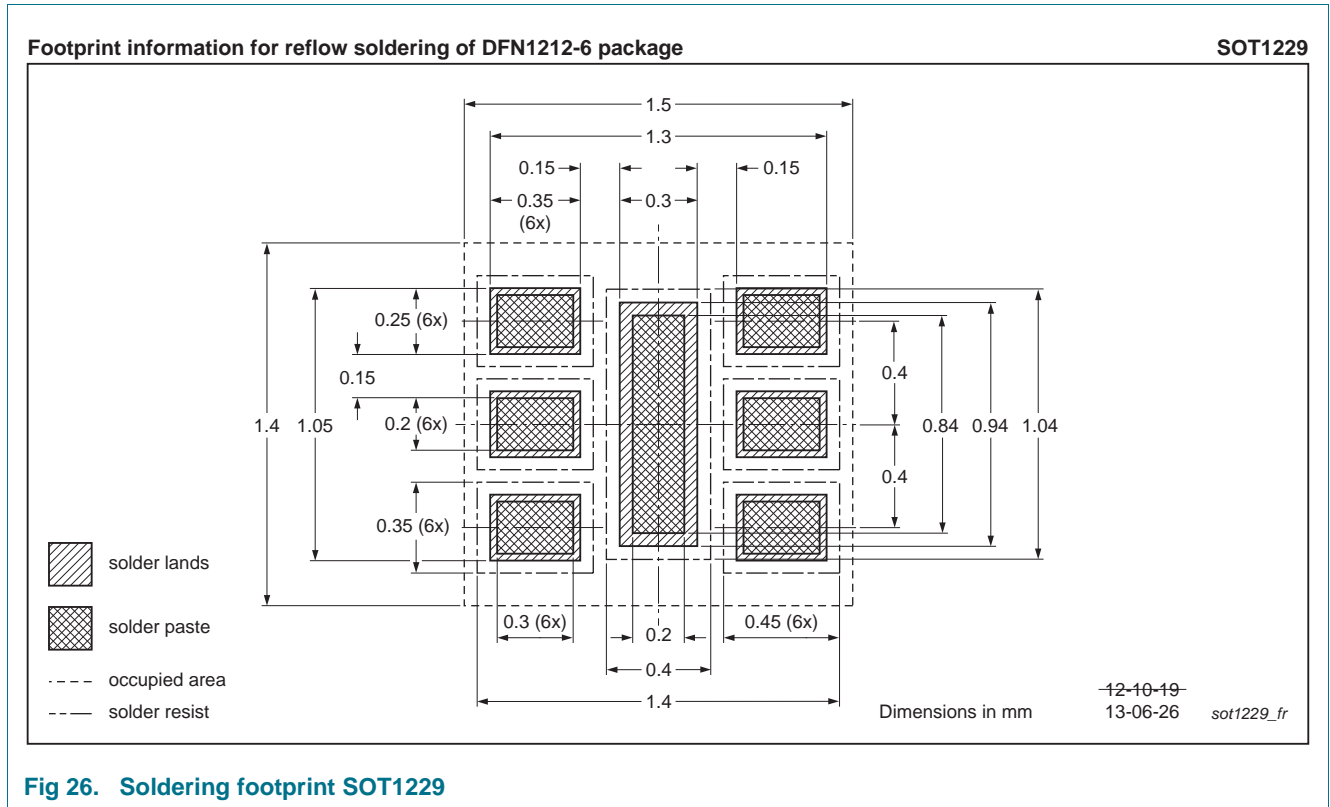


Fig 26. Soldering footprint SOT1229

16. PCB assembly guidelines for Pb-free soldering

Table 19. Assembly recommendations

Parameter	Value or specification
Solder screen thickness	100 μ m (0.004 inch)
Solder paste: Pb-free	SnAg (3 % to 4 %); Cu (0.5 % to 0.9 %)
Solder to flux ratio	50 : 50
Solder reflow profile	see Figure 27

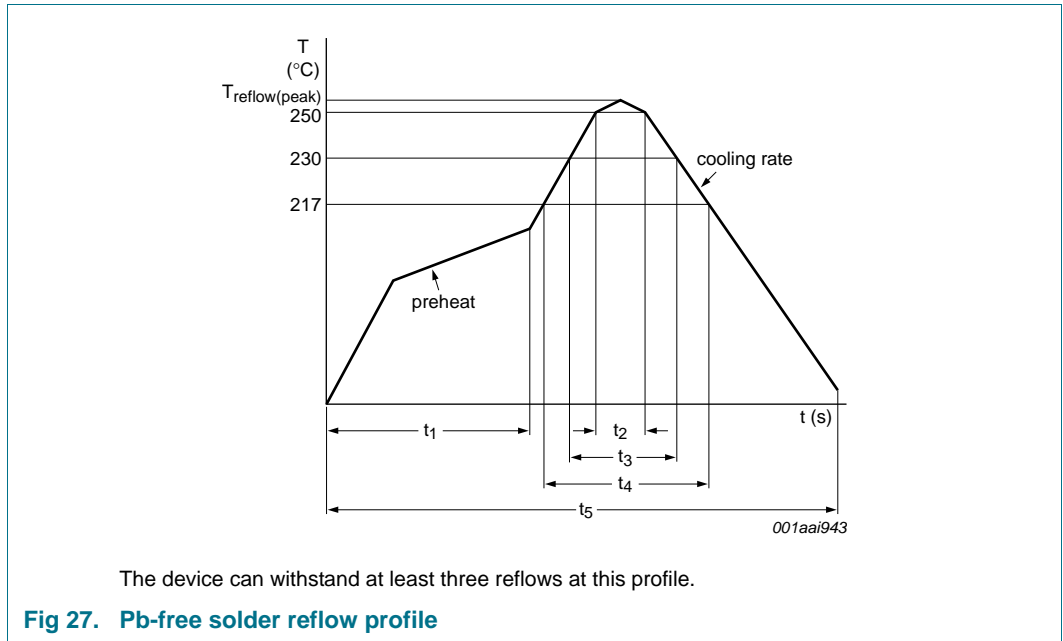


Table 20. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{\text{reflow(peak)}}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during $T \geq 250\text{ °C}$	-	-	30	s
t_3	time 3	time during $T \geq 230\text{ °C}$	10	-	50	s
t_4	time 4	time during $T > 217\text{ °C}$	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	-6	°C/s
		preheat	2.5	-	4.0	°C/s

17. Revision history

Table 21. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LD6915_SER v.1	20130708	Objective data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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