STRUCTURE Silicon Monolithic Integrated Circuit

PRODUCT NAME Dual Synchronous DC/DC converter controller

TYPE **BD9013KV**

FEATURES
- Wide Input Range
- Bult-in over current protect with Auto remove
- High Precision Reference Voltage
- Adjustable Frequency with synchronous function

O ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Parameter	Symbol	Limits	Unit	Parameter	Symbol	Limits	Unit
VCC Voltage	VCC	35 *1	V	VREG5,5A Voltage	VREG5,5A	7 *1	V
EXTVCC Voltage	EXTVCC	35 *1	V	SS1,2, FB1,2 Voltage	SS1,2, FB1,2	VREG5	V
VCCCL1,2 Voltage	VCCCL1,2	35	V	COMP1,2 Voltage	COMP1,2		
CL1,2 Voltage	CL1,2	35	V	RT, SYNC Voltage	RT, SYNC		
SW1,2 Voltage	SW1,2	35 *1	V	Power Dissipation	Pd	1.1 *2	W
BOOT1,2 Voltage	BOOT1,2	40 *1	V	Operating Temperature Range	Topr	-40~+85	°C
BOOT1,2-SW1,2 Voltage	BOOT1,2 -SW1,2	7 *1	V	Storage Temperature Range	Tstg	-55~+150	°C
EN1,2 Voltage	EN1,2	EXTVCC	V	Maximum Junction Temperature	Tj	+150	°C

*1 Do not however exceed Pd.
*2 Pd derated at 7mW/°C for temperature above Ta=25°C, Mounted on PCB 70mm × 70mm × 1.6mm.

O OPERATING CONDITIONS (Ta=25°C)

Parameter	Symbol	Min	Max	Unit
Supply Voltage 1	VCC, EXTVCC	3.9 *3	30	V
Supply Voltage 2	VCCCL, CL	3	VCC	V
BOOT−SW Voltage	BOOT−SW	3.9	VREG5	V
Oscillator Frequency	OSC	250	550	kHz
Synchronizing Frequency	SYNC	OSC	600*4	kHz

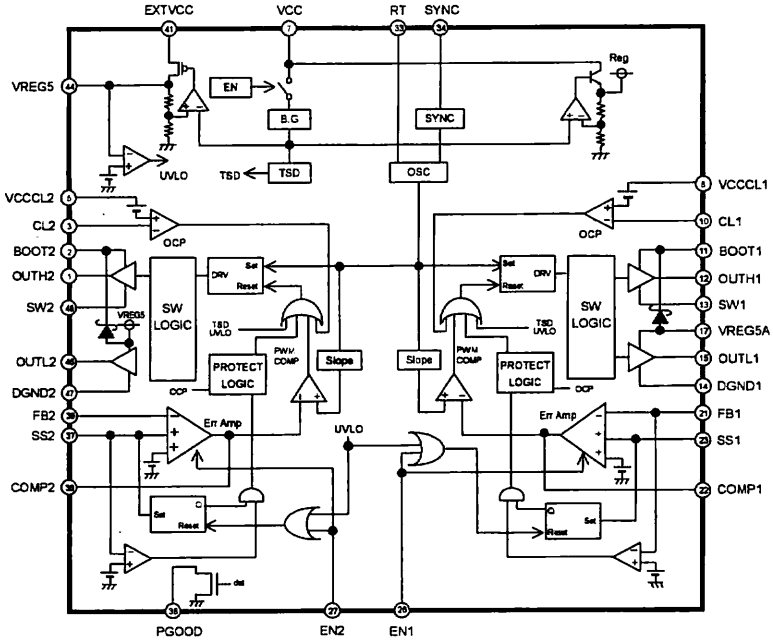
*3 After more than 4.5V, voltage range. In case of using less than 6V, short to VCC, EXTVCC and VREG5.
*4 Please do not exceed OSC×1.5.

*This product is not designed for normal operation within a radio active environment.
*Status of this document
The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

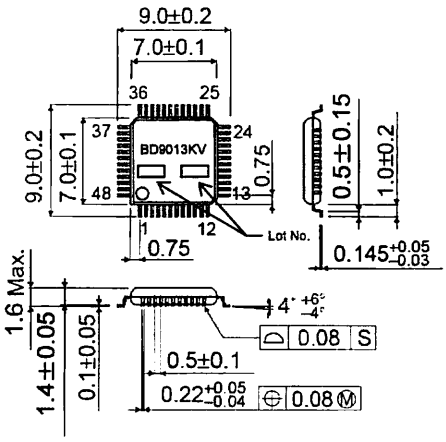
OELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=25℃ VCC/EXTVCC=12V EN1,2=5V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
VIN Bias Current	IIN	-	5	10	mA	
Stand-by Current	IST	-	0	10	μA	EN1, EN2=0V, VREG5 OFF
EN1,2 Low Voltage	VENth1	GND	-	1.0	V	EN=L ⇒ Output OFF
EN1,2 High Voltage	VENth2	2.6	-	Vcc	V	EN=H ⇒ Output ON
EN1,2 input Current	IEN	12	23	48	μA	VEN=5V
[VREG5]						
Output Voltage	VREG5	4.8	5	5.2	V	IREF=6mA
[UVLO]						
VREG5 Threshold Voltage	VREG_UVLO	3.5	3.7	3.9	V	VREG:Sweep down
VREG5 Hysteresis Voltage	DVREG_UVLO	100	200	400	mV	VREG:Sweep up
[Oscillator Section]						
Oscillator Frequency	FOSC	270	300	330	kHz	RT=100 kΩ
Synchronizing Frequency	Fsync	-	500	-	kHz	RT=100 kΩ SYNC=500kHz
SYNC Pulse Low voltage	Vsynclow	GND	-	0.5	V	
SYNC Pulse High voltage	Vsynchigh	2.5	-	7	V	
SYNC input Current	Isync	10	20	40	μA	Vsync=5V
[Error Amp]						
VO Bias Current	Ivo+	-	-	1	μA	
Comp Source Current	Isource	-14	-7	-3	mA	VFB=0.6V
Comp Sink Current	Isink	1	2	4	mA	VFB=1.0V
Reference Voltage	VOB	0.792	0.800	0.808	V	
[Soft Start]						
Charging Current	ISS	6.5	10	13.5	μA	Vss=1V
Discharging Current	IDIS	0.6	1.7	3	mA	Vss=1V,VCC=3V
Maximum Voltage	Vss_MAX	2.05	2.25	2.45	V	
Stand-by Voltage	Vss_STB	-	-	0.3	V	VCC=3V
[Over Current Protect]						
CL Threshold voltage	Vswth	70	90	110	mV	
CL Bias current 1,2	Iswin	-	-	10	μA	
Output Short Threshold	Vosh	0.46	0.56	0.66	V	VFB
Output Short det Threshold	Vodet	0.51	0.61	0.71	V	VFB
[PGOOD]						
PGOOD output sink current	Ipgoods	0.5	0.7	-	mA	PGOOD=1V, FB=0V
PGOOD output leak current	Ipgoodl	-	0	10	μA	PGOOD=1V, FB=0.8V
Over Voltage Threshold	VFBO	0.87	0.92	0.97	V	VFB

OBLOCK DIAGRAM



OPHYSICAL DIMENSIONS・MARKING



VQFP48C(単位:mm)

※Refer to the Technical Note about the details of the application.

OPin No. ・ Pin Name

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	OUTH2	High Side FET Gate Driver 2	25	N.C.	Non Connect
2	BOOT2	OUTH2 Driver Supply Input	26	EN1	Control Voltage Input 1
3	CL2	OCP Setting terminal by External Resistance 2	27	EN2	Control Voltage Input 2
4	N.C.	Non Connect	28	N.C.	Non Connect
5	VCCCL2	Supply Voltage for OCP 2	29	N.C.	Non Connect
6	N.C.	Non Connect	30	GND	Ground
7	VCC	Power Input	31	N.C.	Non Connect
8	VCCCL1	Supply Voltage for OCP 1	32	N.C.	Non Connect
9	N.C.	Non Connect	33	RT	Connect to External Resistor Setting Operating Frequency
10	CL1	OCP Setting terminal by External Resistance 2	34	SYNC	Synchronized Pulse Input
11	BOOT1	OUTH1 Driver Supply Input	35	N.C.	Non Connect
12	OUTH1	High Side FET Gate Driver 1	36	PGOOD	Power Good Terminal
13	SW1	High Side FET Source 1	37	SS2	Soft Start 2
14	DGND1	Low Side FET Source 1	38	COMP2	Error Amp Output 2
15	OUTL1	Low Side FET Gate Drive 1	39	FB2	Error Amp Inverting Input 2
16	N.C.	Non Connect	40	N.C.	Non Connect
17	VREG5A	FET Driver REG Input	41	EXTVCC	External Power Input
18	N.C.	Non Connect	42	N.C.	Non Connect
19	N.C.	Non Connect	43	N.C.	Non Connect
20	N.C.	Non Connect	44	VREG5	5V Regulator Output
21	FB1	Error Amp Inverting Input 1	45	N.C.	Non Connect
22	COMP1	Error Amp Output 1	46	OUTL2	Low Side FET Gate Driver 2
23	SS1	Soft Start 1	47	DGND2	Low Side FET Source 2
24	N.C.	Non Connect	48	SW2	High Side FET Source 2

NOTES FOR USE

1. Absolute maximum range
   Absolute Maximum Ratings are those values beyond which the life of a device may be destroyed we cannot be defined the failure mode, such as short mode or open mode. Therefore physical security countermeasure, like fuse, is to be given when a specific mode to be beyond absolute maximum ratings is considered.

2. GND pin voltage
   GND terminal should be connected the lowest voltage, under all conditions. And all terminals except SW should be under GND terminal voltage under all conditions including transient situations. If a terminal exists under GND, it should be inserting a bypass route.

3. Power dissipation
   If IC is used on condition that the power loss is over the power dissipation, the reliability will become worse by heat up, such as reduced output current capability. Also, be sure to use this IC within a power dissipation range allowing enough of margin.

4. Input supply voltage
   Input supply pattern layout should be as short as possible.

5. Electrical characteristics described in these specifications may vary, depending on temperature, supply voltage, external circuits and other conditions. Therefore, be sure to check all relevant factors, including transient characteristics.

6. Thermal Shut Down Circuit
   A temperature control is built in the IC to prevent the damage due to overheat. Therefore, the outputs are turned off when the thermal circuit works and are turned on when the temperature goes down to the specified level.

7. Mounting Failures
   Mounting failure, such as misdirection or mismount, may cause a malfunction in the device.

8. Internal circuits or elements may be damaged when Vcc and pin voltage are reversed. For example, Vcc short circuit to GND while an external capacitor is charged. Capacitor of Vreg5 output is recommended no larger than 12μF. In addition, inserting a Vcc series countercurrent prevention diode, or a bypass diode between the various pins and the Vcc, is recommended.

9. Malfunction may be happened when the device is used in the strong electromagnetic field.

10. We recommend to put Diode for protection purpose in case of output pin connected with large load of impedance or reserve current occurred at initial and output off.

11. Precautions for board inspection
    Connecting low-impedance capacitors to run inspections with the board may produce stress on the IC. Therefore, be certain to use proper discharge procedure before each process of the test operation. To prevent electrostatic accumulation and discharge in the assembly process, thoroughly ground yourself and any equipment that could sustain ESD damage, and continue observing ESD-prevention procedures in all handing, transfer and storage operations. Before attempting to connect components to the test setup, make certain that the power supply is OFF. Likewise, be sure the power supply is OFF before removing any component connected to the test setup.

12. GND pattern
    When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid voltage fluctuations in any connected external component GND.

13. SW Terminal
    A counter-electromotive force may generate a negative potential at the SW terminal during connection to the particular application. Therefore, it should be inserting a bypass route between SW to GND.

14. FET
    The shoot-through may happen when the input parasitic capacitance of FET is extremely big. Less than or equal to 1200pF input parasitic capacitance is recommended. Please confirm operation on the actual application since this character is affected by PCB layout and components.

15. External capacitor of VREG5
    An external capacitor is necessary for VREG5. Moreover, please insert the capacitor also in the terminal VREG5A. The insertion of the ceramic capacitor that ESR is low and the capacity is from 6.6 to 12μF in totals, is recommended to the terminal VREG5 and VREG5A.

16. External parts
    The circuit that discharge it BOOT and VREG5 (VREG5A) is necessary at EN=H→L, depending on use conditions.
    Please refer to a technical note for details of the discharge circuit.