FC95772LR4-C

Fujitsu® FC95772LR4 Compatible TAA 100GBase-LR4 CFP4 Transceiver (SMF, 1310nm, 10km, LC, DOM)

Features:

- CFP MSA 1.1 Compliance
- Duplex LC Connector
- Single-mode Fiber
- Commercial Temperature 0 to 70 Celsius
- Hot Pluggable
- Metal with Lower EMI
- Excellent ESD Protection
- RoHS Compliant and Lead Free

Applications:

- 100GBase Ethernet
- Access and Enterprise

Product Description

This Fujitsu® FC95772LR4 compatible CFP4 transceiver provides 100GBase-LR4 throughput up to 10km over single-mode fiber (SMF) using a wavelength of 1310nm via an LC connector. It is guaranteed to be 100% compatible with the equivalent Fujitsu® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

ProLabs' transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."

Rev. 051623

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	TS	-40		+85	˚C	
Power Supply Voltage	VCC	0		+3.6	V	+3.3V
Operating Case Temperature Range	Tc	0	25	70	˚C	
Optical Receiver Input	Pimax			+5.5	dBm	Average
Power Supply Noise	Vrip			2 3	% %	DC – 1MHz 1 – 10MHz

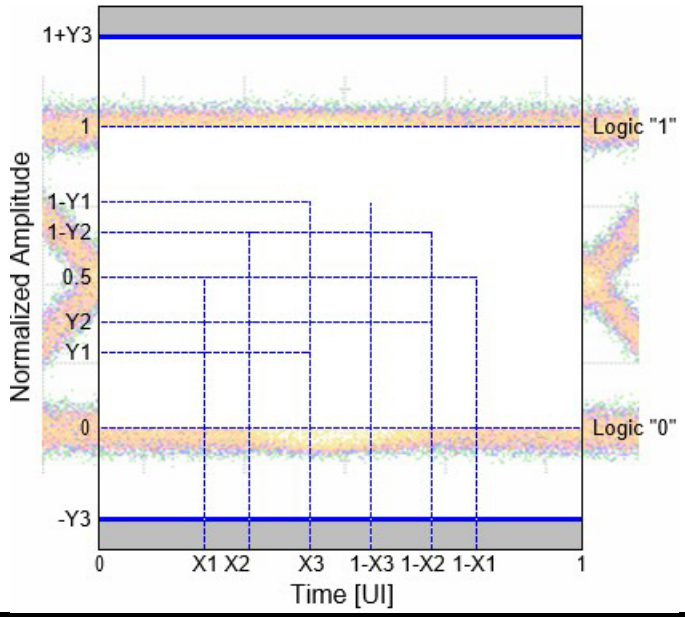
Optical Characteristics (Note 1)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter							
Channel data rate		fDC		25.78125		Gbit/s	2
Aggregate data rate		fD		103.125		Gbit/s	2
Signal speed variation from nominal		∆fD	-100		+100	ppm	2
Optical Center Wavelength	**Lane 0**	λ_{CT0}	1294.53		1296.59	nm	
	Lane 1	λ_{CT1}	1299.02		1301.09	nm	
	Lane 2	λ_{CT2}	1303.54		1305.63	nm	
	Lane 3	λ_{CT3}	1308.09		1310.19	nm	
Optical Output Power in OMA		OMA	-1.3		+4.5	dBm	3
Average Optical Output Power of Off Transmitter		Poff			-30	dBm	
Optical Waveform				Eye Diagram			2
Extinction Ratio		ER	4			dB	
Receiver							
Receiver Sensitivity in OMA		PminOMA	-8.6		+4.5	dBm	
Stressed Receiver Sensitivity in OMA		PminSOMA			-6.8	dBm	4
Receive Power, each lane in OMA					+4.5	dBm	

Notes:

1. Data Rate; NRZ, Mark Ratio 50%, PRBS=2^{31}-1, 1x10^{-12} BER unless otherwise specified.
2. Per IEEE 802.3ba specification
3. OMA=10$\log_{10}$[2P{(A-1)/(A+1)}], A = $10^{(ER/10)}$, P = $10^{(Pf/10)}$
4. Stressed Receiver Sensitivity measurement method is under study

Mask of Optical Output Eye Diagram



X1	X2	X3	Y1	Y2	Y3	Max hit ratio (Note)
0.25	0.4	0.45	0.25	0.28	0.4	5×10^{-5}

Note:

The acceptable ratio of samples inside to outside the hatched area (the “hit ratio”) must be met.

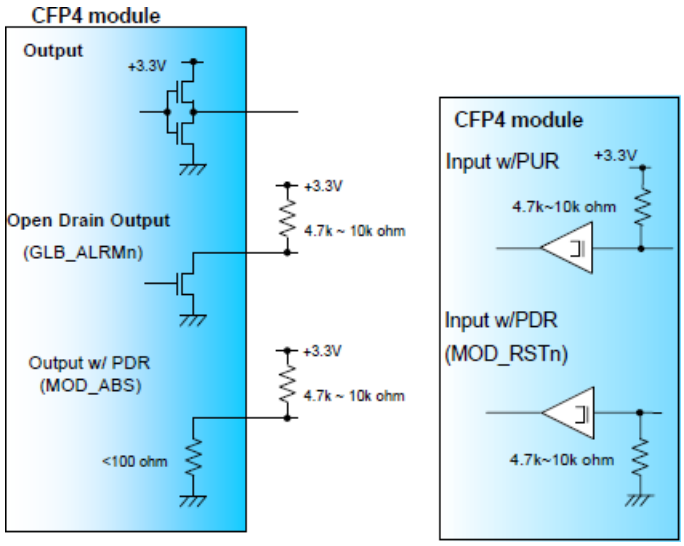
Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	VCC	3.2	3.3	3.4	V	
Supply Current	ICC			1.9	A	1
Supply Current @Low Power Mode	ICCL			0.3	A	
Power Consumption	P			6	W	
Power Consumption @Low Power Mode	Plow			1	W	
3.3V LVCMOS level						
Input High Voltage	VIH	2		VCC + 0.3	V	
Input Low Voltage	VIL	-0.3		0.8	V	
Input Leakage Current	IIN	-10		+10	μA	
Output High Voltage	VOH	VCC – 0.2			V	I_{OH}=-100μA
Output Low Voltage	VOL			0.2	V	I_{OL}=100μA
Minimum Pulse Width of Control Pin Signal	t_CNTL	100				μs
1.2 VLVCMOS Level						
Input High Voltage	VIH	0.84		1.5	V	
Input Low Voltage	VIL	-0.3		0.36	V	
Input Leakage Current	IIN	-100		+100	μA	
Output High Voltage	VOH	1.0		1.5	V	
Output Low Voltage	VOL	-0.3		0.2	V	
Output High Current	IOH			-4	mA	
Output Low Current	IOL	+4			mA	
Input capacitance	Ci			10	pF	

Notes:

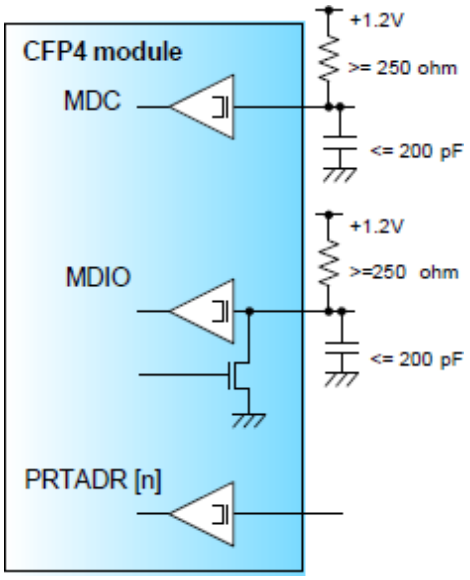
1. Maximum module current ramp rate is 100 mA /μs.

3.3V LVCMOS Interface



MDIO Interface

The below drawings, with maximum host load capacitance of 200pF, also define the measurement set-up for module MDC timing verification. The capacitor in the drawing indicates the stray capacitance on the line. Don't put any physical capacitor on the line.



High Speed Electrical Input Characteristics

Parameter	Symbol	Min.	Max.	Unit	Conditions
Differential Voltage Overload pk-pk	Module Input	900		mV	Calibrated at TP1a
Differential Termination Mismatch	Module Input		10	%	at 1 MHz
Differential Return Loss	Module Input		Note 1	dB	
Common Mode to differential conversion Loss	Host Output	Note 2		dB	

Notes:

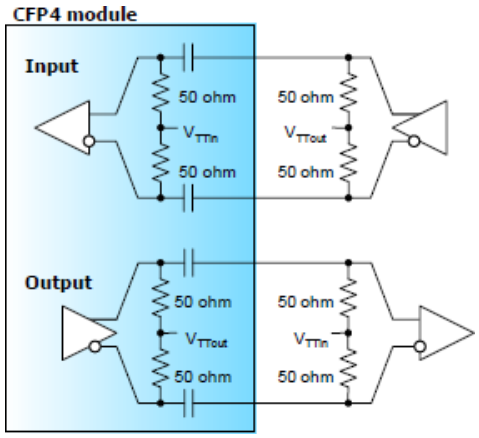
1. SDD11, SDD22 < -11dB for f<fb/7, SDD11, SDD22 < -6.0+9.2*log(2f/fb) dB for fb/7<f<fb (fb=25.78 GHz)
2. SDC11 < -25+20*(f/fb) dB for f<fb/2, SDC11 < -15 dB for fb/2<f<fb (fb=25.78 GHz)

High Speed Electrical Output Characteristics

Parameter	Direction	Min.	Max.	Unit	Conditions
Differential Voltage, pk-pk	Module Output		900	mV	
Common Mode Noise, rms	Module Output		17.5	mV	
Differential Termination Mismatch	Module Output		10	%	at 1 MHz
Differential Return Loss	Module Output		Note 1	dB	
Transition Time: 20/80%	Module Output	9.5		ps	
Vertical Eye Closure (VEC)			6.5	dB	
Eye width at 10-15 probability (EW15)	Module Output	0.57		UI	
Eye height at 10-15 probability (EH15)	Module Output	240		mV	

Notes:

1. SDD11, SDD22 < -11dB for f<fb/7, SDD11, SDD22 < -6.0+9.2*log(2f/fb) dB for fb/7<f<fb (fb=25.78 GHz)



High speed I/O for Data and Clocks

Transmitter & Receiver Monitor Clock Characteristics

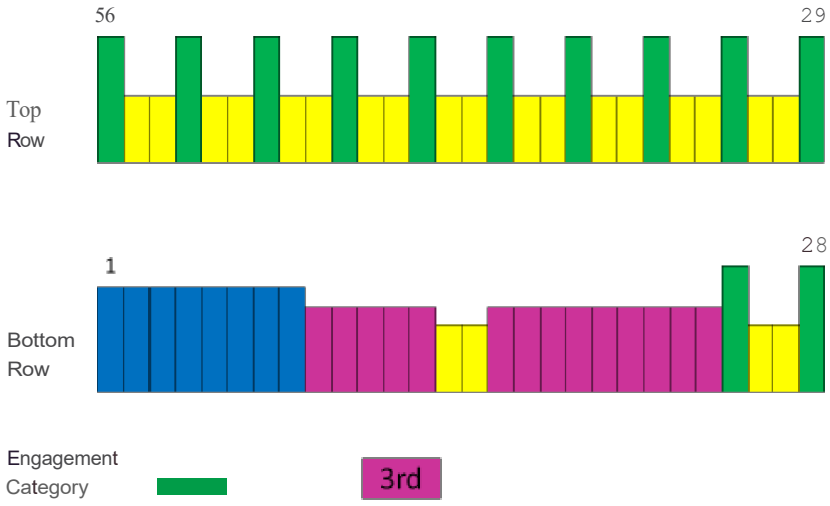
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock Differential Input Impedance	Zd	80	100	120	ohm	
Differential Output Clock Amplitude	V_{DIFF}	400		1200	mVpp	AC coupled CML
Reference Clock Duty Cycle		40		60	%	

Optical signal, Electrical signal, MCLK and REFCLK frequency relation

Parameter	Symbol	Rate	Unit	Remarks
Aggregate data rate	fDC	103.125	Gbit/s	
Optical signal rate per lane (Channel data rate)	fD	25.78125	Gbit/s	$f_{DC}/4$
Electrical signal rate per lane	fhost	25.78125	Gbit/s	
TXMCLK rate	fm	1/8 of network lane rate (3.22266 GHz) or 1/32 of network lane rate (805.665 MHz)		Default: Disabled Note 1
RXMCLK rate	fm	1/8 of network lane rate (3.22266 GHz) or 1/32 of network lane rate (805.665 MHz)		Default: disabled
REFCLK rate	fo	161.1328 ($f_{host}/160$)	MHz	MDIO reg. Selectable

Notes:

1. For optical signal measurement trigger



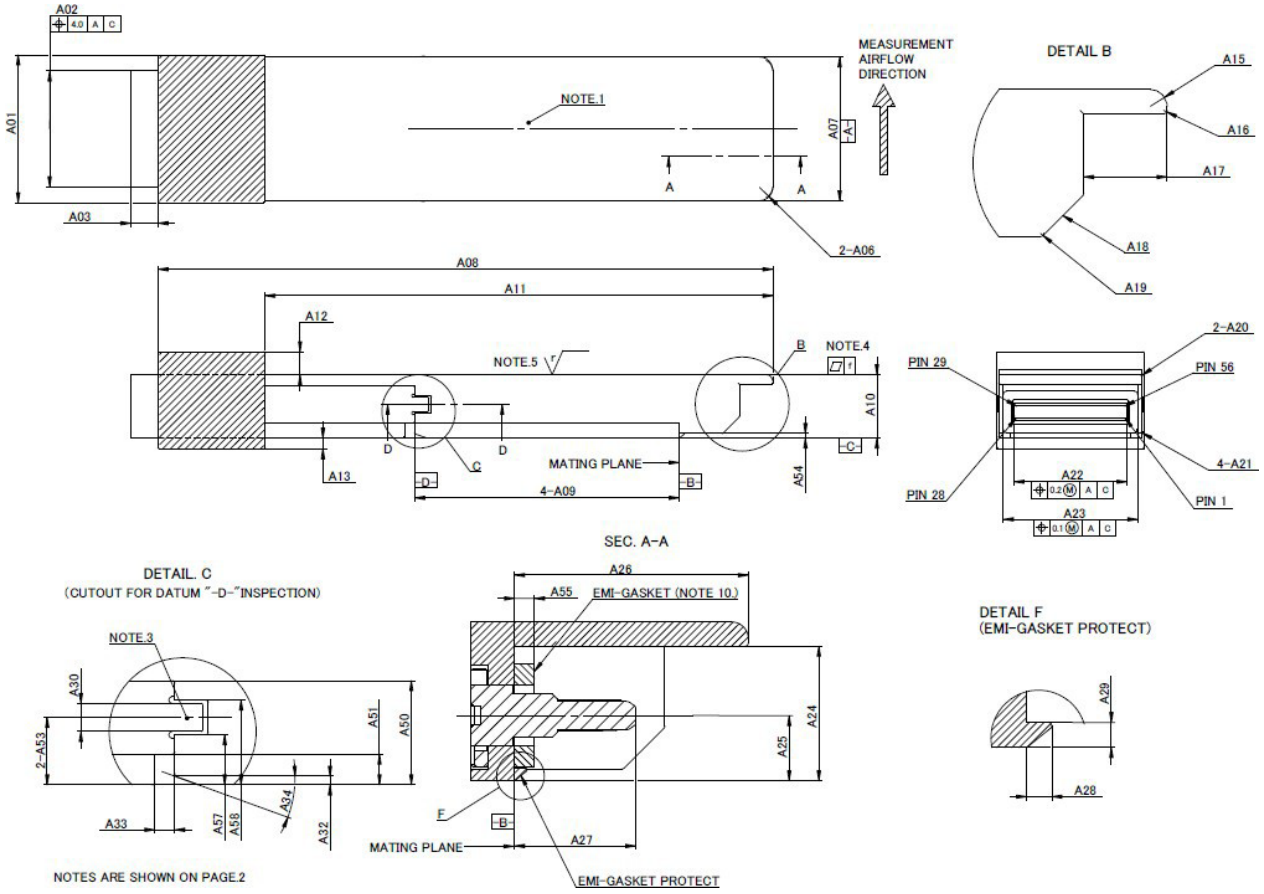
	CFP4 Bottom
1	**3.3V GND**
2	**3.3V GND**
3	3.3V
4	3.3V
5	3.3V
6	3.3V
7	**3.3V GND**
8	**3.3V GND**
9	VND 10 A
10	VND 10 B
11	TX DIS *(PRG CNTL1)*
12	RX LOS *(PRG ALRM1)*
13	GLB ALRMn,
14	MOD LOPWR
15	MOD ABS
16	MOD RSTn
17	MDC
18	MDIO
19	PRTADR0
20	PRTADR1
21	PRTADR2
22	VND 10 C
23	VND 10 D
24	VND 10 E
25	**GND**
26	*I{MCLKnJ*
27	*I{MCLKDI*
28	**GND**

	CFP4 Top
56	**GND**
55	TX3n
54	TX3o
53	**GND**
52	TX2n
51	TX2p
50	**GND**
49	TX1n
48	TX1o
47	**GND**
46	TX0n
45	TX0p
44	**GND**
43	*(REFCLKnJ*
42	*(REFCLKp)*
41	**GND**
40	RX3n
39	RX3p
38	**GND**
37	RX2n
36	RX2o
35	**GND**
34	RX1n
33	RX1p
32	**GND**
31	RXOn
30	RXOp
29	**GND**

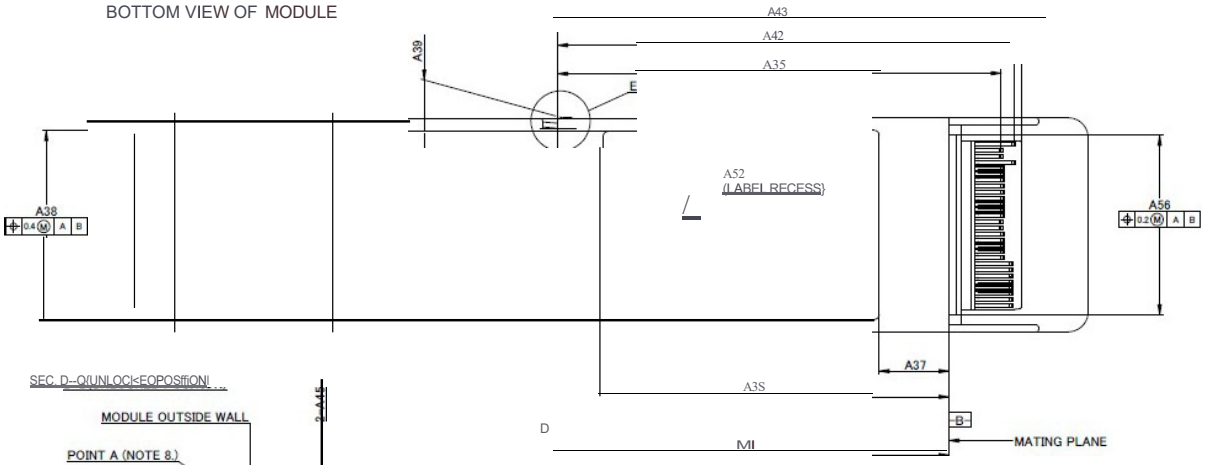
Pin Descriptions

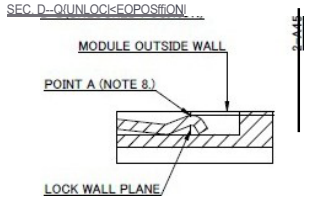
PIN	Name	I/O	Logic	Description
1	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separated or tied together with Signal Ground
2	3.3V_GND			
3	3.3V			
4	3.3V			
5	3.3V			
6	3.3V			3.3V Module Supply Voltage
7	3.3V_GND			
8	3.3V_GND			
9	VIND_IO_A	I/O		Module Vendor I/O A. Do Not Connect
10	VIND_IO_B	I/O		Module Vendor I/O B. Do Not Connect
11	TX_DIS (PRG_CNT L1)	I	LVCMOS w/PUR	Transmitter Disable for all lanes. "1" or NC: Transmitter disabled; "0": transmitter enabled. (Optionally configurable as Programmable Control1 after Reset)
12	RX_LOS (PRG_ALR M1)	O	LVCMOS w/PUR	Receiver Loss of Optical Signal. "1": low optical signal; "0": normal condition (Optionally configurable as Programmable Alarm1 after Reset)
13	GLB_ALR M	O	LVCMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register; "1": no alarm condition, Open Drain, Pull up Resistor on Host
14	MOD_LOP WR	I	LVCMOS w/PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode; "0": power-on enabled
15	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent; "0": module present, Pull up resistor on Host
16	MOD_RSTn	I	LVCMOS w/PDR	Module Reset. "0": resets the module; "1" or NC: module enabled, Pull down Resistor in Module
17	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per IEEE Std 802.3-2012)
18	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3ae-2008 and ba-2010)
19	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
20	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
21	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
22	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect
23	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect
24	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect
25	GND			
26	(MCLKn)	O	CML	For optical waveform testing. Not for normal use
27	(MCLKp)	O	CML	For optical waveform testing. Not for normal use
28	GND			

Mechanical Specifications



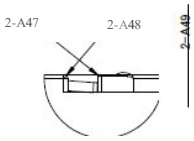
BOTTOM VIEW OF MODULE

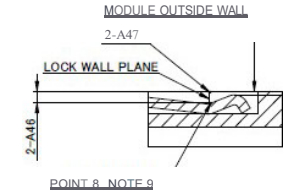




DETAJLE

(CUTOUT FOR DATUM "-0-"INSPECTION)





POINT 8 NOTE 9

NOTE

I. 7deg C MAXIMUM TEMPERATURE DELTA WITH NOHEATSINK ANO 200LFM SIDEWAYS AIA FLOW. (DELTATEMPERAn.JRE SPECIRCATION TO SE VERCAEO WITH FIRST ARTICLES).
2. DRAFT ANGLE TO BE IN THE OECREASCNG MA$$ DIRECTION.
3. MODULE LATCH POSffiON MUST INTEROPERATE WITH CFP4 CAGE SPEC[FJCATIONS.
4. SURFACE FLATNESS: "I" ISSPECIAEO IN CFP4 HARDWARE SPECIACATION.
5. SURFACE ROUGHNESS: "r" ISSPECIFIED IN CFP4 HARDWARE SPEC(FJCATION.
6. DIMENSION APPLIES TOLATCHMECHANISM.
7. MAXIMUM OUTSJOE ENVELOP BETWEEN TWO OPPOSITE LATCHES.
8. "?OINT A" IS ATTHE VUITUAL INTERSECTION OF LOCK WALL PLANE AND OUTER SURrACE OFLATCH.
9.. POINT 8" IS AT THE VIRTIJAL INTERSECTION OF LOCK WALL PLANE AND OUTER SURFACE OF LATCH.
IO. GASKET TO MEET MINIMUM PEELS STRENGTH : 30 Oz/in or 335 gf/cm per ASTM 03330test method.

About ProLabs

Our experience comes as standard; for over 15 years ProLabs has delivered optical connectivity solutions that give our customers freedom and choice through our ability to provide seamless interoperability. At the heart of our company is the ability to provide state-of-the-art optical transport and connectivity solutions that are compatible with over 90 optical switching and transport platforms.

Complete Portfolio of Network Solutions

ProLabs is focused on innovations in optical transport and connectivity. The combination of our knowledge of optics and networking equipment enables ProLabs to be your single source for optical transport and connectivity solutions from 100Mb to 400G while providing innovative solutions that increase network efficiency. We provide the optical connectivity expertise that is compatible with and enhances your switching and transport equipment.

Trusted Partner

Customer service is our number one value. ProLabs has invested in people, labs and manufacturing capacity to ensure that you get immediate answers to your questions and compatible product when needed. With Engineering and Manufacturing offices in the U.K. and U.S. augmented by field offices throughout the U.S., U.K. and Asia, ProLabs is able to be our customers best advocate 24 hours a day.

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