User's Guide

LP8764x-Q1 Evaluation Module

ABSTRACT

The LP8764x-Q1 Evaluation Module (EVM) highlights the performance and flexibility of the LP8764x-Q1 power management integrated circuit (PMIC). The modular design allows the EVMs to be stacked to provide a multi-PMIC solution with a single PMIC acting as the controller and up to five PMICs as target. This document should be used in conjunction with the Scalable PMIC's GUI User's Guide and the LP8764-Q1 Four-Phase, 20-A Buck Converter With Integrated Switches datasheet.

	Caution	Caution Hot surface. Contact may cause burns. Do not touch!

High current connectors are marked with maximum current text next to the corresponding connector.

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1 Introduction

The LP8764x-Q1 power management integrated circuit (PMIC) family is extremely flexible and scalable, providing configurability at the device and system level. At the device level, a single PMIC can provide up to four separate step down converters (buck regulators). These buck regulators can be used in multiphase mode to provide a single 20 A source. At the system level, several PMICs can be configured to work in a controller-target topology with one controller and up to five target PMICs. The LP8764x-Q1 evaluation module (EVM) is both an evaluation and development tool. With the EVM both device level and system level configurability are available through an easy to use graphical user interface (GUI) tool.

Table 1-1 shows the available controller and target EVMs, the silicon associated with those EVMs, the initial non-volatile memory (NVM) configuration, and the hardware components associated with the configurations. Because of the configurable nature of both the part and the EVM, any EVM can be configured as a controller or target device.

Table 1-1. EVM Descriptions

EVM Part Number	PMIC Device Part Number	NVM Phase Configuration	f_{SW}	Populated phase components	
				R1-R7	J3-J8
LP87642Q1EVM	LP876411E2RQKRQ1	4-phase, single output: BUCK1+BUCK2+BUCK3+BUCK4	2.2MHz	R1, R2, R5 and R6	J3-J8
LP87644Q1EVM	LP876441E4RQKRQ1	4-output: BUCK1, BUCK2, BUCK3, BUCK4	4.4MHz	R1, R3, R4 and R7	-

2 Getting Started

Only a power supply and the EVM are required to evaluate and test the LP8764x-Q1 default configuration under load conditions. This section contains the controller and controller+target configurations and how to run these two default configurations.

2.1 Getting Started: Single EVM

1. Connect Power to the EVM.
2. Connect the EVM to the Host PC through the USB. If the power is provided by the USB cable, apply the appropriate jumper connection to connect EN_5V0 with 3.3V and VCCA with 5.0V, see Table 3-5.
3. Launch the GUI and evaluate.

Terminal J9, labeled VCCA in Figure 2-1, can accept wire gauges up to 14 AWG. The voltage supplied must be within the input range of the device, 2.8 V to 5.5 V. The power supply providing the input to VCCA is required to supply 135 % of the output power. Once power has been supplied to VCCA, the GPIO4 / ENABLE jumper can be used to power on the output rails (in LP87644Q1EVM GPIO2 can be used to control BUCK4 after GPIO4 has been set high). The default ON Request for the controller device is the ENABLE pin which is a level sensitive input. Please refer to LP8764-Q1 datasheet for more details.

Figure 2-1 shows the LP8764x-Q1 EVM (controller).

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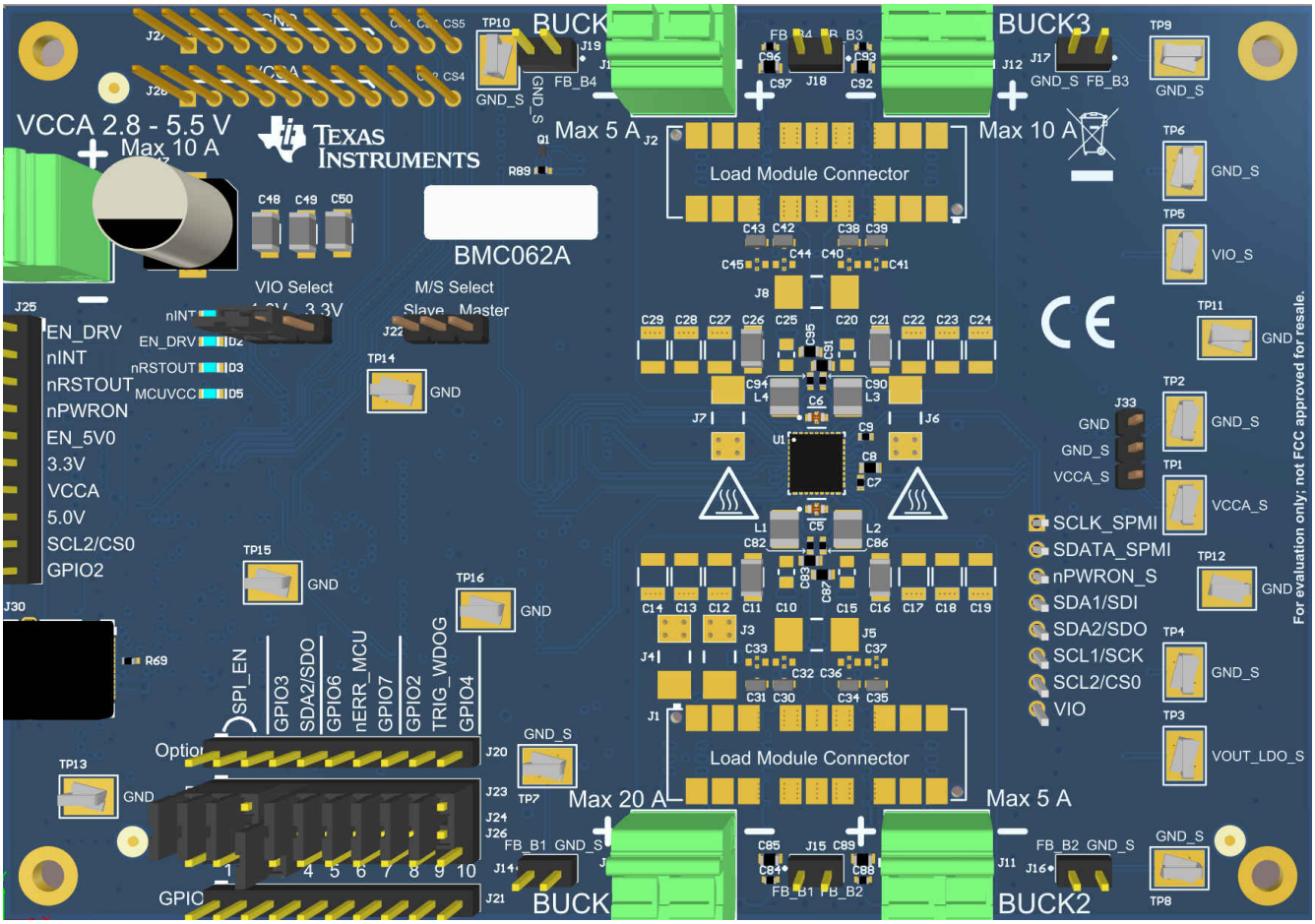

Figure 2-1. EVM Top View

2.2 Getting Started: Multiple EVM Evaluation

1. Connect Power to one EVM and remove the jumpers on all EVMs shorting 5.0V with VCCA and EN_5V0 with 3.3V (J25). All VCCA and GND power pins are shared between the stacked EVMs. Remove the VIO jumper (J32) from the target EVM.
2. Connect controller EVM to the Host PC through the USB. In the event that the power is provided by the USB cable, apply the appropriate jumper connection to connect VCCA with 5.0V and 3.3V with EN_5V0 as shown Table 3-5.
3. Stack controller EVM and target EVM(s). For convenience it is recommended to place the controller on the top of the stack.
4. Launch the GUI and evaluate.

The EVM can be powered solely from the 5 V USB connection, provided that the total power taken from the USB port is less than 2 W. This removes the requirement for a separate supply when evaluating a number of the digital features of the PMIC with the EVM.

The distinguishing characteristics of the target EVM are the PMIC and the jumper position on J22. With the jumper on J22 placed in the target position, SPMI connection between controller and target EVMs is enabled. When EVM is defined as target the EVM I2C pull-ups are disabled to avoid too strong pull-up on I2C bus. Once the controller and target devices are stacked, supplying power on J9 is the only requirement for getting started. VCCA is distributed across all stacked boards through J28. The power supply can be applied to any of the available J9 terminals in the stack.

2.3 GUI Tool

Texas Instruments provides a GUI tool to enable, configure, and evaluate the various features of the LP8764x-Q1 with the EVM. Please refer to the GUI User's Guide for a more detailed description of this tool.

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The GUI will run on most PC platforms and requires an available USB port. The EVM USB connector is type-C and a type-A to type-C cable is provided with the EVM to connect to the host computer. The EVM will enumerate as two COM ports and one additional port for the device firmware updates. The GUI should be using ACCtrl COM port which can be found from the device manager of the operating system. The COM port can be changed from the GUI from Options - Serial port menu.

A tool for estimating the efficiency of LP8764-Q1 device is also available called PMIC Efficiency Estimator Tool. The tool can be accessed here.

3 EVM Details

The following sections describe the various interfaces for measuring and controlling the configuration. Note: the configurations are in coordination with the settings of the PMIC. It is important to understand that both the EVM configuration and the settings of the PMIC must match. For example, if the GUI is used to change the PMIC interface to SPI from I^2C, then the appropriate SPI related jumpers should be in place on J20 and J25. Please refer to the GUI User's Guide SLVUBT8 on how to update the PMIC communication protocol.

3.1 Terminal Blocks

The terminal blocks are simple push and release terminals which can accommodate wire sizes up to 14 AWG. Table 3-1 lists the terminal blocks found around the perimeter of the EVM. J9, VCCA, is the input voltage for the regulators. The rest of the terminal blocks are for the BUCK outputs.

Table 3-1. Terminal Blocks

Terminal	Designator	Description
VCCA	J9	All Regulator Input, 2.8 V to 5.5 V Range
BUCK1	J10	Buck 1 Output, 5 A Capable
BUCK2	J11	Buck 2 Output, 5 A Capable
BUCK3	J12	Buck 3 Output, 5 A Capable
BUCK4	J13	Buck 4 Output, 5 A Capable

3.2 Test Point Descriptions

Numerous test points are provided to access voltages and signals. Test points marked with _S are designed for sensing voltages only and are not designed to carry large DC currents.

Table 3-2. Test Point Descriptions

Test Point	Device Pin	Description
TP1	VCCA_S	VCCA voltage sense point. Routed from close to the VCCA pin of the LP8764-Q1.
TP2, TP4, TP6, TP7, TP8, TP9, TP10	GND_S	Ground sense points routed from various locations.
TP3	VOUT_LDO_S	Voltage sense point for the internal LDO output voltage.
TP5	VIO_S	VIO voltage sense routed from the VIO pin of the LP8764-Q1.
TP11, TP12, TP13, TP14, TP15, TP16	GND	Solid ground points. Are able to carry larger DC currents.
J14, J16, J17, J19	FB_B1, FB_B2, FB_B3, FB_B4	Buck output voltage sense points. Secondary buck unused FBs are possible to use as voltage monitor as well.

3.3 Configuration Headers

There are four headers available to configure the EVM function. Header J22 configures controller and target mode of operation. Header J20, as shown in the silk screen picture in Figure 3-1, is used to configure the EVM to match the feature setting written to the LP8764x-Q1 configuration registers. J32 is used to select the PMIC IO voltage, either 1.8 V or 3.3 V. The fifth header is J25 which allows VCCA to be powered from the USB connection and the configuration of GPIO2, I2C2 or SPI.

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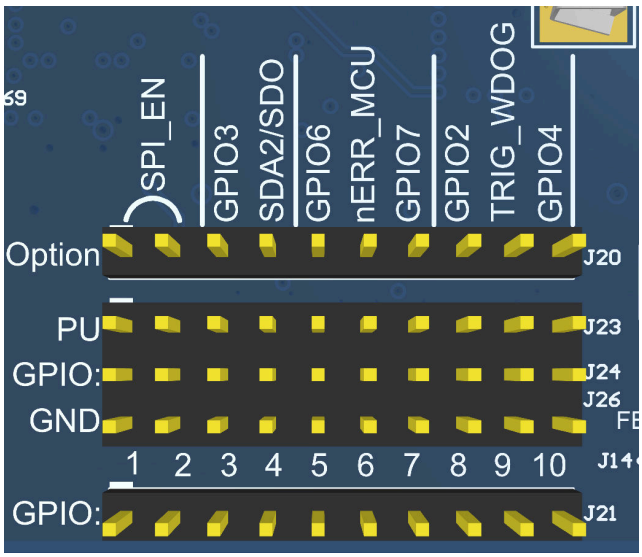

Figure 3-1. EVM Header J20

Table 3-3. Header J20 Description

Option Pins	Configuration	Description	
SPI_EN	Open (Default)	I²C Mode. The signal path for I²C communication between the MCU and the PMIC is enabled.	
	Closed	SPI mode. The signal path for SPI communication between the MCU and the PMIC is enabled.	
GPIO3, SDA2/SDO	Open (Default)	GPIO mode. GPIO2 from PMIC is connected to PM7 of the MCU through a level translator.	
	GPIO3,SDA2/SDO: Closed	I²C Mode (J20 VIO, I2C/SPI: Open)	Q&A Watchdog mode. GPIO3 of the PMIC should be in the Alternative function to support the Q&A Watchdog and the I²C mode is selected. This setting should also be done on connector J25 by closing GPIO2 to SCL2/CS if I2C2 is wanted to be used.
		SPI mode (J20 VIO, I2C/SPI: Closed)	SPI mode, Chip Select. GPIO2 and GPIO3 of the PMIC should be in the Alternative function to support SPI communication. This setting should also be done on connector J25 by closing GPIO2 to SCL2/CS if I2C2 is wanted to be used.
GPIO6, nERR_MCU, GPIO7	Open (Default)	GPIO mode. GPIO6 of the PMIC is connected to PP5 of the through a level translator.	
	GPIO6, nERR_MCU Closed	System error count down input signal from the MCU. VIO Select must be 3.3 V. GPIO6 or GPIO7 of the PMIC should be in the Alternative function to support the system error count down from the MCU.	
	nERR_MCU, GPIO7 Closed		
GPIO2, TRIG_WDG, GPIO4	Open (Default)	GPIO mode. GPIO7 of the PMIC is connected to PH0 of the through a level translator.	
	GPIO2, TRIG_WDG Closed	Trigger signal for trigger mode watchdog. VIO Select must be 3.3 V. GPIO7 or GPIO6 of the PMIC should be in the Alternative function to support the trigger mode watchdog signal.	
	TRIG_WDG, GPIO4 Closed		

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Table 3-4. Header J32 VIO Voltage Select

Configuration	Description
Open	Not Allowed for single or controller EVM, 1.8 V or 3.3 V must be selected. Leave open on target EVM.
VIO Select, 3.3 V: Closed (Default)	VIO is 3.3 V.
VIO Select, 1.8 V: Closed	VIO is 1.8 V.

Table 3-5. Header J25, VCCA, GPIO2/I2C/SPI

Configuration	Description	
3.3V, VCCA: Closed (Default)	3.3 V from TLV733P-Q1 (U11) is connected to VCCA. The input for U11 is the 5 V from the USB connection (VBUS). VBUS is not intended to support heavy load conditions. 2 W should be the maximum power drawn from the USB.	
EN_5V0, 3.3V, VCCA, 5.0V Open	On board 5V regulator is disabled and VCCA isolated from other on board supplies. VCCA should be powered from J9.	
EN_5V0, 3.3V: Closed	5V on board regulator (powered from USB) is enabled. 5V regulated supply can be used to power VCCA.	
VCCA, 5.0V: Closed	5V on board regulator (powered from USB) is connected to the LP8764-Q1 VCCA. 5V on board regulator is not intended for heavy load condition.	
SCL2/CS, GPIO2: Open	GPIO mode. GPIO2 of the PMIC is connected to IO2 of the MCU.	
SCL2/CS, GPIO2: Closed (Default)	I^2C mode (J22 SPI_EN: Open)	Q&A Watchdog mode. GPIO2 and GPIO3 of the PMIC should be in the Alternative function to support the Q&A Watchdog and the I^2C mode selected. This setting should also be done on connector J20 by closing GPIO3 to SDA2/SDO if I2C2 is wanted to be used.
	SPI mode (J22 SPI_EN: Closed)	SPI mode, Chip Select. GPIO2 and GPIO3 of the PMIC should be in the Alternative function to support SPI communication. This setting should also be done on connector J20 by closing GPIO3 to SDA2/SDO.

Note

The PMIC device can be configured for a power good level of 3.3 V or 5.0 V for the VCCA pin. If VCCA_VMON feature is enabled please check that the input voltage is correct and use sense connection to compensate IR voltage drop with heavy load currents. Align the VCCA/3.3V/5.0V jumper with the PMIC configuration. The default PMIC configuration supports the whole recommended VCCA voltage range.

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3.4 Stack-up Headers

As shown in Figure 3-2, multiple boards can be configured into a controller-target relationship (1 controller and up to 5 targets) and physically stacked upon each other. Stacked boards can be either LP87642Q1EVM, LP87644Q1EVM, TPS65941111EVM or TPS65941212EVM evaluation modules. VCCA and GND are shared between boards on headers J27 and J28. Communication between the boards is shared on header J29. This header, J29, is marked on the bottom silkscreen, as shown in Figure 3-3.

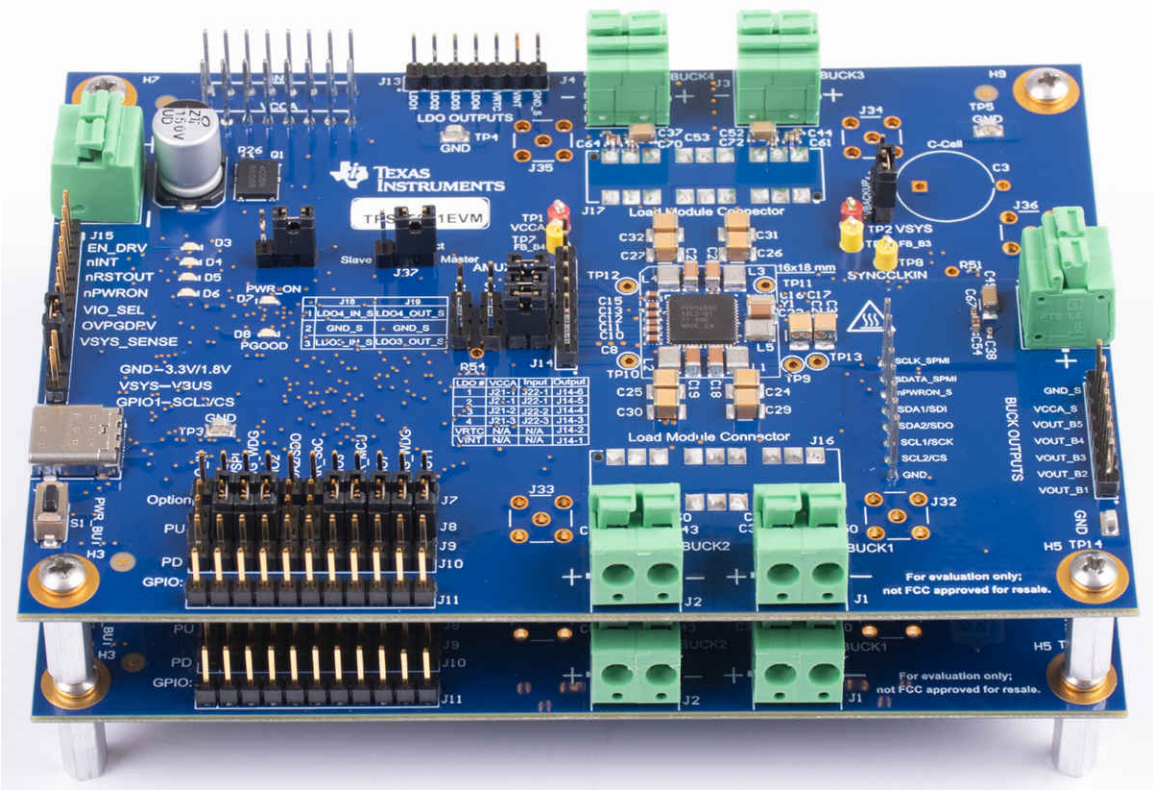

Figure 3-2. EVM Controller-Target Configuration

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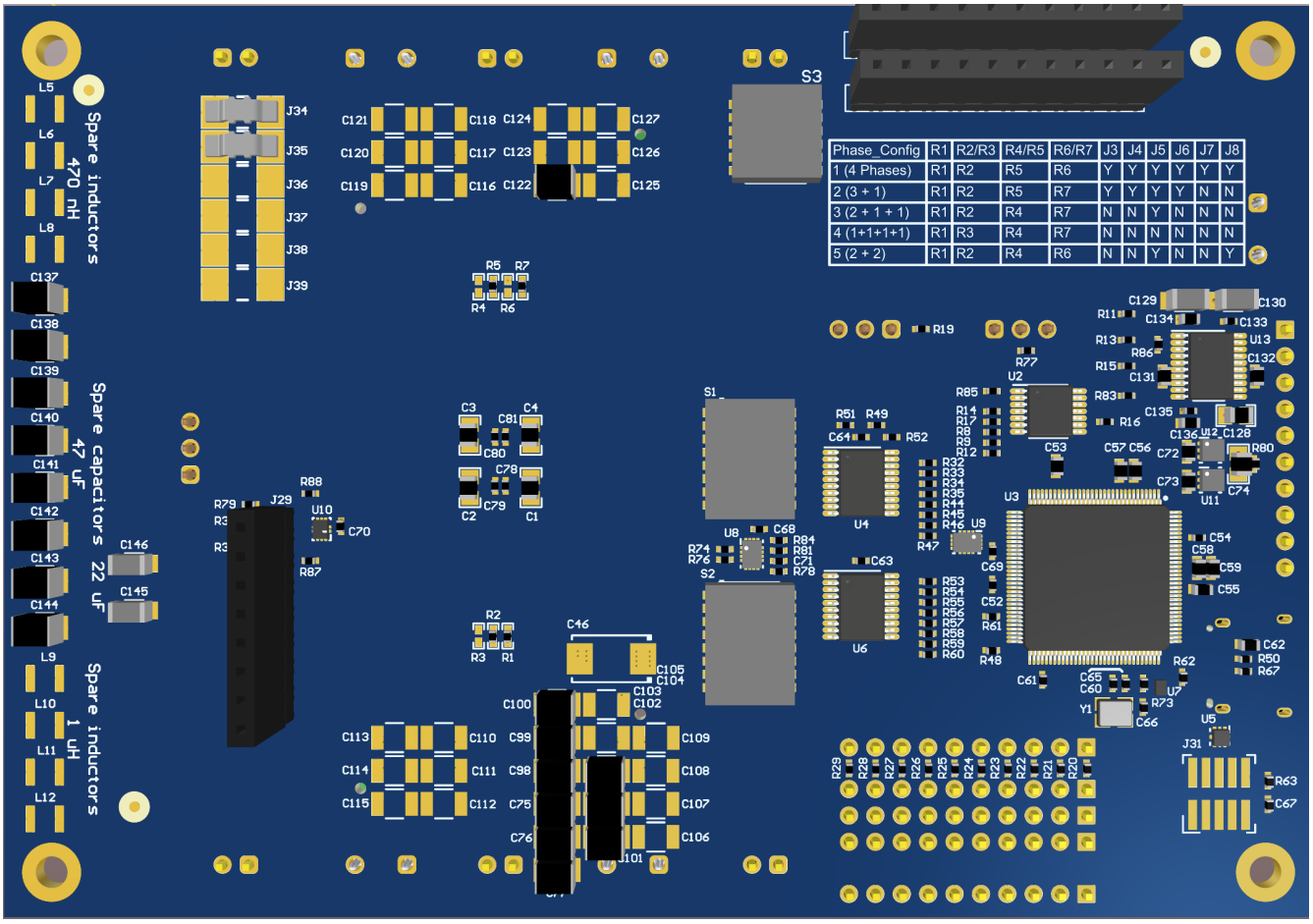

Figure 3-3. EVM Bottom View

Setting J22 to controller position connects nPWRON signal from controller to target through nPWRON_S pin on connector J29. This signal allows a SPMI connection between controller and target PMICs. Jumper J22 needs to be set to target position on target EVMs to disable pull-up resistors. By using this stackup configuration, the power up sequences of one or more target EVMs will always follow the controller.

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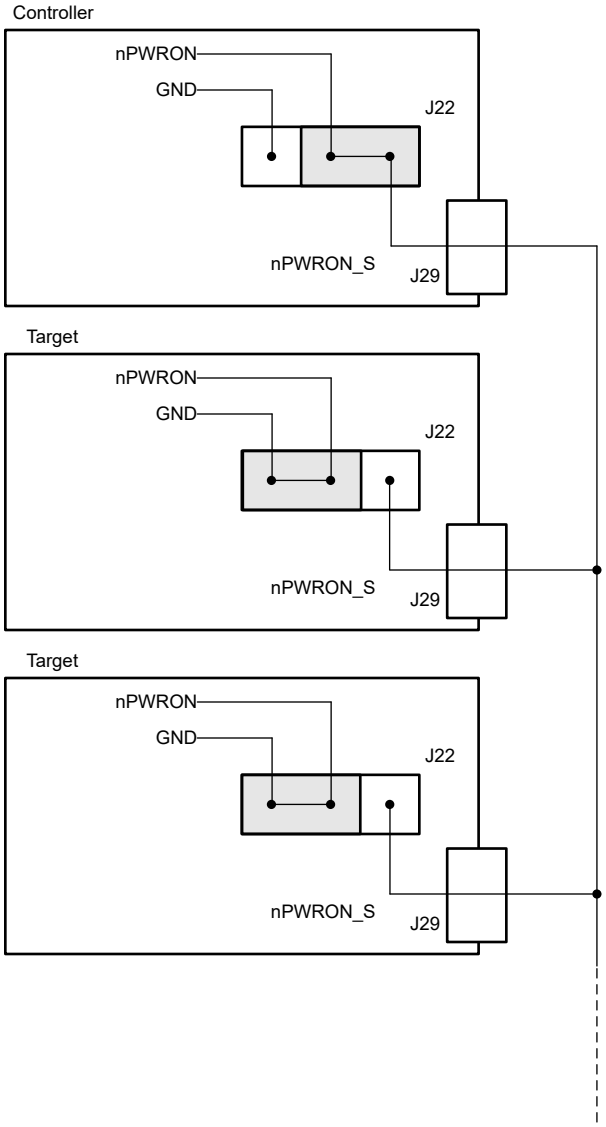

Figure 3-4. Header J22, Recommended Power Sequence (Enable) for Controller and One or More Targets

Table 3-6. Header J22 Controller/target Select

Configuration	Description
Open	When used as a single PMIC (no stacking). The controller EVM can use GPIO8 and GPIO9 to be connected to a MCU on EVM. I2C pull-up resistors are enabled.
Target, M/S Select: Closed	Target Mode. The target EVM can use GPIO8 and GPIO9 for SPMI communication between PMICs. I2C pull-up resistors are disabled on target EVMs.
M/S Select, Controller: Closed	Controller Mode. The controller EVM can use GPIO8 and GPIO9 for SPMI communication between PMICs. I2C pull-up resistors are enabled on controller EVM.

3.5 Connectors

Two load module connector footprints are provided, J1 and J2. These load module connectors are intended to be used with PMICLOADBOARDEVM which is sold separately. The connector components are not populated and the required connectors are shipped with PMICLOADBOARDEVM.

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3.6 Dip Switches

There are three DIP switches S1, S2, and S3 on the back side of the PCB. S1 and S2 switches allow the user to disconnect the level shifter from the PMIC GPIOs or serial interfaces. The level shifter has pull-ups on the MCU side that can cause unwanted high state on the GPIO signals if configured in high impedance state. S3 switch is used for configuring chip select for target device in multi PMIC/stacked use case. See the Table 3-7 for the descriptions of the switches.

Table 3-7. Dip switches

Switch	Pin	Signal line
S1	1-16	SDA_I2C1/SDI_SPI
	2-15	SCL_I2C1/SCK_SPI
	3-14	SDA_I2C2/SDO_SPI
	4-13	SCL_I2C2/CS_SPI
	5-12	GPIO1
	6-11	GPIO2
	7-10	GPIO3
	8-9	GPIO4
S2	1-16	GPIO5
	2-15	GPIO6
	3-14	GPIO7
	4-13	GPIO8
	5-12	GPIO9
	6-11	GPIO10
	7-10	Not connected
	8-9	nINT
S3	1-12	CS5
	2-11	CS4
	3-10	CS3
	4-9	CS2
	5-8	CS1
	6-7	GPIO2

3.7 EVM Control and GPIO

The EVM has a built-in USB interface based on the MSP432E401Y (U3) to allow the GUI, from the host computer, to communicate with the PMIC. The supply voltage required by the MSP432E401Y is generated automatically by the TLV73333PQDRVRQ1 (U11) and TLV73318PQDRVRQ1 (U12) LDOs which provides 3.3V and 1.8V from USB power, +VBUS. These voltages are available for supplying VIO for the PMIC (selectable from J32). Two SN74GTL2003 level shifters (U4, U6) are used in order to support the use case of the PMIC VIO of 1.8 V (the MCU IO will always be 3.3 V). In addition to the level shifters, the TS3A5018RSVR (U8) switch is used to apply the pullup voltages to the I^2C lines only when the EVM is configured as controller (J22). Additional TS3A5018RSVR (U9) switch for SPI enable/disable. The application of the pullup resistors is for I^2C mode only and is only intended for one board in a stack-up application. Note: in the stack-up configuration only controller board can have a valid +VBUS voltage on the board. This means that the controller board can have a connected USB cable supplying +VBUS and that controller board VCCA can be connected to +5.0V through J25, see Table 3-5. The EVM has 4 LEDs to indicate board power, on or off, and some pre-defined PMIC GPOs status. The signals are listed in Table 3-8.

Table 3-8. EVM LED Indicators

LED Designator	Indication
D1	LED is on when nINT is low.
D2	LED is on when EN_DRV is high.
D3	LED is on when nRSTOUT is low.

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Table 3-8. EVM LED Indicators (continued)

LED Designator	Indication
D5	EVM power indicator.

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4 Customization

The EVM, in conjunction with GUI tool, provides various degrees of customization. A couple of examples are provided here which can be generalized to a number of functions. There are spare components assembled on the EVM to help with the customization, namely inductors L5...L12, capacitors C137...C146, and jumper bridges J34...J39.

4.1 Changing the Communication Interface

The default settings for communication with the PMIC is I^2C. Changing to SPI requires a minor change to the jumper settings and those settings will change in the case of multiple EVMs in a stackup configuration. These jumper settings are highlighted in red in Figure 4-1. The first jumper to place is on the SPI_EN option on connector 20. Placing this jumper will connect the micro controller to the SPI bus which is connected to all available PMICs through the EVM stack connection through J29. In a multiple EVM stackup, this jumper should only be placed on the controller EVM with the USB connection to the host computer. The SPI does not have a device ID and therefore the chip select is used to determine which PMIC will receive and respond to commands on the SPI bus. The signals SCL2/CS and GPIO2 on J25 should only be jumpered on the controller EVM which connects to the USB. Stacked target EVMs should have the CS selected with the S3 dip switch on the bottom of the board. For example with first target board GPIO2 switch and SPI_CS1 switches should be closed, other switches open. And on second target board GPIO2 and SPI_CS2 switches should be closed and so on. See Table 3-7 for details on S3 switch settings.

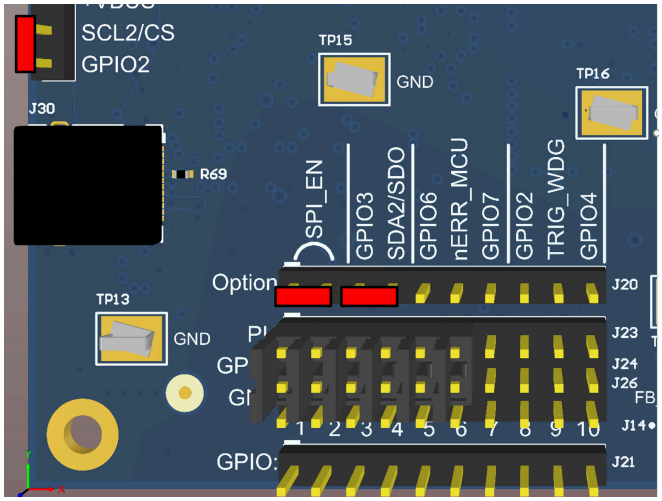

Figure 4-1. Interface Settings for SPI Communication

4.2 Changing the Phase Configuration

There are five possible phase configurations as shown in Table 4-1. It is important that the phase configuration of the EVM matches the phase configuration of the PMIC. Jumpers J3-J8 are located on the top side of the PCB whereas the resistors R1-R7 are on the bottom side of the PCB.

Table 4-1. Phase configurations

Phase configuration	R1	R2/R3	R4/R5	R6/R7	J3	J4	J5	J6	J7	J8
1 (4-phase)	R1	R2	R5	R6	Y	Y	Y	Y	Y	Y
2 (3+1)	R1	R2	R5	R7	Y	Y	Y	Y	N	N
3 (2+1+1)	R1	R2	R4	R7	N	N	Y	N	N	N
4 (1+1+1+1)	R1	R3	R4	R7	N	N	N	N	N	N
5 (2+2)	R1	R2	R4	R6	N	N	Y	N	N	Y

This table is also printed on the EVM on the bottom side of the PCB. All the feedback voltages can be measured from J14-J19 where J15 and J18 are differential feedbacks.

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Note: it is possible to use unused secondary buck's feedbacks for voltage monitoring. 0ohm resistor connecting the FB pin to GND must be opened in this case (e.g. R5/R6).

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5 Schematic, Layout, and Bill of Materials

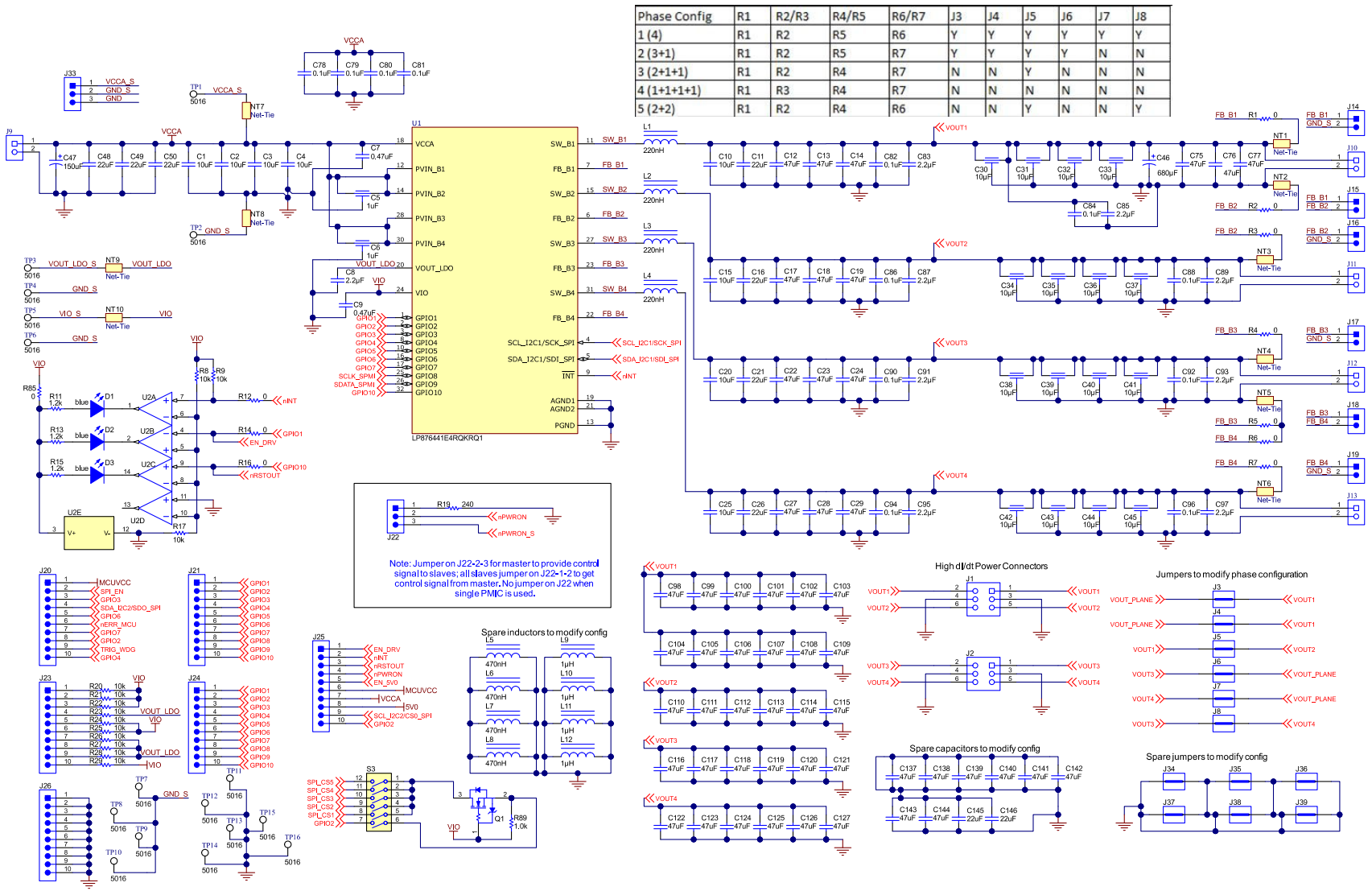

Figure 5-1. Schematic Page 1

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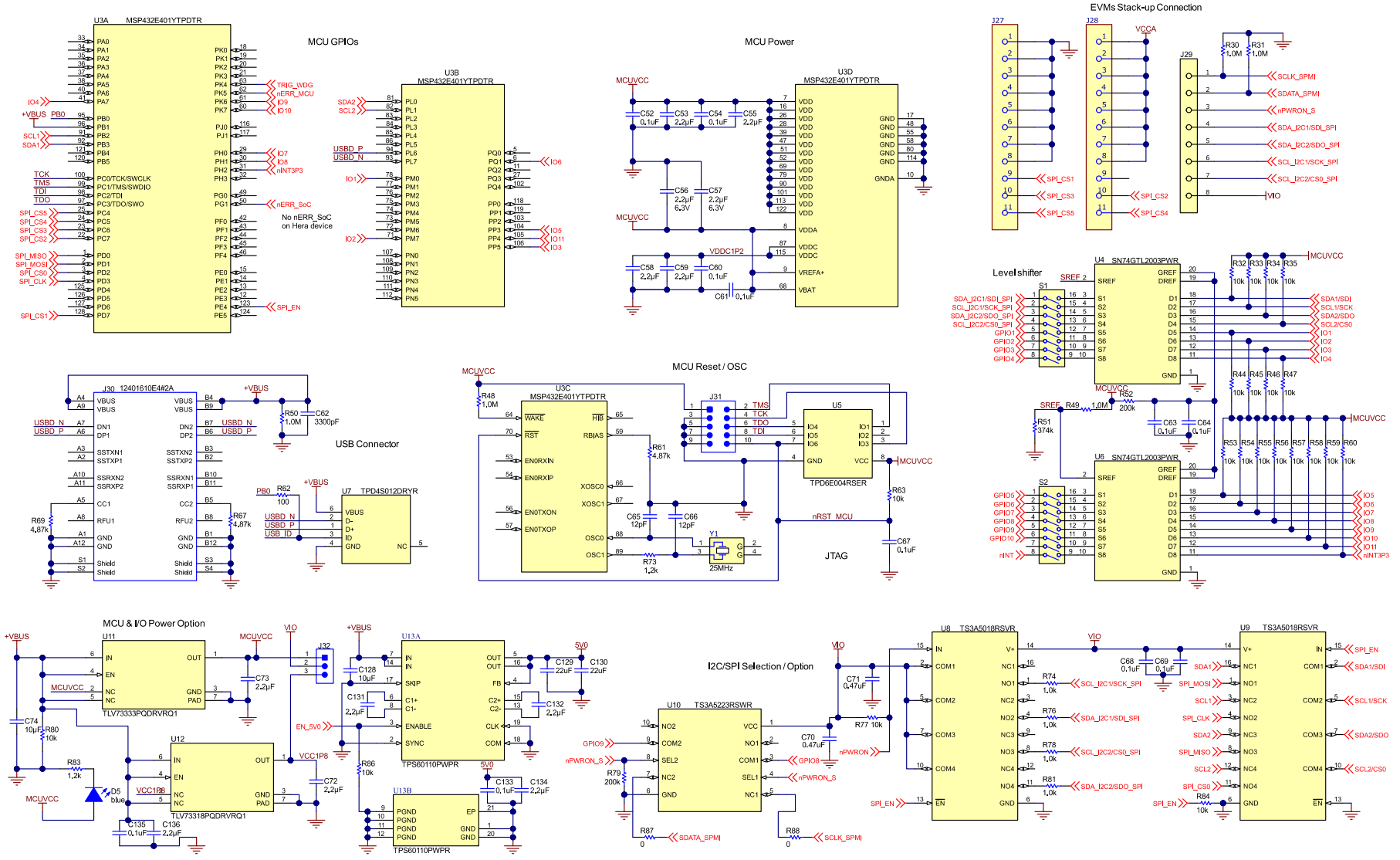

Figure 5-2. Schematic Page 2

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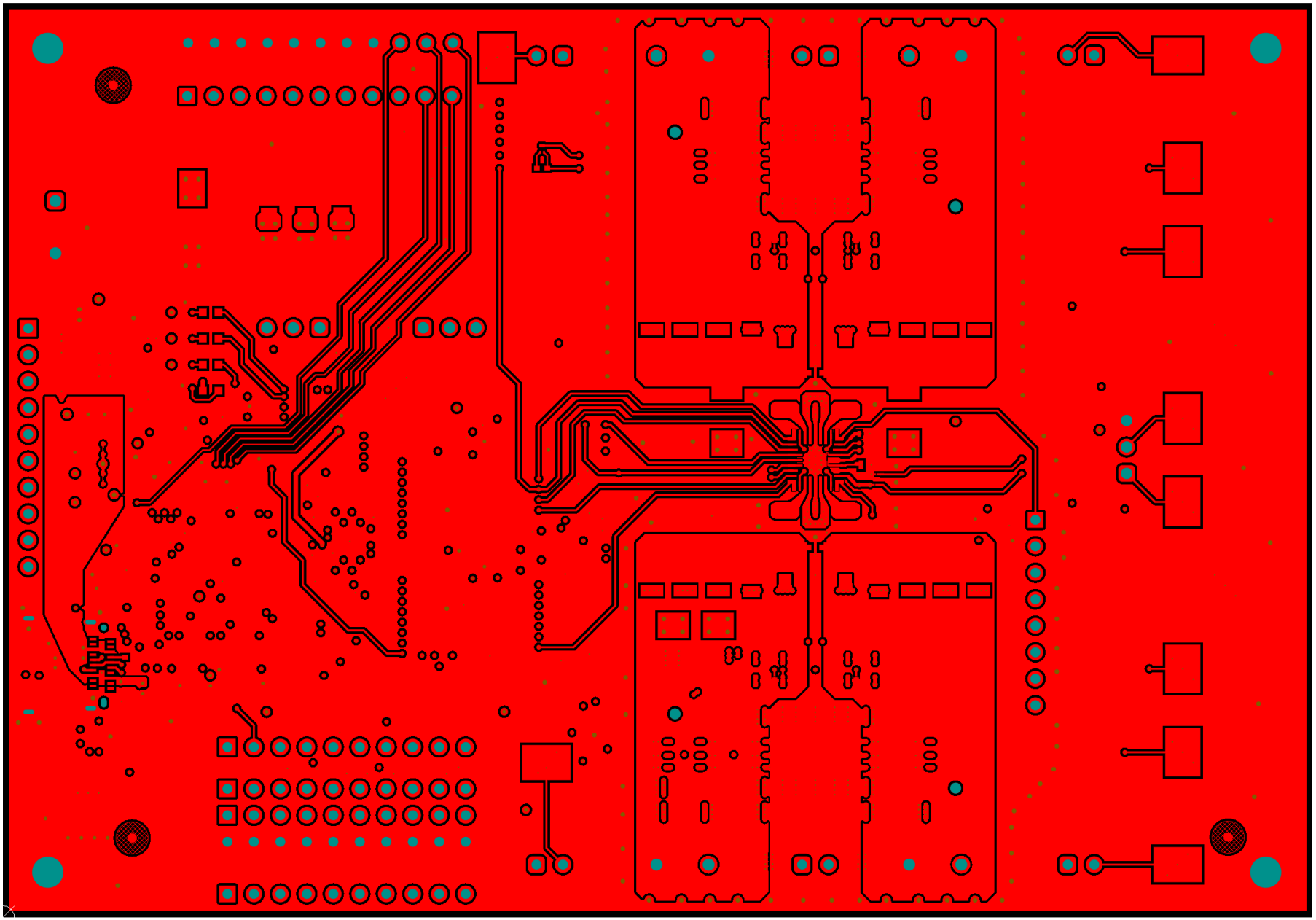

Figure 5-3. Layout Top, Layer 1

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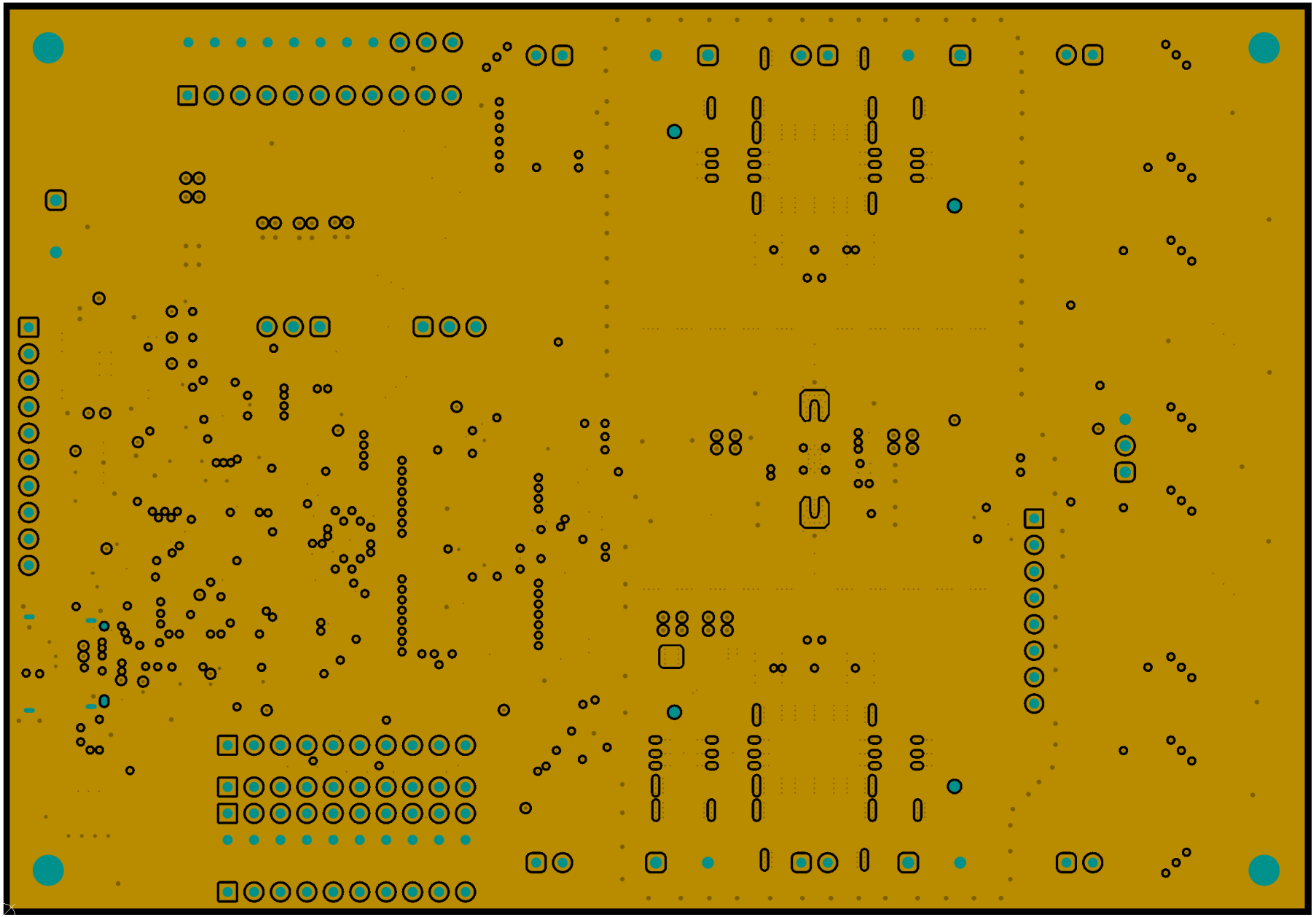

Figure 5-4. Layout Ground, Layer 2

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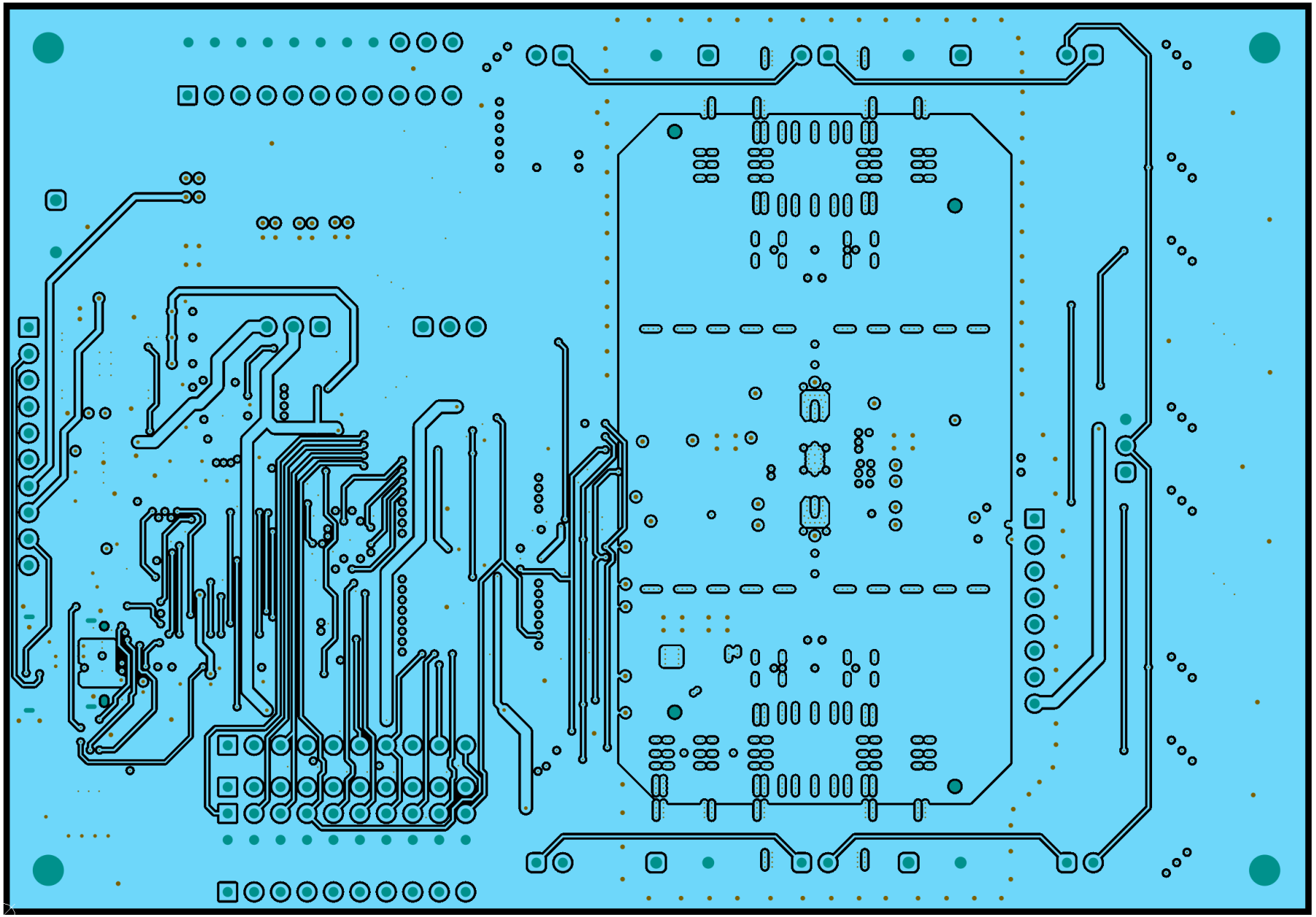

Figure 5-5. Layout Signal, Layer 3

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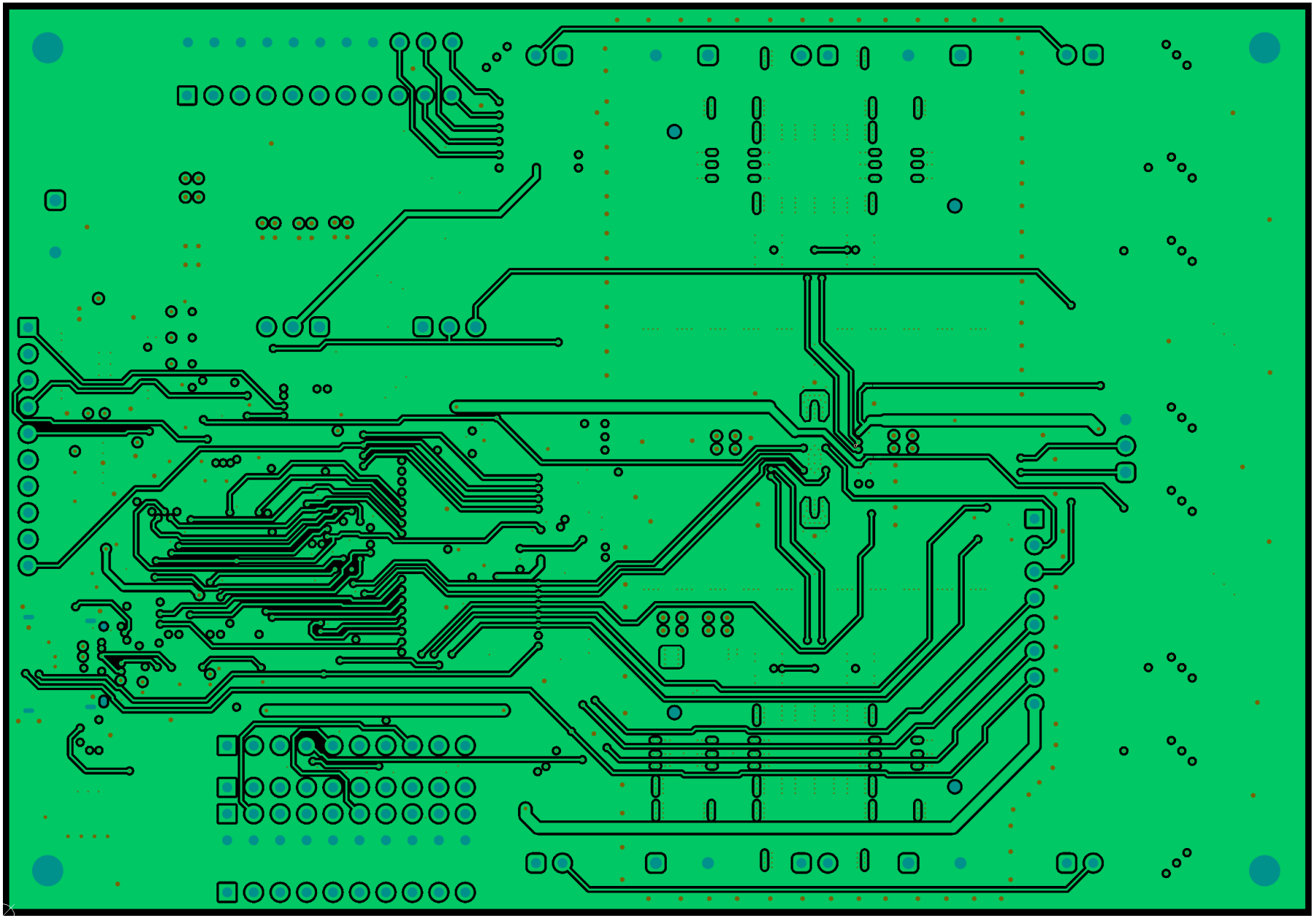

Figure 5-6. Layout Signal, Layer 4

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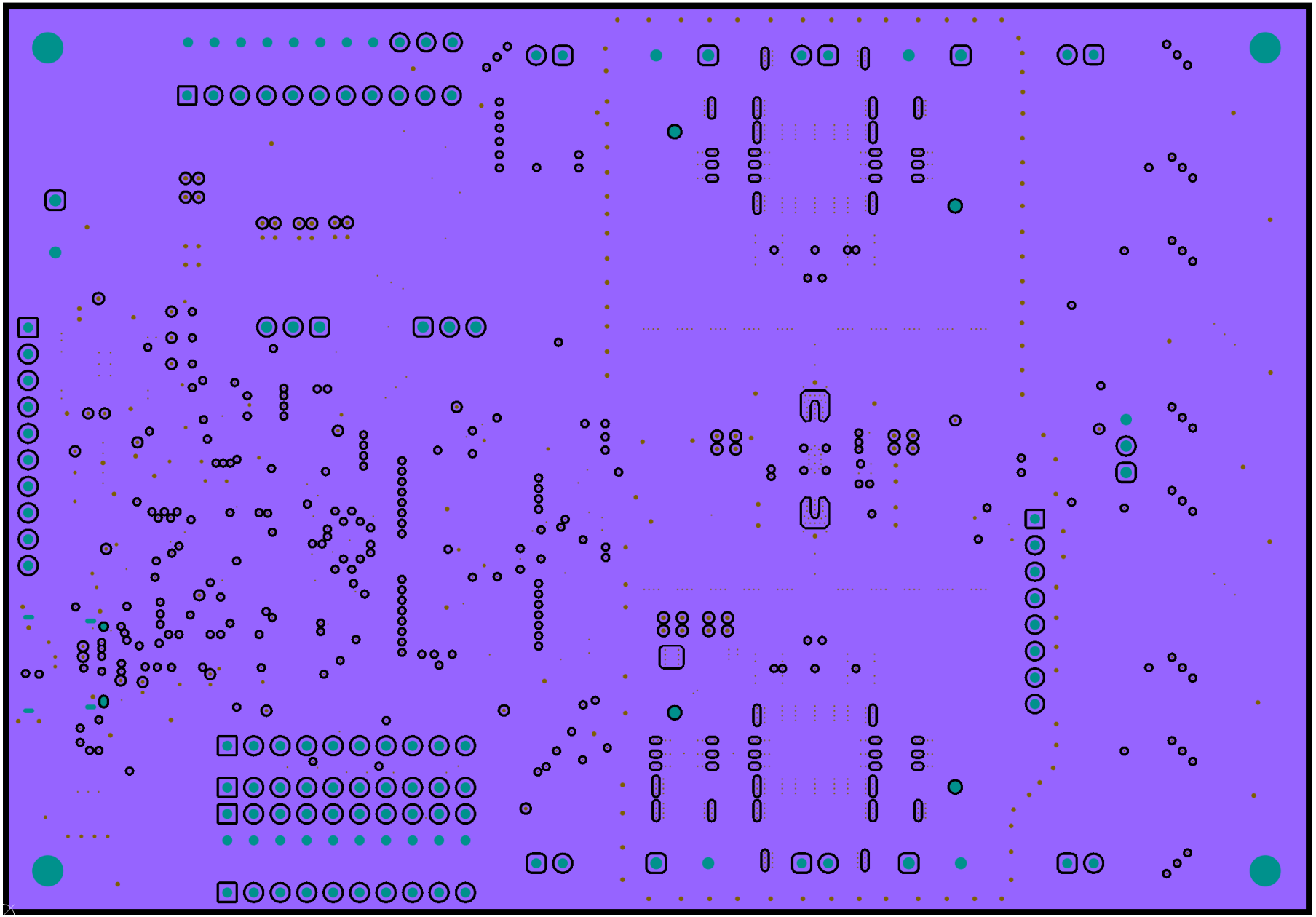

Figure 5-7. Layout Ground, Layer 5

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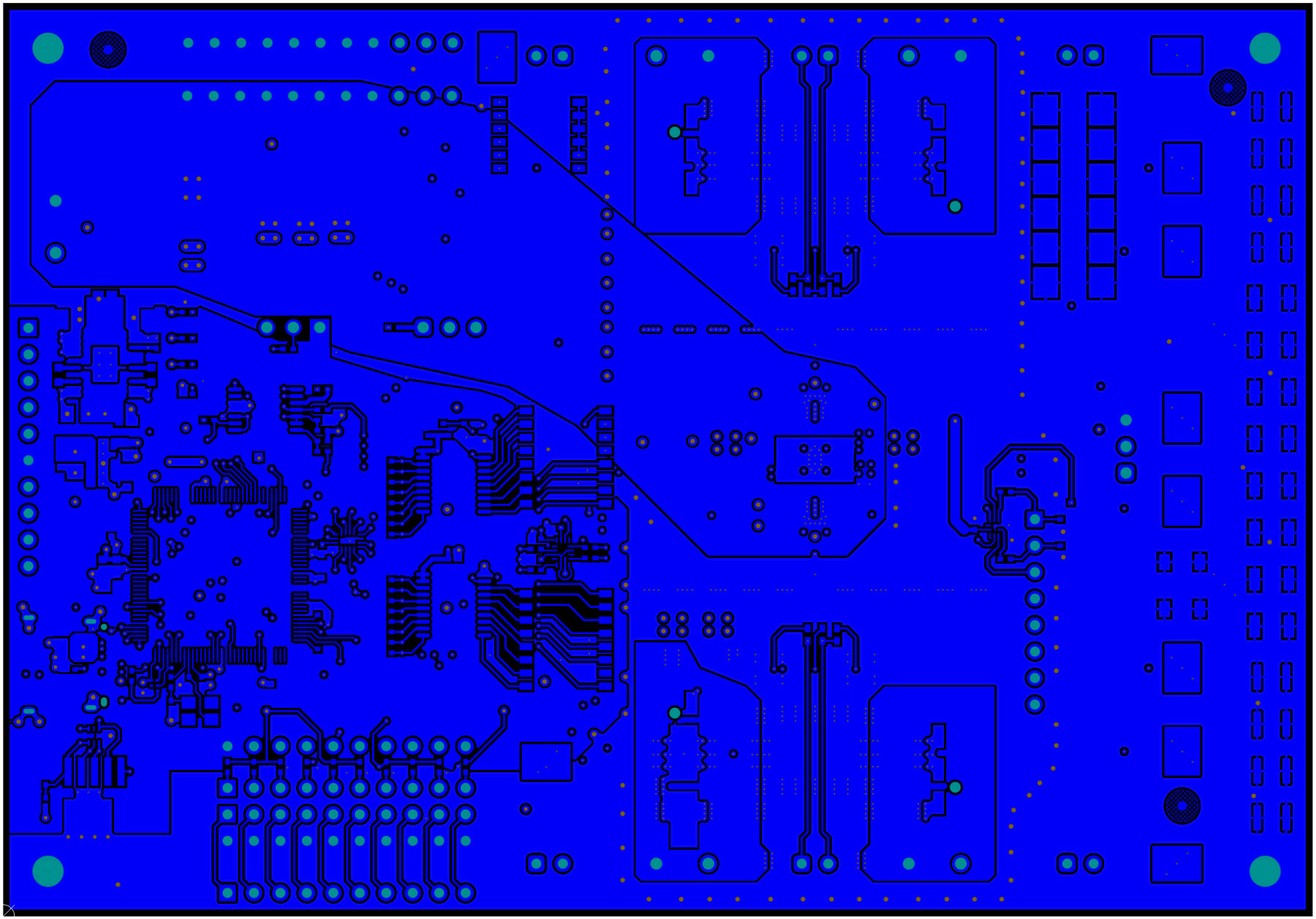

Figure 5-8. Layout Bottom

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Table 5-1. Bill of Materials

Item #	Designator	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
1	PCB1	1		BMC062	Any	Printed Circuit Board	
2	C1, C2, C3, C4, C10, C15, C20, C25, C74, C128	10	10uF	GCM21BR71A106KE22L	MuRata	CAP, CERM, 10 uF, 10 V, +/- 10%, X7R, 0805	0805
3	C5, C6	2	1uF	NFM18HC105C1C3D	Murata	3 Terminals Low ESL Chip Multilayer Ceramic Capacitors for Automotive	0603
4	C7, C9, C70, C71	4	0.47uF	GCM155C71A474KE36D	MuRata	CAP, CERM, 0.47 uF, 10 V,+/- 10%, X7S, 0402	0402
5	C8, C53, C55, C56, C57, C58, C59, C72, C73, C83, C85, C87, C89, C91, C93, C95, C97, C131, C132, C134, C136	21	2.2uF	GCM188R70J225KE22D	MuRata	CAP, CERM, 2.2 uF, 6.3 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603
6	C11, C16, C21, C26, C48, C49, C50, C129, C130, C145, C146	11	22uF	GCM31CR71A226KE02L	MuRata	CAP, CERM, 22 uF, 10 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206	1206
7	C12, C13, C14, C17, C18, C19, C22, C23, C24, C27, C28, C29, C75, C76, C77, C98, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124, C125, C126, C127, C137, C138, C139, C140, C141, C142, C143, C144	53	47uF	GCM32ER70J476ME19L	MuRata	CAP, CERM, 47 uF, 6.3 V, +/- 20%, X7R, 1210	1210
8	C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45	16	10uF	NFM18HC106D0G3	MuRata	CAP, CERM, 10 µF, 4 V,+/- 20%, 1.6x0.8mm	1.6x0.8mm

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Table 5-1. Bill of Materials (continued)

Item #	Designator	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
9	C46	1	680uF	T510X687K006AGA023	Kemet	CAP, TA, 680 µF, 6.3 V, +/- 10%, 0.023 ohm, AEC-Q200 Grade 1, SMD	7343-40
10	C47	1	150uF	UUD1V151MNL1GS	Nichicon	CAP, AL, 150 uF, 35 V, +/- 20%, 0.17 ohm, SMD	8x10
11	C52, C54, C60, C61, C63, C64, C67, C68, C69, C78, C79, C80, C81, C82, C84, C86, C88, C90, C92, C94, C96, C133, C135	23	0.1uF	GCM155R71C104KA55D	MuRata	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0402	0402
12	C62	1	3300pF	C0603C332K5RACTU	Kemet	CAP, CERM, 3300 pF, 50 V, +/- 10%, X7R, 0603	0603
13	C65, C66	2	12pF	GCM1555C1H120JA16J	MuRata	CAP, CERM, 12 pF, 50 V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	0402
14	D1, D2, D3, D5	4	Blue	LB Q39G-L2N2-35-1	OSRAM	LED, Blue, SMD	BLUE 0603 LED
15	H1, H2, H3, H4	4		FC2058-440-A	Fascomp		SPACER
16	H5, H6, H7, H8	4		9900	Keystone	MACHINE SCREW PAN PHILLIPS 4-40	
17	H9	1		3021090-01M	Qualtek	USB A MALE TO USB C Male	
18	J1, J2	2		6651712-1	TE Connectivity	Receptacle, 2.5mm, 3x2, Gold, SMT	Receptacle, 2.5mm, 3x2, SMT
19	J3, J4, J5, J6, J7, J8, J34, J35, J36, J37, J38, J39	12		S1911-46R	Harwin	JUMPER TIN SMD	6.85x0.97x2.51 mm
20	J9, J10, J11, J12, J13	5		1792863	Phoenix Contact	Terminal Block, 5mm, 2x1, R/A, TH	Terminal Block, 5mm, 2x1, R/A, TH
21	J14, J15, J16, J17, J18, J19	6		TSW-102-07-G-S	Samtec	Header, 100mil, 2x1, Gold, TH	2x1 Header
22	J20, J21, J23, J24, J25, J26	6		TSW-110-07-G-S	Samtec	Header, 100mil, 10x1, Gold, TH	10x1 Header
23	J22, J32, J33	3		61300311121	Wurth Elektronik	Header, 2.54 mm, 3x1, Gold, TH	Header, 2.54mm, 3x1, TH

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Table 5-1. Bill of Materials (continued)

Item #	Designator	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
24	J27, J28	2		ESQ-111-14-T-S	Samtec	Conn Elevated Socket SKT 11 POS 2.54mm Solder ST Thru-Hole Tube	HDR11
25	J29	1		ESQ-108-14-T-S	Samtec	Board-To-Board Connector, Vertical, ESQ Series, 8 Contacts, Receptacle, 2.54 mm, Through Hole	HDR8
26	J30	1		12401610E4#2A	Amphenol Canada	Receptacle, 0.5mm, USB TYPE C, R/A, SMT	Receptacle, 0.5mm, USB TYPE C, R/A, SMT
27	J31	1		FTSH-105-01-F-DV-K	Samtec	Header (Shrouded), 1.27mm, 5x2, Gold, SMT	Header(Shrouded), 1.27mm, 5x2, SMT
28	L1, L2, L3, L4	4	220nH	TFM322512ALMAR22MTAA	TDK	Inductor, Thin Film, 220 nH, 7.6 A, 0.01 ohm, AEC-Q200 Grade 0, SMD	TDK Inductor
29	L5, L6, L7, L8	4	470nH	TFM322512ALMAR47MTAA	TDK	Inductor, Thin Film, 470 nH, 5.3 A, 0.021 ohm, AEC-Q200 Grade 0, SMD	TDK Inductor
30	L9, L10, L11, L12	4	1uH	TFM322512ALMA1R0MTAA	TDK	Inductor, Thin Film, 1 µH, 4 A, 0.037 ohm, AEC-Q200 Grade 0, SMD	TDK Inductor
31	LBL1	1		THT-14-423-10	Brady	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch
32	Q1	1	12V	CSD13381F4	Texas Instruments	MOSFET, N-CH, 12 V, 2.1 A, YJC0003A (PICOSTAR-3)	YJC0003A
33	R1, R2, R3, R4, R5, R6, R7, R12, R14, R16, R85, R87, R88	13	0	CRCW04020000Z0ED	Vishay-Dale	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402

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Table 5-1. Bill of Materials (continued)

Item #	Designator	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
34	R8, R9, R17, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R32, R33, R34, R35, R44, R45, R46, R47, R53, R54, R55, R56, R57, R58, R59, R60, R63, R77, R80, R84, R86	34	10k	CRCW040210K0JNED	Vishay-Dale	RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
35	R11, R13, R15, R73, R83	5	1.2k	CRCW04021K20JNED	Vishay-Dale	RES, 1.2 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
36	R19	1	240	CRCW0402240RJNED	Vishay-Dale	RES, 240, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
37	R30, R31, R48, R49, R50	5	1.0Meg	CRCW04021M00JNED	Vishay-Dale	RES, 1.0 M, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
38	R51	1	374k	CRCW0402374KFKED	Vishay-Dale	RES, 374 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
39	R52, R79	2	200k	CRCW0402200KJNED	Vishay-Dale	RES, 200 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
40	R61, R67, R69	3	4.87k	CRCW04024K87FKED	Vishay-Dale	RES, 4.87 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
41	R62	1	100	CRCW0402100RJNED	Vishay-Dale	RES, 100, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
42	R74, R76, R78, R81, R89	5	1.0k	CRCW04021K00JNED	Vishay-Dale	RES, 1.0 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
43	S1, S2	2		218-8LPST	CTS Electrocomponents	Switch, SPST, 8 Pos, 25mA, 24VDC, SMD	11.33x5.8mm
44	S3	1		218-6LPST	CTS Electrocomponents	Switch, SPST, Slide, Off-On, 6 Pos, 0.025A, 24V, SMD	5.8x8.79mm
45	SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12	12		881545-2	TE Connectivity	Shunt, 100mil, Gold plated, Black	Shunt 2 pos. 100 mil

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Table 5-1. Bill of Materials (continued)

Item #	Designator	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
46	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16	16		5016	Keystone	Test Point, Compact, SMT	Testpoint_Keystone_Compact
47	U1	1		LP876441E4RQKRQ1	Texas Instruments	Four-Phase, 20-A Buck Converter With Integrated Switches	VQFN-HR32
48	U2	1		LM2901AVQPWRQ1	Texas Instruments	AEC-Q100 Quad Comparator, PW0014A (TSSOP-14)	PW0014A
49	U3	1		MSP432E401YTPDTR	Texas Instruments	MSP432E401YTPDT, PDT0128A (TQFP-128)	PDT0128A
50	U4, U6	2		SN74GTL2003PWR	Texas Instruments	8-BIT BIDIRECTIONAL LOW-VOLTAGE TRANSLATOR, PW0020A (TSSOP-20)	PW0020A
51	U5	1		TPD6E004RSER	Texas Instruments	Low-Capacitance 6-Channel +/-15 kV ESD Protection Array for High-Speed Data Interfaces, RSE0008A (UQFN-8)	RSE0008A
52	U7	1		TPD4S012DRYR	Texas Instruments	4-Channel USB ESD Solution with Power Clamp, DRY0006A (USON-6)	DRY0006A
53	U8, U9	2		TS3A5018RSVR	Texas Instruments	10-Ohm Quad SPDT Analog Switch, RSV0016A (UQFN-16)	RSV0016A
54	U10	1		TS3A5223RSWR	Texas Instruments	0.5Ω Dual SPDT Bidirectional Analog Switch, RSW0010A (UQFN-10)	RSW0010A
55	U11	1		TLV73333PQDRVRQ1	Texas Instruments	Capacitor-Free, 300-mA, Low-Dropout Regulator for Automotive, DRV0006A (WSON-6)	DRV0006A

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Table 5-1. Bill of Materials (continued)

Item #	Designator	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
56	U12	1		TLV73318PQDRVRQ1	Texas Instruments	Capacitor-Free, 300-mA, Low-Dropout Regulator for Automotive, DRV0006A (WSON-6)	DRV0006A
57	U13	1		TPS60110PWPR	Texas Instruments	5 V, Boost Charge Pump, 300 mA, 2.7 to 5.4 V Input with Synchonrization pin, -40 to 85 degC, 20-pin SOP (PWP20), Green (RoHS & no Sb/Br)	PWP0020C
58	Y1	1		NX3225SA-25.000M-STD-CRS-2	NDK	CRYSTAL 25.0000MHZ 8PF SMD	SMT_XTAL_3MM2_2MM5

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6 Additional Resources

- Scalable PMIC's GUI User's Guide
- LP8764-Q1 Four-Phase, 20-A Buck Converter With Integrated Switches

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2020) to Revision A (February 2022)	Page
• Updated datasheet link, changed all instances of legacy terminology to controller and target.	1
• Updated list of EVMs and orderable part numbers	3
• Updated datasheet link. Updated EVM picture. Added details on LP8744Q1EVM GPIO2 usage	3
• Updated VCCA connection options	4
• Updated links	4
• Updated part numbers. Added FB pin test points	5
• Updated EVM image. Updated part numbers. Updated J25 options	5
• Updated EVM image. Updated part numbers.	8
• Updated +VBUS and VCCA connection description	11
• Updated SPI CS settings	13
• Updated Schematic and Layout images. Updated BOM	15
• Updated datasheet link	29

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