

Multilayer Ceramic Chip Capacitor

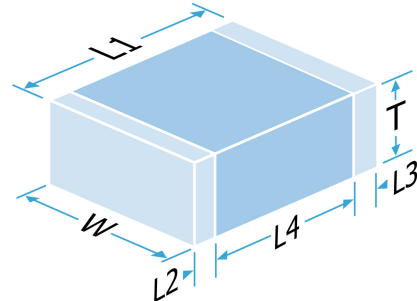
Part Number: 2220YA250102KSTSYX

Description: 2220 250Vac (Y2), 305Vac (X1), 50/60Hz / 1000Vdc 1.0nF ±10% X7R (2R1) to AEC-Q200

Approval Specifications: IEC/EN60384-14:2013+A1
UL60384-14, CAN/CSA E60384-14:14

Certification: TÜV R60156291 / ID1111239246
UL/cUL E228790-20210208

Classification: IEC/EN 60384-14:2013+A1 Class Y2 / X1
UL/cUL FOWX2, FOWX8



Component Marking and Certification Bodies:

Material Group I : CTI >= 600



Mechanical Specification

| | |
|--|--|
| Size Code | 2220 |
| Length (L1) in mm (") | 5.7 ± 0.40 (0.225 ± 0.016) |
| Width (W) in mm (") | 5.0 ± 0.40 (0.197 ± 0.016) |
| Thickness (T) in mm (") | 2.0 Max (0.08 Max) |
| Minimum Termination Band (L2,L3) in mm (") | 0.25 (0.010) |
| Maximum Termination Band (L2,L3) in mm (") | 1.00 (0.040) |
| Minimum Band Gap (L4) in mm (") | 4.0 (0.158) |
| Termination Material | FlexiCap™ Polymer termination, Nickel barrier, Sn Plated Solder (RoHS compliant) |
| Solderability | IEC-60068-2-58 |
| Packaging | 7" Reel Horizontal Orientation, 500 per reel |

General Electrical Specification

| | |
|---|--|
| Rated Voltage | Class Y2 (250Vac), Class X1 (305Vac), 50/60Hz, 5kV impulse |
| Humidity Grade | Grade III (IEC/EN60384-14:2013 Annex 1) |
| Maximum DC Working Voltage | 1000Vdc certified / (2500Vdc outside scope of any specification) |
| Nominal Capacitance Value | 1.0nF |
| Capacitance Tolerance | ±10% |
| Tangent of Loss Angle (Tan δ) | ≤0.025 |
| Capacitance and Tan δ Test Conditions | 1.0Vrms @ 1kHz |
| Voltage Proof (50mA max charging current for DC tests) | 100% test: 4000Vdc 1s min / 5s max AQL test: 4000Vdc / 3000Vac 60s min / 5kV 1.2x50µs impulse |
| Min Insulation Resistance (IR) | 100.00GOhm @ 100Vdc |
| Dielectric Classification | X7R (2R1) to AEC-Q200 |
| Rated Temperature Range | -55°C / +125°C |
| Maximum Capacitance Change over Temperature Range | No DC Voltage ±15% Rated DC Voltage - |
| Climatic Category (IEC) | 55/125/56 |
| Ageing Characteristic | <2% per decade |

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This datasheet is for a standard item and is confirmed valid on the date generated, the latest published data for this part may differ and is available at <http://www.knowlescapacitors.com> or by contacting us.

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Data is correct to the best of our knowledge, errors and omissions excepted.

Date: Thursday, September 02, 2021

20210902 214051808UTC

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Environmental

| | |
|--|------------------|
| RoHS Compliant to 2011/65/EC as amended by 2015/863/EU | Compliant |
| REACH Compliant | 211 compliant |
| California Proposition 65 | No exposure risk |

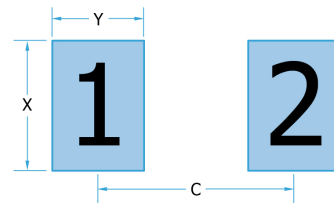
Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover. Refer to application note AN0043 for further information.

IPC-7351 pad design

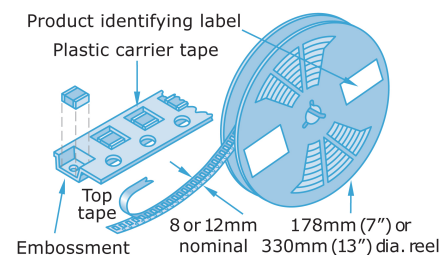
| | 2220 | |
|---|--------|--------|
| C | 5.30mm | 0.209" |
| Y | 1.50mm | 0.059" |
| X | 5.40mm | 0.213" |



Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



Soldering

Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

Application notes with mounting and handling guidance are available on request.



Complex

DLI

Johanson MFG

Novacap

Syfer

Voltronics

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