

# FDMC4D9P20X8

## P-Channel Power Trench<sup>®</sup> MOSFET

-20 V, -75 A, 4.9 mΩ

### General Description

This P-Channel MOSFET is produced using ON Semiconductor's advanced PowerTrench<sup>®</sup> process that has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

### Features

- Max  $r_{DS(on)}$  = 4.9 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -18$  A
- Max  $r_{DS(on)}$  = 16.4 mΩ at  $V_{GS} = -1.8$  V,  $I_D = -9$  A
- High Performance Trench Technology for Extremely Low  $r_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Load Switch
- Battery Management
- Power Management
- Reverse Polarity Protection

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-20	V
$V_{GS}$	Gate to Source Voltage	±12	V
$I_D$	Drain Current: Continuous, $T_C = 25^\circ\text{C}$ (Note 5) Continuous, $T_C = 100^\circ\text{C}$ (Note 5) Continuous, $T_A = 25^\circ\text{C}$ (Note 1a) Pulsed (Note 4)	-75 -47 -18 -335	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	54	mJ
$P_D$	Power Dissipation: $T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1a)	40 2.4	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

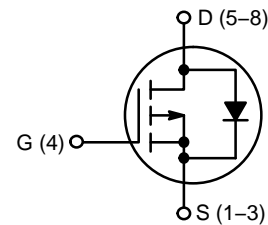
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



ON Semiconductor<sup>®</sup>

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$V_{DS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
-20 V	4.9 mΩ @ -4.5 V	-75 A
	6.5 mΩ @ -2.5 V	
	16.4 mΩ @ -1.8 V	

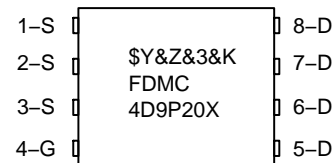


P-Channel MOSFET



PQFN8  
CASE 483AX

### MARKING DIAGRAM



\$Y = ON Semiconductor Logo  
 &Z = Assembly Plant Code  
 &3 = Data Code (Year & Week)  
 &K = Lot  
 FDMC4D9P20X8 = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

# FDMC4D9P20X8

## THERMAL CHARACTERISTICS

Symbol	Parameter	FDMC4D9P20X8	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250 \mu\text{A}$ , $V_{GS} = 0 \text{ V}$	-20			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-15		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}$ , $V_{GS} = 0 \text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 12 \text{ V}$ , $V_{DS} = 0 \text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250 \mu\text{A}$	-0.4	-0.7	-1.6	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		4		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5 \text{ V}$ , $I_D = -18 \text{ A}$		3.3	4.9	m $\Omega$
		$V_{GS} = -2.5 \text{ V}$ , $I_D = -11 \text{ A}$		4.1	6.5	
		$V_{GS} = -1.8 \text{ V}$ , $I_D = -9 \text{ A}$		6.2	16.4	
		$V_{GS} = -4.5 \text{ V}$ , $I_D = -18 \text{ A}$ , $T_J = 125^\circ\text{C}$		4.5	6.8	
$g_{FS}$	Forward Transconductance	$V_{DS} = -5 \text{ V}$ , $I_D = -18 \text{ A}$		113		S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = -10 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$		7535	10550	pF
$C_{oss}$	Output Capacitance			1100	1540	pF
$C_{rss}$	Reverse Transfer Capacitance			1040	1455	pF
$R_g$	Gate Resistance		0.1	4.5	10	$\Omega$

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10 \text{ V}$ , $I_D = -18 \text{ A}$ , $V_{GS} = -4.5 \text{ V}$ , $R_G = 6 \Omega$		13	23	ns
$t_r$	Rise Time			17	31	ns
$t_{d(off)}$	Turn-Off Delay Time			312	499	ns
$t_f$	Fall Time			176	282	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ V}$ to $-4.5 \text{ V}$ , $V_{DD} = -10 \text{ V}$ , $I_D = -18 \text{ A}$		78	109	nC
			$V_{GS} = 0 \text{ V}$ to $-2.5 \text{ V}$ , $V_{DD} = -10 \text{ V}$ , $I_D = -18 \text{ A}$		50	70
$Q_{gs}$	Gate to Source Charge	$V_{DD} = -10 \text{ V}$ , $I_D = -18 \text{ A}$		12		nC
$Q_{gd}$	Gate to Drain "Miller" Charge	$V_{DD} = -10 \text{ V}$ , $I_D = -18 \text{ A}$		24		nC

### DRAIN-SOURCE DIODE CHARACTERISTICS

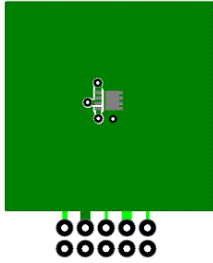
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}$ , $I_S = -18 \text{ A}$ (Note 2)		-0.7	-1.2	V
		$V_{GS} = 0 \text{ V}$ , $I_S = -2 \text{ A}$ (Note 2)		-0.6	-1.2	
$t_{rr}$	Reverse Recovery Time	$I_S = -18 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$		41	66	ns
$Q_{rr}$	Reverse Recovery Charge			22	35	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

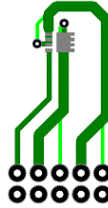
# FDMC4D9P20X8

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.

**NOTES:**



a) 53 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b) 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %
3.  $E_{AS}$  of 54 mJ is based on starting  $T_J = 25\text{ C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = -6\text{ A}$ ,  $V_{DD} = -20\text{ V}$ ,  $V_{GS} = -10\text{ V}$ .
4. Pulsed Id please refer to Fig 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

**PACKAGE MARKING AND ORDERING INFORMATION**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC4D9P20X8	FDMC4D9P20X8	PQFN8 (Pb Free)	13"	12 mm	3000 Units

# FDMC4D9P20X8

## TYPICAL CHARACTERISTICS

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

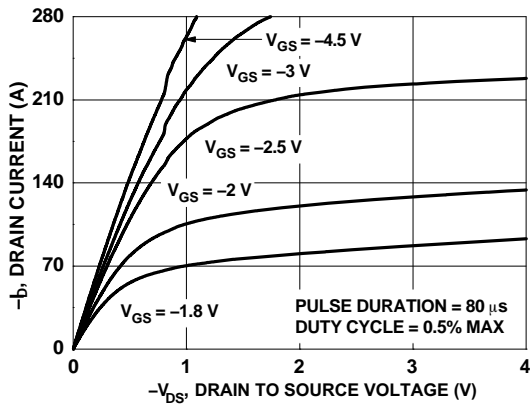


Figure 1. On-Region Characteristics

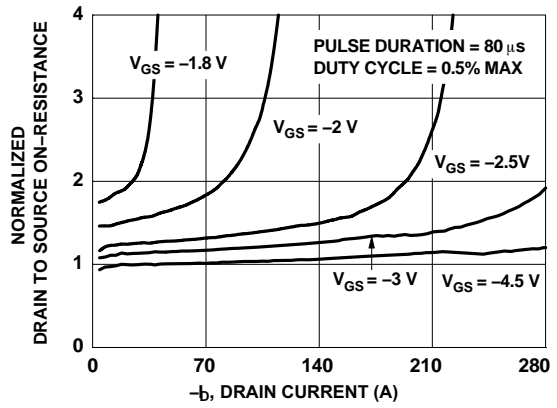


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

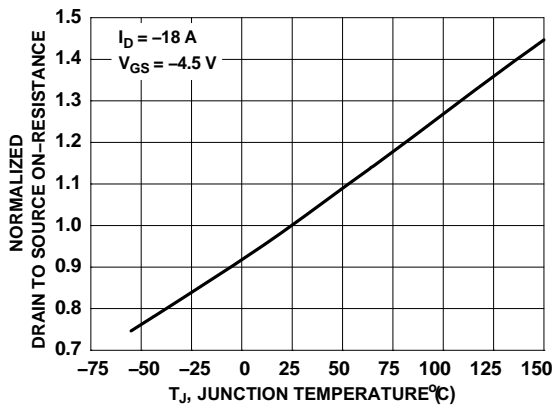


Figure 3. Normalized On-Resistance vs Junction Temperature

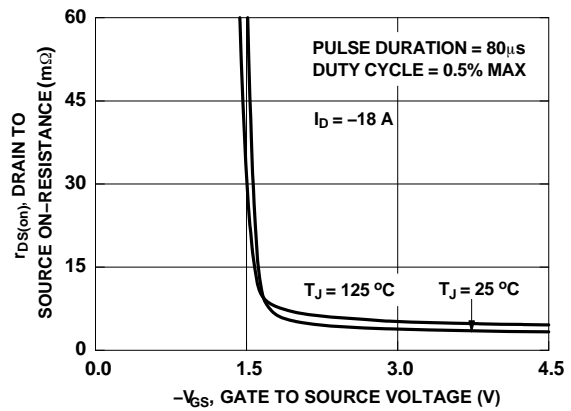


Figure 4. On-Resistance vs Gate to Source Voltage

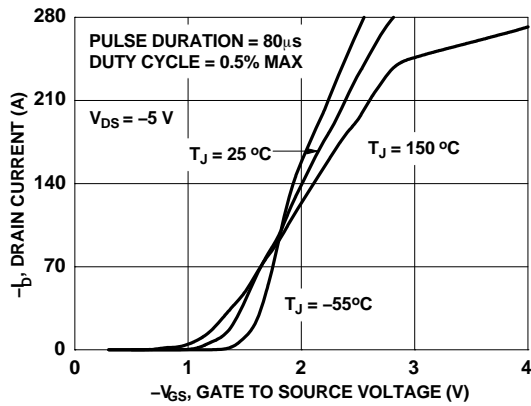


Figure 5. Transfer Characteristics

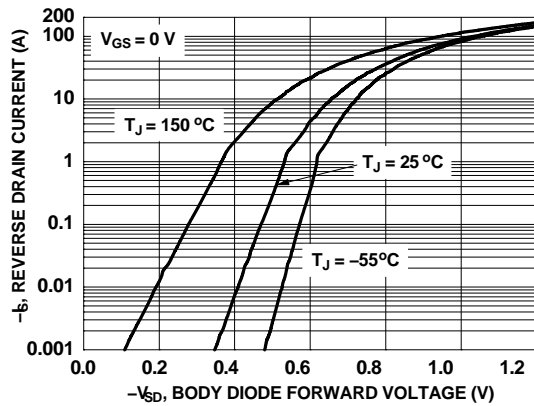


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

# FDMC4D9P20X8

## TYPICAL CHARACTERISTICS

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

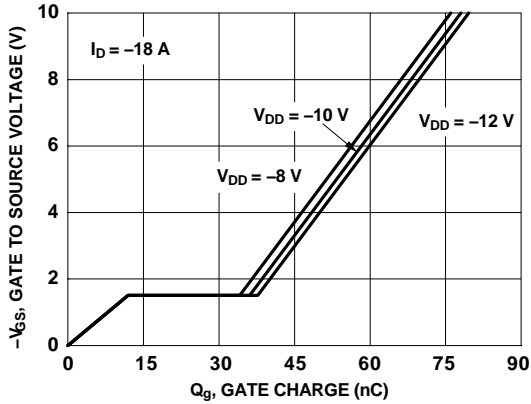


Figure 7. Gate Charge Characteristics

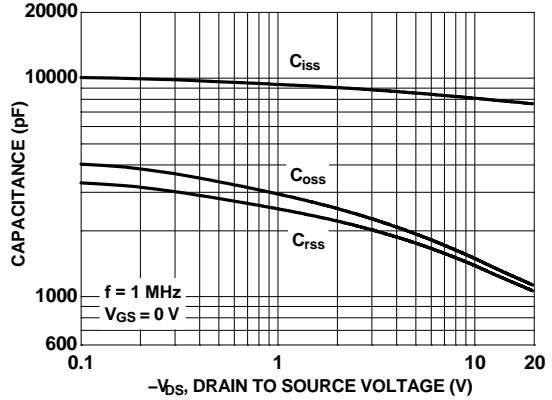


Figure 8. Capacitance vs Drain to Source Voltage

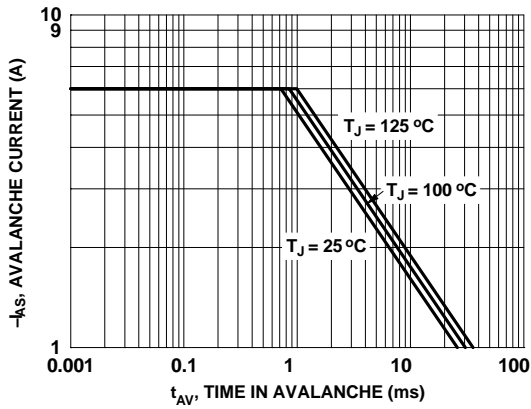


Figure 9. Unclamped Inductive Switching Capability

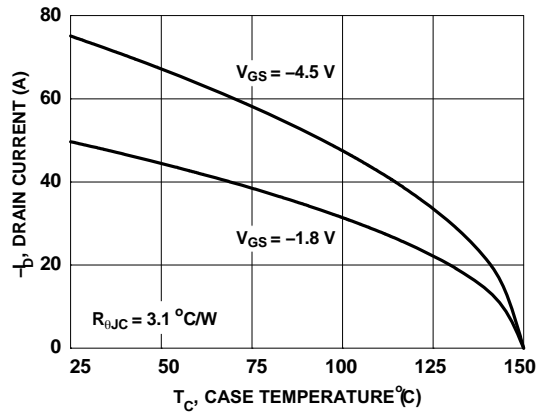


Figure 10. Maximum Continuous Drain Current vs Case Temperature

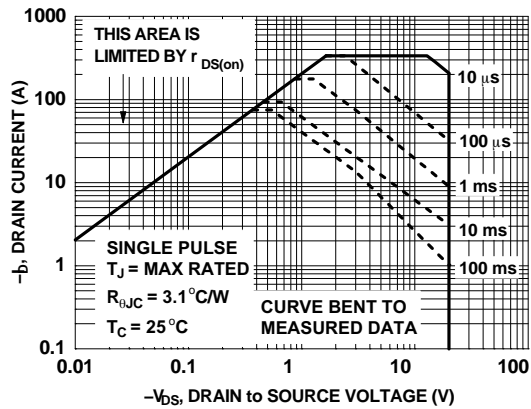


Figure 11. Forward Bias Safe Operating Area

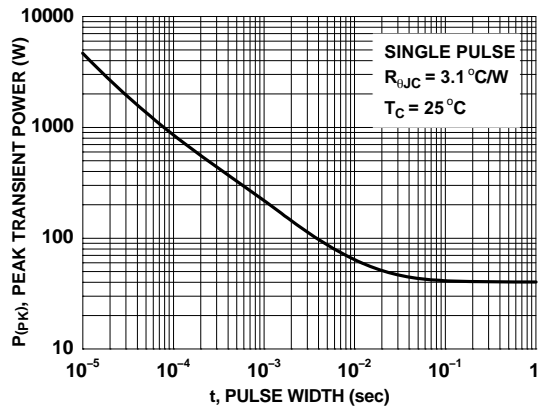


Figure 12. Single Pulse Maximum Power Dissipation

# FDMC4D9P20X8

## TYPICAL CHARACTERISTICS

( $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted)

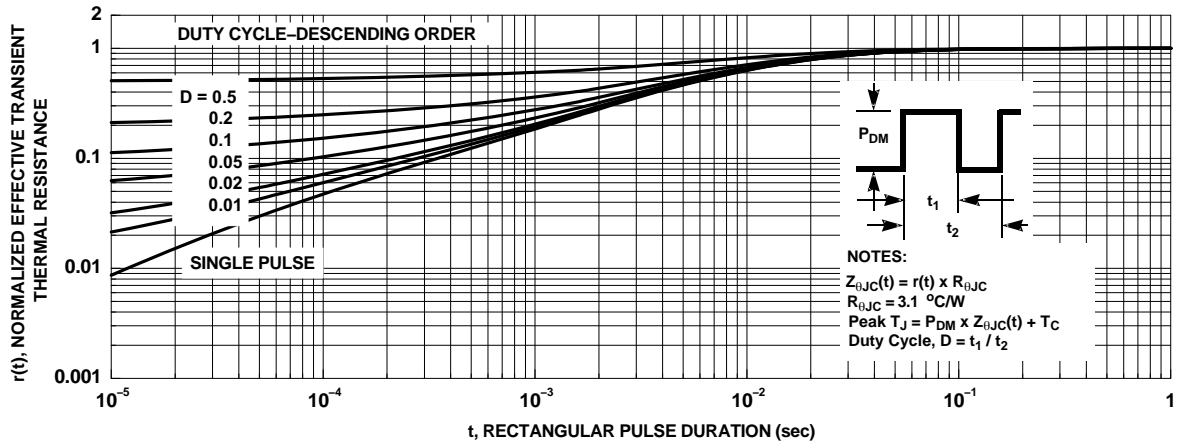


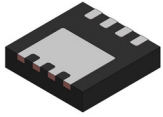
Figure 13. Junction-to-Case Transient Thermal Response Curve

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# MECHANICAL CASE OUTLINE

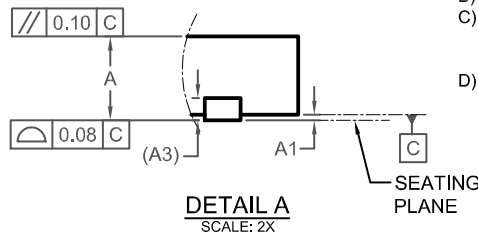
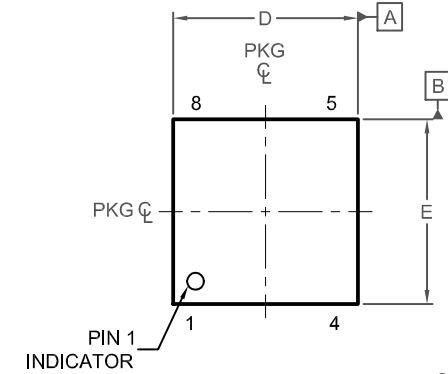
## PACKAGE DIMENSIONS

ON Semiconductor®



**PQFN8 3.3X3.3, 0.65P**  
**CASE 483AX**  
**ISSUE B**

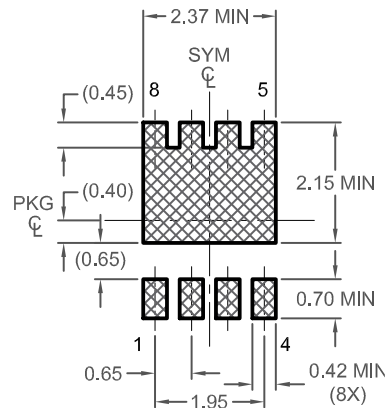
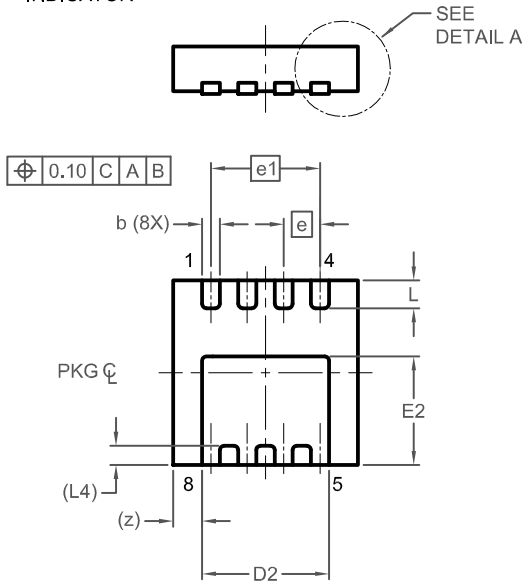
DATE 24 JUN 2022



NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	2.17	2.27	2.37
E	3.20	3.30	3.40
E2	1.84	1.94	2.04
e	0.65 BSC		
e1	1.95 BSC		
L	0.40	0.50	0.60
L4	0.34 REF		
z	0.52 REF		



LAND PATTERN RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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