## Features

- Broadband Performance
- Low Loss @ 2.7 GHz:
  TX = 0.25 dB
  RX = 0.35 dB
- High Isolation @ 2.7 GHz:
  RX = 44 dB
- Power Handling @ 2.7 GHz:
  200 W CW @ +85 ºC
  122 W CW @ +120 ºC
- Lead-Free 5 mm 20-Lead HQFN Package
- RoHS* Compliant
- Designed for High Power TDD-LTE Applications

## Description

The MASW-011120 is a SPDT high power, broadband, high linearity, PIN diode T/R switch for 0.03 - 6.0 GHz high power applications. The device is provided in an industry standard lead free 5 mm HQFN plastic package.

This device incorporates PIN diode die fabricated with a low loss, high isolation switching diode process.

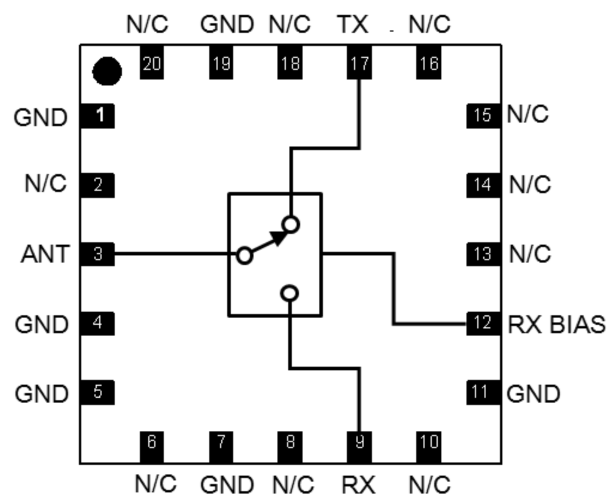
MASW-011120 can be used in any application requiring a low-loss, high-isolation, and high-power-handing SPDT.

## Ordering Information[1,2]

| Part Number | Package |
|---|---|
| MASW-011120-TR1000 | 1000 Piece Tape and Reel |
| MASW-011120-TR3000 | 3000 Piece Tape and Reel |
| MASW-011120-SMB | Sample Board |

1. Reference Application Note M513 for reel size information.
2. All sample boards include 3 loose parts.

## Functional Schematic




## Pin Configuration[3]

| Pin # | Pin Name | Function |
|---|---|---|
| 1,4,5,7,11,19 | GND | Ground |
| 2,6,8,10,13,14, 15,16,18,20 | N/C | No Connection |
| 3 | ANT | RF Port |
| 9 | RX | RF Port |
| 12 | RX BIAS | RX Bias Input |
| 17 | TX | RF Port |
| 21 | Paddle | Ground[4] |

3. MACOM recommends connecting all No Connection (N/C) pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

## Electrical Specifications:
## Freq. = 2.7 GHz, 3.5 GHz, $T_A$ = +25 °C, $Z_0$ = 50 Ω, Bias = 60 V / 0 V. See Bias Table.

| Parameter | Test Conditions | Units | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| Insertion Loss | ANT to TX ON @ 2.7 GHz<br>ANT to TX ON @ 3.5 GHz<br>ANT to RX ON @ 2.7 GHz<br>ANT to RX ON @ 3.5 GHz | dB | — | 0.25<br>0.30<br>0.35<br>0.50 | 0.45<br>0.50<br>0.60<br>0.70 |
| Isolation | ANT to RX (TX ON) @ 2.7 GHz<br>ANT to RX (TX ON) @ 3.5 GHz<br>ANT to TX (RX ON) @ 2.7 GHz<br>ANT to TX (RX ON) @ 3.5 GHz | dB | 35<br>35<br>12<br>10 | 44<br>44<br>15<br>13 | — |
| ANT Return Loss | ANT to RX ON<br>ANT to TX ON | dB | — | 23<br>25 | — |
| TX Return Loss | ANT to TX ON | dB | — | 22 | — |
| RX Return Loss | ANT to RX ON | dB | — | 26 | — |
| Input P0.1 dB[5] | ANT to TX ON | dBm | — | 51 | — |
| IIP3 TX | ANT to TX, $P_{IN}$ = 30 dBm | dBm | — | 68 | — |
| IIP3 RX | ANT to RX, $P_{IN}$ = 30 dBm | dBm | — | 68.5 | — |
| RF Input Power CW[5]<br>ANT to TX ON | 85°C @ 2.7 GHz; 100 mA<br>85°C @ 2.7 GHz; 200 mA<br>120°C @ 2.7 GHz; 100 mA<br>120°C @ 2.7 GHz; 200 mA | W | — | 145<br>200<br>97<br>122 | — |
| Switching Speed<br>TX $T_{ON}$<br>TX $T_{OFF}$<br>RX $T_{ON}$<br>RX $T_{OFF}$ | $T_{ON}$ - 50% control to 90% RF<br>$T_{OFF}$ - 50% control to 10% RF | µs | — | 0.5<br>1.6<br>0.3<br>0.3 | — |
| Group Delay | — | ns | — | 50 | — |
| In-band Ripple | 20 MHz<br>200 MHz | dB | — | 0.05<br>0.1 | — |

5. Maximum source and load VSWR < 1.2:1.

## Bias Table

| Bias Table | TX | RX | RX BIAS | ANT |
|---|---|---|---|---|
| Pin | 17 | 9 | 12 | 3 |
| ANT to TX ON (Insertion Loss) | (GND), -100 mA[6] | (+60 V), 10 mA[6] | (GND), -10 mA[6] | +5 V, 100 mA[6] |
| ANT to RX (Isolation) | (GND), -100 mA[6] | (+60 V), 10 mA[6] | (GND), -10 mA[6] | +5 V, 100 mA[6] |
| ANT to RX ON (Insertion Loss) | (+60 V), 0 mA | (GND), -100 mA[6] | (+60 V), 0 mA | +5 V, 100 mA[6] |
| ANT to TX (Isolation) | (+60 V), 0 mA | (GND), -100 mA[6] | (+60 V), 0 mA | +5 V, 100 mA[6] |

6. Currents level comply with the schematic on page 8.

## Maximum Operating Conditions[7]

| Parameter | Operating Maximum |
|---|---|
| TX Forward Current | 250 mA |
| RX Forward Current | 250 mA |
| Reverse Voltage (RF & DC) | 200 V |
| ANT to TX Power CW | See Power Derating Curve |
| ANT to TX Peak Power (LTE Signal) | 1000 W |
| Junction Temperature[8, 9] | +175 °C |
| Case (Paddle) Temperature | -40 °C to +120 °C |
| Storage Temperature | -55 °C to +150 °C |

7. Exceeding these limits may cause permanent damage.
8. MACOM does not recommend sustained operation near these survivability limits.
9. Operating at nominal conditions with $T_J \leq +175$ °C will ensure MTTF > 1 x $10^6$ hours.

## Handling Procedures

Please observe the following precautions to avoid damage:

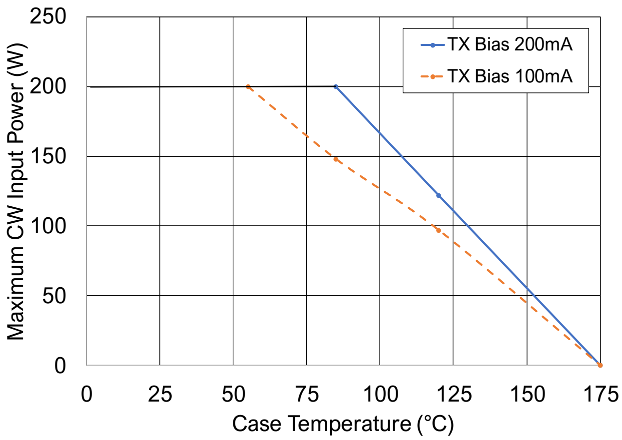
## Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

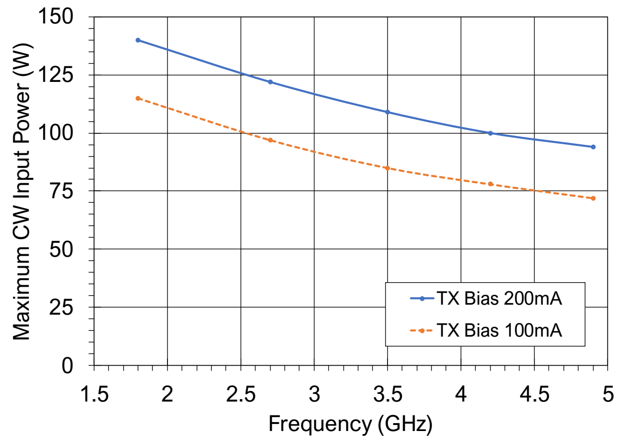
| Parameter | Rating | Standard |
|---|---|---|
| Human Body Model (HBM) | 500 V (Class 1B) | ESDA / JEDEC JS-001 |
| Charged Device Model (CDM) | 2000 V (Class C7) | JEDEC JESD22-C101 |

## Typical Performance Curves

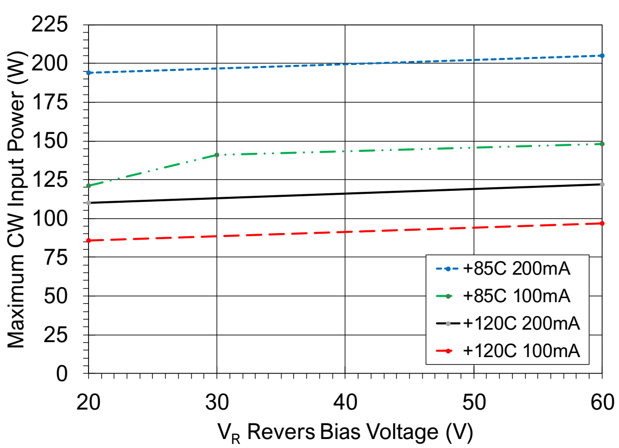
### *ANT to TX Input Power Derating Curve @ 2.7 GHz*




### *ANT to TX Input Power Derating Curve over Frequency @ 120 °C Case Temp*



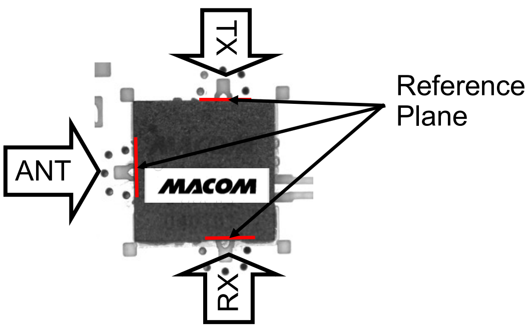

### *ANT to TX Input Power Derating Curve over Reverse Bias Voltage @ 2.7 GHz*



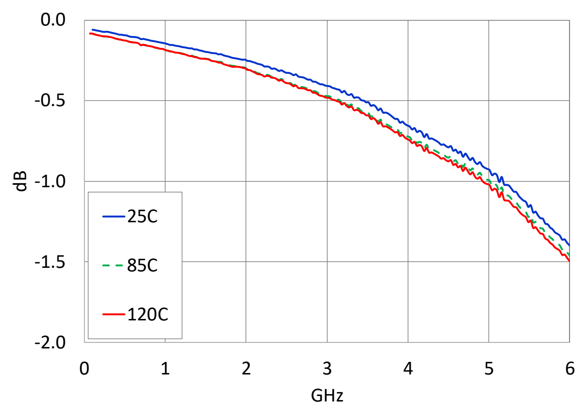
## Typical Performance Curves over Temperature

All plots herein are taken with bias per the Bias Table on Page 2 unless otherwise specified.

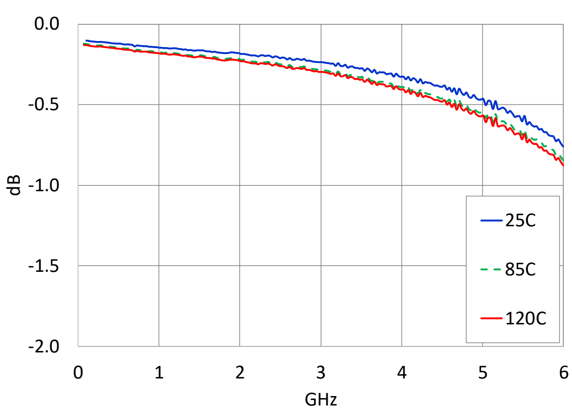
S-parameters were measured using G-S-G probes on a sample board; reference planes are at the part's RF ports. The sample board and its layer stack-up are on page 7



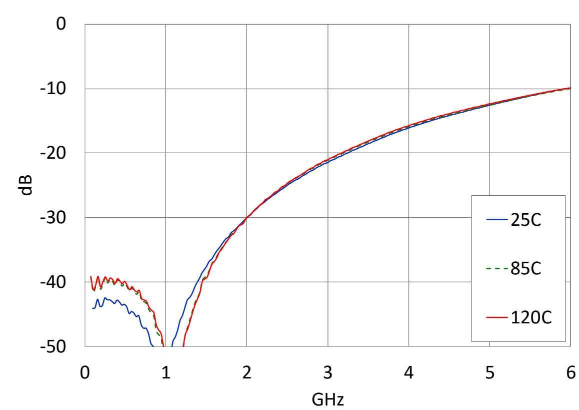

### *ANT to RX Insertion Loss*



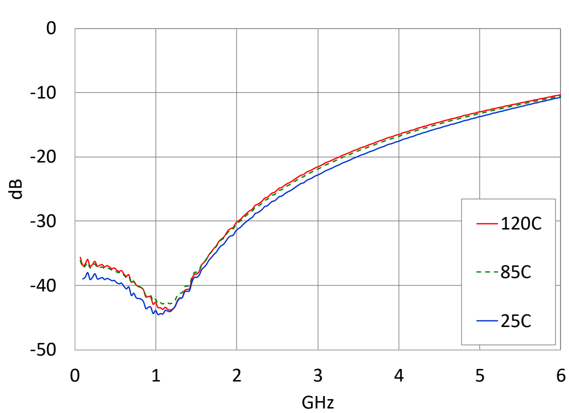

### *ANT to TX Insertion Loss*



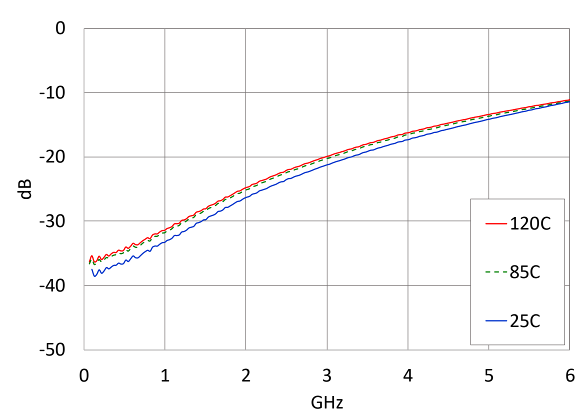

### *ANT Return Loss in RX ON state*




### *ANT Return Loss in TX ON state*

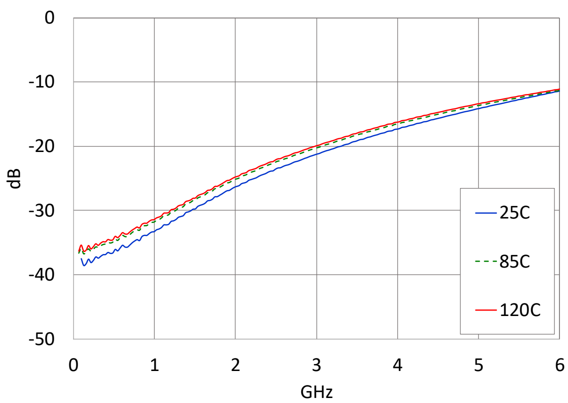



### *RX Return Loss in RX ON state*

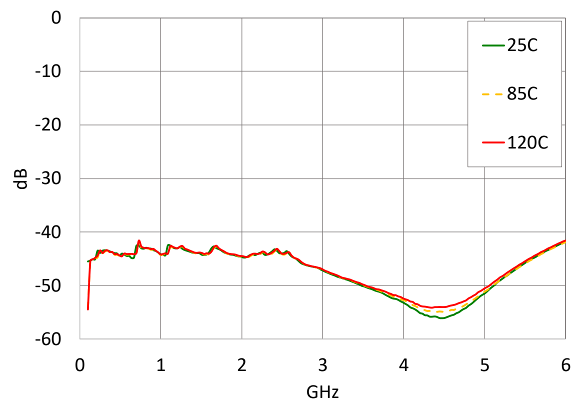


## Typical Performance Curves over Temperature

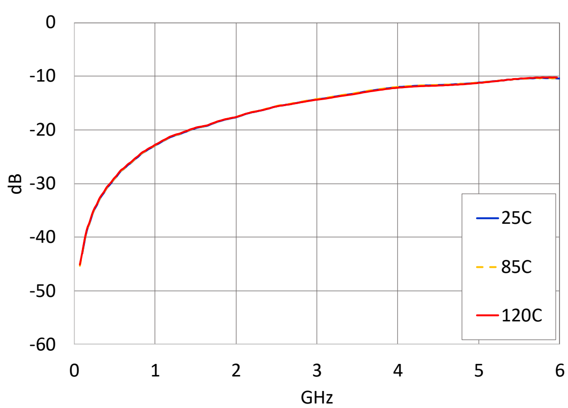
***TX Return Loss in TX ON state***



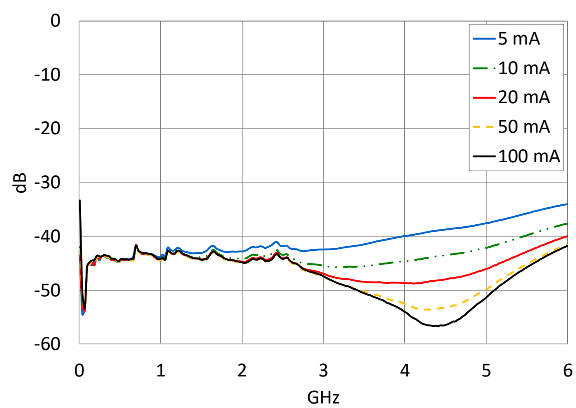

***ANT to RX Isolation in TX ON state @ 100 mA***



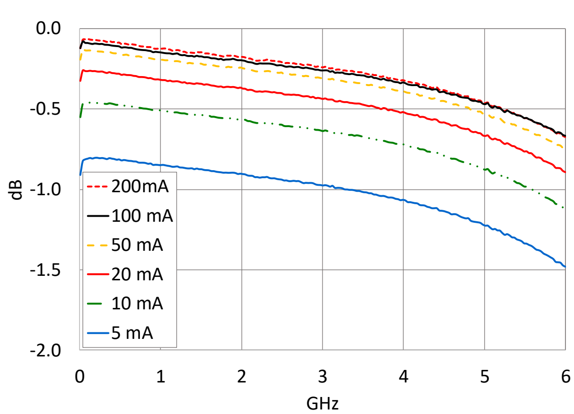

***ANT to TX Isolation in RX ON state***



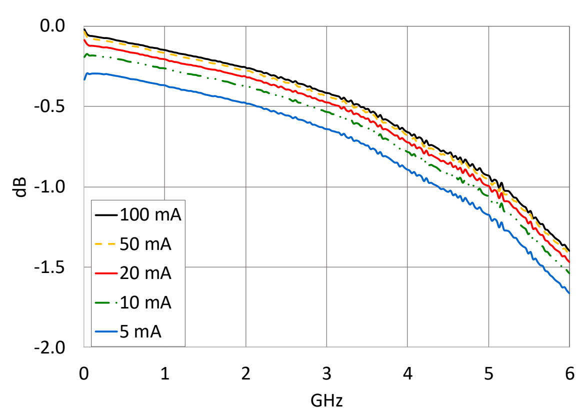

***ANT to RX Isolation in TX ON state, over RX Bias Current @ 25°C***



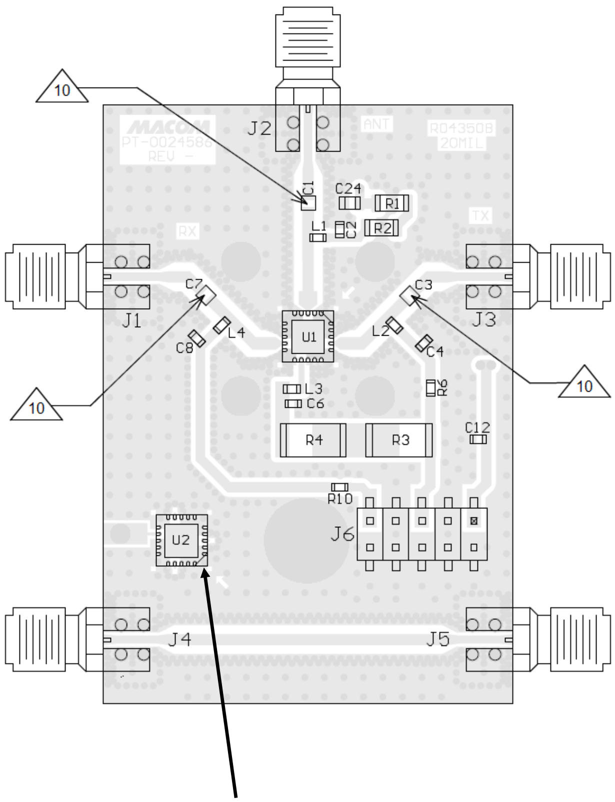

***ANT to TX Insertion Loss over Current @ 25 °C***




***ANT to RX Insertion Loss over Current @ 25 °C***

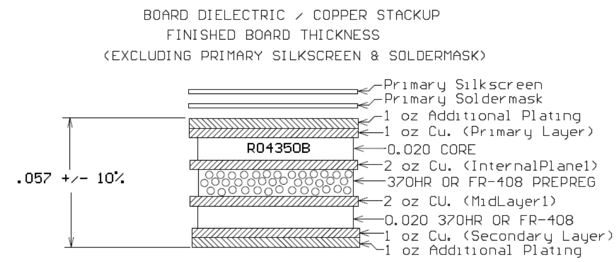


## Sample Board




Optional part for probing, provided per request

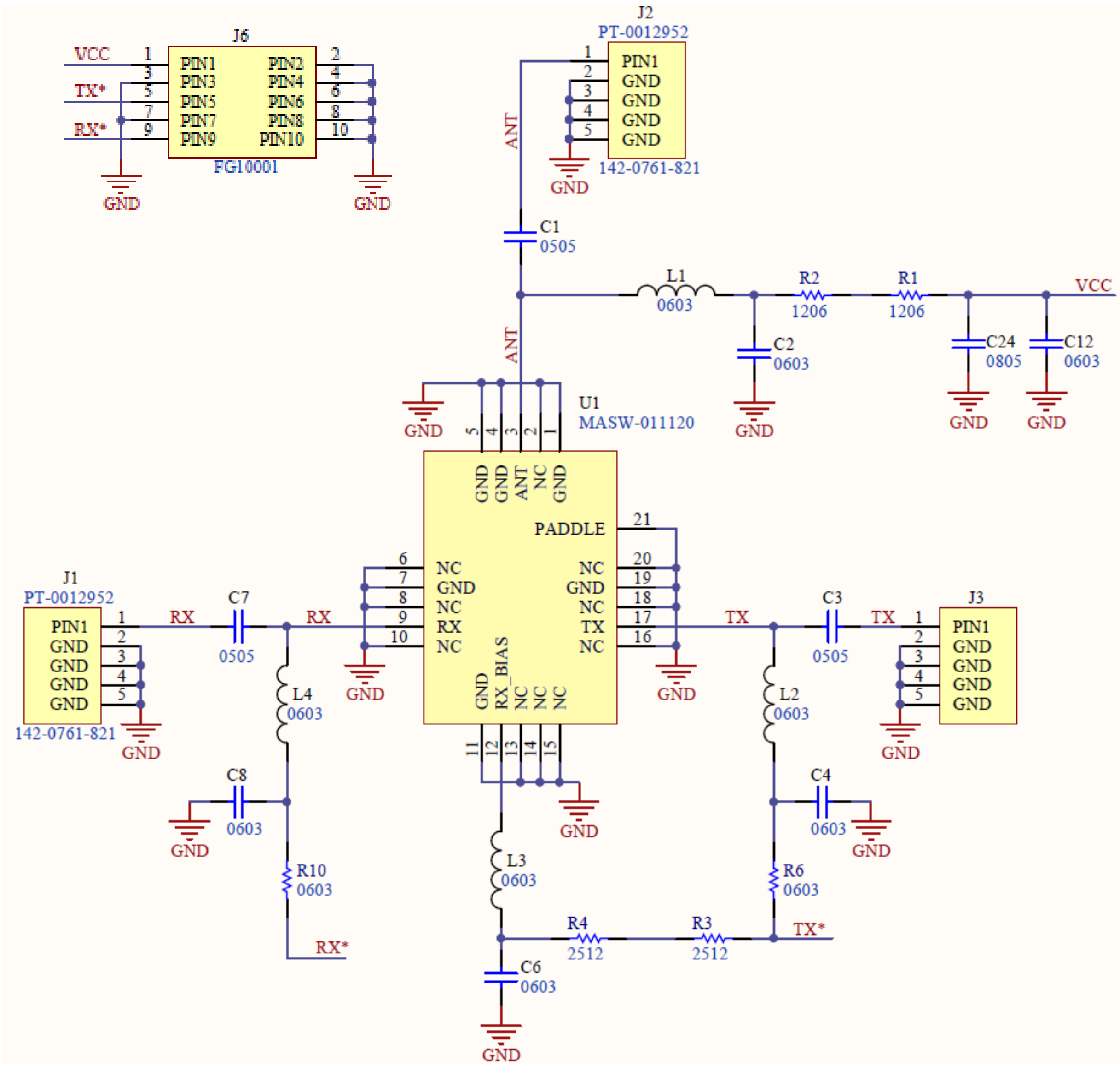
## PCB Layout Stack-Up




Dimensions are in inches.

To use the sample board: bias VCC at 5 V (current will be limited to 100 mA by on-board resistors R1, R2) and bias RX and TX according to the control table on page 8.

## Sample Board Schematic (parts list on page 9)



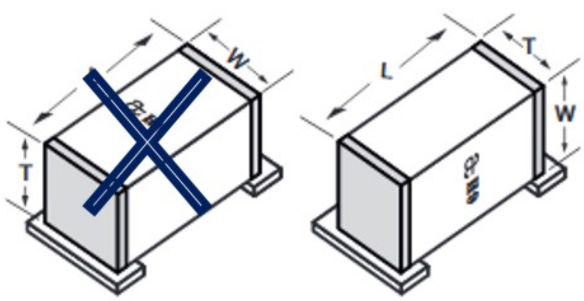

## Control Table

| Configuration | VCC | RX | TX/RX_Bias |
|---|---|---|---|
| TX ON<br>RX OFF | 5 V (100 mA) | 60 V (10 mA) | GND |
| TX OFF<br>RX ON | 5 V (100 mA) | GND | 60 V |

## Parts List

| Component ID | Value | Package | Mfg. Part# | Spec |
|---|---|---|---|---|
| U1 | — | HQFN-20LD 5 mm | MASW-011120 | — |
| L1, L2, L3, L4 | 33 nH | 0603 | LQW18AN33NJ8ZD | >200 mA |
| C1, C3, C7[10] | 10 pF | 0505 | 800A100JT250X | High Freq |
| C2, C4, C6,C8, C12 | 22 pF | 0603 | 600S220FT250XT | High Freq |
| C24 | 1 µF | 0805 | C2012X7S2A105K125AB | High Freq |
| R1, R2 | 20 Ω | 1206 | CRCW120620R0FKEA | 0.25 W |
| R3, R4 | 2.37 kΩ | 2512 | CRCW25122K37FKEA | 1.0 W |
| R6, R10 | 0 Ω | 0603 | — | — |
| J1-J5 | RF CONN | SMA | 142-0761-821 | — |
| J6 | DC CONN | 10-pin | — | Surmount |

10. Required vertical mounting orientation of C1, C3, & C7. Noted on PCB Layout on page 7.




Horizontal
Electrode Orientation

Vertical
Electrode Orientation

## Determination of Minimum Reverse Bias Voltage

The minimum reverse bias voltage required to maintain a PIN diode out of conduction in the presence of a large RF signal is given by:

$$|V_{DC}| = \frac{|V_{RF}|}{\sqrt{1 + \left[\left(\frac{0.0142 \times f_{MHz} \times W_{mils}^2}{V_{RF} \times \sqrt{D}}\right) \times \left(1 + \sqrt{1 + \left(\frac{0.056 \times V_{RF} \times \sqrt{D}}{W_{mils}}\right)^2}\right)\right]^2}}$$

Where:

$|V_{DC}|$ = magnitude of the minimum DC reverse bias voltage
$|V_{RF}|$ = magnitude of the peak RF voltage (including the effects of the voltage standing wave ratio, VSWR)
$f_{MHz}$ = lowest RF signal frequency expressed in MHz
D = duty factor (DF) of the RF signal
$W_{mils}$ = thickness of the diode I layer, expressed in mils (thousands of an inch)

(R. Caverly and G. Hiller, “Establishing the Minimum Reverse Bias for a PIN Diode in a High Power Switch”, IEEE Transactions on Microwave Theory and Techniques, Vol. 38, No. 12, December 1990)

In the transmit state, the large transmit signal voltage appears across a series PIN diode in the receive side of the switch. This diode must be held in its nonconducting state in order to isolate the receiver output port from the large transmit signal applied to the transmit input port.

The minimum magnitude of the reverse DC bias which is necessary to maintain the receive diode in its nonconducting state can be seen from the equation above to be a function of the RF signal voltage, the VSWR in the signal path, the characteristic impedance ($Z_0$) of the signal path, the frequency of the RF signal, the DF of the RF signal and the I layer thickness of the diode in the receive side of the switch.

For a continuous wave signal (i.e., DF = 1) in a $Z_0$ = 50 Ω signal path with VSWR = 1.5:1, the minimum reverse bias voltage required for the MASW-011120 switch to operate properly as a function of input signal frequency and signal power applied to the transmit input is shown in the table below.

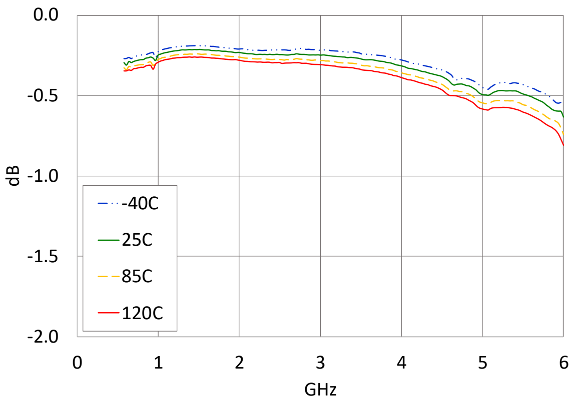
## Minimum Reverse Bias Voltage vs. Signal Frequency & Transmit Input Signal Power
## VSWR = 1.5:1, $Z_0$ = 50 W, Duty Cycle = 1

| Frequency (MHz) | Transmit Input Signal Power (W) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 5 | 10 | 25 | 50 | 100 | 200 |
| 30 | 13 | 18 | 29 | 40 | 63 | 90 | 125 | 175 |
| 100 | 12 | 17 | 27 | 38 | 61 | 85 | 122 | 170 |
| 500 | 5 | 8 | 16 | 26 | 45 | 68 | 98 | 145 |
| 1000 | 3 | 5 | 9.5 | 16 | 30 | 45 | 70 | 105 |
| 2000 | 2 | 3 | 6 | 9 | 17 | 27 | 40 | 60 |
| 4000 | 1 | 2 | 4 | 5 | 9 | 15 | 23 | 35 |
| 6000 | 1 | 1.5 | 2 | 3 | 7.5 | 12 | 15 | 25 |

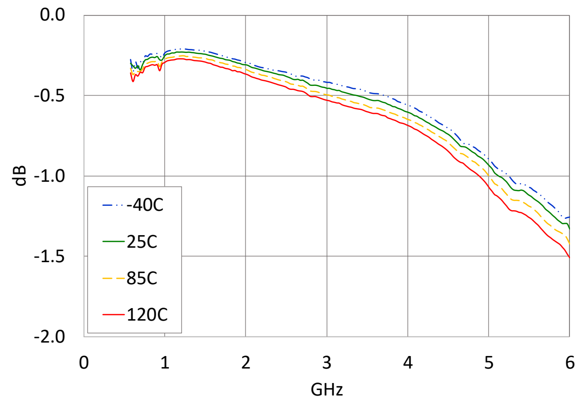
For other conditions, contact the factory for recommended minimum reverse bias voltage.

## Typical Performance Curves on the Sample Board over Temperature

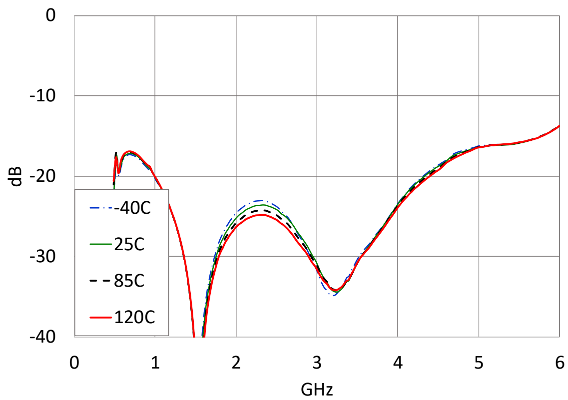
*ANT to TX Insertion Loss (PCB loss de-embedded)*



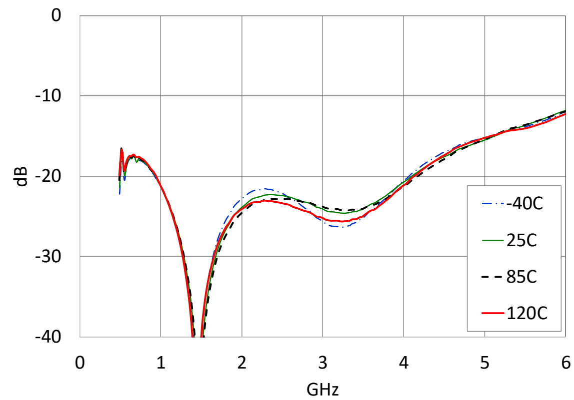

*ANT to RX Insertion (PCB loss de-embedded)*



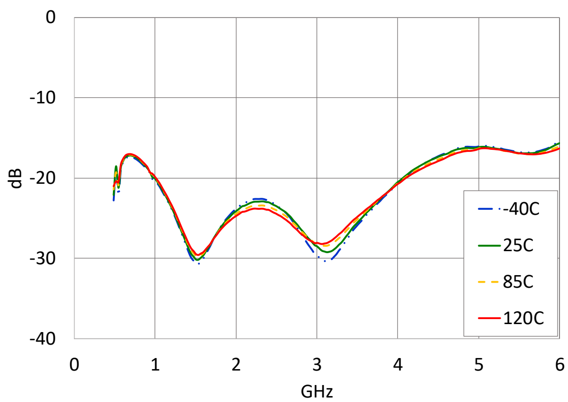

*ANT Return Loss in TX ON state*



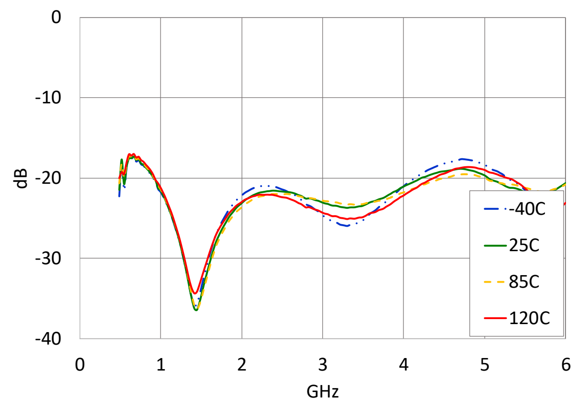

*ANT Return Loss in RX ON state*




*TX Return Loss in TX ON state*

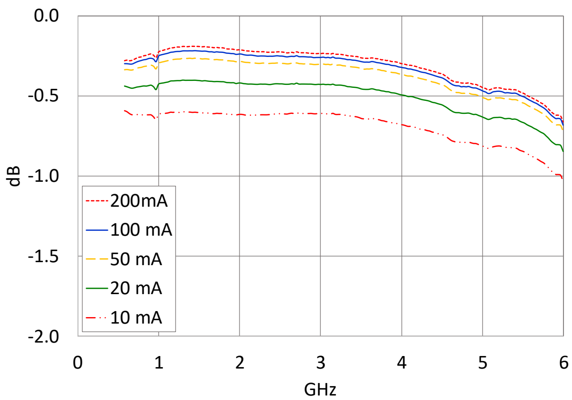



*RX Return Loss in RX ON state*

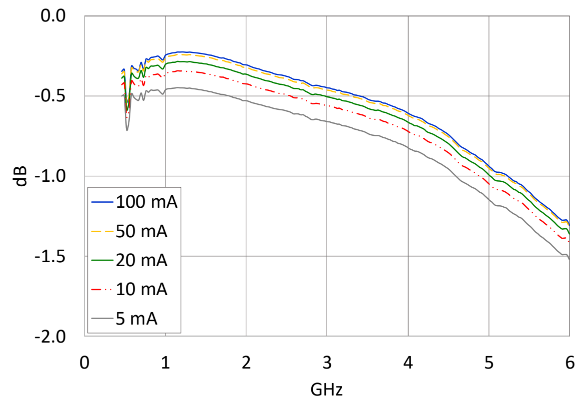


## Typical Performance Curves on the Sample Board over Temperature

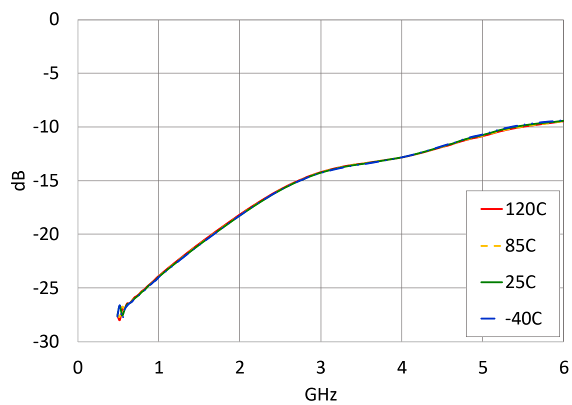
***ANT to TX Insertion Loss over Current @ 25 °C, PCB Loss De-embedded***



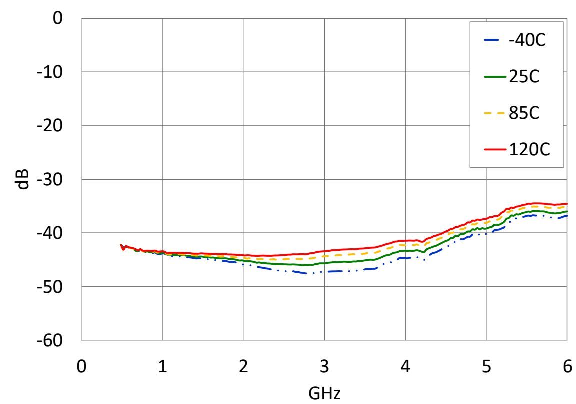

***ANT to RX Insertion Loss over Current @ 25 °C, PCB Loss De-embedded***



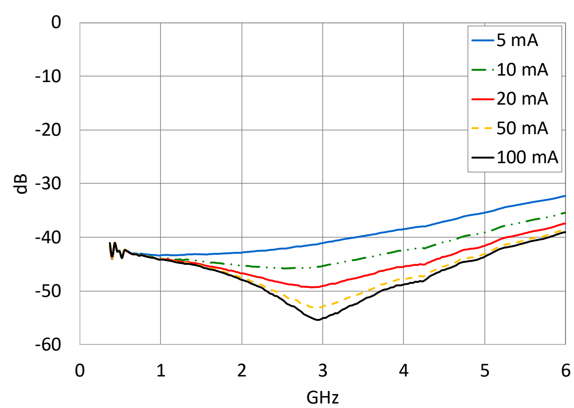

***ANT to TX Isolation***



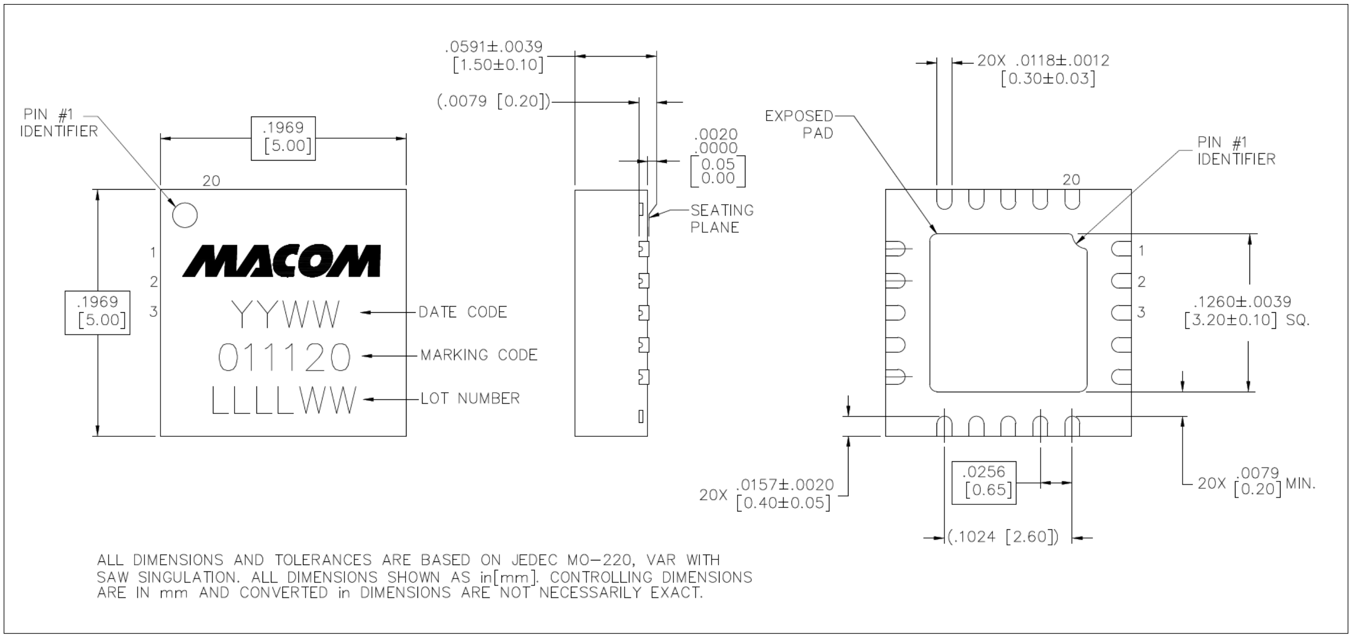

***ANT to RX Isolation***




***ANT to RX Isolation over Current @ 25 °C***



## *Lead-Free 5* mm 20-Lead HQFN†




† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity MSL level 1 requirements.
Plating is NiPdAuAg.