Flat Gain, High Dynamic Range

Monolithic Amplifier PGA-32-75+

75Ω 5 to 300 MHz

The Big Deal

- High IP3
- Flat Gain / Excellent Return Loss
- Low Noise Figure

SOT-89 PACKAGE

Product Overview

PGA-32-75+ (RoHS compliant) is an advanced wideband amplifier fabricated using E-PHEMT technology and offers extremely high dynamic range over a broad frequency range with low noise figure and flat gain. It has repeatable performance from lot to lot and is enclosed in a SOT-89 package for very good thermal performance.

Key Features

Feature	Advantages
Broad Band: 5 to 300 MHz	5 to 300 MHz bandwidth covers primary CATV applications such as DOCSIS 3.1
High IP3 Versus DC power Consumption: 45.5 dBm typical at 100 MHz	The PGA-32-75+ matches industry leading IP3 performance relative to device size and power consumption. The combination of the design and E-PHEMPT structure provides enhanced linearity over a broad frequency range as evidence in the IP3 being typically 15-20 dB above the P 1dB point. This feature makes this amplifier ideal for use in CATV applications.
High IP2, 58.1 dBm at 100 MHz	Suppresses second order product on wideband applications such as CATV
Low Noise Figure, 2.9 dB at 100 MHz	Low noise figure performance in combination with the high output IP3 results in high dynamic range.

75Ω Flat Gain, High Dynamic Range

Monolithic Amplifier

5-300 MHz

Product Features

- High IP3, 45.5 dBm typ. at 100 MHz
- Gain, 15.6 dB typ. at 100 MHz
- High Pout, P1dB 70.5 dBmV typ. at 100 MHz
- Low Noise Figure, 2.9 dB at 100 MHz

Generic photo used for illustration purposes only

CASE STYLE: DF782

Typical Applications

- CATV, DOCSIS 3.1

PGA-32-75+

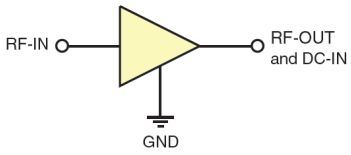
+RoHS Compliant

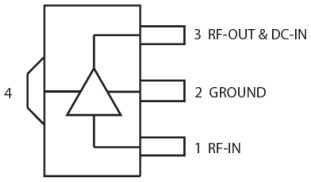
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

General Description

PGA-32-75+ (RoHS compliant) is an advanced wideband amplifier fabricated using E-PHEMT* technology and offers extremely high dynamic range over a broad frequency range and with low noise figure and flat gain. In addition, the PGA-32-75+ has excellent input and output return loss over a broad frequency range. It has repeatable performance from lot to lot and is enclosed in a SOT-89 package for very good thermal performance.

simplified schematic and pin description





Function	Pin Number	Description
RF IN	1	RF input pin. This pin requires the use of an external DC blocking capacitor chosen for the frequency of operation. See Figure 1A & 1B
RF-OUT and DC-IN	3	RF output and bias pin. DC voltage is present on this pin; therefore a DC blocking capacitor is necessary for proper operation. An RF choke is needed to feed DC bias without loss of RF signal due to the bias connection. See Figure 1A & 1B
GND	2,4	Connections to ground. Use via holes as shown in “Suggested Layout for PCB Design” to reduce ground path inductance for best performance.

*Enhanced mode pseudomorhic High Electron Mobility Transistor.

Electrical Specifications at 25°C, 75Ω unless noted

Parameter	Condition (MHz)	TB-966+				TB-916+		Units
		Vd=9V[1]			Vd=5V[1]	Vd=9V[2]	Vd=5V[2]	
		Min.	Typ.	Max.	Typ.	Typ.	Typ.	
Frequency Range		5		300	5-300	5-150	5-150	MHz
Gain	5		15.8		15.3	15.8	15.3	dB
	10		15.7		15.2	15.8	15.2	
	100	14.0	15.6	17.2	15.1	15.7	15.2	
	150		15.6		15.1	15.6	15.1	
	200		15.5		15.0	—	—	
	300		15.4		14.9	—	—	
Gain flatness	5-150		—		—	±0.1	±0.1	dB
	5-300		±0.2		±0.2	—	—	
Input Return Loss	5		13.9		13.4	20.3	18.9	dB
	10		18.2		17.1	19.8	17.5	
	100		22.4		19.8	20.6	18.4	
	150		22.6		19.7	20.7	18.5	
	200		22.4		19.5	—	—	
	300		21.6		18.8	—	—	
Output Return Loss	5		19.8		19.1	19.3	20.0	dB
	10		25.2		23.9	22.5	21.7	
	100		28.4		25.9	23.5	22.0	
	150		26.0		23.8	22.7	21.2	
	200		24.0		21.8	—	—	
	300		18.9		17.4	—	—	
Reversed Isolation	100		20.6		20.5	20.6	20.4	dB
Output Power @1dB Compression	5		20.4(69.1)		19.0(67.8)	23.2(72)	18.5(67.2)	dBm (dBmV)
	10		21.7(70.4)		18.6(67.3)	23.5(72.2)	18.7(67.4)	
	100		23.7(72.5)		18.7(67.4)	23.5(72.3)	18.5(67.3)	
	150		23.7(72.4)		18.6(67.3)	23.6(72.3)	18.5(67.2)	
	200		23.7(72.4)		18.5(67.3)	—	—	
	300		23.6(72.4)		18.3(67.1)	—	—	
Output IP3, Pout= 5dBm	5		43.2		36.8	44.5	37.6	dBm
	10		43.9		37.3	44.7	38.7	
	100		43.3		39.1	45.5	39.9	
	150		43.7		39.1	45.9	39.7	
	200		43.8		39.1	—	—	
	300		43.8		37.7	—	—	
Output IP2[3] Pout= 5dBm	5		57.3		43.1	59.6	45.2	dBm
	10		58.1		43.2	59.1	44.3	
	100		57.2		44.4	58.1	44.8	
	150		56.3		44.1	57.0	44.2	
	200		55.7		44.2	—	—	
	300		56.1		45.6	—	—	
Noise Figure	5		—		—	—	—	dB
	10		3.8		3.4	3.8	3.4	
	100		2.9		2.7	2.9	2.8	
	150		2.8		2.7	2.8	2.7	
	200		2.9		2.7	—	—	
	300		2.9		2.8	—	—	
Device operating voltage			9		5	9	5	V
Device operating current			110	140	54	110	55	mA
Device current variation vs temperature[5]			-2.2		6.5	-2.2	6.5	uA/degC
Device current variation vs voltage			0.014		0.013	0.014	0.013	mA/mV
Thermal resistance, junction-to-ground lead[4]			30		30	30	30	degC/W

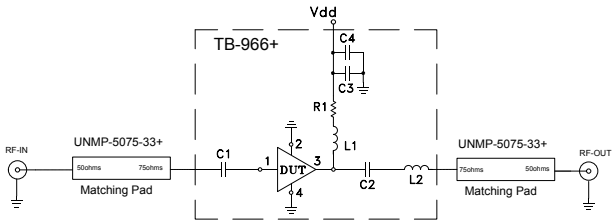
1. Measured on Mini-Circuits Characterization and Test Circuit TB-966+. See Fig. 1A
2. Measured on Mini-Circuits Characterization and Test Circuit TB-916+. See Fig. 1B
3. Output IP2 measured at sum frequency of the two tones(f meas= f1+f2)
4. Junction to ground lead
5. (Current 85°C - Current at -45°C)/130

Absolute Maximum Ratings[5]

Parameter	Ratings
Operating Temperature (ground lead)	-40°C to 85°C
Storage Temperature	-65°C to 150°C
Power Dissipation	2.2 W
Input Power (CW)	+23 dBm (5 minutes) +18 dBm (continuous)
DC Voltage on Pin 3	11 V

5. Permanent damage may occur if any of these limits are exceeded.
Electrical maximum ratings are not intended for continuous normal operation.

Recommended Application Circuit (TB-966+)

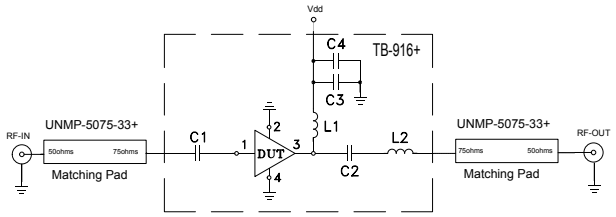


COMPONENT	P/N	VALUE	SIZE
DUT	PGA-32-75+	—	SOT-89
C1,C4	GRM155R71C104KA88D	0.1uF	0402
C2	GRM155R71E103KA01D	0.01uF	0402
C3	GRM1555C1H102JA01D	0.001uF	0402
L1	LQH32MN6R8K23L	6800nH	1210
L2	LQW15AN12NH00D	12nH	0402
R1	RK73H1JTTD4R99F	4.99 Ohm	0603

Fig 1A. Block Diagram of Test Circuit used for characterization. (DUT soldered on TB-966+)
Gain, Return loss, Output power at 1dB compression (P1 dB) , output IP3 (OIP3), output IP2 (OIP2) and noise figure measured using Agilent's N5242A PNA-X microwave network analyzer & E5071C ENA Series Network Analyzer.

Conditions:
1. Gain and Return loss: Pin= -25dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, 5 dBm/tone at output.
3. Output IP2 (OIP2): Two tones, spaced 1 MHz apart, 5 dBm/tone at output.

Characterization Test Circuit (TB-916+)

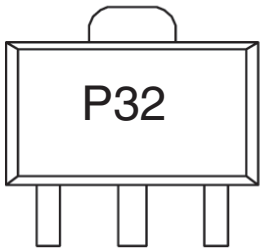


COMPONENT	SUPPLIER P/N	VALUE	SIZE
DUT	PGA-32-75+	—	SOT-89
C1	GRM32ER7YA106KA12L	10uF	1210
C2	GRM155R71E103KA01D	0.01uF	0402
C3	GRM1555C1H102JA01D	0.001uF	0402
C4	GRM155R71C104KA88D	0.1uF	0402
L1	1008CS-682XJLC	6.8uH	1008
L2	LQW15AN12NH00D	12nH	0402

Fig 1B. Block Diagram of Test Circuit used for characterization. (DUT soldered on TB-916+)
Gain, Return loss, Output power at 1dB compression (P1 dB) , output IP3 (OIP3), output IP2 (OIP2) and noise figure measured using Agilent's N5242A PNA-X microwave network analyzer & E5071C ENA Series Network Analyzer.

Conditions:
1. Gain and Return loss: Pin= -25dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, 5 dBm/tone at output.
3. Output IP2 (OIP2): Two tones, spaced 1 MHz apart, 5 dBm/tone at output.

Product Marking



Marking may contain other features or characters for internal lot control

Additional Detailed Technical Information *additional information is available on our dash board. To access this information click here*	
Performance Data	Data Table
	Swept Graphs
	S-Parameter (S2P Files) Data Set (.zip file)
5-200 MHz Operation	See Application Note AN-60-087
Case Style	DF782 (SOT 89) *Plastic package, exposed paddle* *Lead Finish: Matte-Tin*
Tape & Reel **Standard quantities available on reel**	F55 *7" reels with 20, 50, 100, 200, 500 or 1K devices*
Suggested Layout for PCB Design	PL-521
Evaluation Board	TB-966+ (5-300 MHz) & TB-916+ (5-150 MHz)
Environmental Ratings	ENV08T1

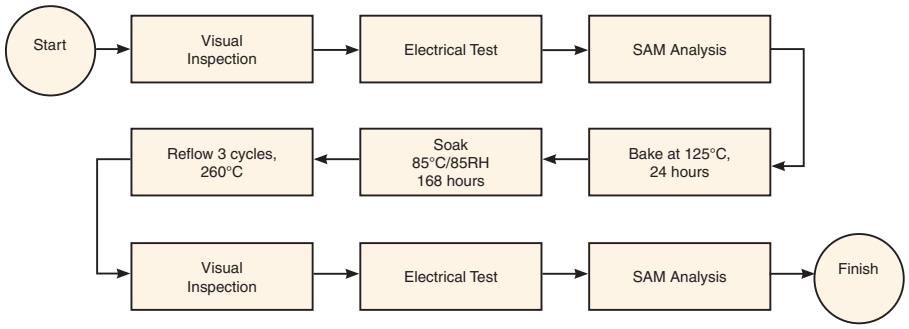
ESD Rating

Human Body Model (HBM): Class 1A (250 to <500) in accordance with ANSI/ESD STM 5.1 - 2001
Machine Model (MM): Class M1 (25V) in accordance with ANSI/ESD STM5.2-1999

MSL Rating

Moisture Sensitivity: MSL1 in accordance with IPC/JEDEC J-STD-020D

MSL Test Flow Chart



Additional Notes

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.

C. The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp