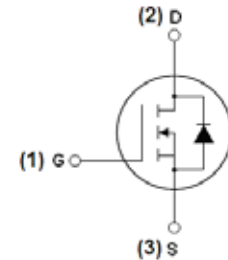


N-Channel Super Trench Power MOSFET

Description

The RM48N100D3 uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.



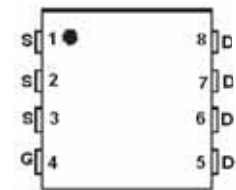
Schematic diagram

General Features

- $V_{DS} = 100V, I_D = 48A$
 $R_{DS(ON)} < 13.6m\Omega @ V_{GS} = 10V$
 $R_{DS(ON)} < 22m\Omega @ V_{GS} = 4.5V$
- Excellent gate charge x $R_{DS(on)}$ product
- Very low on-resistance $R_{DS(on)}$
- Pb-free lead plating
- 100% UIS tested



pin assignment



DFN 3x3 EP top view

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification
- Halogen-free
- P/N suffix V means AEC-Q101 qualified, e.g:RM48N100D3V

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
48N100	RM48N100D3	DFN 3X3	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	20/-12	V
Drain Current-Continuous (Silicon Limited)	I_D	48	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	30	A
Pulsed Drain Current	I_{DM}	192	A
Maximum Power Dissipation	P_D	61	W
Derating factor		0.49	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	115	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-50 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	2.04	°C/W
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Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.5	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	11.3	13.6	$m\Omega$
		$V_{GS}=4.5V, I_D=15A$	-	16.7	22	$m\Omega$
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=3A$	-	8	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0MHz$	-	1640	3280	PF
Output Capacitance	C_{oss}		-	240	480	PF
Reverse Transfer Capacitance	C_{rss}		-	4	10	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=1A$ $V_{GS}=10V, R_G=6\Omega$	-	14.2	28	nS
Turn-on Rise Time	t_r		-	20.8	42	nS
Turn-Off Delay Time	$t_{d(off)}$		-	42	84	nS
Turn-Off Fall Time	t_f		-	30	60	nS
Total Gate Charge	Q_g	$V_{DS}=50V, I_D=10A,$ $V_{GS}=10V$	-	27.8	55	nC
Gate-Source Charge	Q_{gs}		-	3.5	7	nC
Gate-Drain Charge	Q_{gd}		-	8.8	17	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=1A$	-		1.0	V
Diode Forward Current ^(Note 2)	I_S		-	-	48	A
Reverse Recovery Time	t_{rr}	$T_J=25^\circ\text{C}, I_F=I_S$	-	43.5		nS
Reverse Recovery Charge	Q_{rr}	$di/dt=100A/\mu s$ ^(Note 3)	-	59.6		nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^\circ\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

RATING AND CHARACTERISTICS CURVES (RM48N100D3)

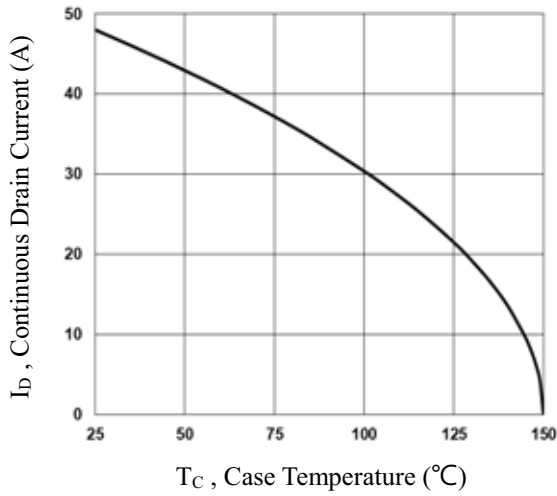


Fig.1 Continuous Drain Current vs. T_c

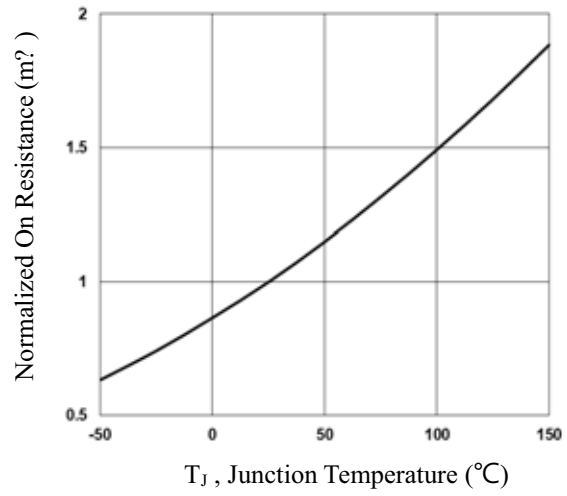


Fig.2 Normalized $R_{DS(on)}$ vs. T_j

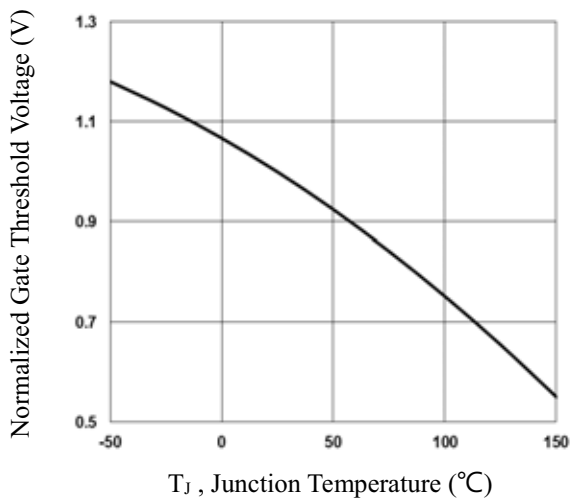


Fig.3 Normalized V_{th} vs. T_j

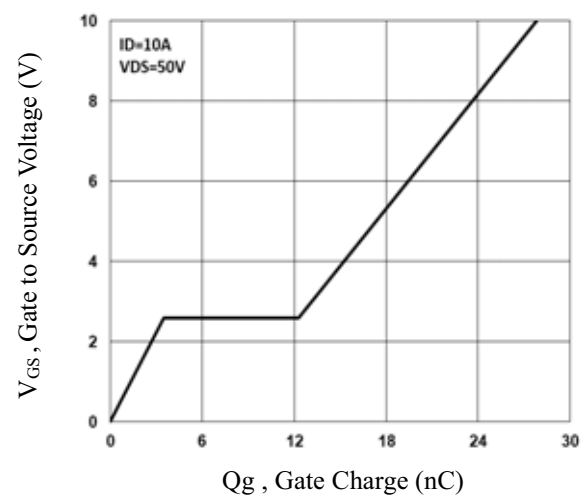


Fig.4 Gate Charge Characteristics

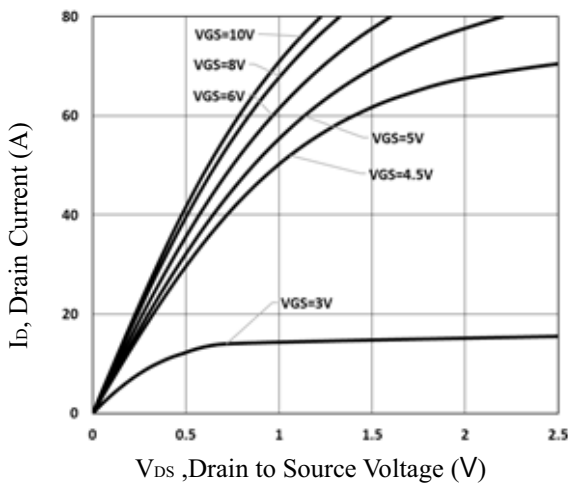


Fig.5 Typical Output Characteristics

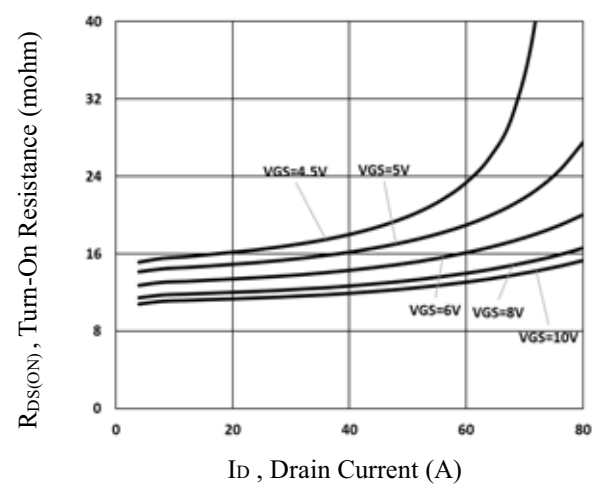


Fig.6 Turn-On Resistance vs. I_D

RATING AND CHARACTERISTICS CURVES (RM48N100D3)

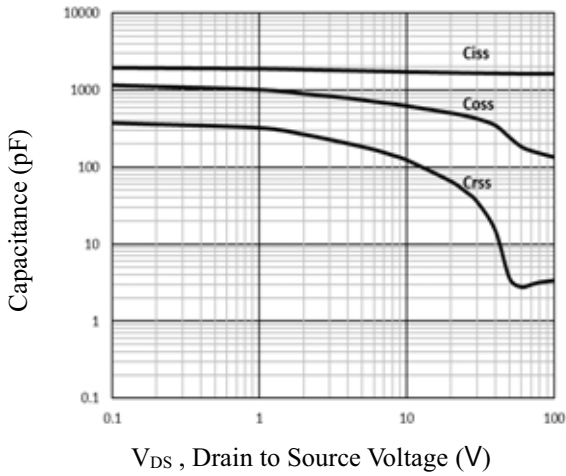


Fig.7 Capacitance Characteristics

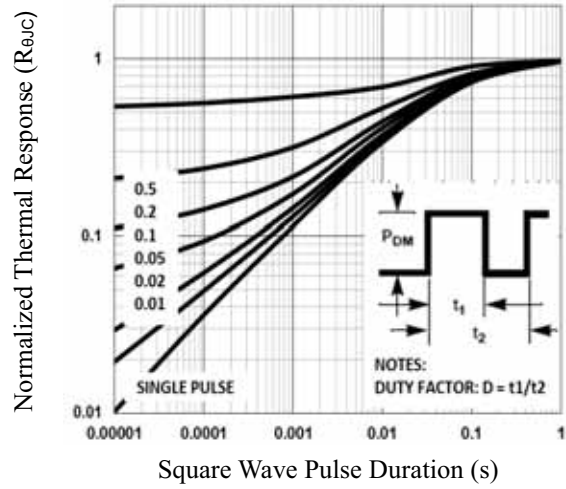


Fig.8 Normalized Transient Impedance

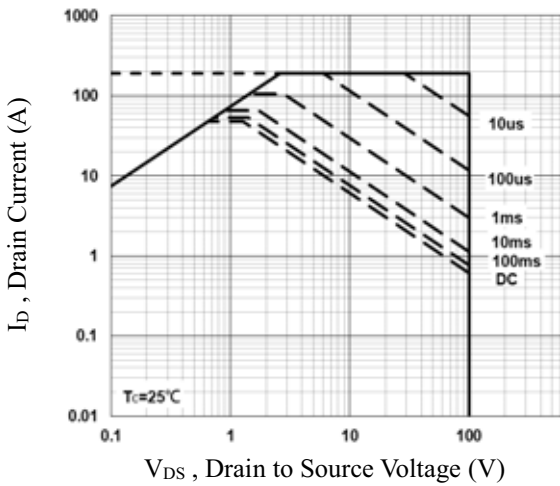


Fig.9 Maximum Safe Operation Area

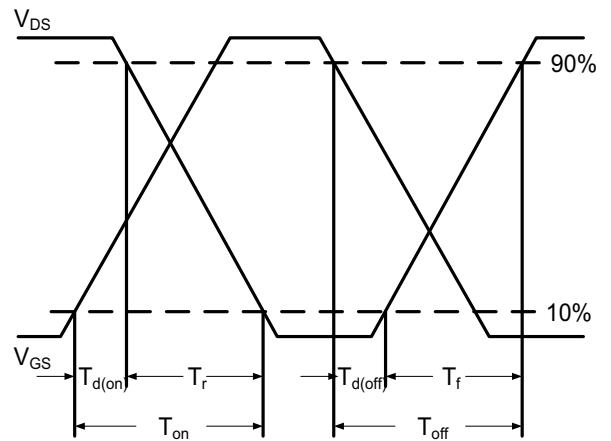


Fig.10 Switching Time Waveform

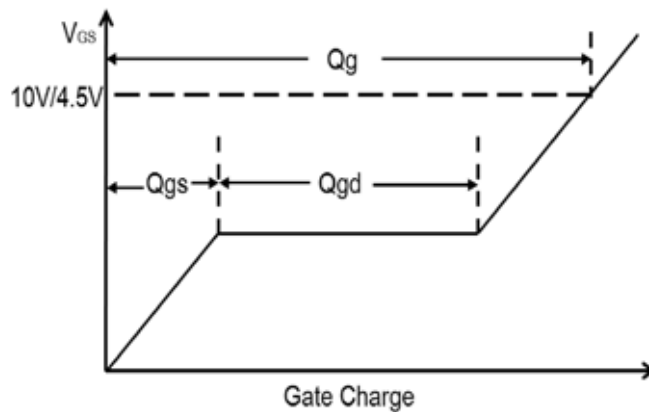
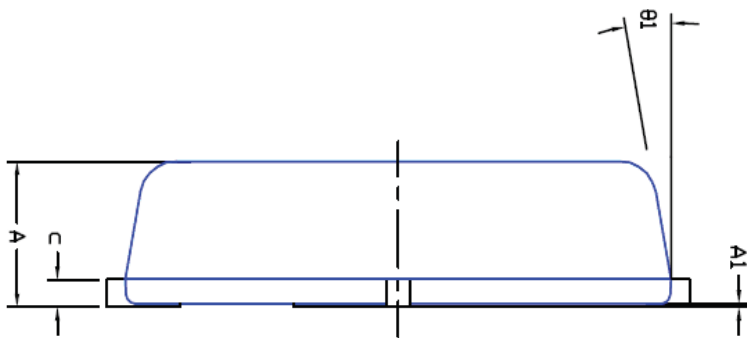
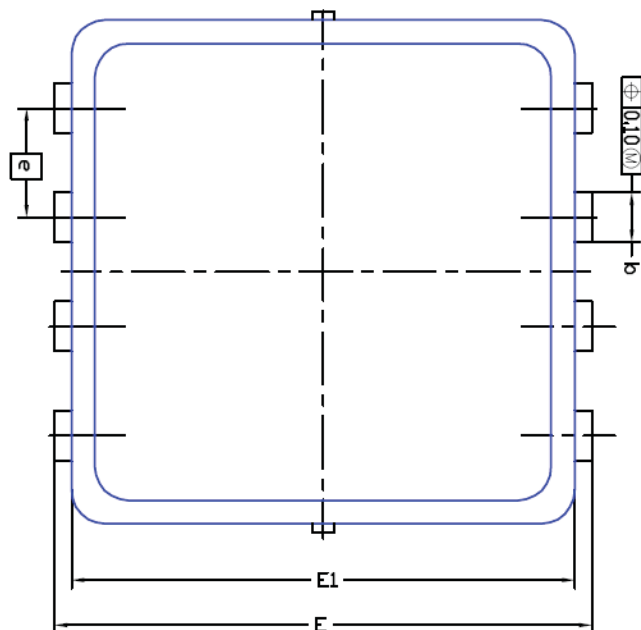
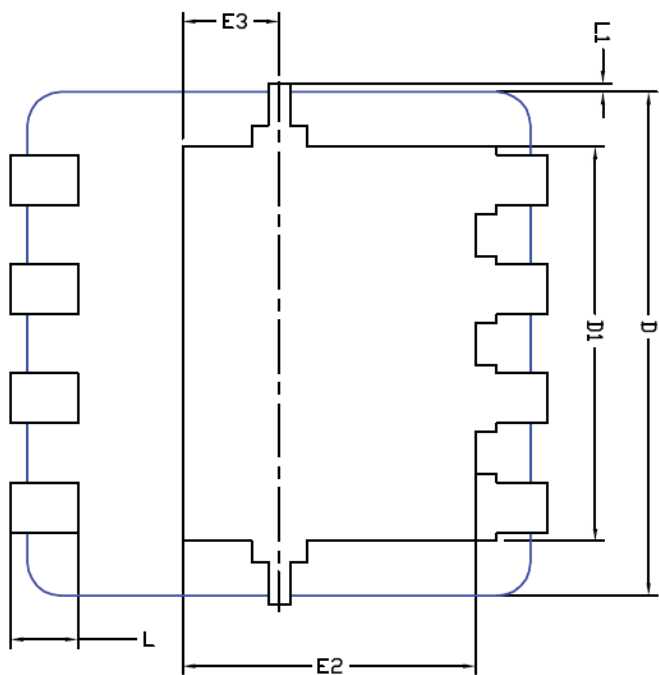


Fig.11 Gate Charge Waveform

DFN3X3 EP Package Information



DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.10	0.152	0.25	0.004	0.006	0.010
D	3.00 BSC			0.118 BSC		
D1	2.35 BSC			0.093 BSC		
E	3.20 BSC			0.126 BSC		
E1	3.00 BSC			0.118 BSC		
E2	1.75 BSC			0.069 BSC		
E3	0.575 BSC			0.023 BSC		
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
L1	0	---	0.100	0	---	0.004
θ1	0°	10°	12°	0°	10°	12°

Package	Tube (pcs/tube)	Tube (pcs/inner box)	Tube (pcs/cartoon)	Tape&Reel (pcs/reel)	Tape&Reel (pcs/inner box)	Tape&Reel (pcs/cartoon)
DFN5x6/DFN3x3	100	10,000	100,000	2,500	5,000	40,000
DFN1006	—	—	—	10,000	10,000	400,000
SOP-8	100	10,000	100,000	4,000	4,000	64,000
TSSOP-8	100	32,000	128,000	3,000	6,000	48,000
SOT-23-3L	—	—	—	3,000	30,000	120,000
SOT-23-6L	—	—	—	3,000	30,000	120,000
SOT-23(6R)	—	—	—	3,000	30,000	120,000
SOT-363	—	—	—	3,000	30,000	120,000
SOT-523	—	—	—	3,000	30,000	120,000
SOT223	—	—	—	2,500	2,500	20,000
TO-220	50	1,000	5,000	—	—	—
TO-220F	50	1,000	10,000	—	—	—
TO-247	30	300	1,200	—	—	—
TO-251	80	4,000	40,000	—	—	—
TO-251S(4R)	80	4,000	40,000	—	—	—
TO-252-2L(4R)	80	4,000	40,000	2,500	2,500	25,000
TO-263-2L	50	1,000	10,000	800	800	8,000
TO-3P	30	300	3,000	—	—	—
TO-92	—	—	—	1,000(袋装)	10,000	100,000

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