

MOSFET – Single, N-Channel, POWERTRENCH®

80 V, 6 A, 36.5 mΩ

FDMA037N08LC

Description

This device has been designed to provide maximum efficiency and thermal performance for synchronous buck converters. The low $R_{DS(on)}$ and gate charge provide excellent switching performance.

Features

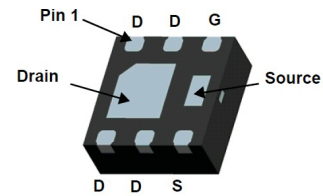
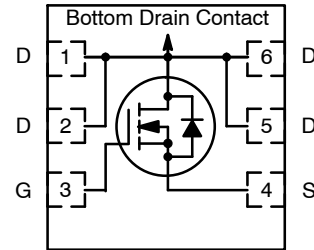
- PTNG MOSFET Technology
- Max $R_{DS(on)}$ = 36.5 mΩ at V_{GS} = 10 V, I_D = 4 A
- Max $R_{DS(on)}$ = 56.9 mΩ at V_{GS} = 4.5 V, I_D = 3 A
- 5 V Drive Capable
- 50% Lower Q_{rr} than Other MOSFET Suppliers
- Lower Switching Noise/EMI
- Low Profile – 0.8 mm Maximum in the New Package MicroFET™ 2x2 mm
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- DC-DC Buck Converters

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
80 V	36.5 mΩ @ 10 V	6 A

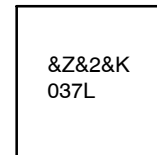
Single N-Channel



MicroFET 2X2 (Bottom View)

WDFN6 2x2, 0.65P
CASE 511DB

MARKING DIAGRAM



- &Z = Assembly Plant Code
- &2 = Numeric Date Code
- &K = Lot Code
- 037L = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDMA037N08LC

MOSFET MAXIMUM RATINGS (T_A = 25°C, Unless otherwise specified)

Symbol	Parameter	Ratings	Unit
V _{DS}	Drain to Source Voltage	80	V
V _{GS}	Gate to Source Voltage	±20	V
I _D	Continuous T _A = 25°C (Note 1a)	6	A
	Pulsed	55	
P _D	Power Dissipation T _A = 25°C (Note 1a)	2.4	W
	Power Dissipation T _A = 25°C (Note 1b)	0.9	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1b)	145	

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Shipping (Qty / Packing) [†]
037L	FDMA037N08LC	WDFN6 2x2, 0.65P (MicroFET) (Pb-Free/Halogen Free)	7"	8 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	80	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	-	69	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 64 V, V _{GS} = 0 V	-	-	-1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	-	-	±1	μA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 20 μA	1.0	1.3	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 20 μA, referenced to 25°C	-	-5	-	mV/°C
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 4 A	-	30.9	36.5	mΩ
		V _{GS} = 4.5 V, I _D = 3 A	-	42.1	56.9	
		V _{GS} = 10 V, I _D = 4 A, T _J = 125°C	-	51.4	61	
g _{FS}	Forward Transconductance	V _{DD} = 5 V, I _D = 4 A	-	15	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz	-	425	595	pF
C _{oss}	Output Capacitance		-	110	155	pF
C _{rss}	Reverse Transfer Capacitance		-	6.0	8.3	pF

FDMA037N08LC

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS						
t _{d(on)}	Turn-on Delay Time	V _{DD} = 40 V, I _D = 4 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	4.9	10	ns
t _r	Rise Time		–	1.3	10	
t _{d(off)}	Turn-off Delay Time		–	14	24	
t _f	Fall Time		–	1.7	10	
Q _g	Total Gate Charge	V _{GS} = 0V to 10 V, V _{DD} = 40 V, I _D = 4 A	–	6.5	9.0	nC
Q _g	Total Gate Charge	V _{GS} = 0V to 4.5 V, V _{DD} = 40 V, I _D = 4 A	–	3.2	4.5	nC
Q _{gs}	Gate to Source Charge	V _{DD} = 40 V, I _D = 4 A	–	0.9	–	nC
Q _{gd}	Gate to Drain "Miller" Charge	V _{DD} = 40 V, I _D = 4 A	–	0.9	–	nC
Q _{oss}	Output Charge	V _{DD} = 40 V, V _{GS} = 0 V	–	6.4	–	nC
Q _{sync}	Total Gate Charge Sync	V _{DS} = 0 V, I _D = 4 A	–	5.9	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2 A (Note 2)	–	0.8	1.2	V
		V _{GS} = 0 V, I _S = 4 A (Note 2)	–	0.8	1.3	V
t _{rr}	Reverse Recovery Time	I _F = 2 A, di/dt = 300 A/μs	–	10	20	ns
Q _{rr}	Reverse Recovery Charge		–	9	14	nC
t _{rr}	Reverse Recovery Time	I _F = 2 A, di/dt = 1000 A/μs	–	8	16	ns
Q _{rr}	Reverse Recovery Charge		–	26	51	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θJA} is determined by the user's board design.



- a) 52°C/W when mounted on a 1 in² pad of 2 oz copper.



- b) 145°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

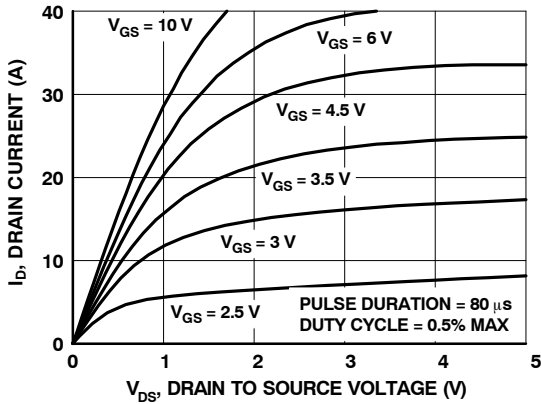


Figure 1. On Region Characteristics

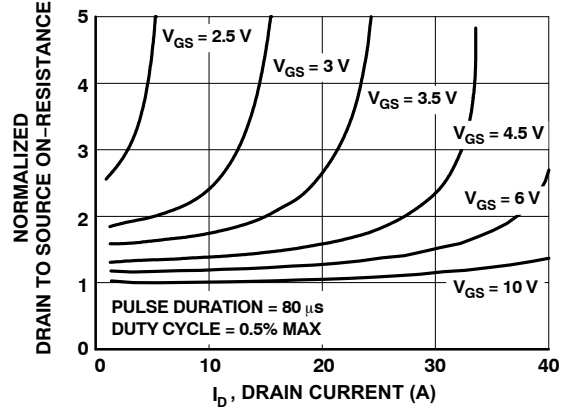


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

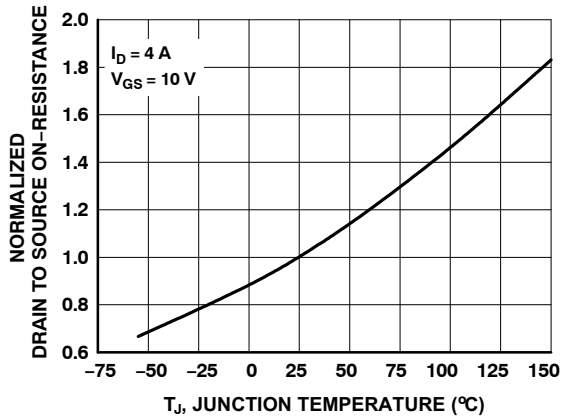


Figure 3. Normalized On Resistance vs. Junction Temperature

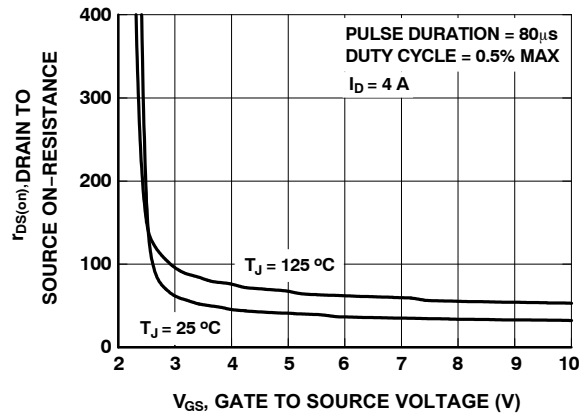


Figure 4. On-Resistance vs. Gate to Source Voltage

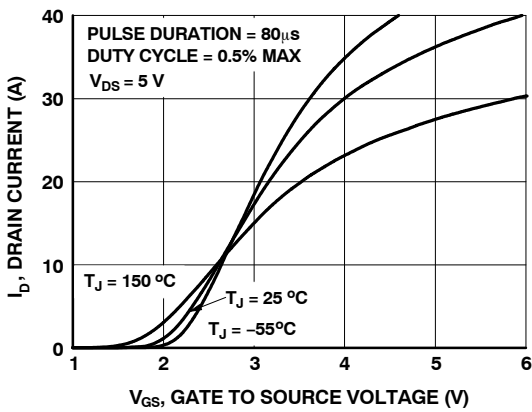


Figure 5. Transfer Characteristics

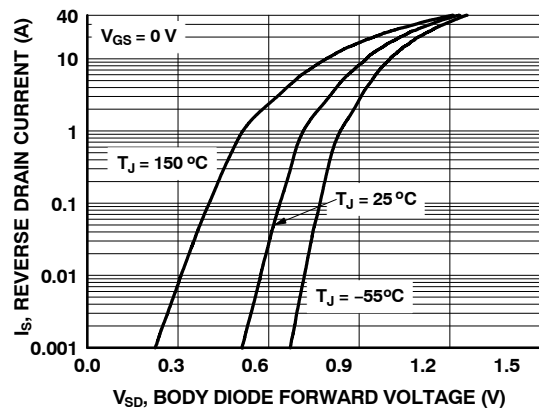


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (CONTINUED)

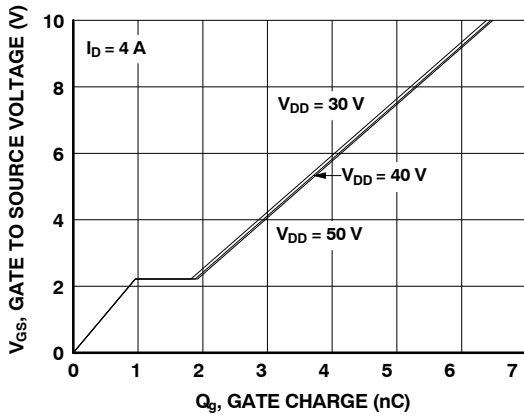


Figure 7. Gate Charge Characteristics

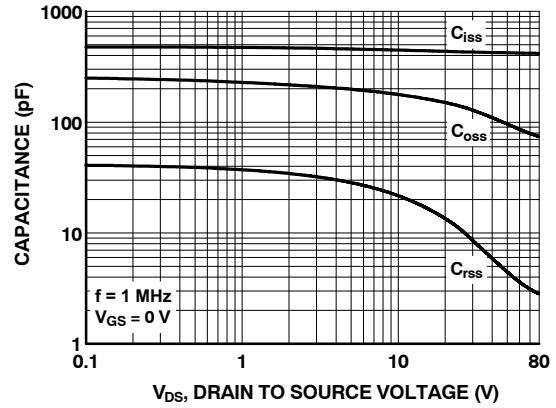


Figure 8. Capacitance vs. Drain to Source Voltage

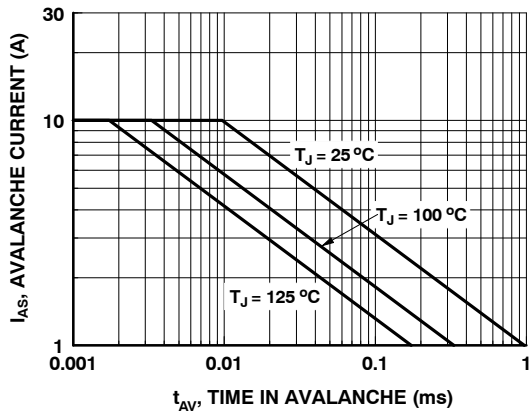


Figure 9. Unclamped Inductive Switching Capability

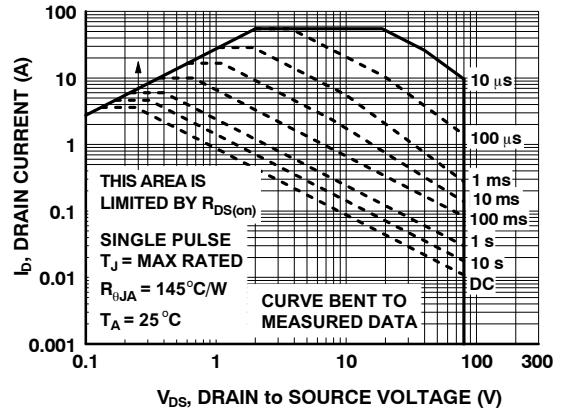


Figure 10. Forward Bias Safe Operating Area

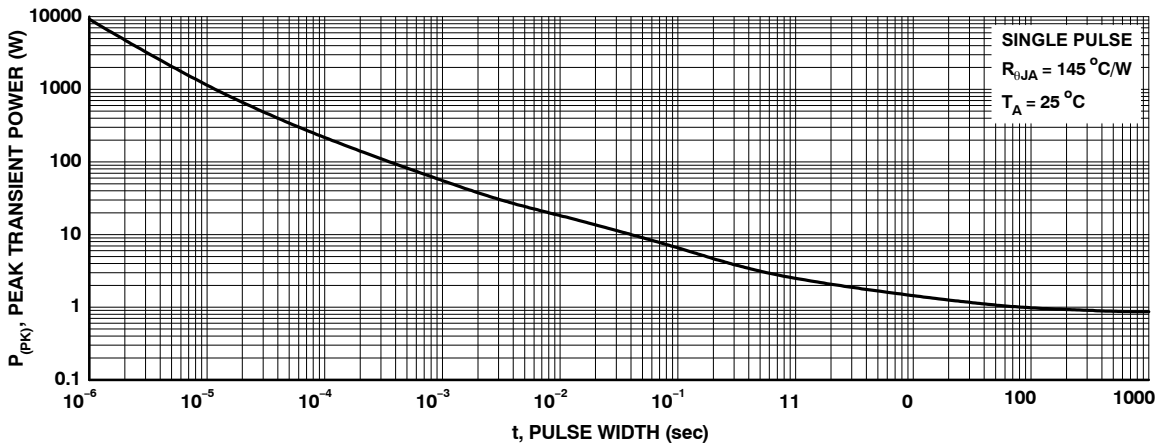


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (CONTINUED)

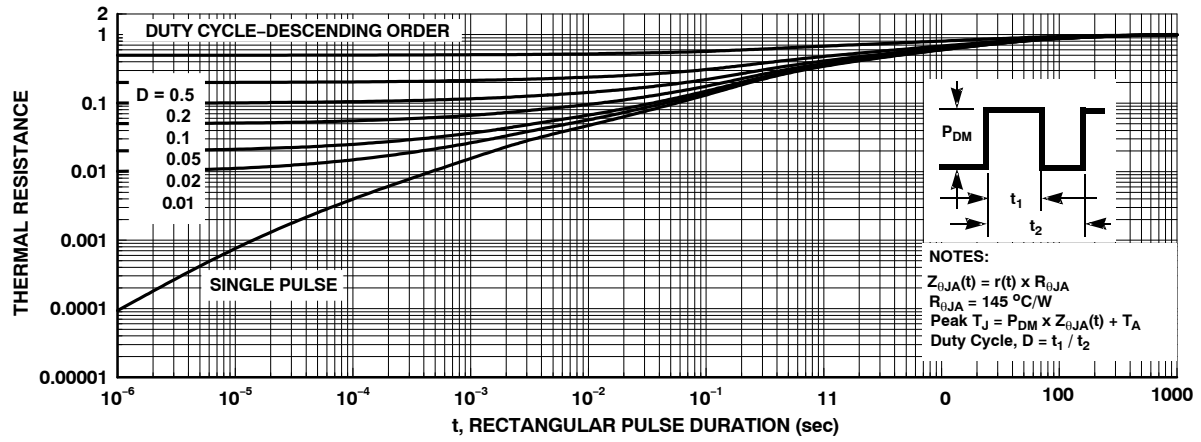


Figure 12. Junction-to-Case Transient Thermal Response Curve

MECHANICAL CASE OUTLINE

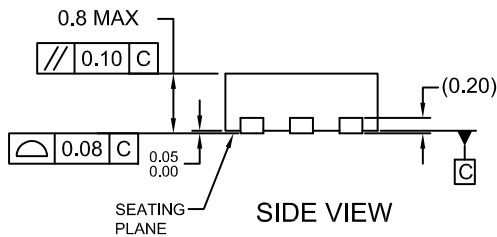
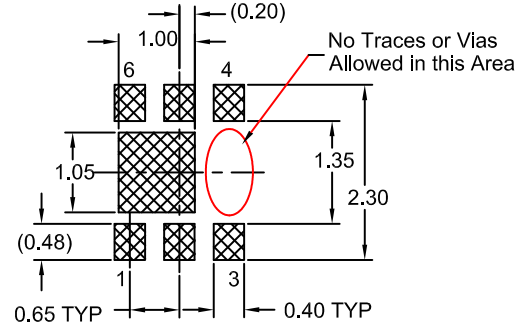
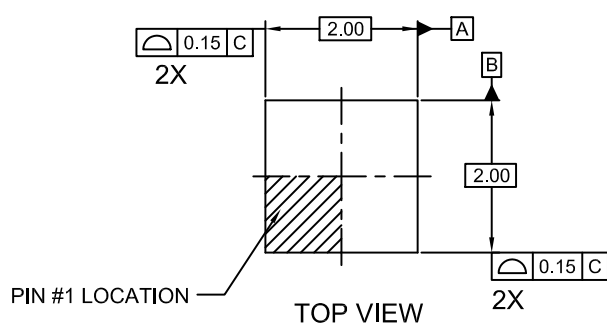
PACKAGE DIMENSIONS

ON Semiconductor®

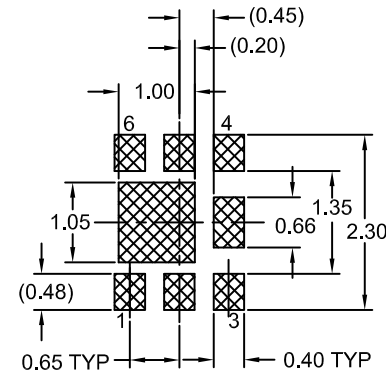
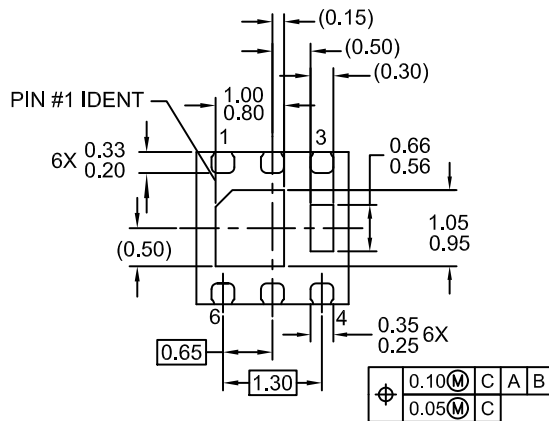


WDFN6 2x2, 0.65P
CASE 511DB
ISSUE O

DATE 31 AUG 2016



RECOMMENDED LAND PATTERN OPT 1



BOTTOM VIEW

RECOMMENDED LAND PATTERN OPT 2

NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-229 DATED AUG/2003
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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