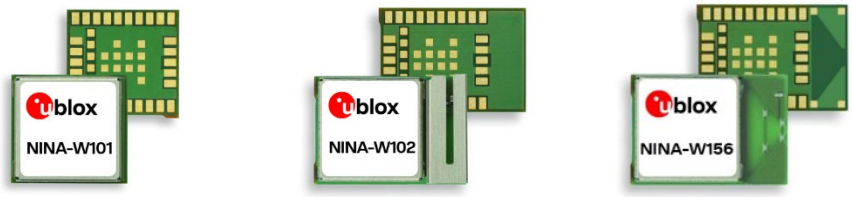
NINA-W1 series

Stand-alone Wi-Fi and multiradio modules

System integration manual



Abstract

This document describes the system integration of NINA-W1 series stand-alone modules, which includes the NINA-W13 (Wi-Fi) and NINA-W10 and NINA-W15 series (multiradio) modules. These modules feature a number of useful embedded security features, including secure boot that ensures that only authenticated software can run on the module. NINA-W1 modules are ideal for critical IoT applications where security is important. The modules connect to a host system using UART, high-speed RMII, or GPIO interfaces.

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Document information

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Document status descriptions	
Draft	For functional testing. Revised and supplementary data will be published later.
Objective Specification	Target values. Revised and supplementary data will be published later.
Advance Information	Data based on early testing. Revised and supplementary data will be published later.
Early Production Information	Data from product verification. Revised and supplementary data may be published later.
Production Information	Document contains the final product specification.

This document applies to the following products:

Product name	**Document status**
NINA-W101	Early Production Information
NINA-W102	Early Production Information
NINA-W106	Early Production Information
NINA-W131	Early Production Information
NINA-W132	Early Production Information
NINA-W151	Early Production Information
NINA-W152	Early Production Information
NINA-W156	Advance Information

☞ For information about the hardware, software, and current status of the available product types, see the NINA-W10, NINA-W13 and NINA-W15 data sheets [3], [2] and [4].

Contents

1 System description

1.1 Overview

The NINA-W1 series of wireless and multiradio MCU IoT is suitable for industrial markets where security is important. NINA-W1 includes the following stand-alone modules:

Model	Description
NINA-W13 series	Wireless MCU modules integrate a powerful microcontroller (MCU) and a Wi-Fi radio for wireless communication. NINA-W13x modules come with pre-flashed application software and support 802.11b/g/n in the 2.4 GHz ISM band. Host systems set up and control the modules through an AT command interface to reduce the time and complexity of including Wi-Fi connectivity into your application designs. NINA-W13x modules offer top-grade security with secure boot functionality that ensures that applications start only with the original u-blox software, u-connectXpress.
NINA-W10 series	Multiradio MCU modules integrate a powerful microcontroller (MCU) and radio for wireless communication. With open CPU architecture, NINA-W10 series modules are ideal for advanced applications that run on dual core 32-bit MCUs. The radio provides support for Wi-Fi 802.11b/g/n in the 2.4 GHz ISM band, Bluetooth BR/EDR, and Bluetooth low energy communication. Leveraging integrated cryptographic hardware accelerators, NINA-W10 series modules offer top-grade security capable of secure boot.
NINA-W15 series	NINA-W15x modules have similar performance as NINA-W10x modules, but come with pre-flashed application software. Serving as a multiradio gateway, these modules provide support for Wi-Fi 802.11b/g/n and dual-mode Bluetooth (Bluetooth BR/EDR low energy v4.2). Host systems set up and control the modules through an AT command interface to reduce the time and complexity of including Wi-Fi connectivity into your application designs. NINA-W15x series modules offer top-grade security with secure boot functionality that ensures that applications start only with the original u-blox software, u-connectXpress.

The modules are qualified for professional grade and support an extended temperature range of -40°C to +85°C.

1.2 Architecture

1.2.1 Block diagrams

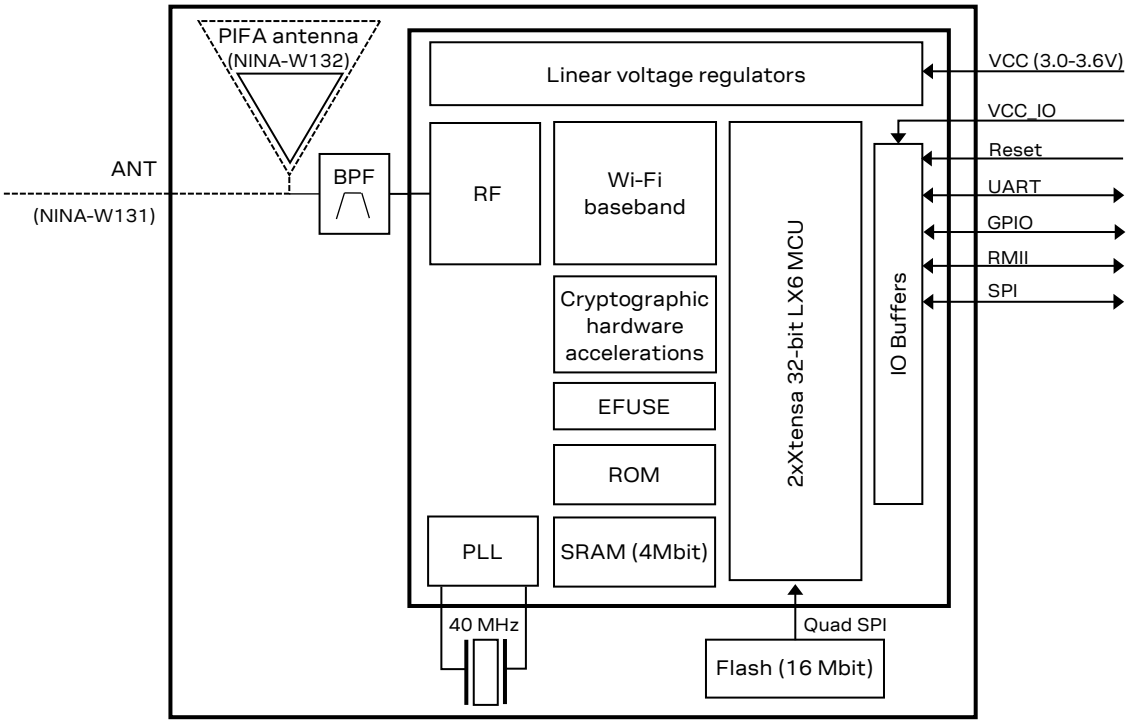
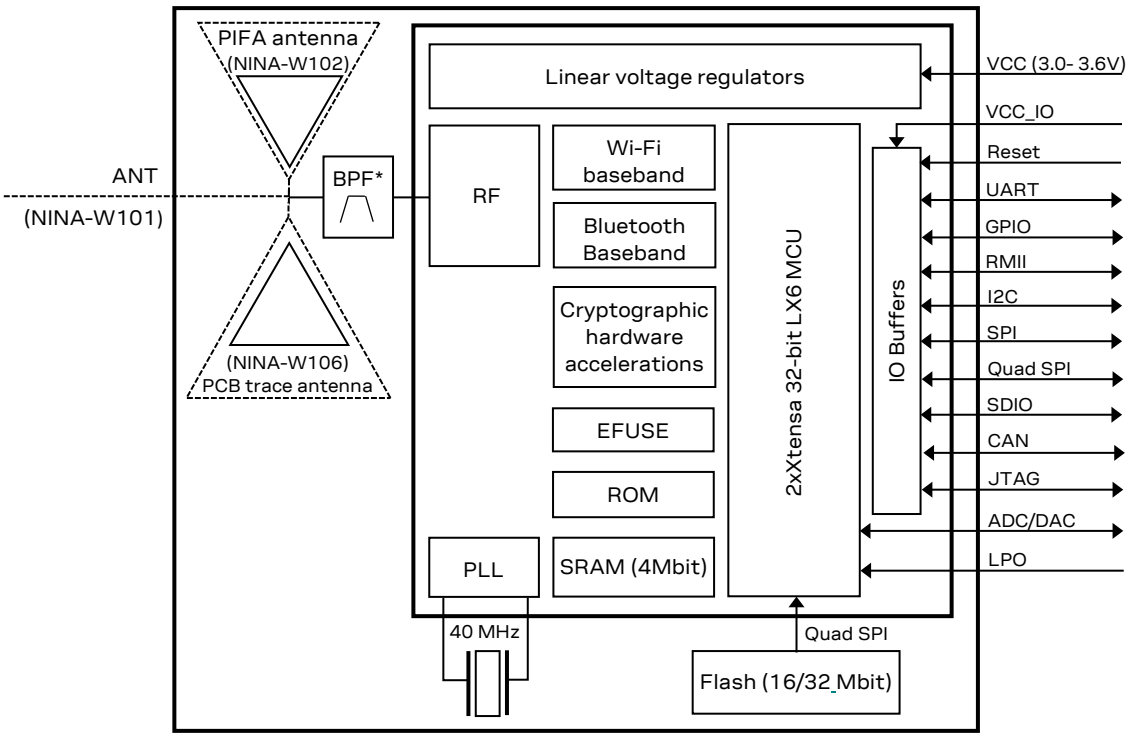


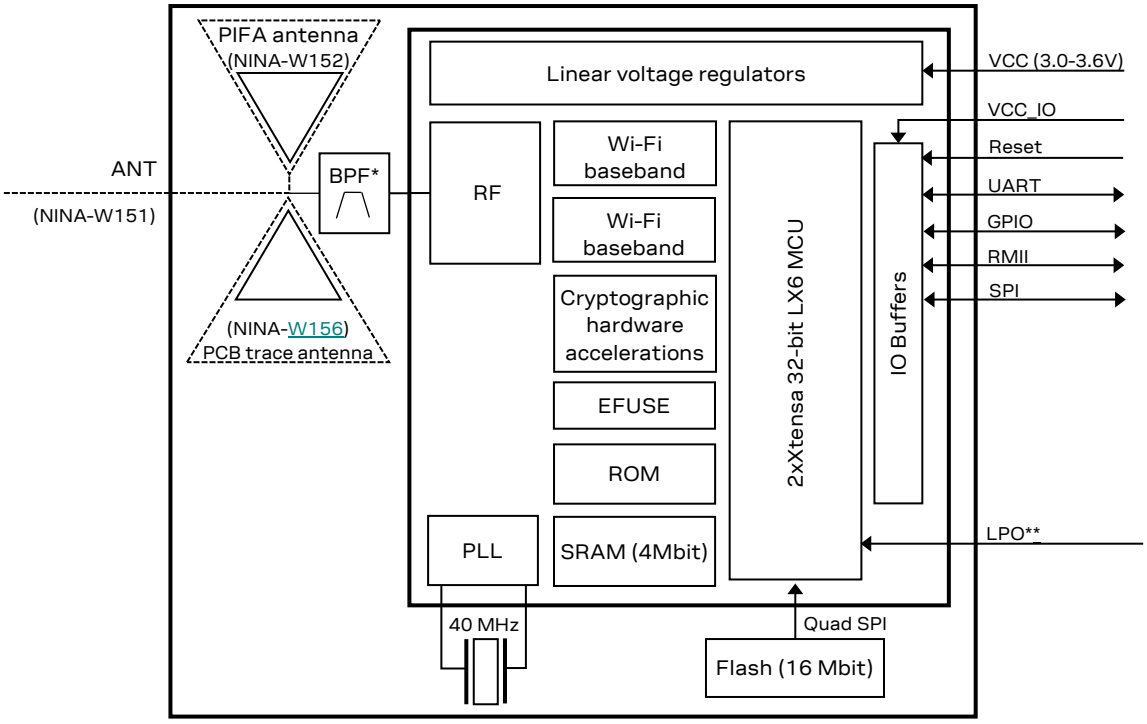
Figure 1: NINA-W13 series block diagram



* Only on NINA-W101 and NINA-W102.

** 16Mbit NINA-W101 and NINA-W102; 32Mbit NINA-W106.

Figure 2: NINA-W10 series block diagram



* Only on NINA-W152 and NINA-W152

** Only on NINA-W156. Support in u-connectXpress – pending implementation

Figure 3: NINA-W15 series block diagram

1.3 CPU

NINA-W1 series modules use a dual-core system that includes two Harvard Architecture Xtensa LX6 CPUs with maximum 240 MHz internal clock frequency. The internal memory of NINA-W1 supports:

- 448 kB ROM for booting and core functions
- 520 kB SRAM for data and instruction
- 16 or 32 Mbit FLASH memory for code storage, including hardware encryption to protect programs and data.
- 1 kbit EFUSE (non- erasable memory) for MAC addresses, module configuration, flash-encryption, and Chip-ID.

Open CPU variants (NINA-W10) also support external FLASH and SRAM memory through a Quad SPI interface.

1.4 Operating modes

1.4.1 Power modes

NINA-W1 series modules are power efficient devices capable of operating in different power saving modes and configurations. Different sections of the modules can be powered off when they are not needed, and complex wake up events can be generated from different external and internal inputs.

For details on the available power modes, see the data sheet for the corresponding module [2][3][4].

1.4.2 Low power modes with LPO

An external 32.768 kHz LPO (Low Power Oscillator) signal is required for NINA-W10 series modules to enable the lowest possible power consumption, frequency stability, and RTC accuracy in the various ESP32 sleep and hibernate modes.

☞ Support for LPO in u-connectXpress is pending implementation.

On NINA-W106 series modules, the LPO can be implemented using an external oscillator. The oscillator must be connected to the **LPO_IN** signal on **pin 5**. Also, a > 200 nF capacitor must be placed between **pin 7** and ground. The amplitude range is 0.6 V < Vpp < VCC. If the input signal is square wave, the bottom voltage should be higher than 200 mV .

☞ **Pin 7** cannot be used as GPIO when LPO is used on NINA-W106 series modules.

For more information on the LPO, see the Espressif ESP32 datasheet [12], Espressif ESP32 Technical reference manual [13], and Espressif ESP32 Hardware design guidelines [14].

☞ On NINA-W101 and NINA-W102, the functions of **pin 5** and **pin 7** are reversed.

It is possible to wake-up the module using several methods, out of which “wake-up on external GPIO” requires attention.

On NINA-W10 series modules, isolate the ESP32 GPIO **pin 12** using `rtc_gpio_isolate()` to avoid current leakage prior to the invocation of `esp_deep_sleep_start()`:

```
void cbPWR_MGR_enterDeepSleep()
{
    rtc_gpio_isolate(GPIO_NUM_12);
    esp_deep_sleep_start();
}
```

The `rtc_gpio_isolate()` function disables input, output, pullup, pulldown, and enables the hold feature for an RTC I/O pin. Use this function if any other RTC I/O pin also needs to be disconnected from ESP32-internal circuits in deep sleep and hibernation modes. Disconnecting minimizes leakage currents. The use of this function is typically necessary when an external pull-up or pull-down is used on a pin that also contains a pull-up or pull-down.

In other cases, it might be possible to manually use the internal pull-ups and pull-downs of the ESP32 using the specific enable/disable functions, followed by `rtc_gpio_hold_en()`.

```
void cbPWR_MGR_enterDeepSleep()
{
    rtc_gpio_set_direction(EXT_WAKEUP_1_GPIO, RTC_GPIO_MODE_INPUT_ONLY);
    rtc_gpio_pullup_dis(EXT_WAKEUP_1_GPIO);
    rtc_gpio_pulldown_en(EXT_WAKEUP_1_GPIO);
    rtc_gpio_hold_en(EXT_WAKEUP_1_GPIO);
    esp_deep_sleep_start();
}
```

The `rtc_gpio_hold_en()` preserves the last known value during deep sleep and hibernate modes.

See the Espressif ESP32 data sheet [12] for more information about ESP32-internal circuits and external GPIOs capable of waking up the module.

The power consumption in the various sleep modes is affected by the RTC clock source. Define the appropriate RTC clock source, used during the sleep modes, by setting the `CONFIG_ESP32_RTC_CLK_SRC` configuration option accordingly.

When using an LPO, also enable boot-time calibration by setting `CONFIG_ESP32_RTC_CLK_CAL_CYCLES` to at least 3000. The higher the number, the better accuracy, on the expense of boot time.

Frequency stability and system time accuracy is decreased when using sleep modes. To increase accuracy, use an LPO and enable both high-resolution and RTC timers by setting `CONFIG_ESP32_TIME_SYSCALL` accordingly.

If the ULP (ultra-low-power) co-processor is not required, the ULP functionality can be disabled by unsetting the `CONFIG_ESP32_ULP_COPROC_ENABLED` option.

If the LPO detection fails, increase the `CONFIG_ESP32_RTC_XTAL_CAL_RETRY` option.

If "`flash read err, 1000`" messages are printed to the console after deep sleep reset, increase the `CONFIG_ESP32_DEEP_SLEEP_WAKEUP_DELAY` value from its default 2000 µs.

See the Espressif ESP32 SDK [8] for more information on how these, and additional configuration options and API functions, affect power consumption, frequency stability, and boot-time behavior.

1.5 Supply interfaces

1.5.1 Module supply design (VCC)

NINA-W1 series modules include an integrated Linear Voltage converter that transforms the supply voltage. The output of the converter, presented at the **VCC** pin, provides a stable system voltage.

1.5.2 Digital I/O interfaces reference voltage (VCC_IO)

NINA-W1 series modules include an additional voltage supply input for setting the I/O voltage level.

A separate **VCC_IO** pin enables module integration in many applications with different voltage supply levels (1.8 V or 3.3 V for example) without level converters. NINA-W1 series modules currently support 3.3 V IO levels only.

1.5.3 VCC application circuits

The power for NINA-W1 series modules is applied through the VCC pins. These supplies are taken from either of the following sources:

- Switching Mode Power Supply (SMPS)
- Low Drop Out (LDO) regulator

An SMPS is the ideal design choice when the available primary supply source is of a higher value than the operating supply voltage of the module. This offers the best power efficiency for the application design and minimizes the amount of current drawn from the main supply source.

⚠ When taking VCC supplies from an SMPS make sure that the AC ripple voltage is kept as low as possible at the switching frequency. Design layouts should focus on minimizing the impact of any high-frequency ringing.

Use an LDO linear regulator for primary VCC supplies that have a relatively low voltage. As LDO linear regulators dissipate a considerable amount of energy, LDOs are not recommended for the step down of high voltages.

DC/DC efficiency should be regarded as a trade-off between the active and idle duty cycles of an application. Although some DC/DC devices achieve high efficiency at light loads, these efficiencies typically degrade as soon as the idle current drops below a few milliamps. This can have a negative impact on the life of the battery.

If decoupling capacitors are needed on the supply rails, it is best practice to position these as close as possible to the NINA-W1 series module. The power routing of some host system designs makes decoupling capacitance unnecessary.

For electrical specifications, refer to the appropriate NINA-W1 series data sheet [2] [3] [4].

1.6 System function interfaces

1.6.1 Boot strapping pins

There are several boot configuration pins available on the module that must be set correctly during boot, or the module may not boot properly. Table 1 shows the condition of the bootstrap signals that determine the behavior of the module during the system startup.

☞ Boot strap pins are configured to the default state internally on the module and must NOT be configured externally, unless otherwise stated.

Pin	State during boot	Default	Behavior	Description
27	0		ESP boot mode (factory boot)	ESP Factory boot Mode/RMII clock line.
	1	Pull-up	Normal Boot from internal Flash	
32	0		Silent	Printout on UART0 TXD during boot
	1	Pull-up	UART0 TXD Toggling	
36	0		VDD_SDIO=3.3V (Not allowed)	Internal flash voltage
	1	10 kΩ pull-up	VDD_SDIO=1.8V (VDD_SDIO should always be at 1.8 V)	

Table 1: NINA-B2 series boot strapping pins

☞ Additional requirements apply to pin **27**, depending on the intended use-case for the module:
- On NINA-W13/W15 modules, pin **27** must be in default state during the boot.
- Care must be taken if an RMII interface is to be included in the application design. As pin **27** connect to the RMII, it is important that the pin is in the correct state during the module boot and before the RMII interface turns on. For further connection information, see section 1.7.2.1.
- On NINA-W10 modules, pin **27** is used to enter the ESP bootloader. Consequently, this pin must be exposed on a pin header (or similar) to flash the module.

☞ During boot, pin **32** controls if additional system information should be transmitted on the UART interface during startup. After the system has booted it is reconfigured to **SPI_CS,** the SPI chip select signal.

☞ During boot, pin **36** controls the voltage level of the internal flash during startup. After the system has booted it is reconfigured to **SPI_MISO**, the SPI slave data output signal. It must NOT be pulled down by an external MCU or circuitry.

For the timing and algorithm for the detection of the SPI and RMII interfaces, also see the “Data and command interfaces” section in the NINA-W13 and NINA-W15 data sheets [2], [4].

1.7 Data interfaces

1.7.1 Universal asynchronous serial interface (UART)

For data communication and firmware upgrade purposes, NINA-W1 series modules support an interface comprised of three UARTs. Each UART supports the following signals:

- Data lines (**RXD** as input, **TXD** as output)
- Hardware flow control lines (**CTS** as input, **RTS** as output)
- **DSR** and **DTS** set and indicate the system modes

You can use the UARTs in 4-wire mode with hardware flow control, or in 2-wire mode with **TXD** and **RXD** only. In 2-wire mode, **CTS** must be connected to the GND on the NINA-W1 module.

☞ 2-wire mode is not recommended, because it is prone to buffer overruns.

The UART interface is also be used for firmware upgrade. See the Software section for more information.

The u-connectXpress software adds the **DSR** and **DTR** pins to the UART interface. Although these pins are not used as they were originally intended, these control the state of NINA modules.

Depending on the configuration, **DSR** can be used to:

- Enter command mode
- Disconnect and/or toggle connectable status
- Enable/disable the UART interface
- Enter/leave STOP mode

The functionality of the **DSR** and **DTR** pins are configured by AT commands. For further information about these commands, see the u-connectXpress AT commands manual [1].

Typical UART interface characteristics are described in data sheet references [2], [3] and [4] .

Interface	Default configuration
UART interface	115200 baud, 8 data bits, no parity, 1 stop bit, and hardware flow control

Table 2: UART port default settings

It is recommended that the UART is either connected to a header for firmware upgrade or made available for test points.

The IO level of the UART follows **VCC_IO**.

1.7.2 Ethernet (RMII+SMI)

⚠ NINA-W13 only supports Reduced Media-independent Interface (RMII) from software version 2.0.0 onwards.

NINA-W1 series modules include a full RMII for Ethernet MAC to PHY communication over the Station Management Interface (SMI). RMII and SMI use nine signals in total. The RMII and SMI interfaces require an external 50 MHz clock source either from a compatible PHY chip or from an external oscillator.

The two-wire SMI is used to configure the PHY chip. It uses a clock line and a data line to setup the internal registers on PHY chip.

The pin multiplexing of the RMII interface imposes limitations in the functionality of NINA-W13/W15 series module when using the interface. The following functions are turned off when RMII communication is initiated:

- Red, Green and Blue LEDs are disabled
- UART is run without flow control as **CTS** and **RTS** functionality is disabled. In this case, **CTS** must not be connected to ground.
- **DSR** and **DTR** functionality is disabled

The following resistors must be added to enable RMII support:

- 1 kΩ pull up to **RMII_MDIO** pin
- 4.7 kΩ pull up to **RMII_CRSDV** pin
- 10 Ω series resistors for all RMII/SMI pins

1.7.2.1 Startup precautions

To ensure that the boot mode is not entered inadvertently, the **RMII_CLK** input (**GPIO27**) is multiplexed with the ESP boot pin and must be held high 1.2 ms after the reset signal is released.

Using a pull-up on **GPIO27** during the critical period after reset, EVK-NINA-W1 uses two buffers and a low pass filter to override the RMII clock from the PHY. This delays the clock so that it starts a short time after the module is released from reset.

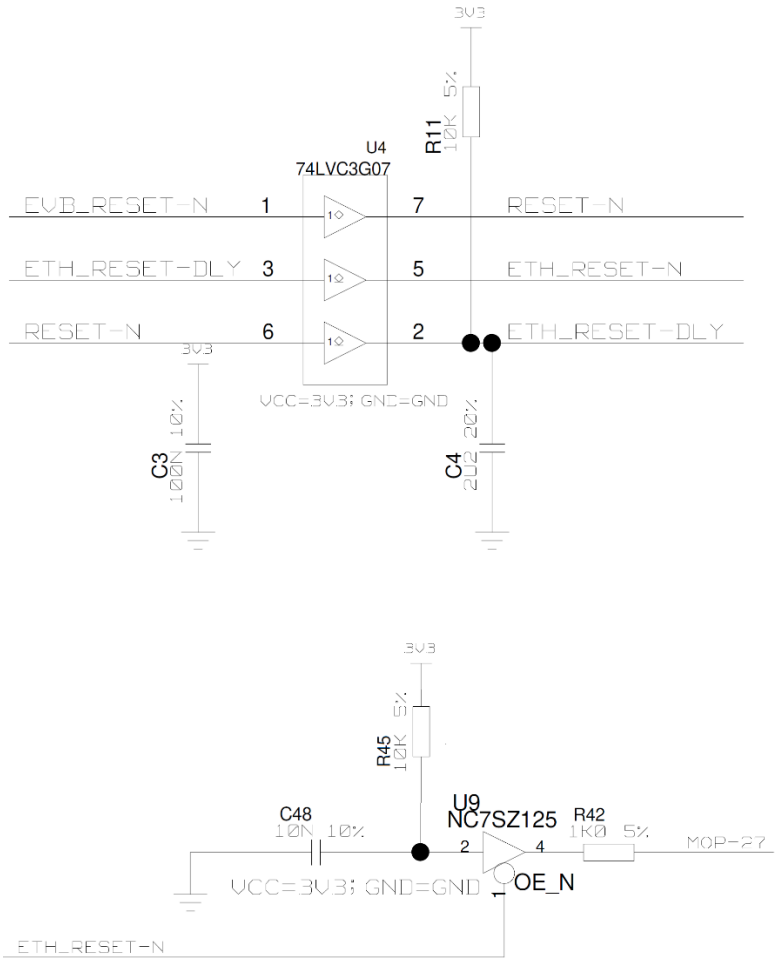


Figure 4: EVK-NINA-W1 RMII clock delay circuit

u-connectXpress software senses the **RMII_CLK** input (**GPIO27**) at startup. If an RMII clock is discovered, then Ethernet communication is initiated.

During startup of NINA-W1 series modules the RMII clock must be started within 100 us, but not before an initial delay of 1.2 ms.

1.7.2.2 MAC to PHY connection

When connecting NINA-W1 series modules to an external PHY circuit, both the RMII and SMI interfaces must be connected. The default PHY address (0x1) must be configured on the PHY side. Follow the recommendations of your chosen PHY chip supplier for implementation details.

An example of a PHY implementation is shown in Figure 5. PHY KSZ8081 is recommended and is used on the EVK-NINA-W1.

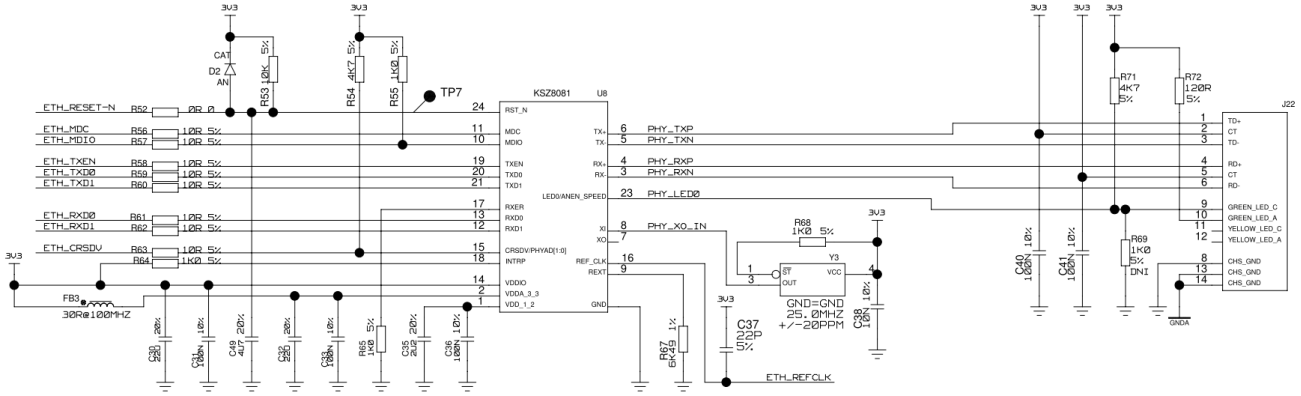


Figure 5: EVK-NINA-W1 Ethernet PHY implementation

1.7.2.3 MAC to MAC connection

When connecting NINA-W1 series modules using a direct MAC to MAC connection, the SMI interface can be left unconnected. Depending on the routing of the RMII interface on the host PCB, termination resistors can also be needed.

An external 50 MHz oscillator is needed while running a MAC-to-MAC connection.

1.7.3 Serial peripheral interface (SPI)

⚠ NINA-W13 and NINA-W15 modules support SPI from software version 3.0.0 onwards.

In addition to UART support, NINA-W13 and NINA-W15 modules also include a Serial Peripheral Interface (SPI) for data communication. The module acts as an SPI slave.

The following SPI signals are available:

- Chip select as input (**SPI_CS**)
- Data lines (**SPI_MOSI** as input, **SPI_MISO** as output)
- Clock (**SPI_SCLK** as input)
- Optional hardware flow control lines (**SPI_NORX** and **SPI_DRDY** as output)

For details on SPI operation, see u-connectXpress SPI peripheral protocol specification, reference [10].

1.8 Antenna interfaces

Antenna interfaces are different for each module variant in the NINA-W1 series.

1.8.1 Antenna pin – NINA-W1x1

NINA-W1x1 modules are equipped with an RF pin. The pin has a nominal characteristic impedance of 50 Ω and must be connected to the antenna through a 50 Ω transmission line. This allows reception of radio frequency (RF) signals in the 2.4 GHz frequency band.

Choose an antenna with optimal radiating characteristics for the best electrical performance and overall module functionality. An internal antenna, integrated on the application board or an external antenna connected to the application board through a proper 50 Ω connector, can be used.

When using an external antenna, the PCB-to-RF-cable transition must be implemented using either a suitable 50 Ω connector, or an RF-signal solder pad (including GND) that is optimized for 50 Ω characteristic impedance.

1.8.1.1 Antenna matching

The antenna return loss should be as low as possible across the entire band when the system is operational to provide optimal performance. The enclosure, shields, other components, and surrounding environment impacts the return loss that is seen at the antenna port. Matching components are often required to retune the antenna to 50 Ω characteristic impedance.

It is difficult to predict the actual matching values for the antenna in the final form factor. Therefore, it is good practice to have a placeholder in the circuit with a "pi" network, with two shunt components and a series component in the middle. This allows maximum flexibility while tuning the matching to the antenna feed.

1.8.1.2 Approved antenna designs

NINA-W1 modules come with a pre-certified design that can be used to save costs and time during the certification process. To take full advantage of this service, you must implement the antenna layout in accordance with u-blox reference designs. Reference designs are available on request from u-blox.

The designer integrating a u-blox reference design into an end-product is solely responsible for any unintentional emission levels produced by the end product.

The module may be integrated with other antennas. In which case, the OEM installer must certify the design with respective regulatory agencies.

1.8.2 NINA-W1x2 and W1x6 integrated antennas

To simplify integration, NINA-W1x2 and W1x6 modules are equipped with an integrated antenna. An integrated antenna design means there is no need for an RF trace design on the host PCB. This means less effort is required in the test lab.

NINA-W1x2 modules use an internal metal sheet PIFA antenna, while the NINA-W1x6 modules are equipped with a PCB trace antenna that is based on technology licensed from Proant AB.

1.9 Reserved pins (RSVD)

Do not connect the reserved (**RSVD**) pin. Reserved pins are allocated for future interfaces and functionality.

1.10 GND pins

Good electrical connection of module GND pins, using solid ground layer of the host application board, is required for correct RF performance. Firm connections provide a thermal heat sink for the module and significantly reduce EMC issues.

2 Software

2.1 NINA-W13 and NINA-W15 u-connectXpress software

NINA-W13/W15 stand-alone modules are delivered with embedded u-connectXpress software.

Using industry-standard AT commands, this is the software that manages the combination of Bluetooth, Bluetooth Low Energy and Wi-Fi connectivity supported in NINA-W13 and NINA-W15 standalone modules, specifically:

- Wi-Fi (NINA-W13 and NINA-W15)
- Bluetooth (NINA-W15)
- Bluetooth Low Energy (NINA-W15)

For information about the features, capabilities and use of u-connectXpress software, see the u-connectXpress AT commands manual [1] and u-connectXpress user guide [6].

Typical examples of the applications and use cases supported by NINA-W13 and NINA-W15 series modules include:

- Gateway connection of Bluetooth low energy sensors to the cloud over Wi-Fi or Ethernet
- Bridge communication over serial, Wi-Fi, PPP, or Ethernet interfaces
- Wi-Fi hotspot connection using Local Area Network or Tethering
- Device configuration using Bluetooth or Wi-Fi connected smartphones
- Secure cloud connection using TLS and MQTT protocols

Figure 6 shows the structure of the embedded u-connectXpress software delivered in NINA-W13 and NINA-W15 standalone modules.

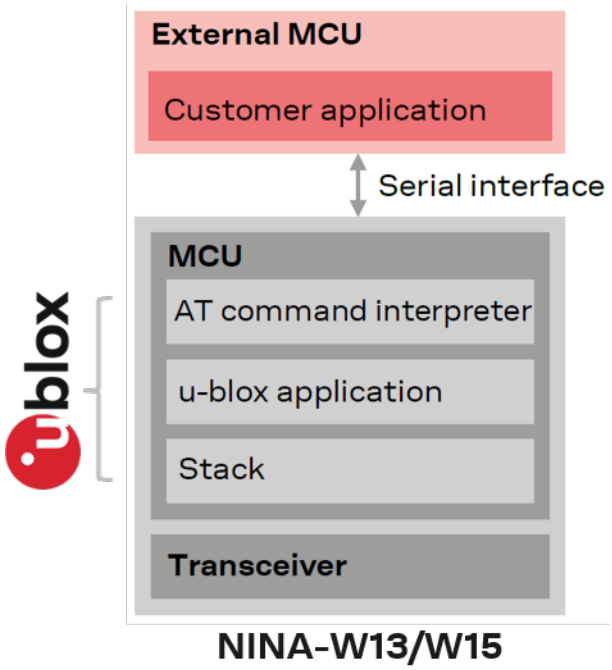


Figure 6: NINA-W13/W15u-connectXpress software structure

2.2 s-center evaluation software

u-blox s-center client software provides a convenient tool with which to configure u-blox standalone modules. It runs on PCs running Windows XP onwards (x86 and x64) with Net Framework 4.5 or later and is available for download from www.u-blox.com. For further information about how to use this tool, see the s-center user guide [8].

2.3 SDK for open-CPU modules

As NINA-W10 open-CPU modules are delivered without flashed software, you develop your application design using the utilities and device-level APIs supported by the module chipset supplier. The ESP-IDF Software Development Kit is available from the Expressif website. It bundles the Wi-Fi stack and the broad range of drivers and libraries necessary for building your development environment. See also section 2.7.

Figure 7 shows the architecture of NINA-W10 open-CPU software in relation to the MCU, transceiver and ESP-IDF SDK.

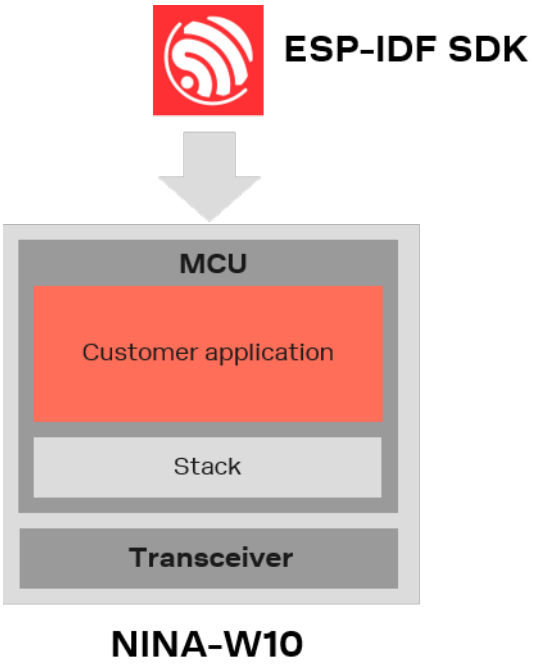


Figure 7: NINA-W10 open CPU software

2.4 Updating NINA-W13 and NINA-W15

NINA-W13 and NINA-W15 u-connectXpress software can be flashed and updated directly from the host or s-center. The flash procedure uses the XMODEM protocol.

The following pins should be made available as either headers or test points to flash the module:

- UART (**RXD**, **TXD**, **CTS**, **RTS**)
- Bootstrap pins **25** and **27**
- **RESET_N**
- **SWITCH_1** and **SWITCH_2**

2.5 Updating u-connectXpress software with s-center

The u-connectXpress software, flashed into NINA-W13/W15 modules prior to delivery, is used to validate the hardware, bootloader, and the binary image. The u-connectXpress software runs only on validated hardware.

Updates of the u-connectXpress software is available for download from www.u-blox.com. The software is delivered in a zip container file, for example, `NINA-W1xX_SW1.0.0.zip`.

To upload the latest u-connectXpress software to the module:

1. Download and unpack the zip container, `NINA-W1xX_SW1.0.0.zip`, to your Windows workstation.
2. Open the s-center client software.
3. From the client, navigate to the `.json` file in the unpacked u-connect archive and select **Update**. The s-center handles the download using information contained in the `*.json` file without any further interaction is needed from the user. See also Figure 8.

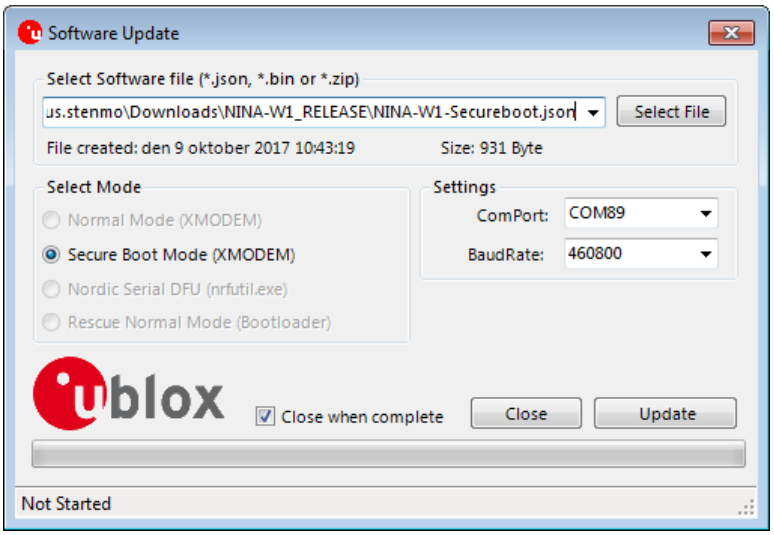


Figure 8: Software Update using s-center

Secure boot functionality is supported in u-connect v4.7 and above.

u-connectXpress cannot be installed on NINA-W10. For information on how to install applications on NINA-W10, see section 2.7 and 2.8.

2.6 Updating u-connectXpress software from host

To manually start the download using a software without using s-center. For example, when downloading from a host microcontroller use the following AT commands to start updating the NINA-W13/W15 u-connectXpress:

```
AT+UFWUPD=<mode>,<baud>,<image id>,<image size>,<base64 encoded signature>,<image
name>,<flags>
```

Sample parameters that can be used while doing the flash update is provided below:

```
AT+UFWUPD=0,115200,0,651840,jzlRIkg37ir/pVpDKVrPot2ZdsaNvUtSYP2pDAUVJc7iQI9yzIo8V
Fv8C1olP/9I4UJ4WmgC5oRay4AC0V8jRJSFFX/wop6x/sBJGOeDEu7yC/s0+Oj7CLs4TzNbiRqK0zLwKR
iHohgVyzWqhwKFpmcxcDXphjkCTIvpffY8TwDLzkowuuD59R+sQCueJtBHBg9KDB3TOs8bsXLaVtT2x1r
LfMg8/pb+BPQEK9NcNB4hbp693ATivYE3cmxzWykIjEje819SIRGhHFt0wAsqh7WFgSJYNgDi5cLdOYz+
r1+j7+l4RqrMl/A/QYyWS9z0Q15QcJ3GlAJlXYa5v/ISjA==,nina-w1-debug,rwx
```

When a "C" character is received from NINA-W13/W15, the XMODEM download is ready to begin from the host.

For more information about the parameters, see the software update command `+UFWUPD` in u-connectXpress AT commands manual [1], u-connectXpress bootloader protocol specification [11], and u-connectXpress user guide [6].

2.7 Developing and flashing NINA-W10 open-CPU software

In NINA-W10 modules, the following pins should be made accessible through a header or similar connector:

- Mandatory:
  - **SWD**
  - ESP_BOOT (**GPIO27**)
- Additionally recommended:
  - **RESET_N**

As the u-connectXpress software embedded in NINA-W13/15 series modules is not available for use with the NINA-W10 open CPU series, you use Espressif SDK utilities and device-level APIs to develop your application hardware.

For the latest Espressif SDK documentation, see reference [8]. This URL provides information on how to set up the software environment using the hardware based on the Espressif ESP32, such as NINA-W10. This resource also describes how to use the latest ESP-IDF (Espressif IoT Development Framework) – which might have been changed since the publication of this document.

The following must be setup in order to compile, flash, and execute a program on NINA-W10:

- Setup Toolchain
  - Windows, Mac, and Linux are supported
- Get ESP-IDF
  - Download the GIT repository provided by Espressif
- Setup Path to ESP-IDF
  - The toolchain program can access the `ESP-IDF` using the `IDF_PATH` environment variable
- Build and Flash
  - Start a Project, Connect, Configure, Build and Flash a program

More information about this is available at - http://esp-idf.readthedocs.io/en/latest/index.html

2.7.1 Setup the ESP-IDF v3 toolchain

☞ ESP-IDF v3 toolchain can be used on NINA-W101/NINA-W102 but has not been verified on NINA-W106. On NINA-W106, use the ESP-IDF v4 toolchain.

To start development with ESP32, it is recommended to use a prebuilt toolchain. Currently, Windows, Mac, and Linux is supported. The example in this document will use a Toolchain for running Windows, that is, a bash shell window. The toolchain contains all programs and compiler to build an application.

The toolchain for Windows can be downloaded from
https://dl.espressif.com/dl/esp32_win32_msys2_environment_and_toolchain-20170918.zip

Unzip the file to `c:\ msys32`. This path is assumed in the following examples, but it can be located in another folder as well. The file size is around 500 MB.

Start the bash shell using the "`mingw32.exe`" ("`mingw64.exe`" is currently not supported).

☞ If you encounter any issues, use the "`autorebase.bat`" and the "`msys2_shell.cmd`" shortcuts. This will reset the path variable with a Cygwin installation on some computers, which can have problems with the path to the compiler or the python tool.

2.7.2 Get ESP-IDF v3

☞ ESP-IDF v3 can be used on NINA-W101/NINA-W102 but has not been verified on NINA-W106. On NINA-W106, use the ESP-IDF v4.

The source files for Espressif ESP-IDF repository is located on github at https://github.com/espressif/esp-idf.

To download the files, open the "`mingw32.exe`", navigate to the directory where you want to have the ESP-IDF (like c:\git), and clone it using "git clone" command.

☞ Use the "`--recursive`" parameter

In this example, the esp-idf repository will be created in the `c:\git` folder.

```
git clone --recursive https://github.com/espressif/esp-idf.git
```

To checkout a specific tag such as v3.1, use the following command as shown in the example below:

```
git clone https://github.com/espressif/esp-idf.git esp-idf-v3.1
cd esp-idf-v3.1/
git checkout v3.1
git submodule update --init --recursive
```

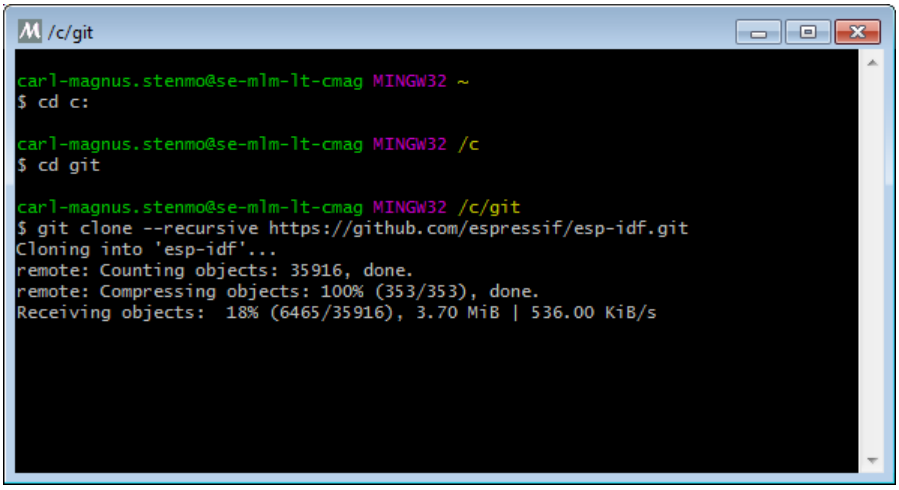


Figure 9: Example of the git clone of ESP-IDF

Go to the new folder by typing "`cd esp-idf`" and then type "`ls`" to show the folder content.

```
cd esp-idf
ls
```

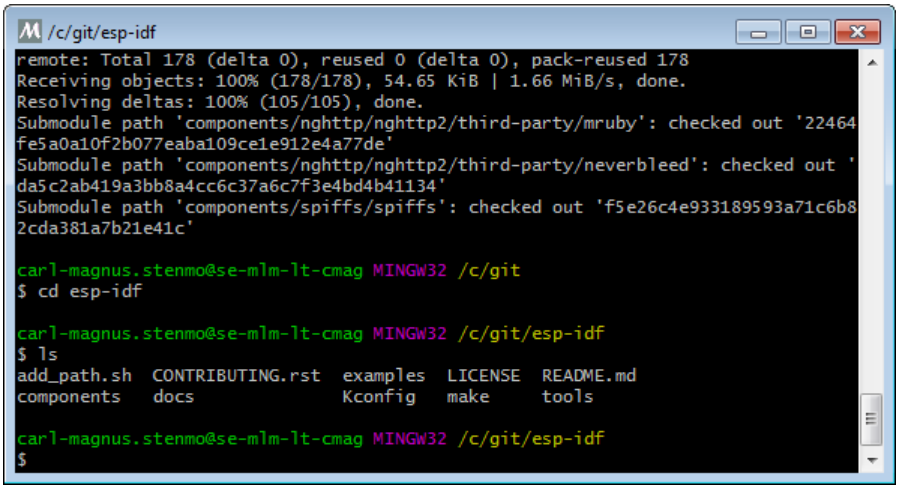


Figure 10: Verification of all the downloaded files

2.7.3 Setup path to ESP-IDF

The toolchain for the ESP-IDF uses the `IDF_PATH` environment variable. This variable must be set up for building the projects.

```
export IDF_PATH="C:/git/esp-idf"
```

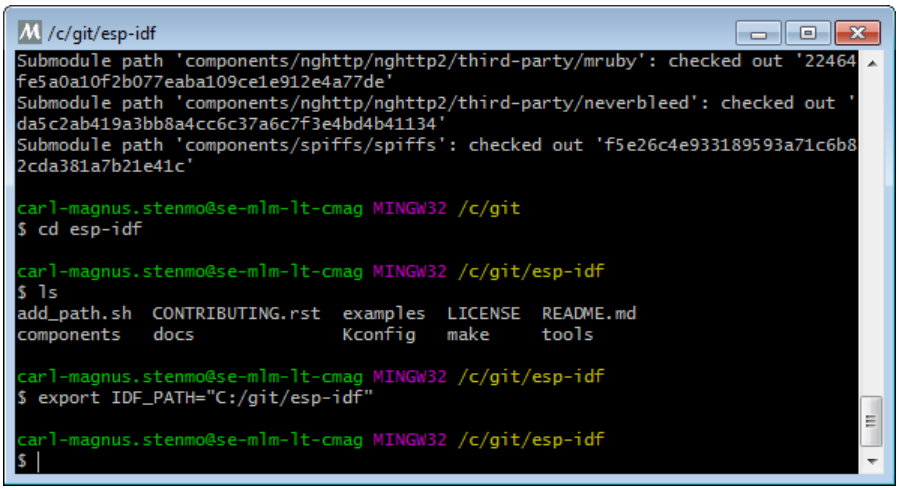


Figure 11: Setting up the PATH variable

2.7.4 Building and flashing ESP-IDF v3

The environment is now ready to build and flash a project. In this case, we use “hello world” as a sample project.

This project will print out “Hello World” ten times on the UART and then reboot.

To build this sample project, go to the “hello world” folder using the following command:

```
cd examples/get-started/hello_world
```

Plug in NINA-W10 to the PC and note down the com port number with which it is connected. In this example, the com port number is assumed to be “COM10”.

Now enter "`make menuconfig`" to open the ESP-IDF configuration window. You can select and modify a lot of configuration options about the environment using this tool; in this example, only the com port that is used to flash NINA-W10 is modified.

```
make menuconfig
```

Use the arrow keys to navigate and select the "Serial flasher config" as shown in Figure 12

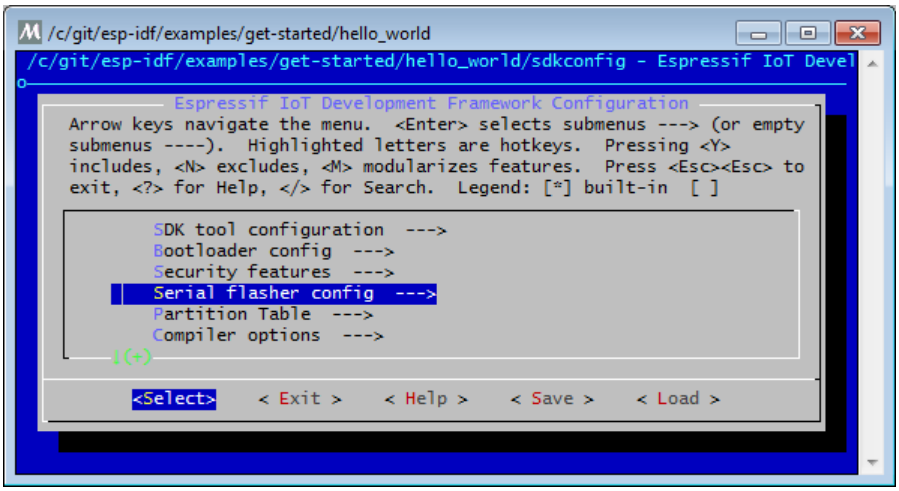


Figure 12: Screenshot that shows selection of "Serial flasher config"

Enter the com port name; in this case, enter "COM10", and click OK.

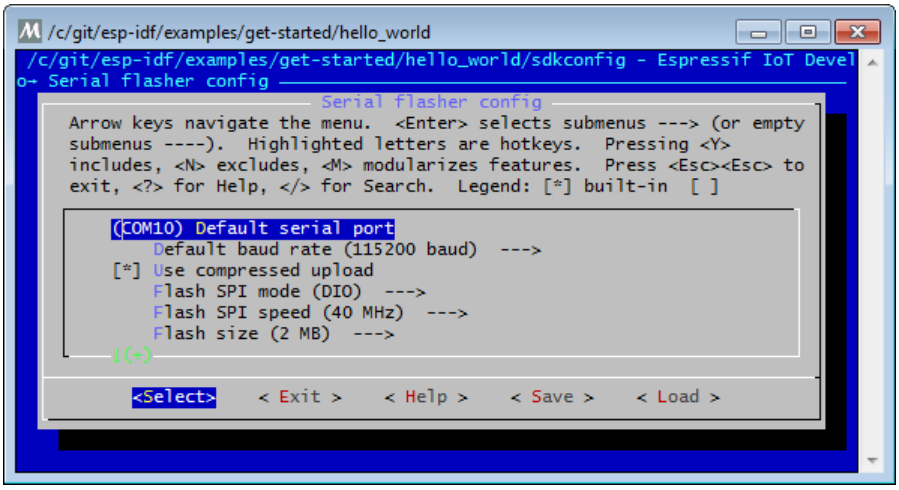


Figure 13: Screenshot that shows selection of the sample com port number ("COM10")

Save the `sdkconfig` by entering a filename to which this configuration should be saved, as shown in Figure 14.

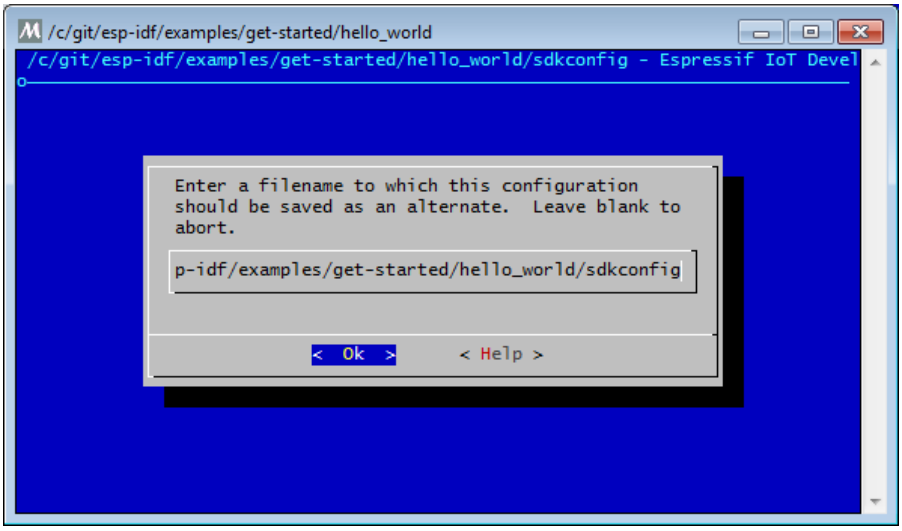


Figure 14: Screenshot after entering the filename for the sdkconfig

☞ Make sure your configuration is saved first and then enter Exit to exit the console.

Now the project is ready to build, but before building and flashing, NINA-W10 should be prepared to accept the downloaded file. This is done by holding the BOOT button while resetting or powering on the board.

Then, enter "`make flash`" to build and flash the NINA-W10 as shown below:

```
make flash
```

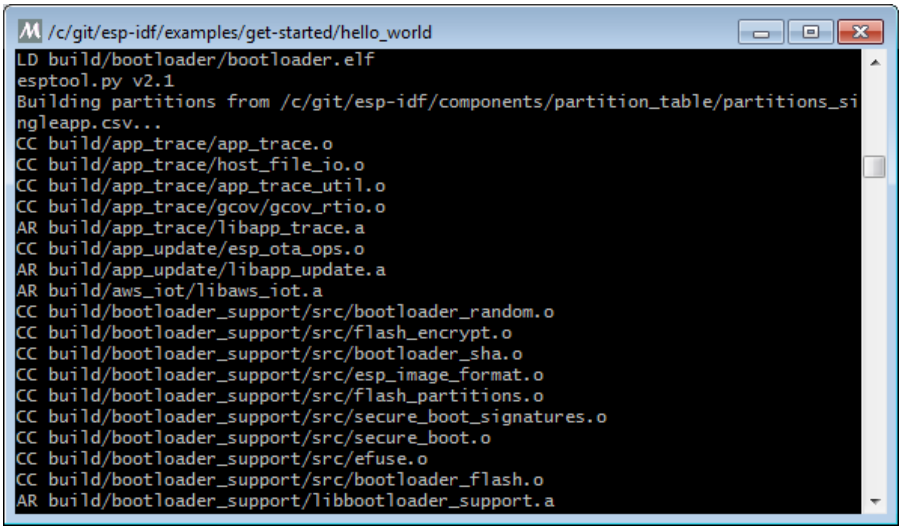


Figure 15: Compiling of the example application

Now, reset the NINA-W10 by clicking the RESET button.

Then, enter "`make monitor`" to open a serial port monitor program to the NINA-W10.

```
make monitor
```

You could also enter "`make flash monitor`" to build and flash and then start the serial port monitor program using only one command.

```
make flash monitor
```

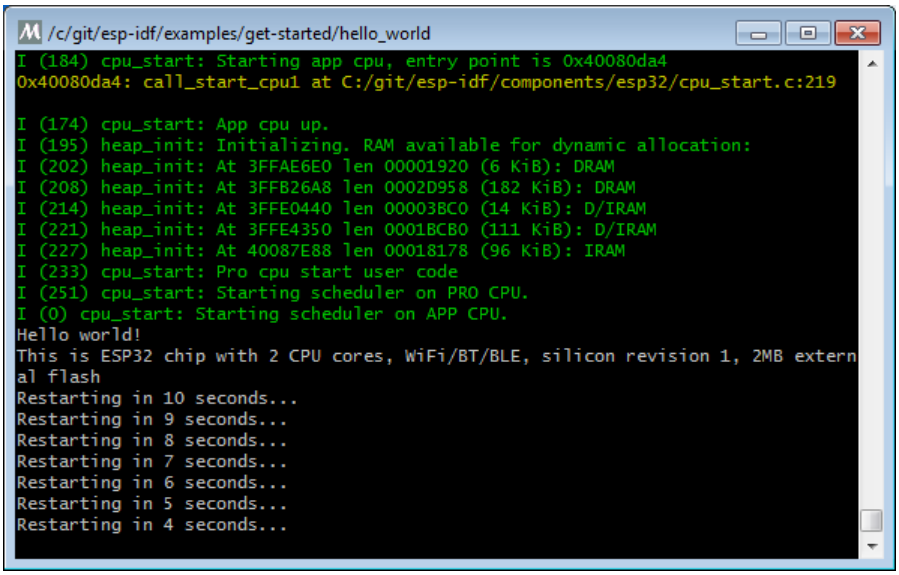


Figure 16: Hello world example as displayed on the monitor

2.7.5 Using ESP-IDF v4

☞ ESP-IDF v4 is mandatory for NINA-W106.

To use ESP-IDF v4, use the appropriate toolchain instructions for your development environment:

- Windows
- Linux
- Pip, homebrew and other macros

After installing the appropriate toolchain, install ESP-IDF using the Get ESP-IDF instructions on the Expressive web site. The toolchain for the ESP-IDF uses the `IDF_PATH` environment variable, which must be set up to build the toolchain projects.

☞ The source files for Espressif ESP-IDF repository is located on github at https://github.com/espressif/esp-idf.

Building and flashing the examples in the ESP-IDF v4 is basically done in the same way as it is for ESP-IDF v3, but rather than using `make`, the `idf.py` script is invoked instead. Generally, the same command-line parameters apply with the following caveats:

☞ NINA-W101/NINA-W102: When running the command `idf.py make menuconfig` set the configuration flag `CONFIG_SPI_FLASH_USE_LEGACY_IMPL` flag to `Y`. The application fails to start unless this flag is set.

☞ NINA-W106: When running command idf.py make menuconfig set the `CONFIG_BOOTLOADER_VDDSDIO_BOOST_1_9V` and `CONFIG_SPI_FLASH_SUPPORT_ISSI_CHIP` configuration flags to Y.

☞ NINA-W106 modules with prototype status: On NINA-W106 prototype modules, it may be necessary to add the `--no-stub` parameter to the `esptool.py` command when flashing the software. This parameter makes a manual verification of the software using a second invocation of `esptool.py` in case the flashing and verification procedure fails.

2.7.6 Automatic bootloader on NINA-W10 EVK

The "`esptool.py`" flash tool supports automatic entry to the bootloader on the NINA-W10 EVK without pressing the BOOT button and RESET the module. To use this functionality, you need to connect the following pins:

- **RESET** to IO19 (**CTS**)
- **IO0** (IO zero) to IO26 (**DSR**)

The jumpers **CTS** (J14-8) and **DSR** (J14-7) should also be removed so that they do not interfere.

☞ It is not possible to use the Hardware Flow control or the **DSR** signals on the UART while using this setup.

More information about `esptool` is available at https://github.com/espressif/esptool

2.8 Arduino support for NINA-W10

It is possible to use Arduino electronics platform on the NINA-W10. The Arduino platform and open-source community provides the possibility to access a lot of third-party hardware such as displays and sensors.

2.8.1 Downloading the Arduino IDE

Windows, Mac, and Linux environment are supported. The example below uses the Windows environment. Download the Arduino IDE using the URL https://www.arduino.cc/en/Main/Software.

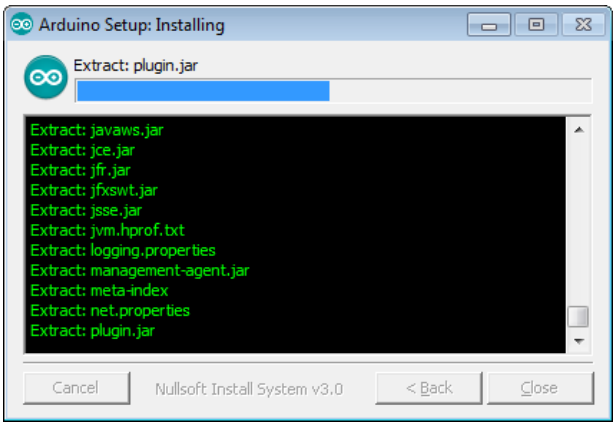


Figure 17: Screenshot during installation of the Arduino IDE

Click **Install** button in the dialog box that pops up during installation as shown Figure 18:

Figure 18: Install device software dialog

Open the Arduino IDE - "`C:\Program Files (x86)\Arduino\arduino.exe`" and then close the program again. Do this to ensure that the folder is created correctly before downloading the Arduino files as mentioned in the next step.

The Arduino IDE user folder is typically located in "`C:\Users\user_name\Documents\Arduino`"

2.8.2 Downloading from the GIT repository

Download from the URL - https://github.com/espressif/arduino-esp32.git

The files should be placed in "`C:\Users\user_name\Documents\Arduino\hardware\espressif\esp32`"

Open the "`mingw32.exe`" located in `c:\msys32`.

The Arduino user folder is normally stored at "`C:\Users\user_name\Documents\Arduino`"

Check if the hardware folder exists. If not, create the same by entering the following command:

```
mkdir hardware
cd hardware
```

Check if the espressif folder exists; if not, create the same by entering the following command:

```
mkdir espressif
cd espressif
```

Now clone the repository to the folder `esp32` folder.

```
git clone --recursive https://github.com/espressif/arduino-esp32.git esp32
```

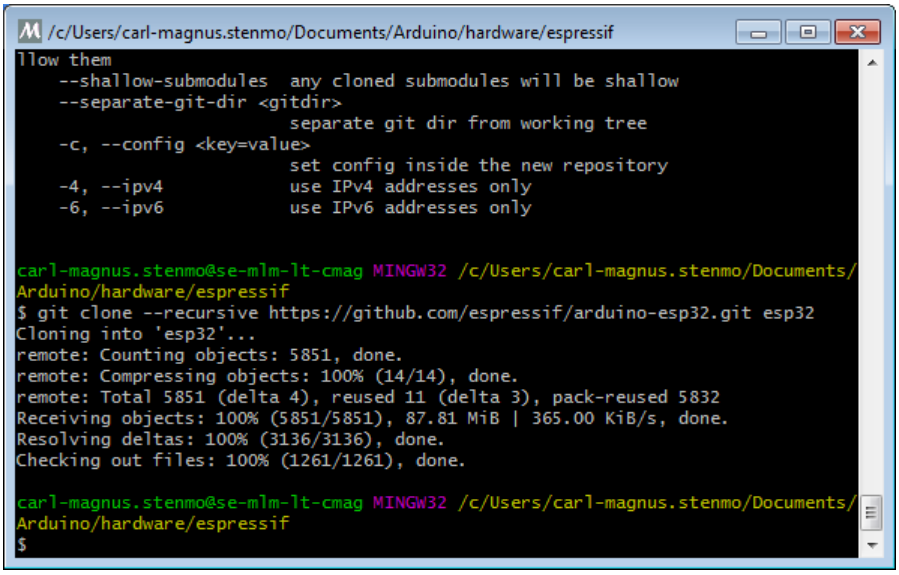


Figure 19: Cloning the Arduino Esp32 repository

2.8.3 Downloading the toolchain

Go to the folder - "`C:\Users\user_name\Documents\Arduino\hardware\espressif\esp32\tools`" to execute the program – "`get.exe`".

Double click on the "`get.exe`" to start the download. This will download the toolchain that is needed to build and flash the project. All the files are extracted on successful download.

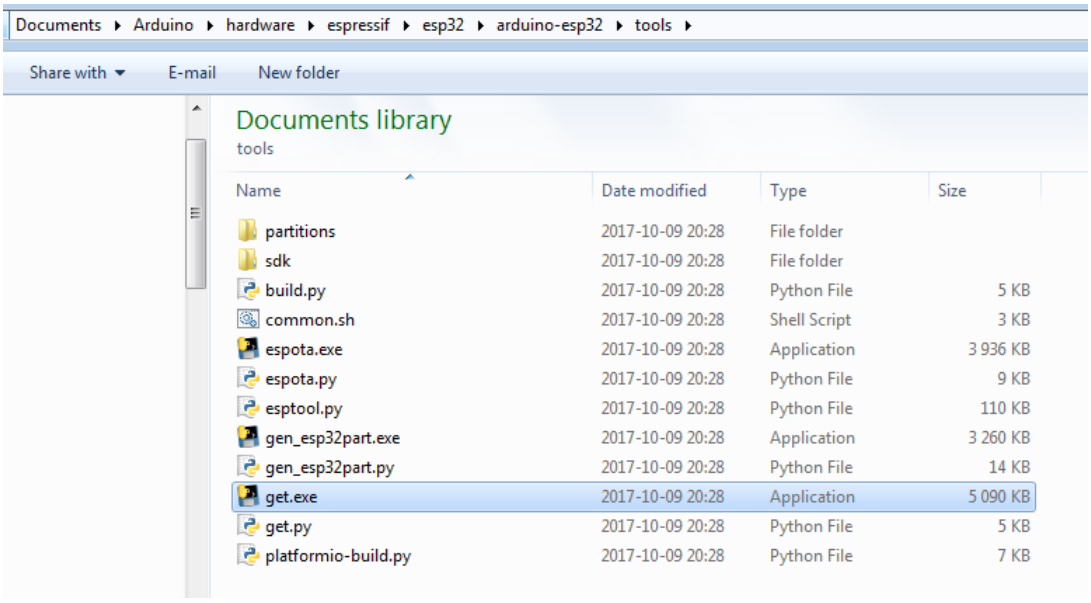


Figure 20: Screenshot after selecting "get.exe"

☞ Normally, it takes around 15-30 minutes to download this program.

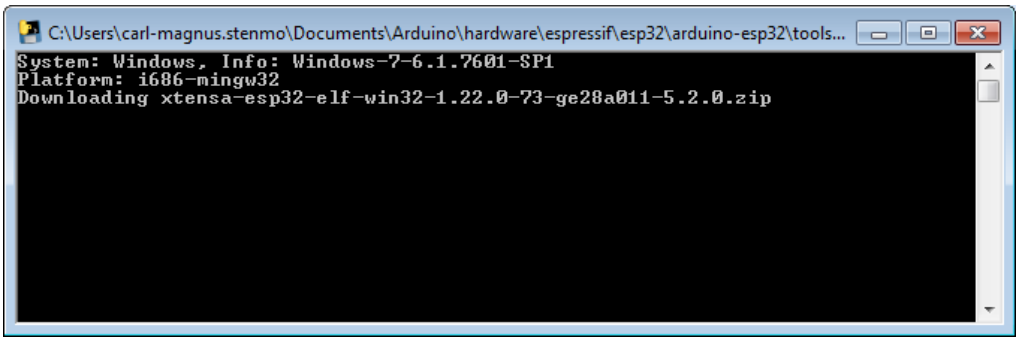


Figure 21: Sample screenshot during download

Open the Arduino application again from the following location - `"C:\Program Files (x86)\Arduino\arduino.exe"`

In the **Tools -> Board** menu, select “ESP32 Dev Module” and then select the following;

- Flash Mode: “DIO”
- Flash Frequency: “40 MHz”
- Flash Size: “2 MB (16 Mb)”
- Upload Speed “921600”
- Core Debug Level “Debug” (optional)

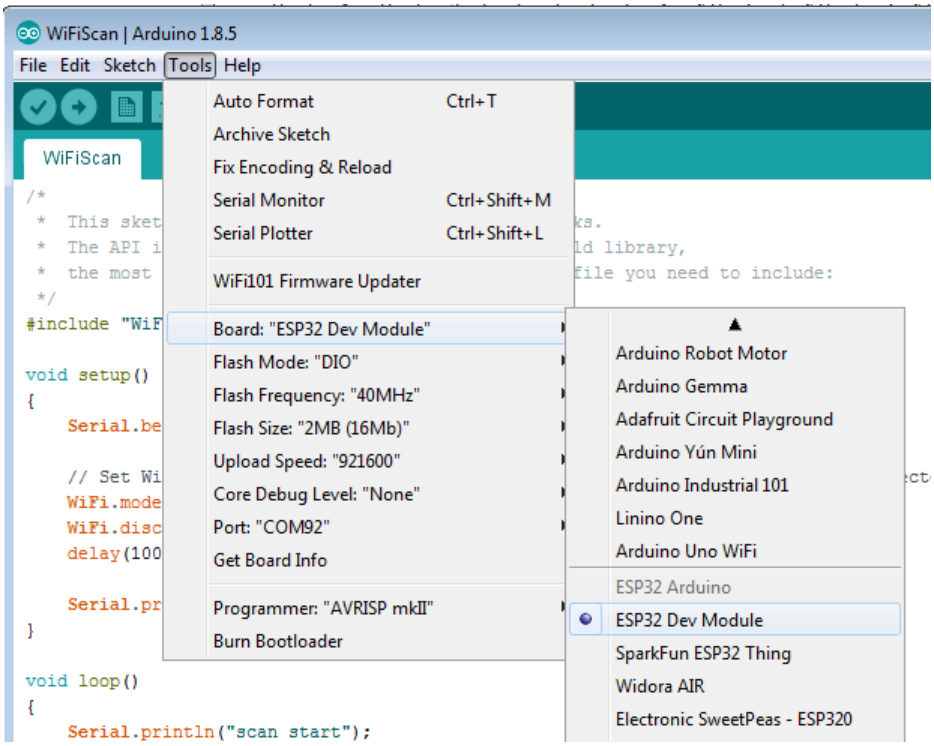


Figure 22: Screenshot that depicts selection of the ESP32 Dev Module

☞ The NINA-W10 module will soon be added to the list of supported boards. Until then, use the ESP32 Dev Module.

Start the WiFiScan example, which is available at the following folder:

```
C:\Users\ user_name
\Documents\Arduino\hardware\espressif\esp32\libraries\WiFi\examples\WiFiScan
```

Press the "**->**" (arrow) button, as shown highlighted in red in the below screenshot (Figure 23), to start the upload to NINA-W10.

Figure 23: Screenshot that depicts the arrow at the top

Select **Serial Monitor** from the Tools menu as shown in Figure 24 to view the events.

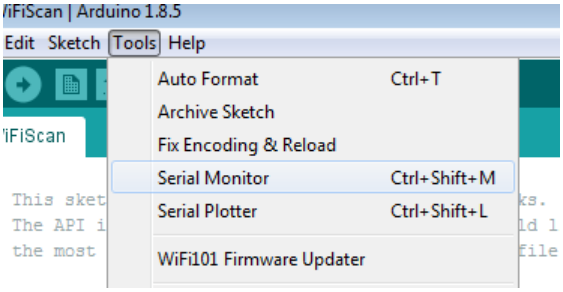


Figure 24: Screenshot that depicts selection of the "Serial Monitor"

The Wi-Fi scan starts and displays the results, as shown in Figure 25.

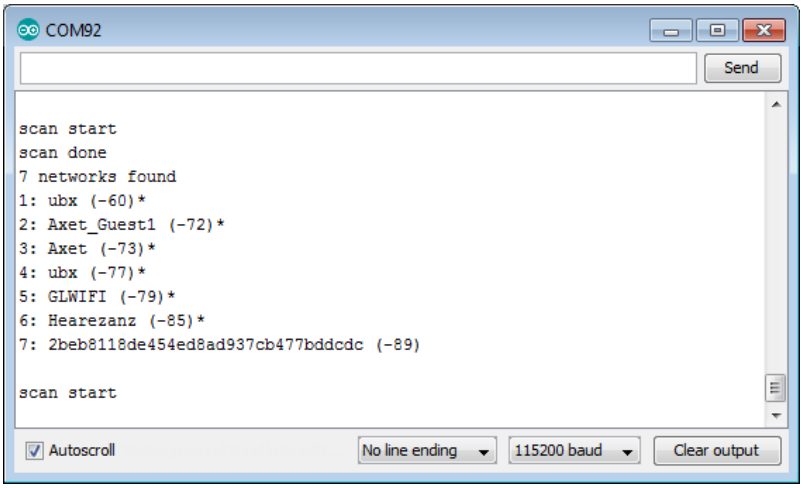


Figure 25: Sample screenshot of the Wi-Fi scan

2.9 Output power configuration

2.9.1 NINA-W10 series

To operate within the regulatory output power limits, the integrator must configure the module as per the instructions in the following subsections.

The following power configurations for Wi-Fi, Bluetooth BR/EDR and Bluetooth low energy are only valid for the official `esp-idf` git repositories.

2.9.1.1 Wi-Fi output power configuration for version v2.1

The original file (`phy_init.c`) is located in the folder `...\esp-idf\components\esp32\` in the official v2.1 `esp-idf` git repository. Update this file with the values provided below:

```
const esp_phy_init_data_t* esp_phy_get_init_data()
{
    int8_t *init_data = malloc(sizeof(esp_phy_init_data_t));
    memcpy(init_data, &phy_init_data, sizeof(esp_phy_init_data_t));
    init_data[44] = 56;//target power 0
    init_data[45] = 58;//target power 1
    init_data[46] = 54;//target power 2
    init_data[47] = 47;//target power 3
    init_data[48] = 44;//target power 4
    init_data[49] = 37;//target power 5

    init_data[50] = 0; //msc0
    init_data[51] = 0; //msc1
    init_data[52] = 0; //msc2
    init_data[53] = 0; //msc3
    init_data[54] = 0; //msc4
    init_data[55] = 2; //msc5
    init_data[56] = 4; //msc6
    init_data[57] = 5; //msc7

    init_data[58] = 1; //11B special rate enable
    init_data[59] = 3; //11B 1m, 2m
    init_data[60] = 3; //11B 5.5, 11m

    init_data[61] = 1; //channel backoff enable

    init_data[62] = 18; //backoff channel 1
    init_data[63] = 4;//backoff channel 2
    init_data[64] = 2;//backoff channel 3
    init_data[65] = 2;//backoff channel 4
    init_data[66] = 2;//backoff channel 5
```

```
    init_data[67] = 0;//backoff channel 6
    init_data[68] = 0;//backoff channel 7
    init_data[69] = 0;//backoff channel 8
    init_data[70] = 0;//backoff channel 9
    init_data[71] = 0;//backoff channel 10
    init_data[72] = 14;//backoff channel 11
    init_data[73] = 26;//backoff channel 12
    init_data[74] = 255;//backoff channel 13
    init_data[75] = 255;//backoff channel 14

    init_data[76] = 15; //backoff rate on channel 1
    init_data[77] = 15; //backoff rate on channel 2
    init_data[78] = 8; //backoff rate on channel 3
    init_data[79] = 8; //backoff rate on channel 4
    init_data[80] = 8; //backoff rate on channel 5
    init_data[81] = 0; //backoff rate on channel 6
    init_data[82] = 0; //backoff rate on channel 7
    init_data[83] = 0; //backoff rate on channel 8
    init_data[84] = 0; //backoff rate on channel 9
    init_data[85] = 0; //backoff rate on channel 10
    init_data[86] = 7; //backoff rate on channel 11
    init_data[87] = 63; //backoff rate on channel 12
    init_data[88] = 63; //backoff rate on channel 13
    init_data[89] = 63; //backoff rate on channel 14
    apply_rf_frequency_calibration(init_data);

    ESP_LOGD(TAG, "loading PHY init data from application binary");
    return (esp_phy_init_data_t*)init_data;
}
```

2.9.1.2 Wi-Fi output power configuration for versions v3.1, v3.2 and v4.0

The original file (`phy_init.c`) is located in the folder `...\esp-idf\components\esp32\` in the official git repositories for the applicable esp-idf. Update the file with the values provided below:

```
const esp_phy_init_data_t* esp_phy_get_init_data()
{
    int8_t *init_data = malloc(sizeof(esp_phy_init_data_t));
    memcpy(init_data, &phy_init_data, sizeof(esp_phy_init_data_t));
    init_data[44] = 56;//target power 0
    init_data[45] = 54;//target power 1
    init_data[46] = 48;//target power 2
    init_data[47] = 46;//target power 3
    init_data[48] = 42;//target power 4
    init_data[49] = 36;//target power 5
    init_data[50] = 0; //msc0
    init_data[51] = 0; //msc1
    init_data[52] = 0; //msc2
    init_data[53] = 0; //msc3
    init_data[54] = 0; //msc4
    init_data[55] = 1; //msc5
    init_data[56] = 3; //msc6
    init_data[57] = 4; //msc7
    init_data[58] = 1; //11B special rate enable
    init_data[59] = 2; //11B 1m, 2m
    init_data[60] = 2; //11B 5.5, 11m
    init_data[61] = 2; //fcc enable 2: enable 62-80 bytes to set maximum power
    init_data[62] = 0x53; //channel 1
    init_data[63] = 0x52;//channel 2
    init_data[64] = 0x30;//channel 3
    init_data[65] = 0x20;//channel 4
    init_data[66] = 0x20;//channel 5
    init_data[67] = 0x20;//channel 6
    init_data[68] = 0x20;//channel 7
    init_data[69] = 0x20;//channel 8
    init_data[70] = 0x20;//channel 9
    init_data[71] = 0x20;//channel 10
    init_data[72] = 0x22;//channel 11
```

```
    init_data[73] = 0x10;//channel 12
    init_data[74] = 0x10;//channel 13
    init_data[75] = 0xAA;//channel 14
    init_data[76] = 0x44; //channel 3, 4
    init_data[77] = 0x44; //channel 5, 6
    init_data[78] = 0x44; //channel 7, 8
    init_data[79] = 0x44; //channel 9, 10
    init_data[80] = 0x44; //channel 11
    apply_rf_frequency_calibration(init_data);
    ESP_LOGD(TAG, "loading PHY init data from application binary");
    return (esp_phy_init_data_t*)init_data;
}
```

2.9.1.3 Bluetooth BR/EDR output power configuration

No output power configuration for Bluetooth BR/EDR is required. With default settings, the module will operate at ~6 dBm, which is within the regulatory limit for NINA-W1.

2.9.1.4 Bluetooth low energy output power configuration

No output power configuration for Bluetooth low energy is required. With default settings, the module will operate at ~6 dBm, which is within the regulatory limit for NINA-W1.

2.9.2 NINA-W13/W15 series

No output power configuration required by the integrator. Using the u-connectXpress guarantees operation within regulatory limits.

3 Design-in

3.1 Overview

For an optimal integration of NINA-W1 series modules in the final application board, it is recommended to follow the design guidelines stated in this chapter. Every application circuit must be properly designed to guarantee the correct functionality of the related interface; however, a number of points require high attention during the design of the application device.

The following list provides important points sorted by rank of importance in the application design, starting from the highest relevance:

1. Module antenna connection: **Ant** pad

   Antenna circuit affects the RF compliance of the device integrating NINA-W1x1 modules with applicable certification schemes. Follow the recommendations provided in section 3.3 for schematic and layout design.

2. Module supply: **VCC**, **VCC_IO**, and **GND** pins

   The supply circuit affects the performance of the device integrating NINA-W1 series module. Follow the recommendations provided in section 3.2 for schematic and layout design.

3. High speed interfaces: **UART** pins

   High speed interfaces can be a source of radiated noise and can affect compliance with regulatory standards for radiated emissions. Follow the recommendations provided in section 3.4.1 for schematic and layout design.

4. System functions: **RESET_N**, GPIO and other System input and output pins

   Accurate design is required to guarantee that the voltage level is well defined during module boot.

5. Other pins:

   Accurate design is required to guarantee proper functionality.

3.2 Supply interfaces

3.2.1 Module supply (VCC) design

Good connection of the module's **VCC** pin with DC supply source is required for correct RF performance. The guidelines are summarized below:

- The VCC connection must be as wide and short as possible.
- The VCC connection must be routed through a PCB area separated from sensitive analog signals and sensitive functional units. It is a good practice to interpose at least one layer of the PCB ground between VCC track and other signal routing.

There is no strict requirement of adding bypass capacitance to the supply net close to the module. However, depending on the layout of the supply net and other consumers on the same net, bypass capacitors might still be beneficial. Though the GND pins are internally connected, connect all the available pins to solid ground on the application board, as a good (low impedance) connection to an external ground can minimize power loss and improve RF and thermal performance.

3.2.2 Digital I/O interfaces reference voltage (VCC_IO)

Good connection of the module's **VCC_IO** pin with DC supply source is required for correct performance. The guidelines are summarized below:

- The **VCC_IO** connection must be as wide and short as possible.
- The **VCC_IO** connection must be routed through a PCB area separated from sensitive analog signals and sensitive functional units. It is a good practice to interpose at least one layer of PCB ground between **VCC_IO** track and other signal routing.

There is no strict requirement of adding bypass capacitance to the supply net close to the module. However, depending on the layout of the supply net and other consumers on the same net, bypass capacitors might still be beneficial. Though the GND pins are internally connected, connect all the available pins to solid ground on the application board, as a good (low impedance) connection to an external ground can minimize power loss and improve RF and thermal performance.

3.3 Antenna interface

As the unit cannot be mounted arbitrarily, the placement should be chosen with consideration so that it does not interfere with radio communication. The NINA-W1x2 and W1x6 modules with an internal surface mounted PIFA antenna or PCB trace antenna cannot be mounted in a metal enclosure. No metal casing or plastics using metal flakes should be used. Avoid metallic based paint or lacquer as well. NINA-W1x1 modules offer more freedom as an external antenna can be mounted further away from the module.

⚠ According to the FCC regulations, the transmission line from the module's antenna pin to the antenna or antenna connector on the host PCB is considered part of the approved antenna design. Therefore, module integrators must either follow exactly one of the antenna reference design used in the module's FCC type approval or certify their own designs.

3.3.1 RF transmission line design (NINA-W1x1)

RF transmission lines, such as the ones from the **ANT** pad up to the related antenna connector or up to the related internal antenna pad, must be designed so that the characteristic impedance is as close as possible to 50 Ω.

Figure 26 shows the design options and the main parameters to be considered when implementing a transmission line on a PCB:

- The micro strip (a track coupled to a single ground plane, separated by dielectric material)
- The coplanar micro strip (a track coupled to the ground plane and side conductors, separated by dielectric material)
- The strip line (a track sandwiched between two parallel ground planes, separated by dielectric material).

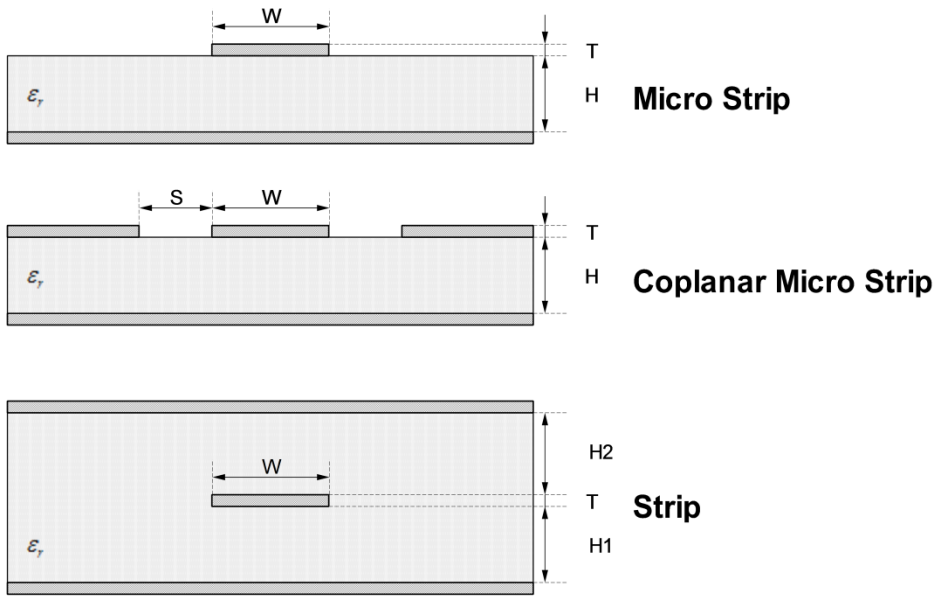


Figure 26: Transmission line trace design

To properly design a 50 Ω transmission line, the following remarks should also be considered:

- The designer should provide enough clearance from surrounding traces and ground in the same layer; in general, a trace to ground clearance of at least two times the trace width should be considered. The transmission line should also be 'guarded' by ground plane area on each side.
- The characteristic impedance can be calculated as first iteration using tools provided by the layout software. It is advisable to ask the PCB manufacturer to provide the final values that are usually calculated using dedicated software and available stack-ups from production. It could also be possible to request an impedance coupon on panel's side to measure the real impedance of the traces.
- FR-4 dielectric material, although its high losses at high frequencies can be considered in RF designs provided that:
    - RF trace length must be minimized to reduce dielectric losses.
    - If traces longer than few centimeters are needed, it is recommended to use a coaxial connector and cable to reduce losses
    - Stack-up should allow for thick 50 Ω traces and at least 200 µm trace width is recommended to assure good impedance control over the PCB manufacturing process.
    - FR-4 material exhibits poor thickness stability and thus less control of impedance over the trace length. Contact the PCB manufacturer for specific tolerance of controlled impedance traces.
- The transmission lines width and spacing to the GND must be uniform and routed as smoothly as possible: route RF lines in 45 °C angle or in arcs.
- Add GND stitching vias around transmission lines.
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer, providing enough vias on the adjacent metal layer.
- Route RF transmission lines far from any noise source (as switching supplies and digital lines) and from any sensitive circuit to avoid crosstalk between RF traces and Hi-impedance or analog signals.
- Avoid stubs on the transmission lines, any component on the transmission line should be placed with the connected pad over the trace. Also avoid any unnecessary component on RF traces.

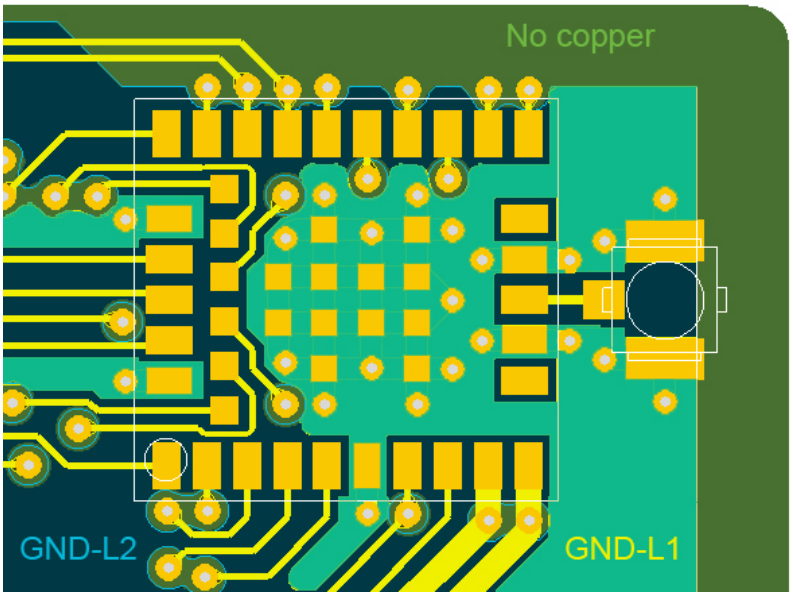


Figure 27: Example of RF trace and ground design from NINA-W1 Evaluation Kit (EVK)

3.3.2 Antenna design (NINA-W1x1)

NINA-W1x1 is suited for designs when an external antenna is needed due to mechanical integration or placement of the module.

Designers must take care of the antennas from all perspective at the beginning of the design phase when the physical dimensions of the application board are under analysis/decision, as the RF compliance of the device integrating NINA-W1 module with all the applicable required certification schemes heavily depends on the radiating performance of the antennas. The designer is encouraged to consider one of the u-blox suggested antenna part numbers and follow the layout requirements.

- External antennas such as linear monopole:
  - External antennas basically do not imply physical restriction to the design of the PCB where the module is mounted.
  - The radiation performance mainly depends on the antennas. It is required to select antennas with optimal radiating performance in the operating bands.
  - RF cables should carefully be selected with minimum insertion losses. Additional insertion loss will be introduced by low quality or long cable. Large insertion loss reduces radiation performance.
  - A high quality 50 Ω coaxial connector provides proper PCB-to-RF-cable transition.
- Integrated antennas such as patch-like antennas:
  - Internal integrated antennas imply physical restriction to the PCB design:
    Integrated antenna excites RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna; its dimension defines the minimum frequency that can be radiated. Therefore, the ground plane can be reduced down to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that has to be radiated, given that the orientation of the ground plane related to the antenna element must be considered.
    The RF isolation between antennas in the system must be as high as possible and the correlation between the 3D radiation patterns of the two antennas has to be as low as possible. In general, an RF separation of at least a quarter wavelength between the two antennas is required to achieve a maximum isolation and low pattern correlation; increased separation should be considered if possible, to maximize the performance and fulfil the requirements described in Table 3.

As a numerical example, the physical restriction to the PCB design can be considered as shown below:
Frequency = 2.4 GHz → Wavelength = 12.5 cm → Quarter wavelength = 3.125 cm[1]

- Radiation performance depends on the whole product and antenna system design, including product mechanical design and usage. Antennas should be selected with optimal radiating performance in the operating bands according to the mechanical specifications of the PCB and the whole product.

Table 3 summarizes the requirements for the antenna RF interface:

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT** pin.
Frequency Range	2400 - 2500 MHz	Wi-Fi and Bluetooth.
Return Loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The Return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the primary antenna RF connection matches the 50 Ω characteristic impedance of the **ANT** pin. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the **ANT** pin over the operating frequency range, thus maximizing the amount of the power transferred to the antenna.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to the antenna input; the efficiency is a measure of how well an antenna receives or transmits.
Maximum Gain	Refer to Data sheet	The maximum antenna gain must not exceed the value specified in type approval documentation to comply with the radiation exposure limits specified by regulatory agencies.

Table 3: Summary of antenna interface (ANT) requirements for NINA-W1x1

Observe the following recommendations while selecting external or internal antennas:

- Select antennas that provide optimal return loss (or VSWR) figure over all the operating frequencies.
- Select antennas that provide optimal efficiency figure over all the operating frequencies.
- Select antennas that provide appropriate gain figure (that is, combined antenna directivity and efficiency figure) so that the electromagnetic field radiation intensity does not exceed the regulatory limits specified in some countries (for example, by FCC in the United States).

3.3.2.1 RF Connector Design

If an external antenna is required, the designer should consider using a proper RF connector. It is the responsibility of the designer to verify the compatibility between plugs and receptacles used in the design.

Table 4 suggests several RF connector plugs that can be used by the designers to connect RF coaxial cables based on the declaration of the respective manufacturers. The Hirose U.FL-R-SMT RF receptacles (or similar parts) require a suitable mated RF plug from the same connector series. Due to wide usage of this connector, several manufacturers offer compatible equivalents.

[1] Wavelength referred to a signal propagating over the air.

Manufacturer	Series	Remarks
Hirose	U.FL® Ultra Small Surface Mount Coaxial Connector	Recommended
I-PEX	MHF® Micro Coaxial Connector	
Tyco	UMCC® Ultra-Miniature Coax Connector	
Amphenol RF	AMC® Amphenol Micro Coaxial	
Lighthorse Technologies, Inc.	IPX ultra micro-miniature RF connector	

Table 4: U.FL compatible plug connector

Typically, the RF plug is available as a cable assembly. Different types of cable assembly are available; the user should select the cable assembly best suited to the application. The key characteristics are:

- RF plug type: select U.FL or equivalent
- Nominal impedance: 50 Ω
- Cable thickness: Typically, from 0.8 mm to 1.37 mm. Select thicker cables to minimize insertion loss.
- Cable length: Standard length is typically 100 mm or 200 mm; custom lengths may be available on request. Select shorter cables to minimize insertion loss.
- RF connector on the other side of the cable: For example, another U.FL. (for board-to-board connection) or SMA (for panel mounting)

Consider that SMT connectors are typically rated for a limited number of insertion cycles. Additionally, the RF coaxial cable may be relatively fragile compared to other types of cables. To increase application ruggedness, connect U.FL connector to a more robust connector such as SMA fixed on panel.

☞ A de-facto standard for SMA connectors implies the usage of reverse polarity connectors (RP-SMA) on Wi-Fi and Bluetooth® end products to increase the difficulty for the end user to replace the antenna with higher gain versions and exceed regulatory limits.

The following recommendations apply for proper layout of the connector:

- Strictly follow the connector manufacturer's recommended layout:
  - SMA Pin-Through-Hole connectors require GND keep-out (that is, clearance, a void area) on all the layers around the central pin up to annular pads of the four GND posts.
  - U.FL. surface mounted connectors require no conductive traces (that is, clearance, a void area) in the area below the connector between the GND land pads.
- If the connector's RF pad size is wider than the micro strip, remove the GND layer beneath the RF connector to minimize the stray capacitance thus keeping the RF line 50 Ω. For example, the active pad of the U.FL. connector must have a GND keep-out (that is, clearance, a void area) at least on the first inner layer to reduce parasitic capacitance to ground.

3.3.2.2 Integrated antenna design

If integrated antennas are used, the transmission line is terminated by the integrated antennas themselves. Follow the guidelines mentioned below:

- The antenna design process should begin at the start of the whole product design process. Self-made PCBs and antenna assembly are useful in estimating overall efficiency and radiation path of the intended design.
- Use antennas designed by an antenna manufacturer providing the best possible return loss (or VSWR).
- Provide a ground plane large enough according to the related integrated antenna requirements. The ground plane of the application PCB may be reduced to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that has to be radiated; however overall antenna efficiency may benefit from larger ground planes.

- Proper placement of the antenna and its surroundings is also critical for antenna performance. Avoid placing the antenna close to conductive or RF-absorbing parts such as metal objects, ferrite sheets and so on as they may absorb part of the radiated power or shift the resonant frequency of the antenna or affect the antenna radiation pattern.
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, antennas may require tuning/matching to comply with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines and plan the validation activities on the final prototypes like tuning/matching and performance measures. See also Table 3.
- RF section may be affected by noise sources like hi-speed digital buses. Avoid placing the antenna close to buses such as DDR or consider taking specific countermeasures like metal shields or ferrite sheets to reduce the interference.

⚠ Take care of the interaction between co-located RF systems like LTE sidebands on 2.4 GHz band. Transmitted power may interact or disturb the performance of NINA-W1 modules.

3.3.3 On-board antenna design

If a plastic enclosure is used, it is possible to use NINA-W1 with the embedded antenna. To reach optimum operating performance, follow the instructions provided in the sections below.

3.3.3.1 NINA-W1x2 – Internal PIFA antenna

- The module shall be placed in the corner of the host PCB with the antennas feed point in the corner (pins 15 and 16), as shown in Figure 28. Other edge placements positions, with the antenna closest to the edge, are also possible. However, these placements give only a moderately reduced antenna performance compared to a corner placement.
- A large ground plane on the host PCB is a prerequisite for good antenna performance.
- The host PCB shall include a full GND plane underneath the entire module, including the antenna section. This to facilitate efficient grounding of the module.
- High / large parts including metal shall not be placed closer than 10 mm to the module's antenna.
- At least 5 mm clearance between the antenna and the casing is needed. If the clearance is less than 5 mm, the antenna performance will be affected. PC and ABS gives less impact and POS type plastic gives more.
- The module shall be placed such that the antenna faces outwards from the product and is not obstructed by any external items in close vicinity of the products intended use case.

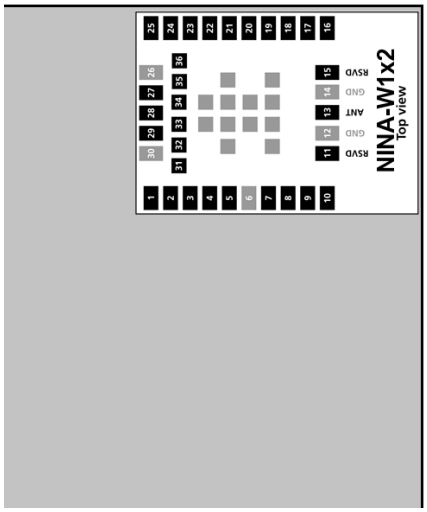


Figure 28: Placement of NINA-W1x2 with internal PIFA antenna

⚠ Take care while handling the EVK-NINA-W1x2. Applying force to the module might damage the internal antenna.

⚠ Make sure that the end-product design is done in such a way that the antenna is not subject to physical force.

3.3.3.2 NINA-W1x6 – PCB trace antenna

- The module shall be placed in the center of an edge of the host PCB.
- A large ground plane on the host PCB is a prerequisite for good antenna performance. It is recommended to have the ground plane extending at least 10 mm on the three non-edge sides of the module. See
- Figure 29.
- The host PCB shall include a full GND plane underneath the entire module, with a ground cut out under the PCB trace antenna according to the description in Figure 30.
- The NINA-W1x6 has four extra GND pads under the antenna that need to be connected for a good antenna performance. Detailed measurements of the footprint including this extra GND pads can be found in the NINA-W1 series data sheets [3] [4].
- High / large parts including metal shall not be placed closer than 10 mm to the module's antenna.
- At least 10 mm clearance between the antenna and the casing is recommended. If the clearance is less than 10 mm, the antenna performance can be adversely affected.
- The module shall be placed such that the antenna faces outwards from the product and is not obstructed by any external items in close vicinity of the products intended use case.

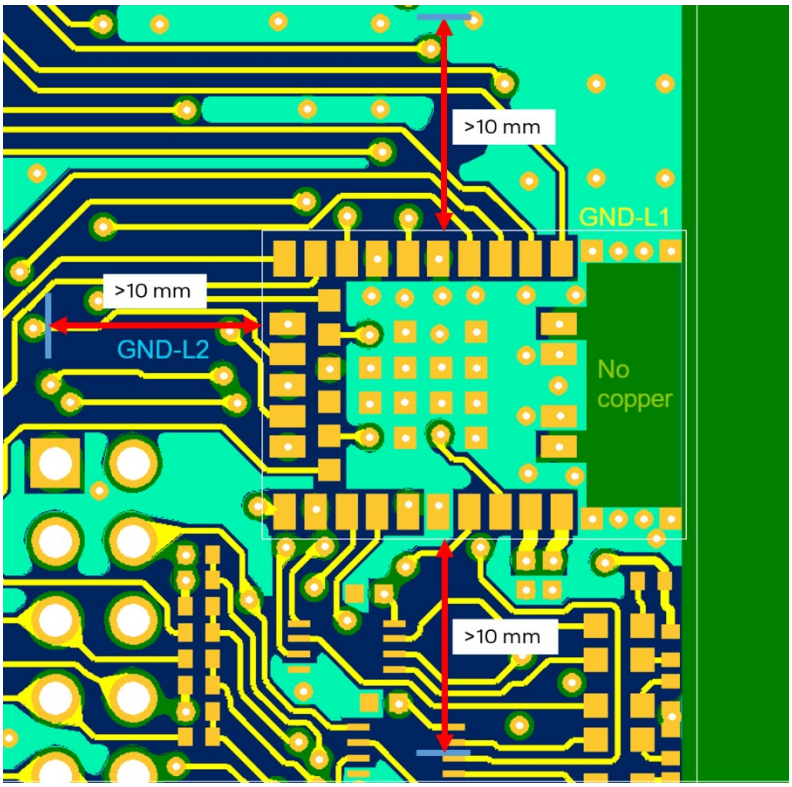


Figure 29: GND plane guard area enclosing the NINA-W1x6 module

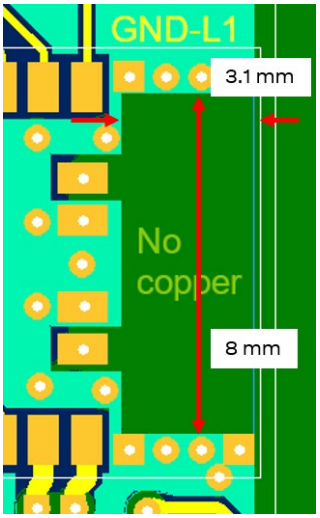


Figure 30: Size of the GND cut out for the NINA-W1x6 module's PCB trace antenna

3.4 Data communication interfaces

3.4.1 Asynchronous serial interface (UART) design

The layout of the UART bus should be done so that noise injection and cross talk are avoided. It is recommended to use the hardware flow control with RTS/CTS to prevent temporary UART buffer overrun.

The flow control signals **RTS/CTS** are active low. Consequently, 0 (ON state =low level) allows the UART to transmit.

- **CTS** is an input to the NINA-W1 module. If the host sets this input to 0 (ON state = low level) the module can transmit.
- **RTS** is an output off the NINA-W1 module. The module sets the output to 0 (ON state = low level) when it is ready to receive transmission.

3.4.2 Ethernet (RMII+SMI)

It is recommended to route all signals in the RMII bus with the same length and have appropriate grounding in the surrounding layers; total bus length should also be minimized. The layout of the RMII bus should be done so that crosstalk with other parts of the circuit is minimized providing adequate isolation between the signals, the clock and the surrounding busses/traces.

Termination resistors are recommended for the RX and TX lines on the RMII bus.

A pull-up resistor is required for **RMII_MDIO** and **RMII_CRSDV**.

The general high-speed layout guidelines described in section 3.5 are applicable for the RMII and the SMI bus.

3.5 General high-speed layout guidelines

These general design guidelines are considered as best practices and are valid for any bus present in the NINA-W1 series modules. The designer should prioritize the layout of higher speed busses. Low frequency signals are generally not critical for layout.

☞ One exception is represented by High Impedance traces (such as signals driven by weak pull resistors) that may be affected by crosstalk. For those traces, supplementary 4W isolation from other busses is recommended.

3.5.1 General considerations for schematic design and PCB floor-planning

- Verify which signal bus requires termination and add series resistor terminations to the schematics.
- Carefully consider the placement of the module with respect to antenna position and host processor.
- Verify with PCB manufacturer allowable stack-ups and controlled impedance dimensioning.
- Verify that the power supply design and power sequence are compliant with the specification of NINA-W1 series module.

3.5.2 Module placement

- Accessory parts like bypass capacitors should be placed as close as possible to the module to improve filtering capability, prioritizing the placement of the smallest size capacitor close to module pads.

⚠ Particular care should be taken not to place components close to the antenna area. The designer should carefully follow the recommendations from the antenna manufacturer about the distance of the antenna vs. other parts of the system. The designer should also maximize the distance of the antenna to Hi-frequency busses like DDRs and related components or consider an optional metal shield to reduce interferences that could be picked up by the antenna thus reducing the module's sensitivity.

- An optimized module placement allows better RF performance. See section 3.3 for more information on antenna consideration during module placement.

3.5.3 Layout and manufacturing

- Avoid stubs on high-speed signals. Even through-hole vias may have an impact on signal quality.
- Verify the recommended maximum signal skew for differential pairs and length matching of buses.
- Minimize the routing length; longer traces will degrade signal performance. Ensure that maximum allowable length for high-speed busses is not exceeded.
- Ensure that you track your impedance matched traces. Consult with your PCB manufacturer early in the project for proper stack-up definition.
- RF and digital sections should be clearly separated on the board.
- Ground splitting is not allowed below the module.
- Minimize bus length to reduce potential EMI issues from digital busses.
- All traces (including low speed or DC traces) must couple with a reference plane (GND or power); Hi-speed busses should be referenced to the ground plane. In this case, if the designer needs to change the ground reference, an adequate number of GND vias must be added in the area of transition to provide a low impedance path between the two GND layers for the return current.
- Hi-Speed busses are not allowed to change reference plane. If a reference plane change is unavoidable, some capacitors should be added in the area to provide a low impedance return path through the different reference planes.
- Trace routing should keep a distance greater than 3W from the ground plane routing edge.
- Power planes should keep a distance from the PCB edge sufficient to route a ground ring around the PCB, the ground ring must then be connected to other layers through vias.

3.6 Module footprint and paste mask

The mechanical outline of the NINA-W1 series modules can be found in the NINA-W1 series Data Sheets [2] [3] [4]. The proposed land pattern layout reflects the pads layout of the module.

The Non Solder Mask Defined (NSMD) pad type is recommended over the Solder Mask Defined (SMD) pad type, which implements the solder mask opening 50 µm larger per side than the corresponding copper pad.

The suggested paste mask layout for the NINA-W1 series modules is to follow the copper mask layout as described in the NINA-W1 series data sheets [2], [3], [4].

⚠ These are recommendations only and not specifications. The exact mask geometries, distances and stencil thicknesses must be adapted to the specific production processes of the customer.

3.7 Thermal guidelines

The NINA-W1 series modules have been successfully tested in -40 °C to +85 °C. A good grounding should be observed for temperature relief during high ambient temperature.

3.8 ESD guidelines

The immunity of devices integrating NINA-W1 modules to Electro-Static Discharge (ESD) is part of the Electro-Magnetic Compatibility (EMC) conformity, which is required for products bearing the CE marking, compliant with the R&TTE Directive (99/5/EC), the EMC Directive (89/336/EEC) and the Low Voltage Directive (73/23/EEC) issued by the Commission of the European Community.

Compliance with these directives implies conformity to the following European Norms for device ESD immunity: ESD testing standard *CENELEC EN 61000-4-2* and the radio equipment standards *ETSI EN 301 489-1*, *ETSI EN 301 489-7*, *ETSI EN 301 489-24*, the requirements of which are summarized in Table 5.

The ESD immunity test is performed at the enclosure port, defined by *ETSI EN 301 489-1* as the physical boundary through which the electromagnetic field radiates. If the device implements an integral antenna, the enclosure port is seen as all insulating and conductive surfaces housing the device. If the device implements a removable antenna, the antenna port can be separated from the enclosure port. The antenna port includes the antenna element and its interconnecting cable surfaces.

The applicability of ESD immunity test to the whole device depends on the device classification as defined by *ETSI EN 301 489-1*. Applicability of ESD immunity test to the related device ports or the related interconnecting cables to auxiliary equipment, depends on the device accessible interfaces and manufacturer requirements, as defined by the *ETSI EN 301 489-1*.

Contact discharges are performed at conductive surfaces, while air discharges are performed at insulating surfaces. Indirect contact discharges are performed on the measurement setup horizontal and vertical coupling planes as defined in the *CENELEC EN 61000-4-2*.

For the definition of integral antenna, removable antenna, antenna port, and device classification, refer to the ETSI EN 301 489-1. For the contact and air discharges definitions, refer to CENELEC EN 61000-4-2.

Parameter	Min.	Typical	Max.	Unit	Remarks
ESD immunity. All exposed surfaces of the radio equipment and ancillary equipment in a representative configuration			8*	kV	Indirect discharge according to IEC 61000-4-2
ESD sensitivity, tested for all pins except ANT and RSVD pins #11, #15, #33			2.5	kV	Human body model according to JEDEC JS001

* Tested on EVK-NINA-W1 evaluation board.

Table 5: Electro-Magnetic Compatibility ESD immunity requirements as defined by CENELEC EN 61000-4-2, ETSI EN 301 489-1, ETSI EN 301 489-7, ETSI EN 301 489-24

NINA-W1 is manufactured with consideration to the specific standards for minimizing the occurrence of ESD events. The highly automated process complies with the IEC61340-5-1 (STM5.2-1999 Class M1 devices) standard. Consequently, the designer should implement proper measures to protect from ESD events on any pin that may be exposed to the end user.

Compliance with standard protection level specified in the EN61000-4-2 can be achieved by including the ESD protections in parallel to the line, close to areas accessible by the end user.

4 Handling and soldering

No natural rubbers, hygroscopic materials or materials containing asbestos are employed.

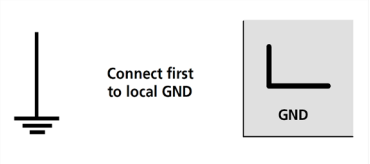
4.1 Packaging, shipping, storage, and moisture preconditioning

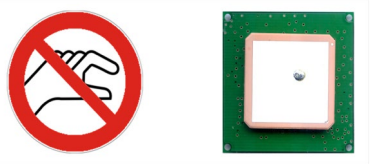
For information pertaining to reels, tapes or trays, moisture sensitivity levels (MSL), shipment and storage, as well as drying for preconditioning refer to NINA-W1 series Data Sheets [2]/[3]/[4], and u-blox package information guide [5].

4.2 Handling

The NINA-W1 series modules are Electro-Static Discharge (ESD) sensitive devices and require special precautions during handling. Particular care must be exercised when handling patch antennas, due to the risk of electrostatic charges. In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the receiver:

- Unless there is a galvanic coupling between the local GND (on the workbench for example) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect ground of the device
- When handling the RF pin, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges; for example, oh the patch antenna (~10 pF), coaxial cable (~50-80 pF/m), soldering iron, and so on.
- To prevent electrostatic discharge through the RF input, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in non ESD protected work area, implement proper ESD protection measures in the design.
- When soldering RF connectors and patch antennas to the receiver's RF pin, make sure to use an ESD safe soldering iron (tip).





4.3 Soldering

4.3.1 Reflow soldering process

NINA-W1 series modules are surface mount modules supplied on a FR4-type PCB with gold plated connection pads and are produced in a lead-free process with a lead-free soldering paste. The bow and twist of the PCB is maximum 0.75% according to IPC-A-610E. The thickness of solder resist between the host PCB top side and the bottom side of the NINA-W1 series module must be considered for the soldering process.

The module is compatible with industrial reflow profile for RoHS solders. Use of "No Clean" soldering paste is strongly recommended.

The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven, and particular type of solder paste used. The optimal soldering profile used has to be trimmed for each case depending on the specific process and PCB layout.

Process parameter		Unit	Value
Pre-heat	Ramp up rate to T_{SMIN}	K/s	3
	T_{SMIN}	°C	150
	T_{SMAX}	°C	200
	t_S (from +25 °C)	s	150
	t_S (Pre-heat)	s	60 to 120
Peak	T_L	°C	217
	t_L (time above T_L)	s	40 to 60
	T_P (absolute max)	°C	245
Cooling	Ramp-down from T_L	K/s	4
	Allowed soldering cycles	-	1

Table 6: Recommended reflow profile

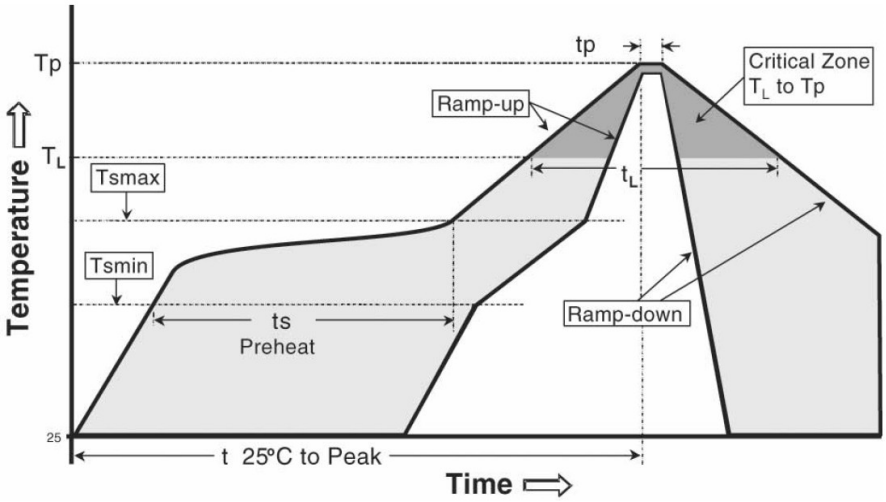


Figure 31: Reflow profile

Lower value of T_P and slower ramp down rate (2 – 3 °C/sec) is preferred.

After reflow soldering, optical inspection of the modules is recommended to verify proper alignment.

⚠ The target values given in Table 6 should be regarded as general guidelines for a Pb-free process. Refer to JEDEC J-STD-020C standard for further information.

4.3.2 Cleaning

Cleaning the modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the crystal oscillators.

For best results, use a "no clean" soldering paste and eliminate the cleaning step after the soldering process.

4.3.3 Other remarks

- Only a single reflow soldering process is allowed for boards with a module populated on it.
- Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices may require wave soldering to solder the THT components. Only a single wave soldering process is allowed for boards populated with the modules. *Miniature Wave Selective Solder* process is preferred over traditional wave soldering process.
- Hand soldering is not recommended.
- Rework is not recommended.
- Conformal coating may affect the performance of the module, it is important to prevent the liquid from flowing into the module. The RF shields do not provide protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating. Conformal coating of the module will void the warranty.
- Grounding metal covers: attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk and will void the warranty of the module. The numerous ground pins are adequate to provide optimal immunity to interferences.
- The module contains components that are sensitive to Ultrasonic Waves. Use of any ultrasonic processes such as cleaning, welding etc., may damage the module. Use of ultrasonic processes on an end product integrating this module will also void the warranty.

5 Approvals

⚠ Country approval for NINA-W1x6 is pending.

For additional regulatory information, see the NINA-W1 series data sheets [2], [3], [4].

5.1 General requirements

The NINA-W1 series modules comply with the regulatory demands of Federal Communications Commission (FCC), Industry Canada (IC)[2] and the CE mark. This section provides the instructions that must be followed by an integrator while including NINA-W1 series into an end product.

- Any changes to hardware, hosts or co-location configuration may require new radiated emission and SAR evaluation and/or testing.
- The regulatory compliance of NINA-W1 series does not exempt the end product from being evaluated against applicable regulatory demands; for example, FCC Part 15B criteria for unintentional radiators [9].
- Only authorized antenna(s) may be used.
- Any notification to the end user about how to install or remove the integrated radio module is NOT allowed.

5.2 FCC/IC End-product regulatory compliance

u-blox warrants that the modular transmitter fulfills the FCC/IC regulations when operating in authorized modes on any host product given that the integrator follows the instructions as described in this document.

5.2.1 NINA-W101 and NINA-W102 FCC ID and IC certification number

The u-blox FCC ID and IC certification number for NINA-W101 and NINA-W102 is restricted and can be used only by u-blox. Integrators other than u-blox may not refer to the u-blox FCC ID and IC certification number on their end products.

Following the processes called “Change in ID” (FCC) and “Multiple listing” (IC), an integrator can use all the certifications done by u-blox. Through these processes, the integrator becomes the grantee of a copy of the original u-blox FCC/IC certification. As grantee, the integrator is free to perform any updates to the new certification if needed; for example, adding new antennas to the authorization for NINA-W101 module using the antenna pin.

u-blox will guide customers through these processes and support with the approval letter that must be filed as a Cover Letter exhibit with the application to the authority.

⚠ It is the responsibility of the integrator to comply with any upcoming regulatory requirements.

5.2.2 NINA-W13/W15 series FCC ID and IC certification number

An end product integrating the NINA-W13 series or NINA-W15 series module using u-connectXpress can refer to the u-blox FCC ID and IC certification number.

u-blox can support updates to the u-blox regulatory authorization, if needed. For example, adding new antennas to the u-blox authorization for NINA-W131 module using the antenna pin.

[2] Official name is Innovation, Science and Economic Development (ISED) Canada.

5.2.3 Antenna requirements

In addition to the general requirement to use only authorized antennas, the u-blox grant also requires a separation distance of at least 20 cm from the antenna to all persons. Also, the antenna must not be co-located with any other antenna or transmitter (simultaneous transmission) as well. If this cannot be met, a Permissive Change as described below must be made to the grant.

5.2.3.1 Separation distance

If the required separation distance of 20 cm cannot be fulfilled, a SAR evaluation must be performed. This consists of additional calculations and/or measurements. The result must be added to the grant file as a Class II Permissive Change.

5.2.3.2 Co-location (simultaneous transmission)

If the module is to be co-located with another transmitter, additional measurements for simultaneous transmission is required. The results must be added to the grant file as a Class II Permissive Change.

5.2.3.3 Adding a new antenna for authorization

If the authorized antennas and/or antenna trace design cannot be used, the new antenna and/or antenna trace designs must be added to the grant file. This is done by a Class I Permissive Change or a Class II Permissive Change, depending on the specific antenna and antenna trace design.

- Antennas of the same type and with less or same gain as an already approved antenna can be added under a Class I Permissive Change.
- Antenna trace designs deviating from the u-blox reference design and new antenna types are added under a Class II Permissive Change.

⚠ Integrators who want to refer to the u-blox FCC ID / IC certification ID must send an email to the support team email address for your area as listed in the Contact section to discuss the Permissive Change Process. Class II Permissive Changes will be subject to NRE costs.

6 Product testing

6.1 u-blox In-Series production test

u-blox focuses on high quality for its products. All units produced are fully tested automatically in production line. Stringent quality control process has been implemented in the production line. Defective units are analyzed in detail to improve the production quality.

This is achieved with automatic test equipment (ATE) in production line, which logs all production and measurement data. A detailed test report for each unit can be generated from the system. Figure 32 shows typical automatic test equipment (ATE) in a production line.

The following tests are performed as part of the production tests:

- Digital self-test (firmware download, MAC address programming)
- Measurement of currents
- Functional tests
- Digital I/O tests
- Measurement and verification of RF characteristics in all supported bands. For example, measurements of receiver RSSI and transmitter power levels and frequency tuning of the reference clock.

Figure 32: Automatic test equipment for module test

6.2 OEM manufacturer production test

As the testing is already done by u-blox, an OEM manufacturer does not need to repeat firmware tests or measurement of the module's RF performance or tests over analog and digital interfaces in their production test.

However, an OEM manufacturer should focus on:

- Module assembly on the device: It should be verified that:
  - Soldering and handling process did not damage the module components
  - All module pins are well soldered on device board
  - There are no short circuits between the pins
- Component assembly on the device: It should be verified that:
  - Communication with the host controller can be established
  - The interfaces between the module and device are working
  - Overall RF performance test of the device including antenna

Dedicated tests can be implemented to check the device. For example, the measurement of module current consumption when set in a specified state can detect a short circuit if compared with a "Golden Device" result.

The standard operational module firmware and test software on the host can be used to perform functional tests (communication with the host controller, check interfaces) and to perform basic RF performance tests.

6.2.1 "Go/No go" tests for integrated devices

A "Go/No go" test compares the signal quality with a "Golden Device" in a location with known signal quality. This test can be performed after establishing a connection with an external device.

A very simple test can be performed by just scanning for a known Bluetooth low energy device and checking the signal level.

These kinds of test may be useful as a "go/no go" test but not for RF performance measurements.

This test is suitable to check the functionality of the communication with the host controller and the power supply. It is also a means to verify if the components are well soldered.

A basic RF functional test of the device including the antenna can be performed with standard Bluetooth low energy devices as remote stations. The device containing the NINA-W1 series module and the antennas should be arranged in a fixed position inside an RF shield box to prevent interferences from other possible radio devices to get stable test results.

Appendix

A Glossary

Abbreviation	Definition
AEC	Automotive Electronics Council
AFA	Automatic Frequency Adaption
AP	Access Point
ARM	Arm (Advanced RISC Machines) Holdings
ASCII	American Standard Code for Information Interchange
ATE	Automatic Test Equipment
BBR	Battery Backed RAM
BER	Bit Error Rate
BP	Band Pass
BPF	Band Pass Filter
BT	Bluetooth
CAN	Controller Area Network
CPU	Central Processing Unit
CPU	Central Processing Unit
CTS	Clear To Send
DC	Direct Current
DC	Direct Current
DCE	Data Circuit-terminating Equipment* / Data Communication Equipment*
DDC	Display Data Channel
DDR	Double Data Rate
DL	Down Link (Reception)
DRX	Discontinuous Reception
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EIRP	Equivalent Isotropically Radiated Power
EMC	Electro-magnetic Compatibility
EMI	Electromagnetic Interference
ESD	Electro-Static Discharge
GND	Ground
IoT	Internet of Things
ISM	Industrial, Scientific, and Medical radio
LED	Light-Emitting Diode
LPO	Low Power Oscillator
LTE	Long-Term Evolution
MAC	Media Access Control
MCS	Modulation Coding Scheme
MCU	Microcontroller
MISO	Master Input Slave Output
MOSI	Master Output Slave Input
MSL	Moisture Sensitivity Level

Abbreviation	Definition
NSMD	Non Solder Mask Defined
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
RF	Radio Frequency
RMII	Reduced Media-independent Interface
ROM	Read-only Memory
RSSI	Received Signal Strength Indicator
RTC	Real-Time Clock
SDK	Software Development Kit
SMA	SubMiniature version A
SMI	Station Management Interface
SPI	Serial Peripheral Interface
SRAM	Static random-access memory
TBD	To be Defined
THT	Through-hole Technology
UART	Universal Asynchronous Receiver-Transmitter
ULP	Ultra-low-power
UTC	Coordinated Universal Time

Table 7: Explanation of the abbreviations and terms used

Related documents

[1] u-connectXpress AT commands manual, UBX-14044127
[2] NINA-W13 series data sheet, UBX-17006694
[3] NINA-W10 series data sheet, UBX-17065507
[4] NINA-W15 series data sheet, UBX-18006647
[5] u-blox Package Information Guide, UBX-14001652
[6] u-connectXpress user guide, UBX-16024251
[7] EVK-NINA-W1/EVK-NINA-B2 user guide, UBX-17011007
[8] Expressif SDK Get Started
[9] s-center user guide, UBX-16012261
[10] u-connectXpress SPI peripheral protocol specification, UBX-20028725
[11] u-connectXpress bootloader protocol specification, UBX-17065404
[12] Espressif ESP32 Datasheet, v3.4
[13] Espressif ESP32 Technical reference manual, v4.3
[14] Espressif ESP32 Hardware design guidelines, v3.0

☞ For regular updates to u-blox documentation and to receive product change notifications, register on our homepage (www.u-blox.com).

Revision history

Revision	Date	Name	Comments
R01	23-Mar-2017	fbro	Initial release.
R02	30-Jun-2017	mwej, cmag	Updated the product status to Engineering Sample. Added info about band pass filter. Updated best conducted Wi-Fi sensitivity to -96 dBm (section 1.3.1). Added additional information about software update (sections 2.3 and 2.5). Removed disclosure restriction.
R03	17-Oct-2017	cmag, kgom, mwej	Modified the software version to 1.0.0 for NINA-W13 series in the table on page 2. Included information about the open CPU variants – NINA-W101 and NINA-W102. Updated section 1 and classified the information for NINA-W13 series and NINA-W10 series separately. Updated Software section (section 2) with more information about NINA-W13 and NINA-W10 software updates. Updated Block diagrams. Included reference to NINA-W101 and NINA-W102 modules in section 3. Minor changes in section 3.2.2.
R04	5-Mar-2018	ajah, mhan, cmag, kgom	Updated the product status to Initial Production. Modified the product description (section 1.3) and information about Boot strapping pins (section 1.6.1). Added output power configuration (section 2.9). Updates Approvals (section 5). Updated Production test (section 6.1) with test and calibration information. Provided reference to NINA-W10 series data sheet in the Related documents section.
R05	20-Apr-2018	cmag, kgom	Updated type numbers and u-connectXpress version in the second table on page 2 with NINA-W13x-00B-01 and 1.0.1 respectively. Updated the Wi-Fi output power configuration for NINA-W10 series (section 2.9.1.1).
R06	6-Dec-2018	mwej, fbro	Added support for NINA-W15 in many sections. Added support for RMII. Removed LPO clock support for NINA-W13 and NINA-W15.
R07	18-Dec-2018	fbro, kgom	Modified the product status to Initial Production for NINA-W131-01B-00 and NINA-W132-01B-00. Updated Bluetooth power (section 2.9).
R08	12-Jul-2019	fbro, flun, kgom	Updated the product status for NINA_W15x to Initial Production. In section 1.1, removed the footnote related to pending modular approvals. Updated soldering profile (Table 6). Updated Wi-Fi output power configuration for NINA-W10 series (section 2.9.1). Minor corrections in section 2.7.2.
R09	25-May-2020	Mlju, hekf	Updated Applicable Products section and added NINA-W106 and W156 modules. Revised software sections 2.1 and 2.2. Introduced the design-in of W1x6 in section 3.3.3.2. Updated ESD Table 5. Added u-connect and s-center user guide references [7] [8].
R10	15-Jul-2020	flun	Clarified chapter 2.5 with regards to ESP-IDF v3 and ESP-IDF v4: Added chapter 2.5.5 noting CONFIG_SPI_FLASH_USE_LEGACY_IMPL must be set to Y if using ESP-IDF 4.0 for NINA-W101/102. and that on NINA-W106, CONFIG_SPI_FLASH_SUPPORT_ISSI_CHIP and CONFIG_BOOTLOADER_VDDSDIO_BOOST_1_9V must be set to Y, and it may be required to add the `--no-stub` parameter to esptool.py during programming. Added ESP IDF 4.0 output power configuration to chapter 2.7.1. Modified the product status to Prototype for NINA-W106. Updated glossary.
R11	30-Sep-2020	flun	Added SPI in section 1.7.3. Updated boot strapping pins in section 1.6.1, and clarified RTS/CTS pins in section 1.7.1. Clarified software update requirements in section 2. Updated the Glossary, Document information and Related documents.

Revision	Date	Name	Comments
R12	18-Dec-2020	flun	Upgraded document status for NINA-W106 to Early Production Information in Applicable products Clarified ethernet startup precautions in section 1.7.2. Clarified the need for 4.7 kΩ pull up to RMII_CRSDV and 10 Ω series resistors for all RMII/SMI pins in section 1.7.2 and 3.4.2. Added section 1.4.2 on low power modes with LPO. Added SPI for NINA-W13 to figure 1.
R13	4-Feb-2021	flun	Updated document to Advanced information for NINA-W156. Clarified LPO in section 1.4.2.

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