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U\_DDR3-RAM  
DDR3-RAM.SchDoc

U\_Ethernet  
Ethernet.SchDoc

U\_USB-PHY  
USB-PHY.SchDoc

U\_SOC  
SOC.SchDoc

U\_CPLD  
CPLD.SchDoc

U\_POWER2  
POWER2.SchDoc

U\_HyperFlash\_RAM  
HyperFlash\_RAM.SchDoc

U\_Clock  
Clock.SchDoc

U\_eMMC  
eMMC.SchDoc

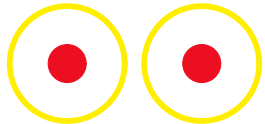
U\_Connectors  
Connectors.SchDoc

U\_POWER  
POWER.SchDoc

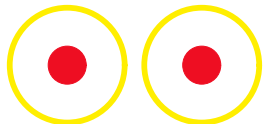
LOGO1

TE Logo PRINT Layer

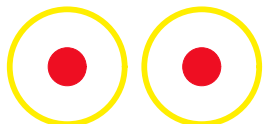
LOGO PRINT



PM1 PM2




PM3 PM4



PM5 PM6

Serial  
Serial  
Serialnumber 6,3 x 6.3mm

		Title: TE0782 - Overview	
		A4	Number: TE0782 TE0782-02-035-2I
Date: 2015-05-27		Copyright: Trenz Electronic GmbH	
Filename: TE0782.SchDoc		Page1 of 31	

1

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A

A

B

B

C

C

D

D

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A

A

U\_HSMC\_CONN\_J1  
HSMC\_CONN\_J1.SchDoc



U\_HSMC\_CONN\_J2  
HSMC\_CONN\_J2.SchDoc



U\_HSMC\_CONN\_J3  
HSMC\_CONN\_J3.SchDoc



B

B

C

C

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D

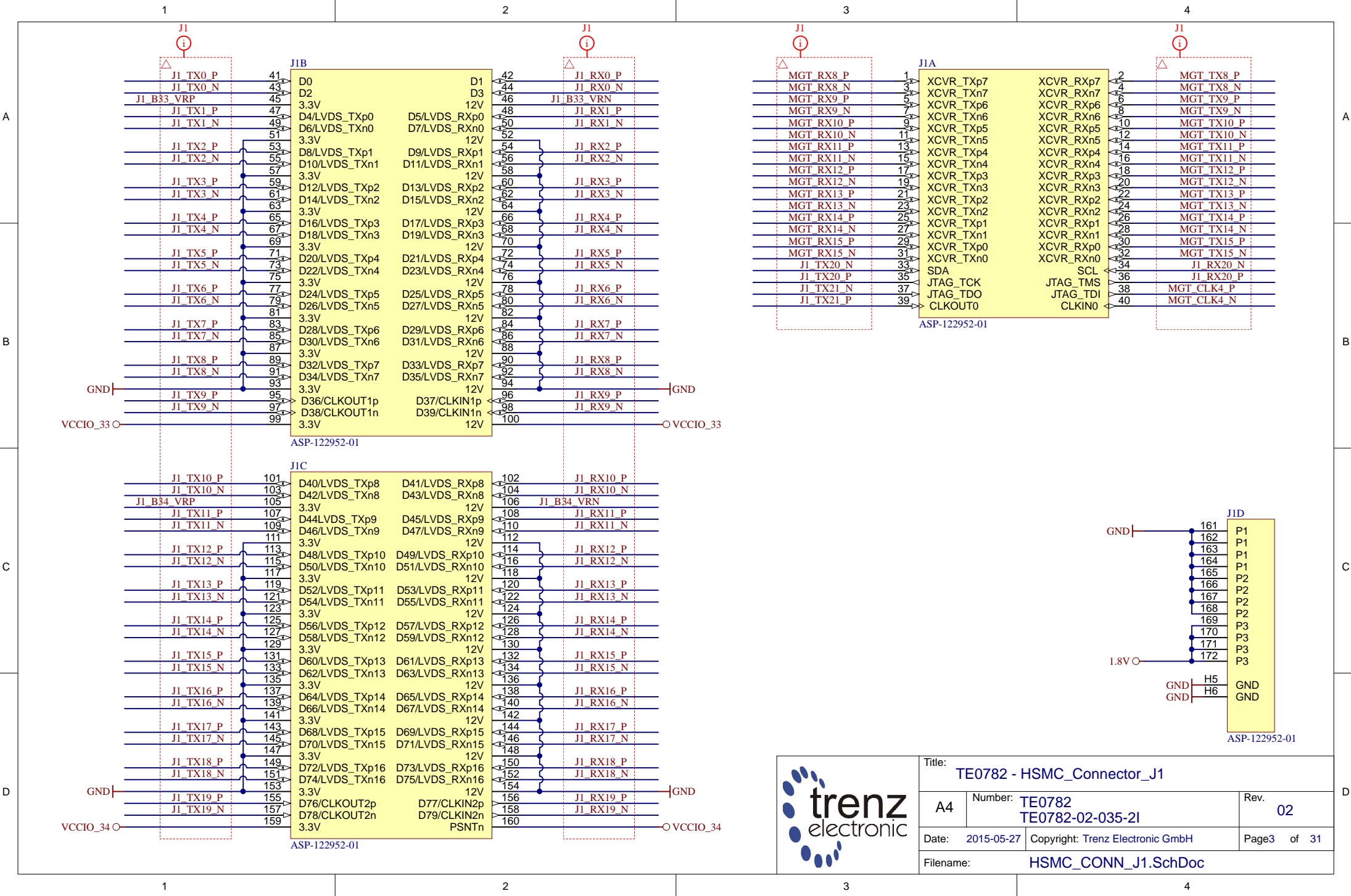
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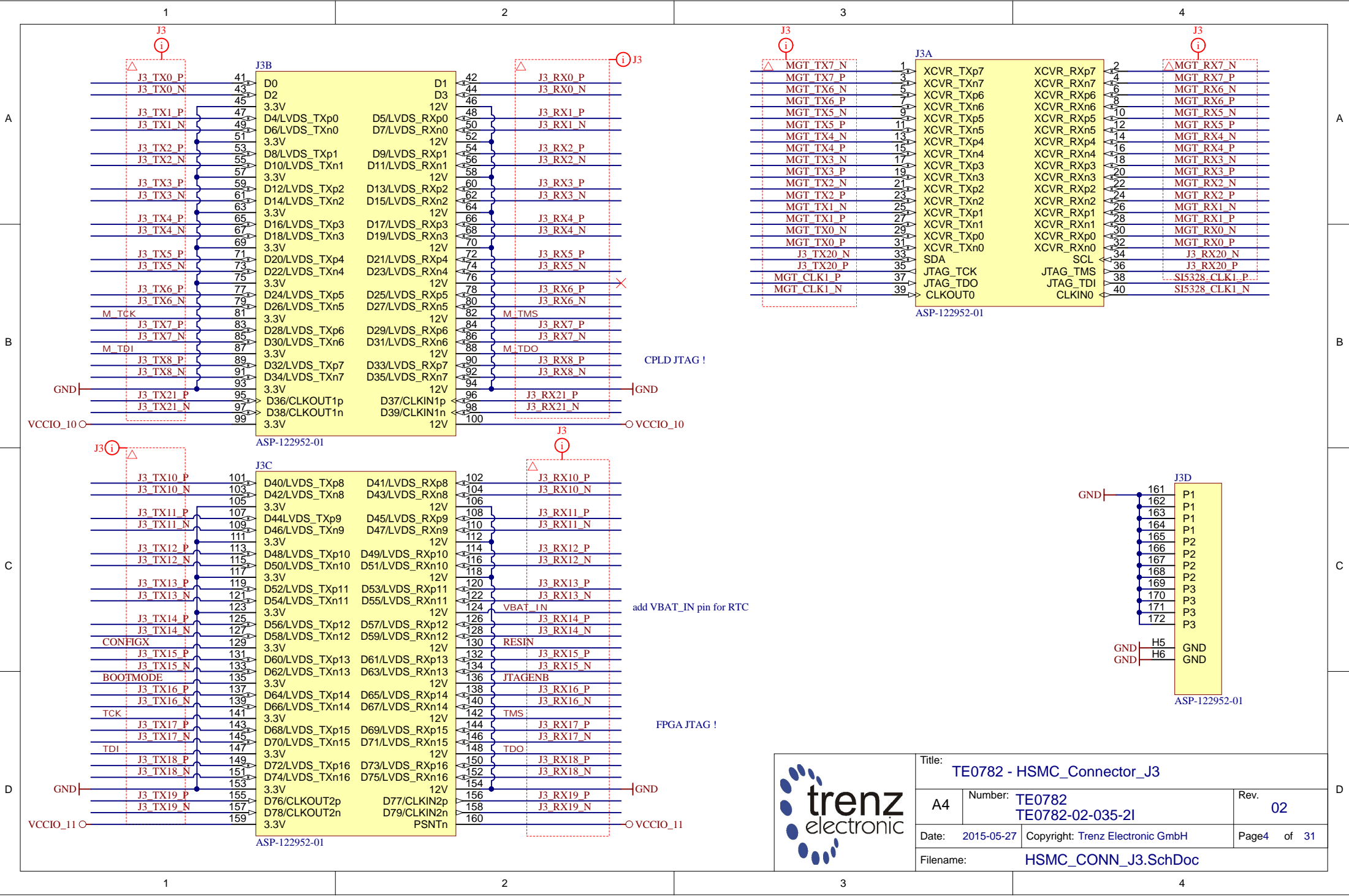
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4

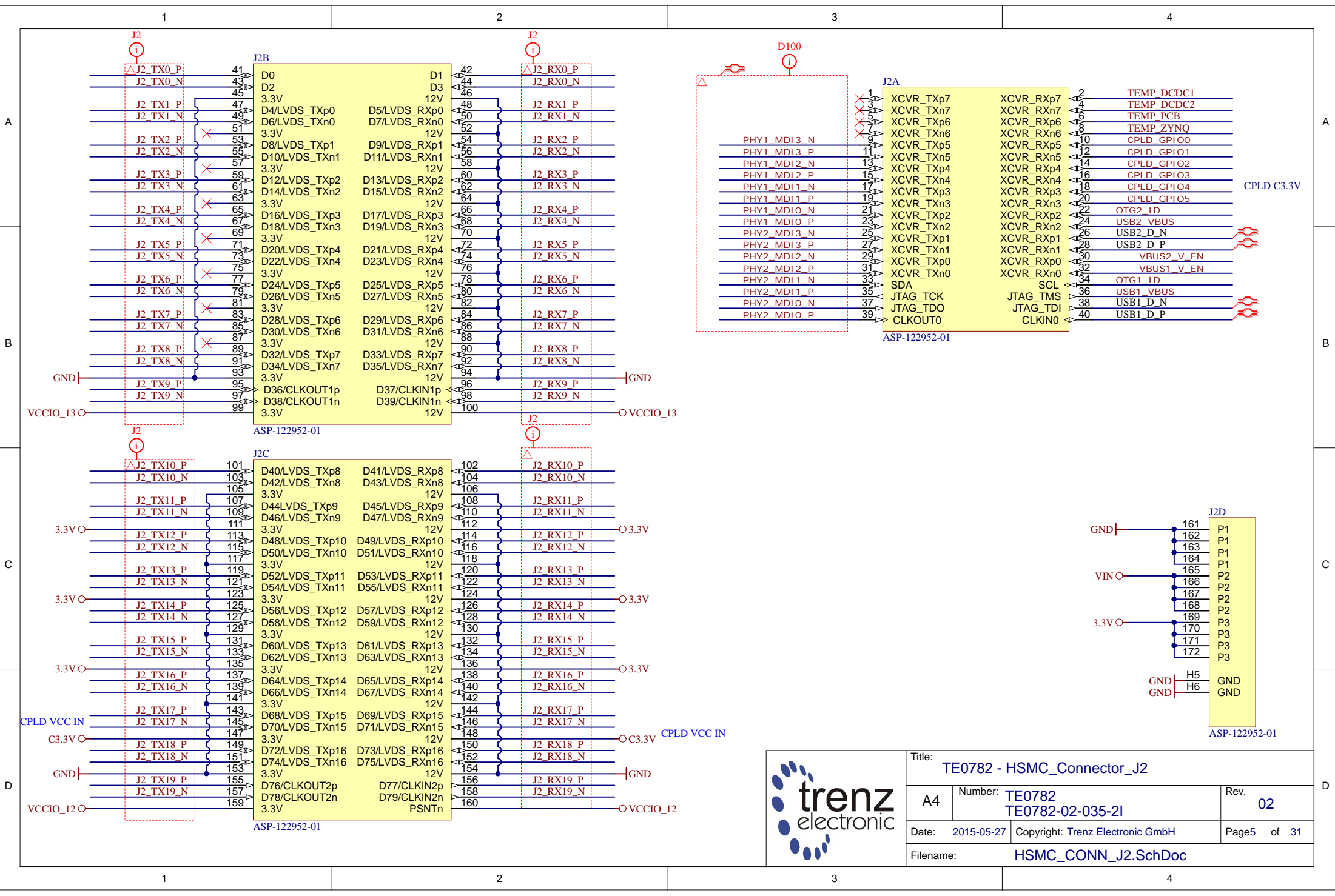
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		A4	Number: <b>TE0782</b> <b>TE0782-02-035-2I</b>
Date: <b>2015-05-27</b>		Copyright: <b>Trenz Electronic GmbH</b>	
Filename: <b>Connectors.SchDoc</b>		Page <b>2</b> of <b>31</b>	



Title: TE0782 - HSMC_Connector_J1		
A4	Number: TE0782 TE0782-02-035-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page3 of 31
Filename: HSMC_CONN_J1.SchDoc		



Title: TE0782 - HSMC_Connector_J3		
A4	Number: TE0782 TE0782-02-035-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page4 of 31
Filename: HSMC_CONN_J3.SchDoc		



Title: <b>TE0782 - HSMC_Connector_J2</b>		
A4	Number: <b>TE0782 TE0782-02-035-21</b>	Rev. <b>02</b>
Date: <b>2015-05-27</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>5</b> of <b>31</b>
Filename: <b>HSMC_CONN_J2.SchDoc</b>		

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A

A

U\_PS-DDR  
PS-DDR.SchDoc



U\_B9  
B9.SchDoc



U\_MIO-BANKS  
MIO-BANKS.SchDoc



U\_B10  
B10.SchDoc



U\_HP-BANKS  
HP-BANKS.SchDoc



U\_B11  
B11.SchDoc



B

B

U\_FPGA-MGT  
FPGA-MGT.SchDoc



U\_B12  
B12.SchDoc



U\_FPGA-CFG  
FPGA-CFG.SchDoc



U\_B13  
B13.SchDoc



C

C

U\_FPGA-PWR  
FPGA-PWR.SchDoc



D

D



Title: <b>TE0782 - SOC</b>		
A4	Number: <b>TE0782 TE0782-02-035-2I</b>	Rev. <b>02</b>
Date: <b>2015-05-27</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>6</b> of <b>31</b>
Filename: <b>SOC.SchDoc</b>		

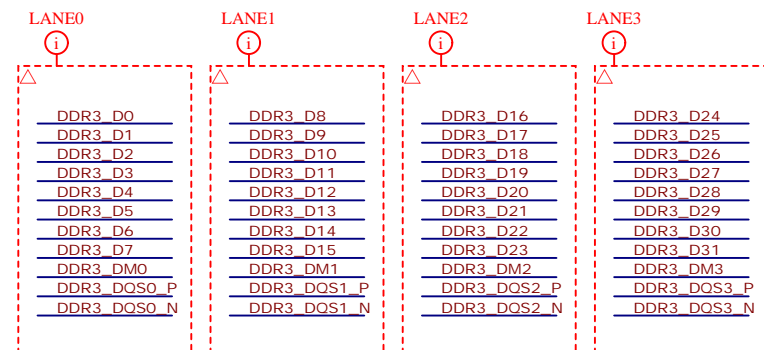
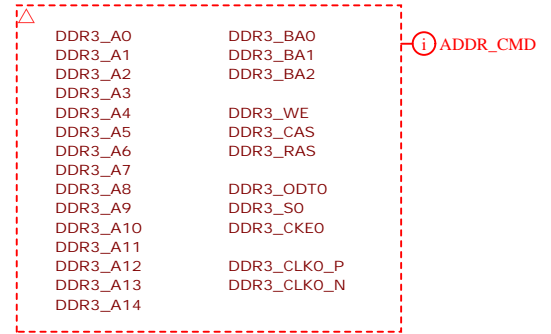
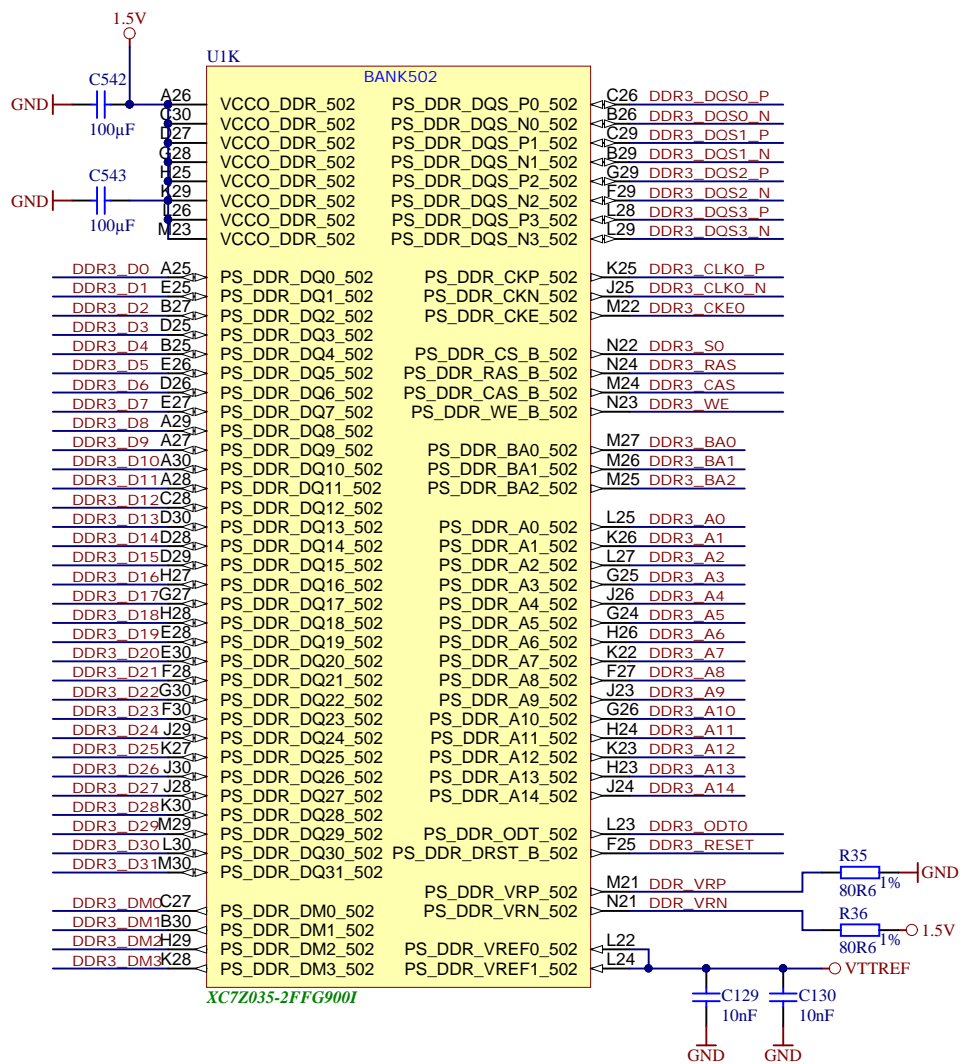
1

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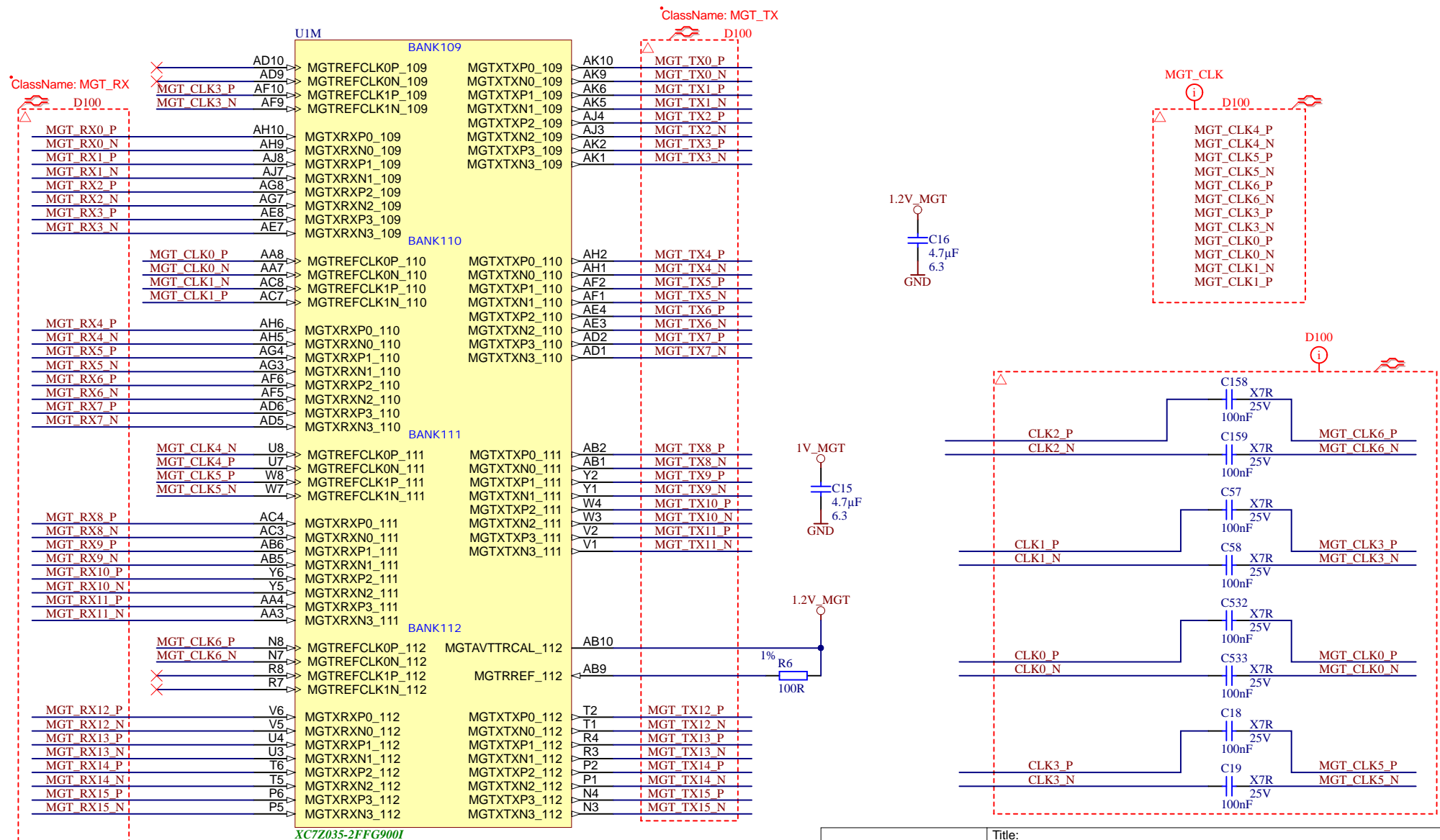
4





Title: TE0782 - FPGA DDR Banks		
A4	Number: TE0782 TE0782-02-035-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 8 of 31
Filename: PS-DDR.SchDoc		





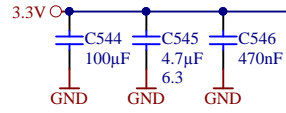
XC7Z035-2FFG900I



Title: <b>TE0782 - FPGA MGT</b>		
A4	Number: <b>TE0782 TE0782-02-035-2I</b>	Rev. <b>02</b>
Date: <b>2015-05-27</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>9</b> of <b>31</b>
Filename: <b>FPGA-MGT.SchDoc</b>		

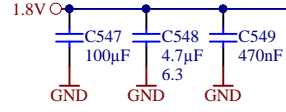
U1J BANK500 & 501

SPI and JTAG modes supported  
Cascade and independent modes supported

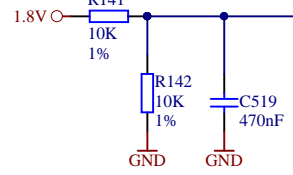


PS\_CLK A22

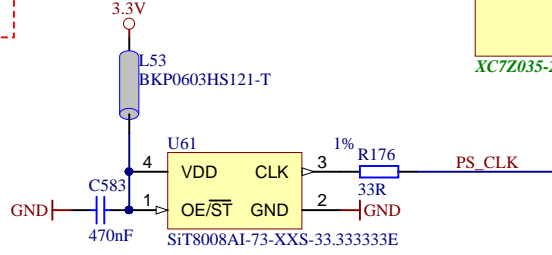
PS\_POR D21



PS\_SRST B19

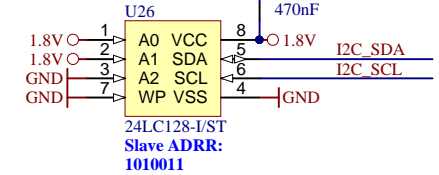


- B500**  
 ⓘ **ClassName: PKG**  
 ⓘ **ClassName: B500**
- SPI\_CS
  - SPI\_DQ0/MIO2
  - SPI\_DQ1/MIO3
  - SPI\_DQ2/MIO4
  - SPI\_DQ3/MIO5
  - SPI\_SCK/MIO6
  - MMC-DO
  - MMC-CMD
  - MMC-CCLK
  - MMC-D1
  - MMC-D2
  - MMC-D3

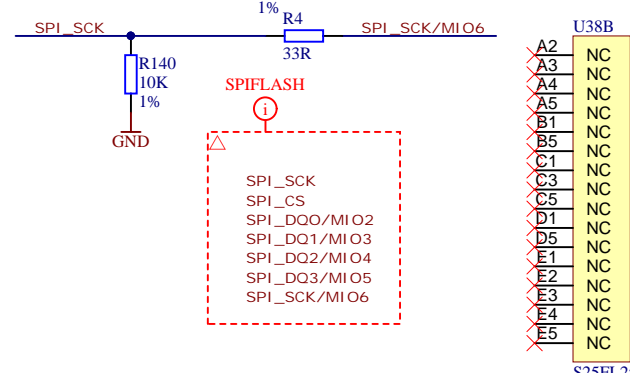
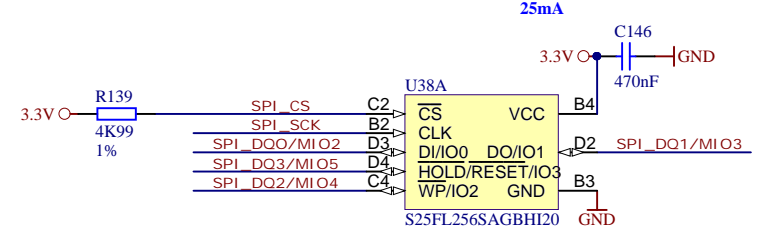


XC7Z035-2FFG9001

- F24 OTG-RST33
- D23 SPI\_CS
- F23 SPI\_DQ0/MIO2
- C23 SPI\_DQ1/MIO3 R133 10K 1%
- E23 SPI\_DQ2/MIO4
- C24 SPI\_DQ3/MIO5 R135 10K 1%
- D24 SPI\_SCK/MIO6
- B24 ETH1\_RESET33
- C21 MIO8 R137 10K 1%
- A24 MIO9
- E22 MMC-DO
- A23 MMC-CMD
- E21 MMC-CCLK
- F22 MMC-D1
- B22 MMC-D2
- C22 MMC-D3
- L19 ETH1\_TXCK
- K21 ETH1\_TXD0
- K20 ETH1\_TXD1
- J20 ETH1\_TXD2
- M20 ETH1\_TXD3
- J19 ETH1\_TXCTL
- L20 ETH1\_RXCK
- J21 ETH1\_RXD0
- M19 ETH1\_RXD1
- G19 ETH1\_RXD2
- M17 ETH1\_RXD3
- G20 ETH1\_RXCTL
- L17 OTG-DATA4
- H22 OTG-DIR
- L18 OTG-STP
- H21 OTG-NXT
- K17 OTG-DATA0
- G22 OTG-DATA1
- K18 OTG-DATA2
- G21 OTG-DATA3
- H17 OTG-CLK
- B21 OTG-DATA5
- A20 OTG-DATA6
- F18 OTG-DATA7
- B20 OTG2-DATA4
- J18 OTG2-DIR
- D20 OTG2-STP
- E18 OTG2-NXT
- E20 OTG2-DATA0
- H18 OTG2-DATA1
- F20 OTG2-DATA2
- A18 OTG2-DATA3
- C19 OTG2-CLK
- D18 OTG2-DATA5
- A19 OTG2-DATA6
- F19 OTG2-DATA7
- D19 ETH1\_MDC
- C18 ETH1\_MDIO



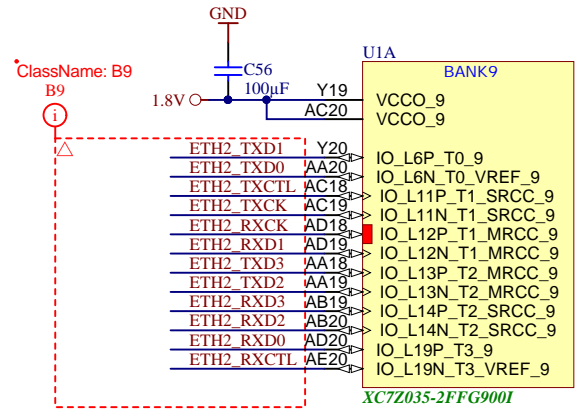
Slave ADDR: 1010011




- B501**  
 ⓘ **ClassName: B501**  
 ⓘ **ClassName: PKG**



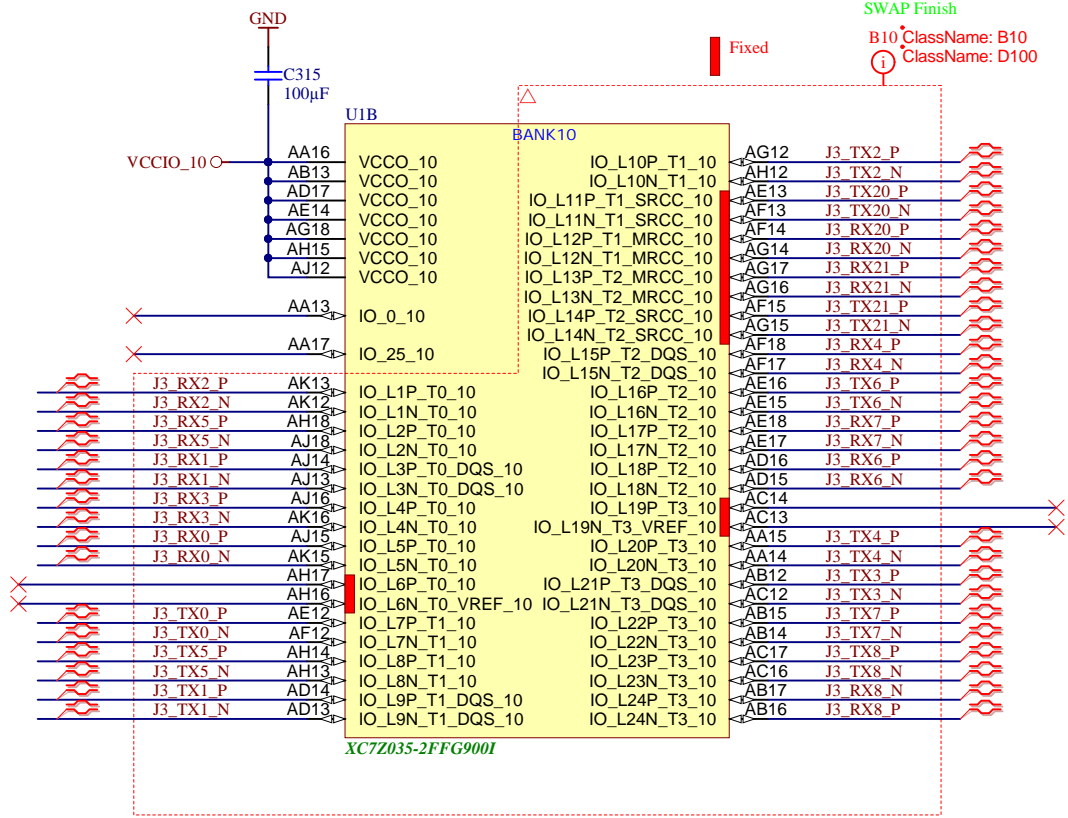
Title: TE0782 - FPGA MIO Banks		
A4	Number: TE0782 TE0782-02-035-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 10 of 31
Filename: MIO-BANKS.SchDoc		



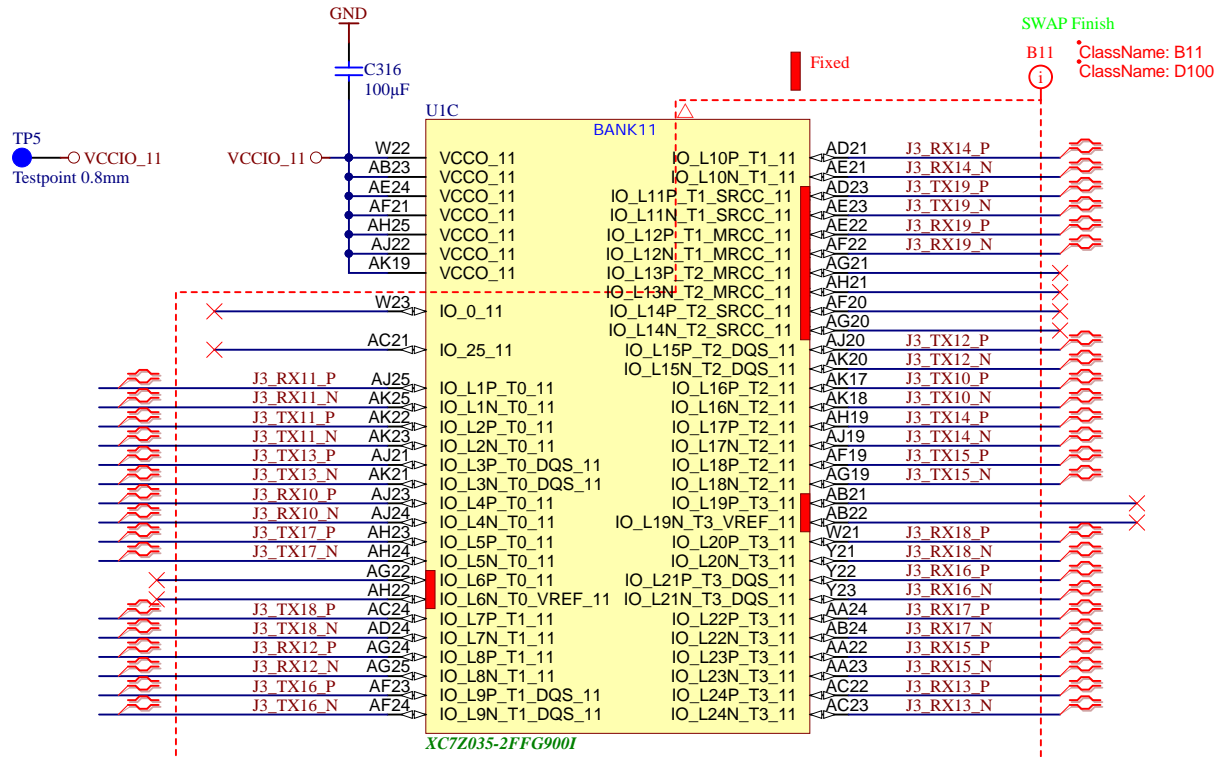
RXCK Fix to MRCCL  
 Fixed


			Title: TE0782 - FPGA B9	
			A4	Number: TE0782 TE0782-02-035-2I
Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page 11 of 31
Filename: B9.SchDoc				


TP4  
 ●—○ VCCIO\_10  
 Testpoint 0.8mm

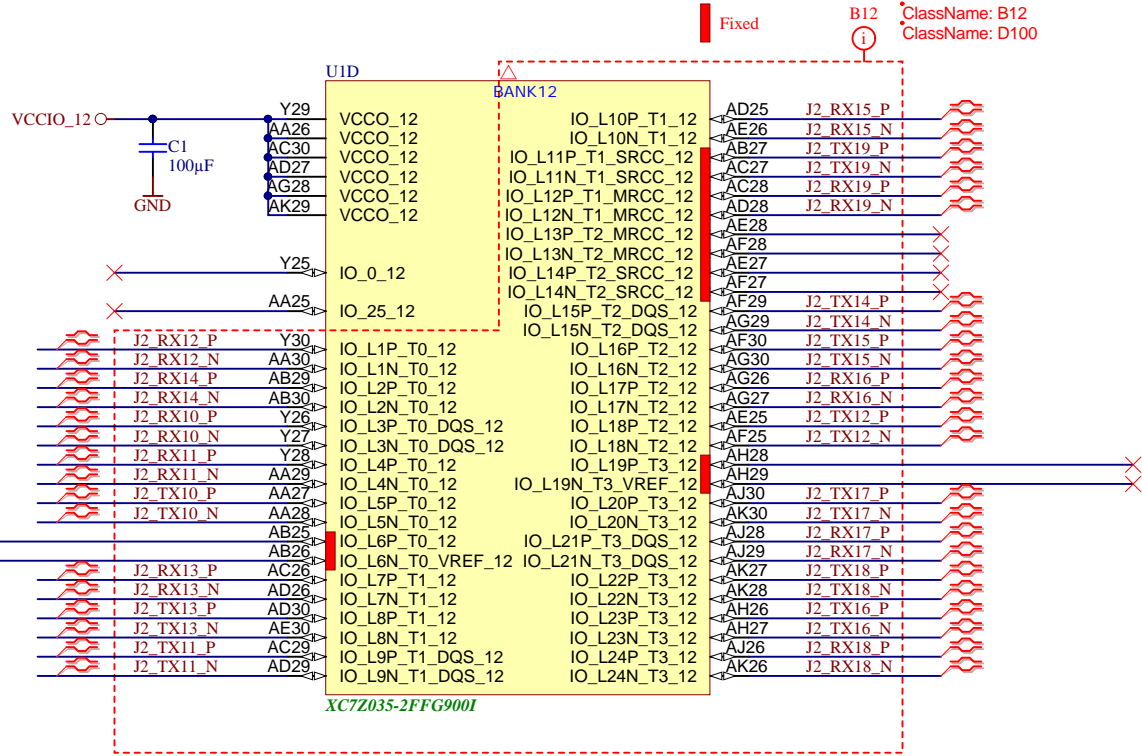


Title: TE0782 - FPGA B10		
A4	Number: TE0782 TE0782-02-035-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 12 of 31
Filename: B10.SchDoc		



	Title: TE0782 - FPGA B11		
	A4	Number: TE0782 TE0782-02-035-2I	Rev. 02
	Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page13 of 31
	Filename: B11.SchDoc		

TP1  
 VCCIO\_12  
 Testpoint 0.8mm



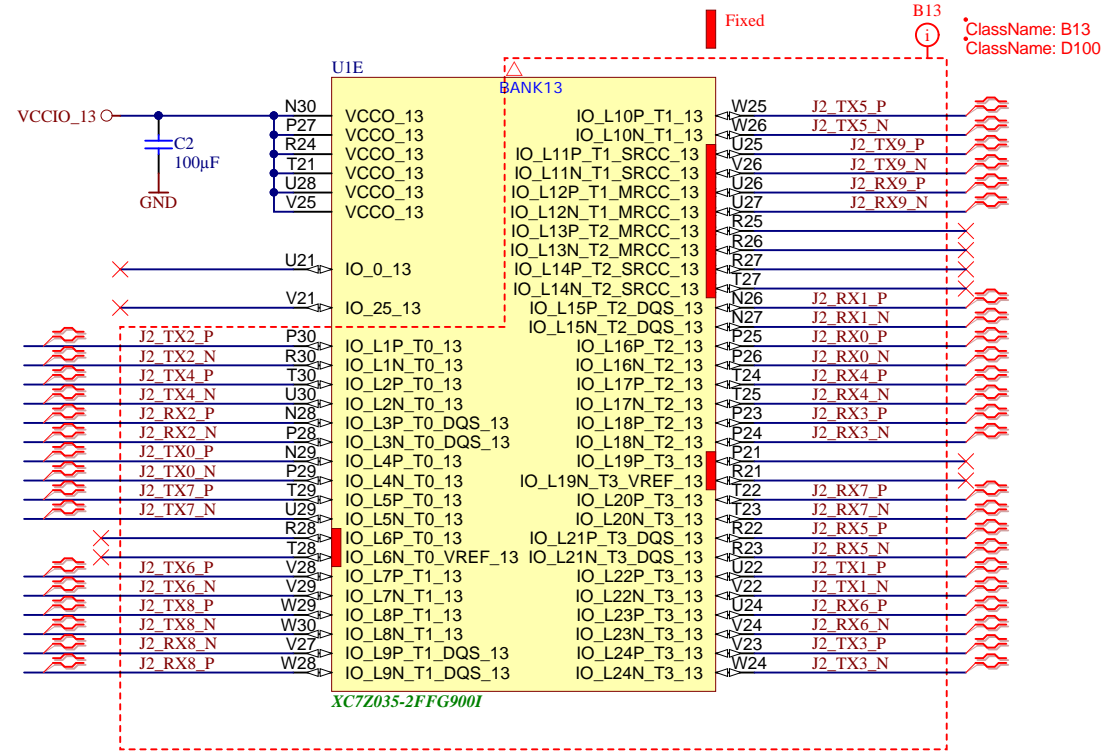
Fixed  
 B12  
 i  
 ClassName: B12  
 ClassName: D100

XC7Z035-2FFG900I



Title: TE0782 - FPGA B12		
A4	Number: TE0782 TE0782-02-035-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 14 of 31
Filename: B12.SchDoc		

TP2  
 ●—○ VCCIO\_13  
 Testpoint 0.8mm



	Title: TE0782 - FPGA B13		
	A4	Number: TE0782 TE0782-02-035-2I	Rev. 02
	Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page15 of 31
	Filename: B13.SchDoc		

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U\_B33  
B33.SchDoc



U\_B34  
B34.SchDoc



U\_B35  
B35.SchDoc



A

A

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C

C

D

D



Title: TES0782 - FPGA HP Banks		
A4	Number: TE0782 TE0782-02-035-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 16 of 31
Filename: HP-BANKS.SchDoc		


1

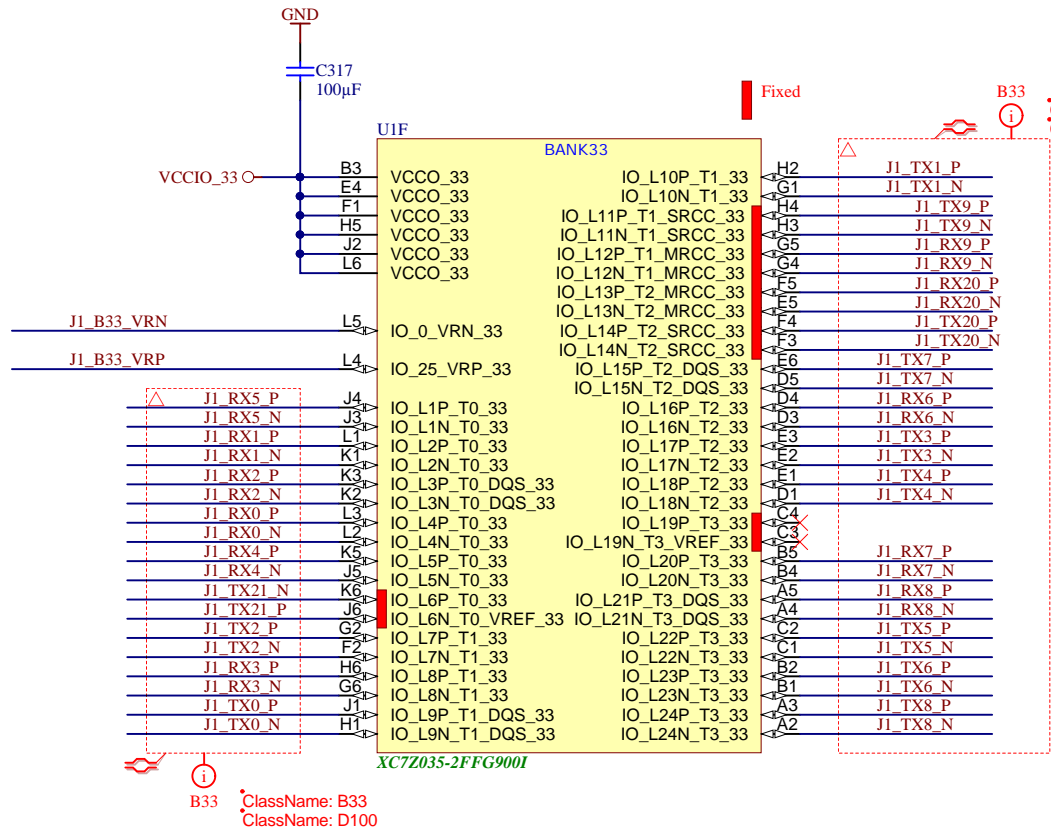
2

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TP6  
 VCCIO\_33  
 Testpoint 0.8mm




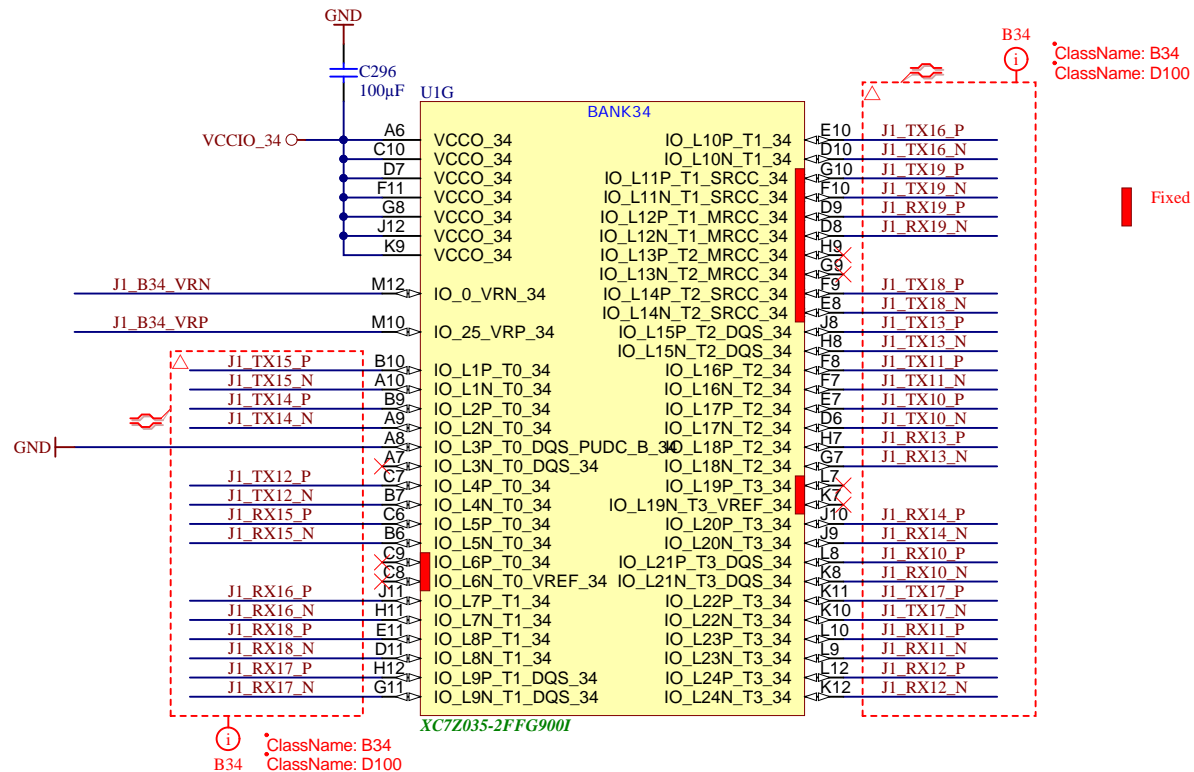
B33  
 ClassName: B33  
 ClassName: D100

B33  
 ClassName: B33  
 ClassName: D100

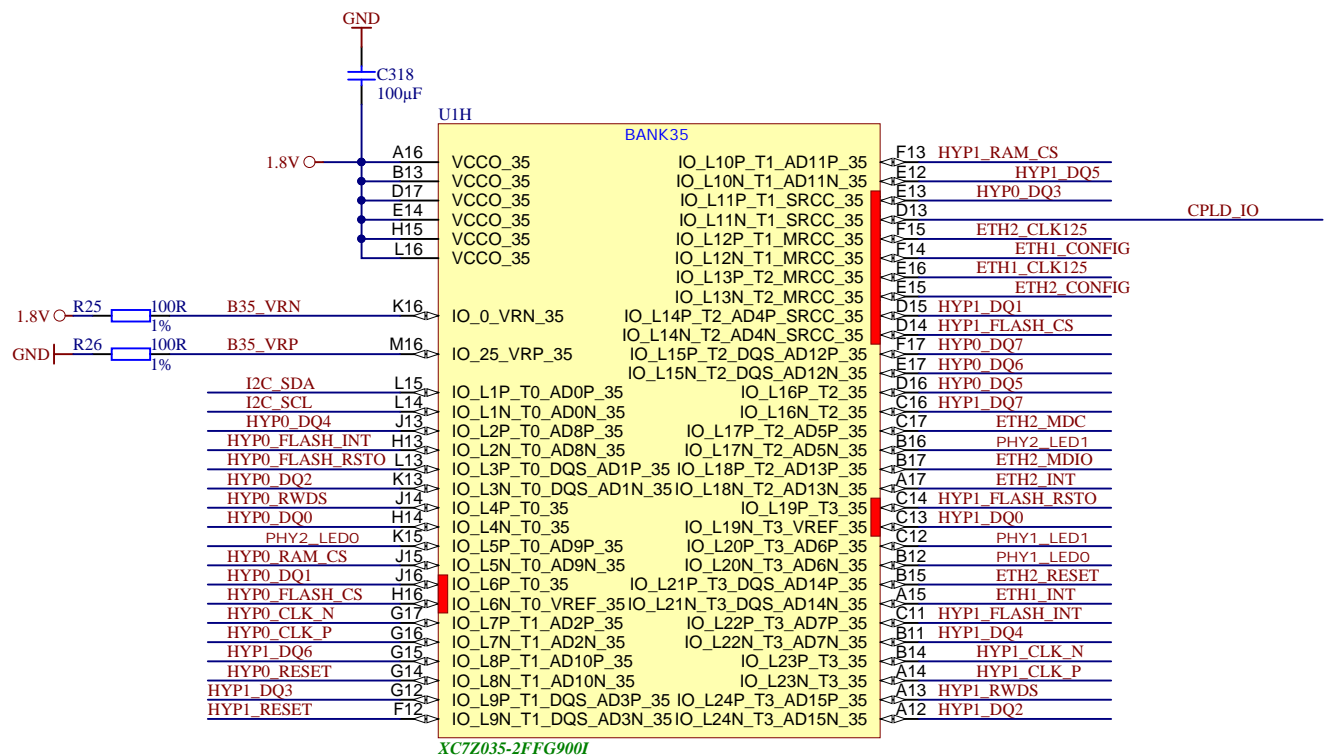


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Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 17 of 31
Filename: B33.SchDoc		

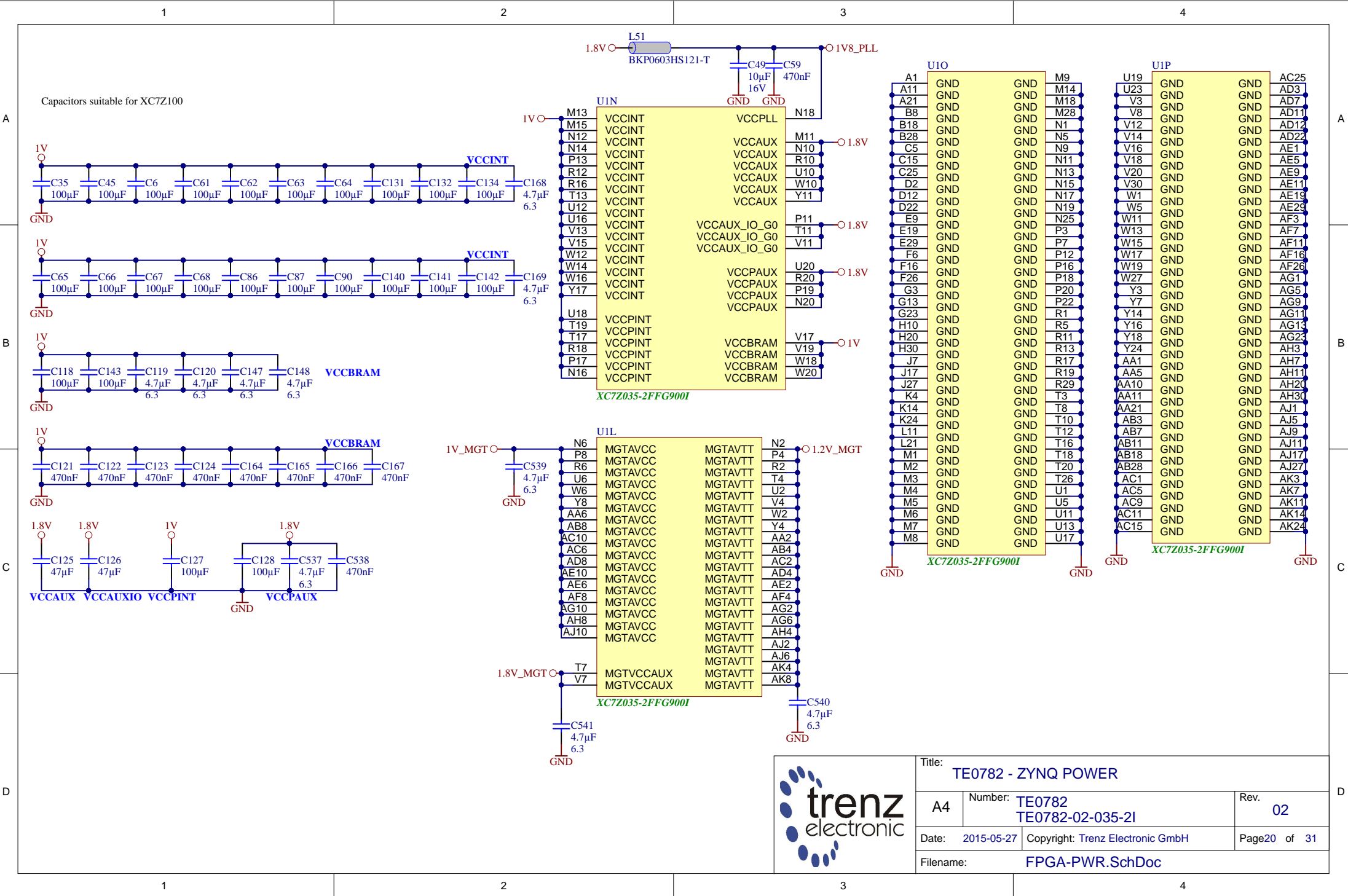

TP3  
 VCCIO\_34  
 Testpoint 0.8mm



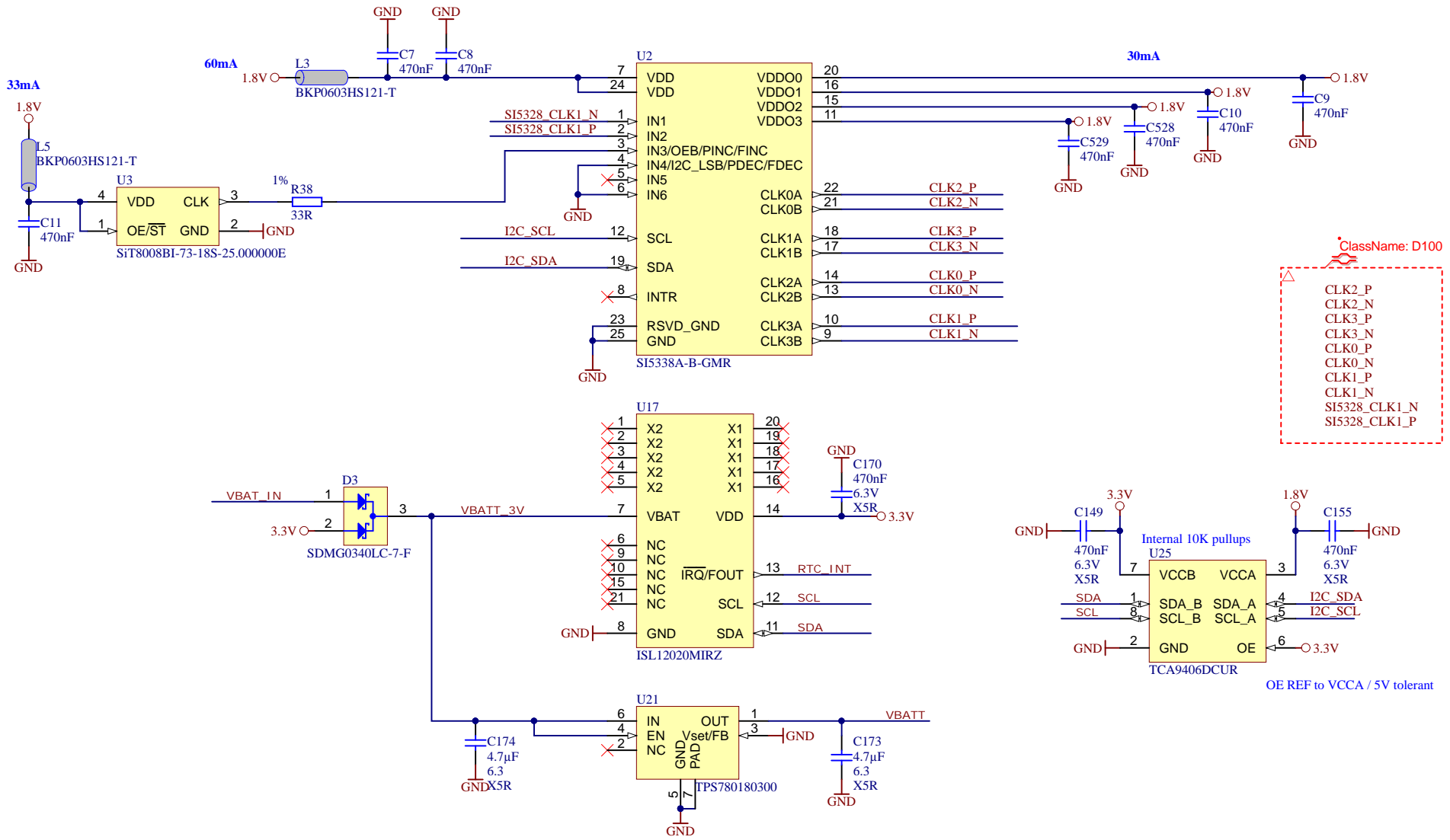
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A4	Number: TE0782 TE0782-02-035-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 18 of 31
Filename: B34.SchDoc		



Title: TE0782 - FPGA B35		
A4	Number: TE0782 TE0782-02-035-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 19 of 31
Filename: B35.SchDoc		

Title: TE0782 - ZYNQ POWER		
A4	Number: TE0782 TE0782-02-035-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page20 of 31
Filename: FPGA-PWR.SchDoc		



ClassName: D100

CLK2\_P  
 CLK2\_N  
 CLK3\_P  
 CLK3\_N  
 CLK0\_P  
 CLK0\_N  
 CLK1\_P  
 CLK1\_N  
 SI5328\_CLK1\_N  
 SI5328\_CLK1\_P

OE REF to VCCA / 5V tolerant



Title: TE0782 - Clock		
A4	Number: TE0782 TE0782-02-035-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page21 of 31
Filename: Clock.SchDoc		

A

B

C

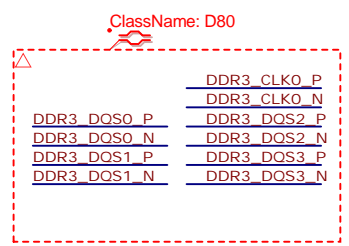
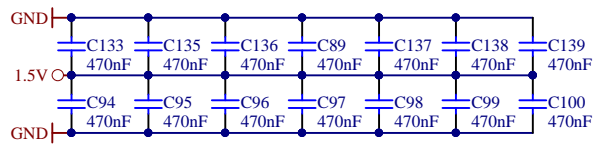
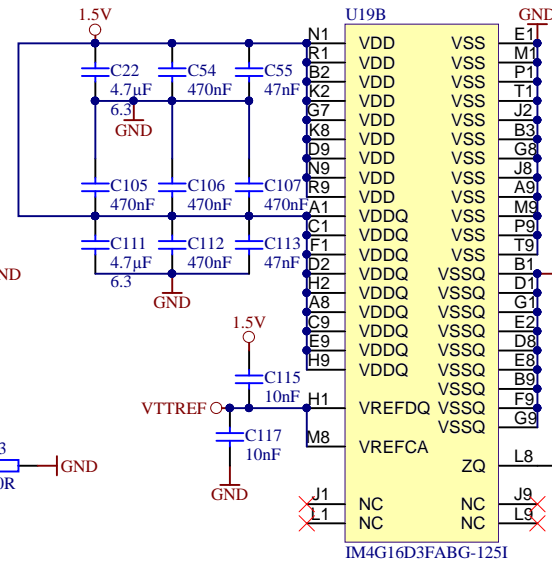
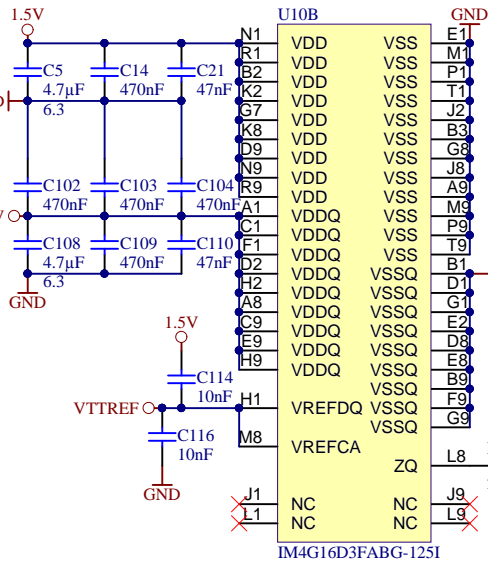
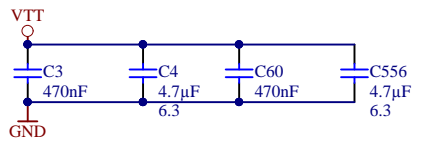
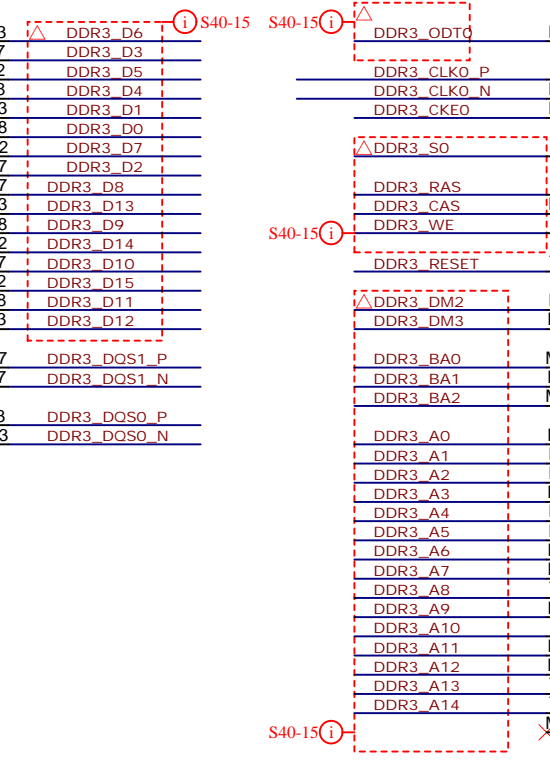
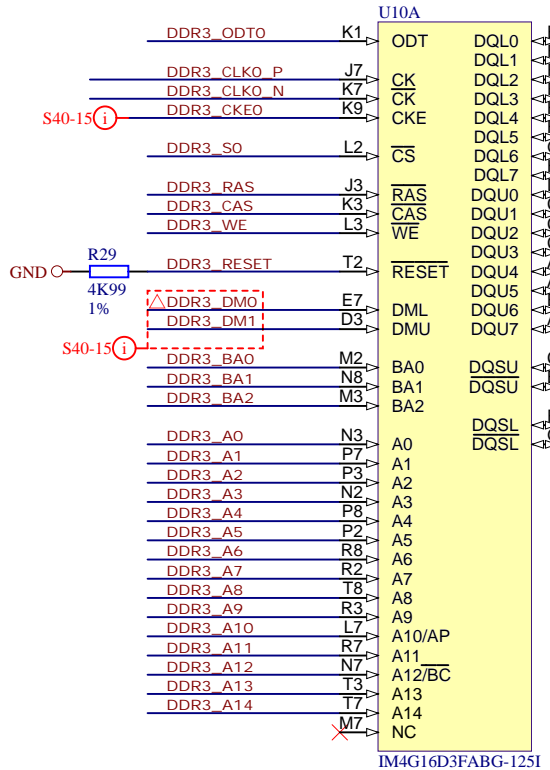
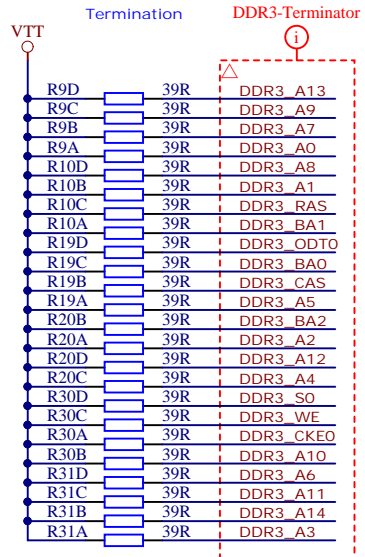
D

A

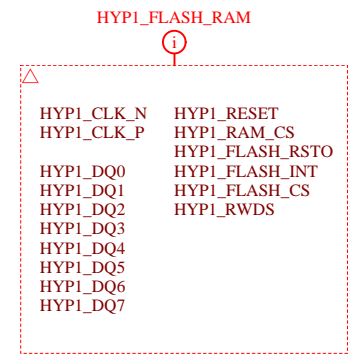
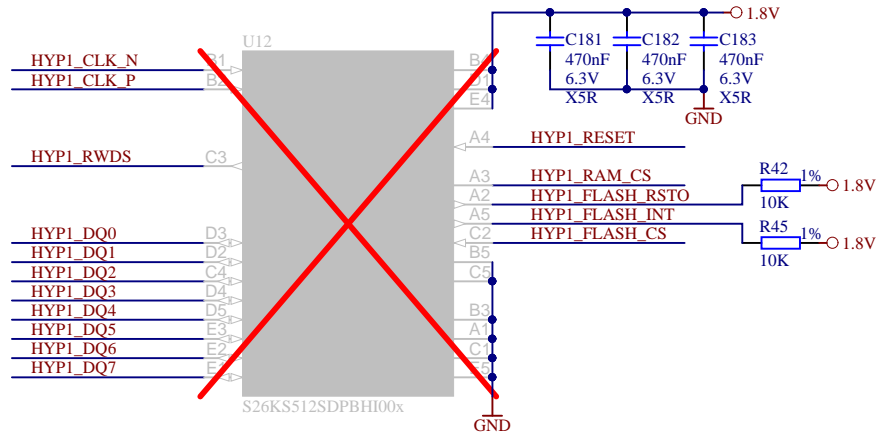
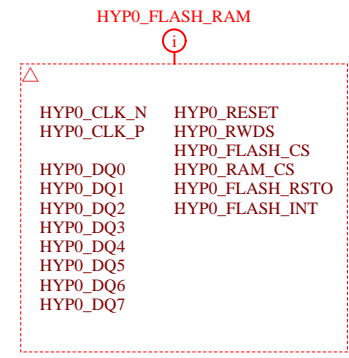
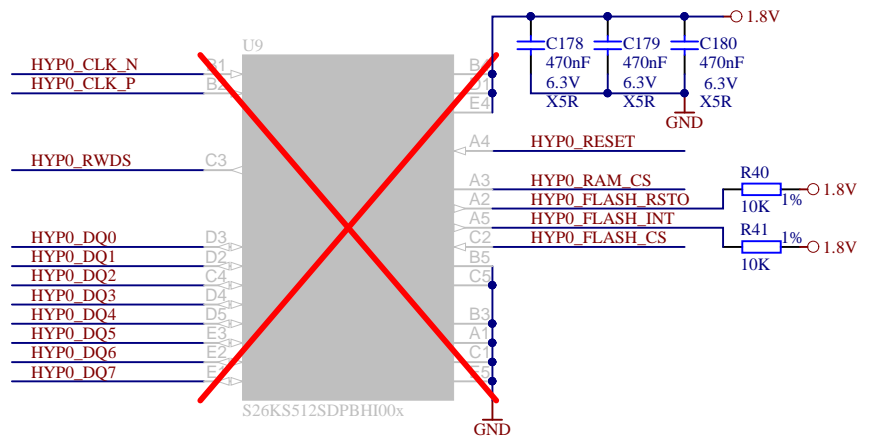
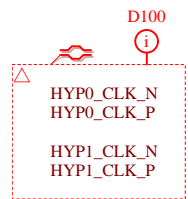
B

C

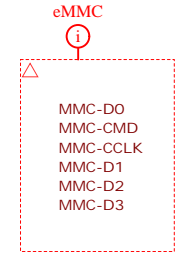
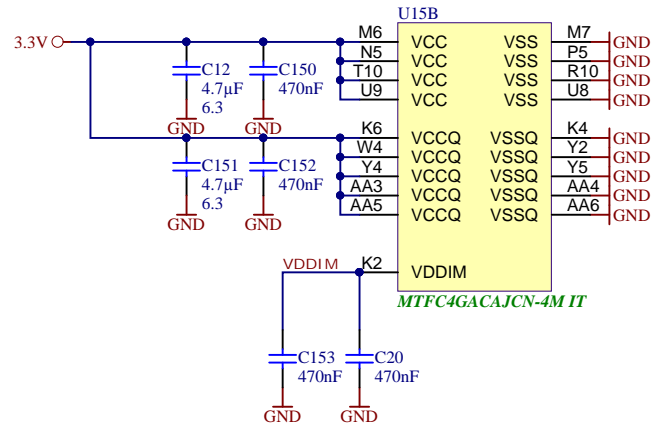
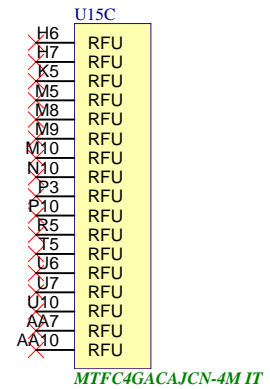
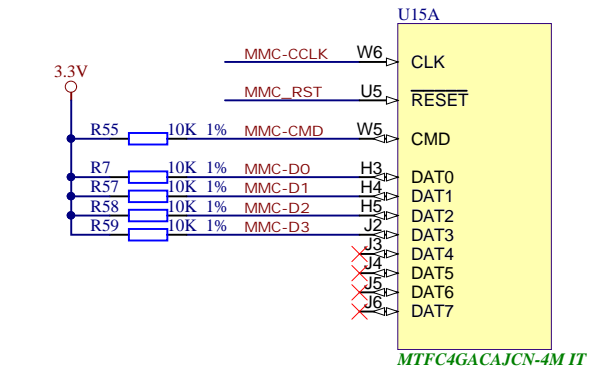
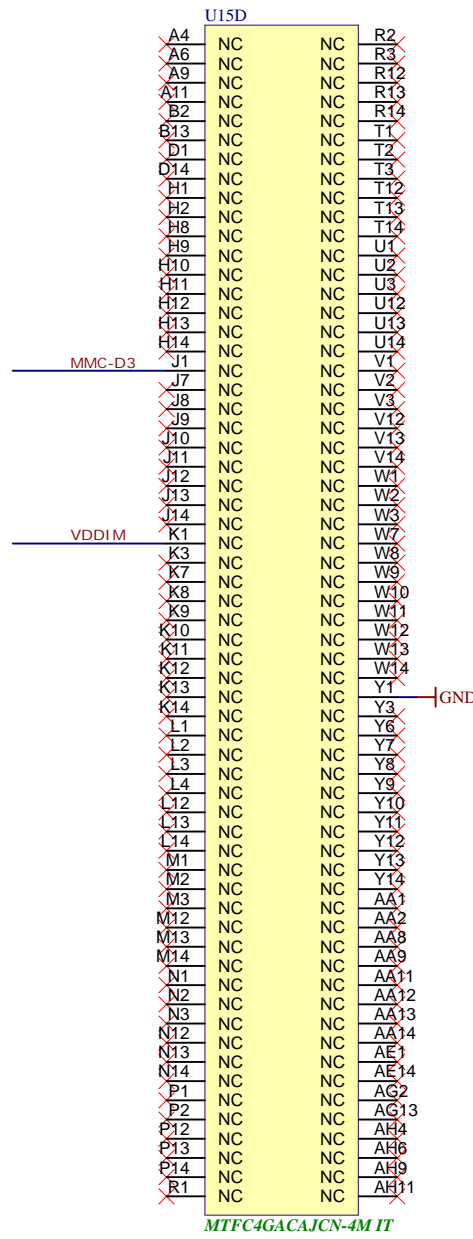
D



Title: <b>TE0782 - DDR3 RAM</b>		
A4	Number: <b>TE0782 TE0782-02-035-21</b>	Rev. <b>02</b>
Date: <b>2015-05-27</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>22</b> of <b>31</b>
Filename: <b>DDR3-RAM.SchDoc</b>		



Title: TE0782 - HyperFlash_RAM		
A4	Number: TE0782 TE0782-02-035-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page23 of 31
Filename: HyperFlash_RAM.SchDoc		

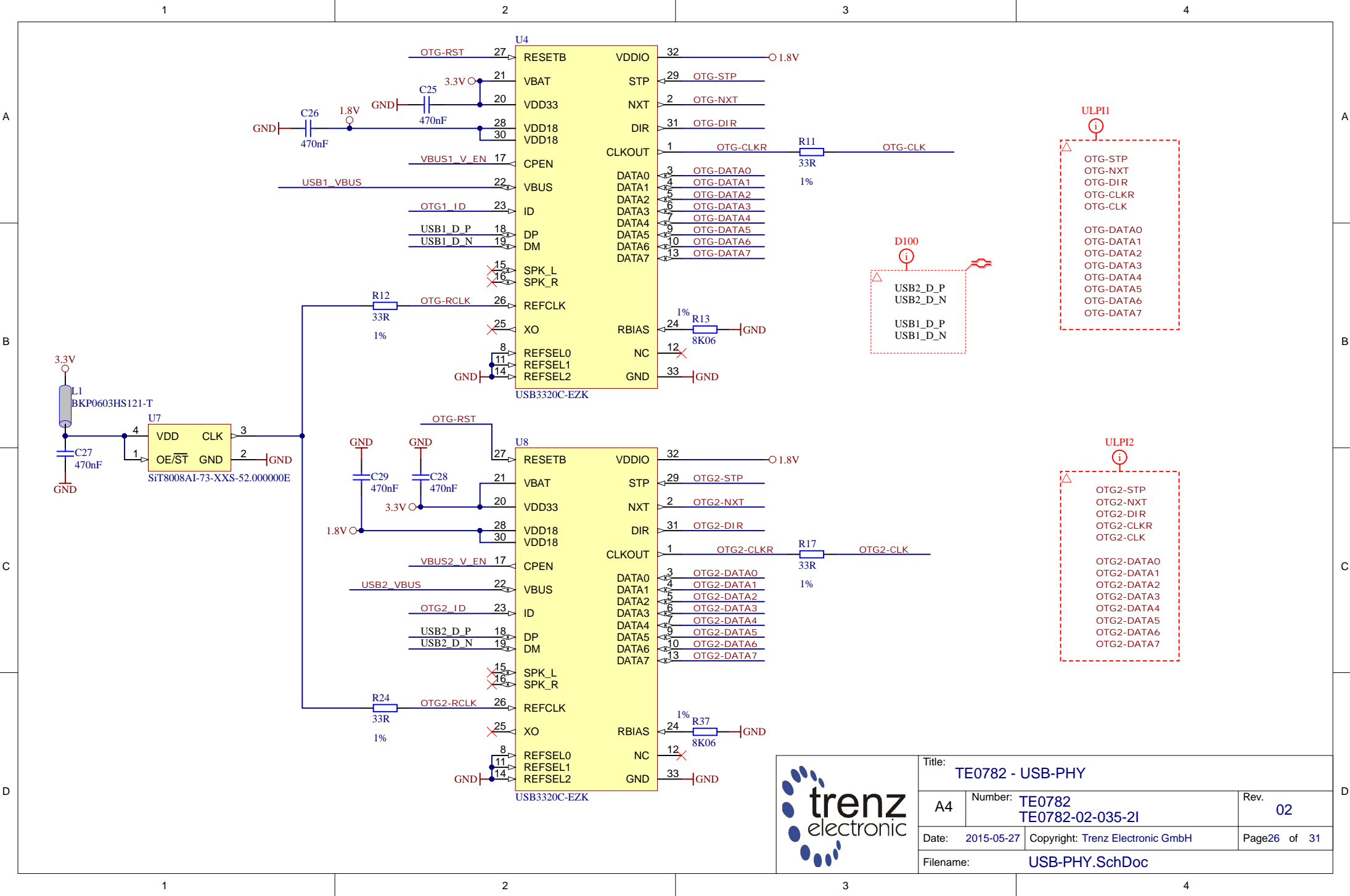



trenz electronic

Title: TE0782 - eMMC		
A4	Number: TE0782 TE0782-02-035-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page24 of 31
Filename: eMMC.SchDoc		







			Title: <b>TE0782 - USB-PHY</b>	
			A4	Number: <b>TE0782 TE0782-02-035-21</b>
Date: <b>2015-05-27</b>		Copyright: <b>Trenz Electronic GmbH</b>		Page <b>26</b> of <b>31</b>
Filename: <b>USB-PHY.SchDoc</b>				

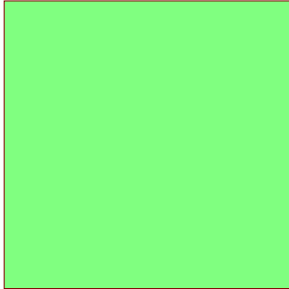
1

2

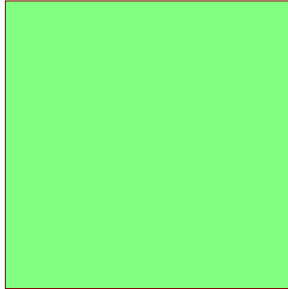
3

4

U\_ETH1  
ETH1.SchDoc



U\_ETH2  
ETH2.SchDoc



A

A

B

B

C

C

D

D



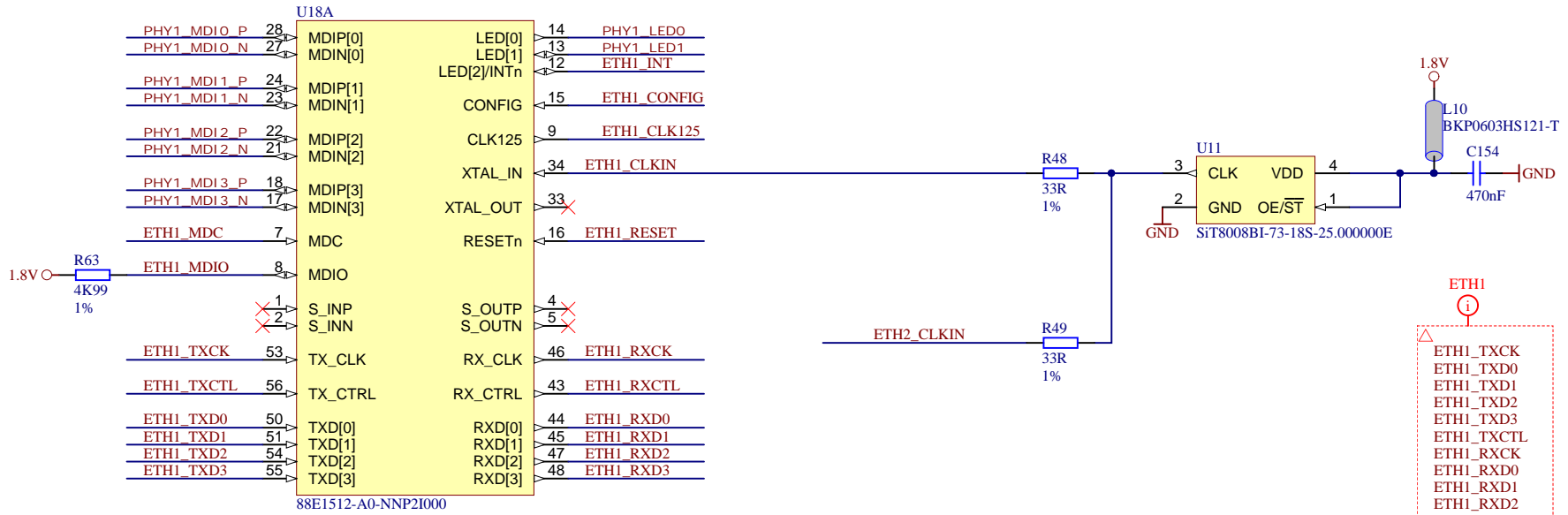
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A4	Number: <b>TE0782 TE0782-02-035-2I</b>	Rev. <b>02</b>
Date: <b>2015-05-27</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>27</b> of <b>31</b>
Filename: <b>Ethernet.SchDoc</b>		

1

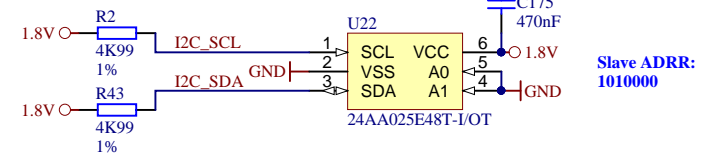
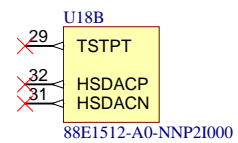
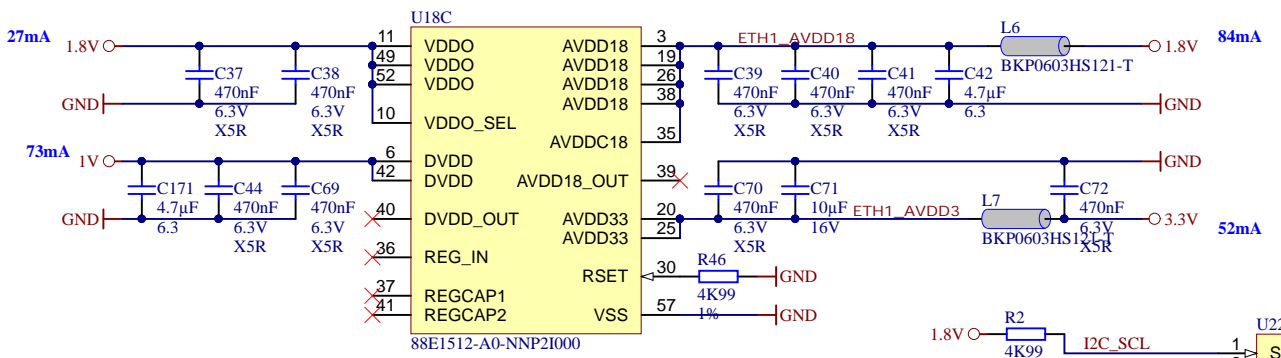
2

3

4



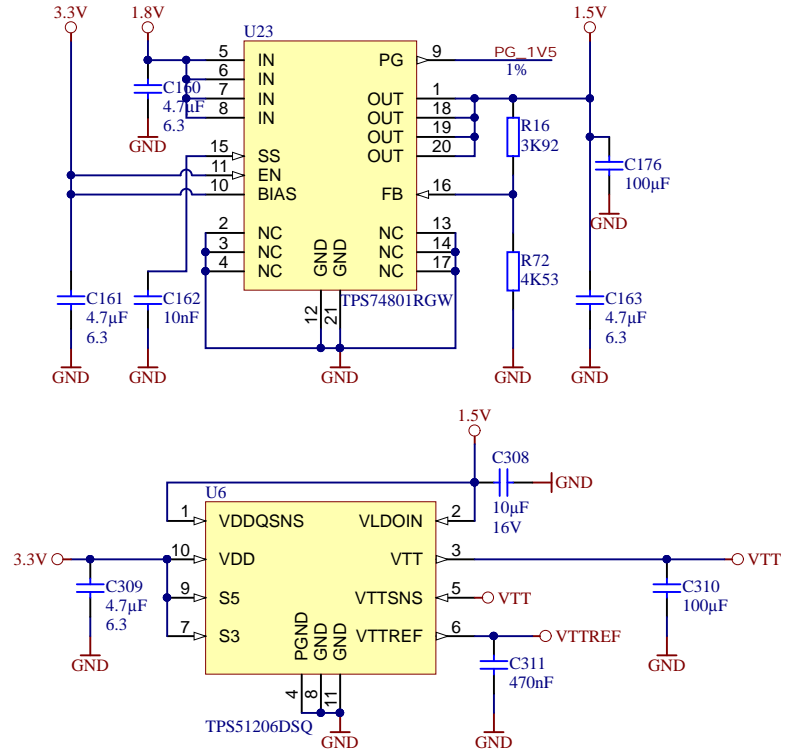
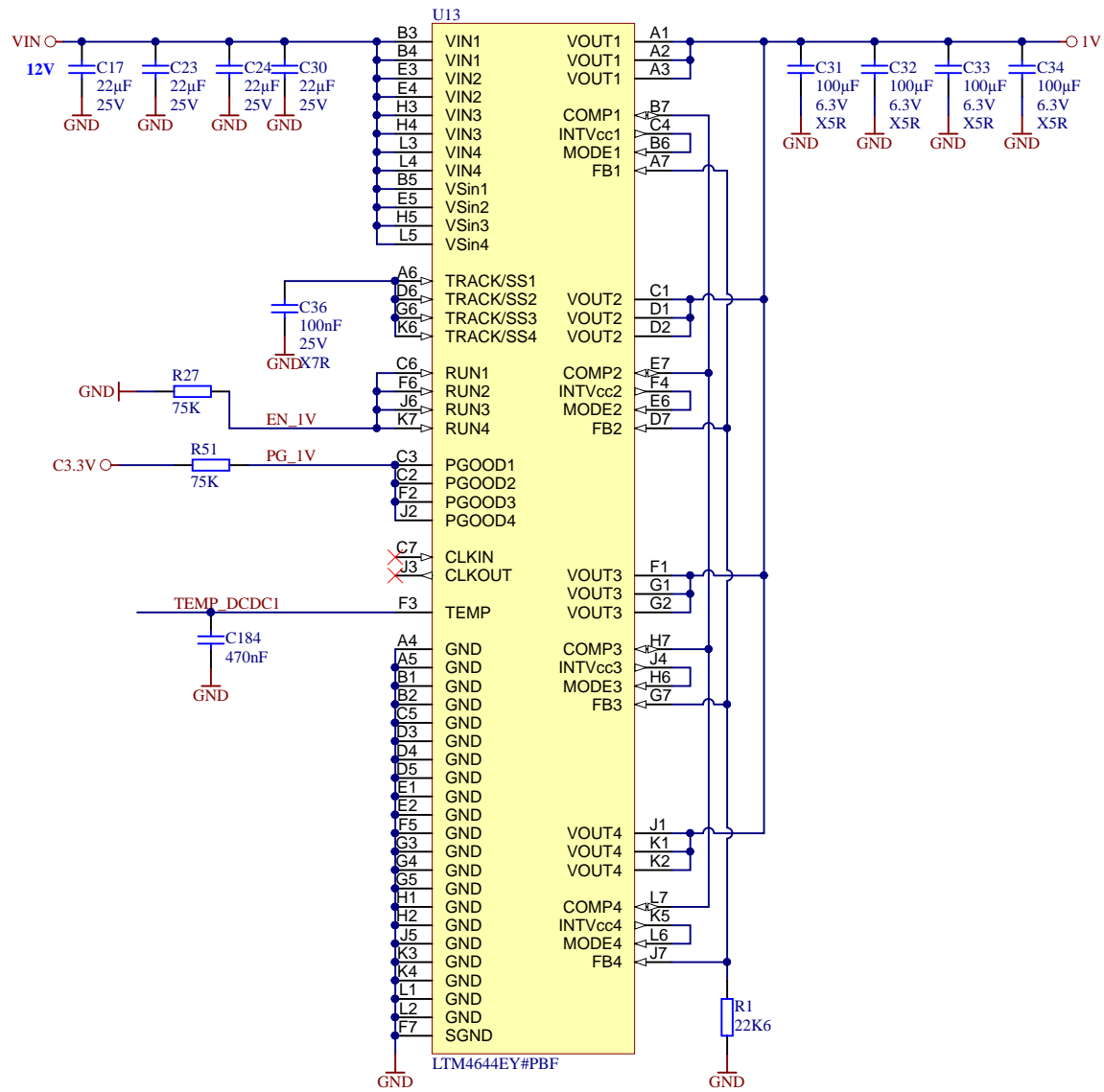
- ETH1**
- ETH1\_TXCK
  - ETH1\_TXD0
  - ETH1\_TXD1
  - ETH1\_TXD2
  - ETH1\_TXD3
  - ETH1\_TXCTL
  - ETH1\_RXCK
  - ETH1\_RXD0
  - ETH1\_RXD1
  - ETH1\_RXD2
  - ETH1\_RXD3
  - ETH1\_RXCTL
  - ETH1\_MDC
  - ETH1\_MDIO
- PHY1\_LED0  
PHY1\_LED1  
ETH1\_INT  
ETH1\_CONFIG  
ETH1\_CLK125  
ETH1\_RESET



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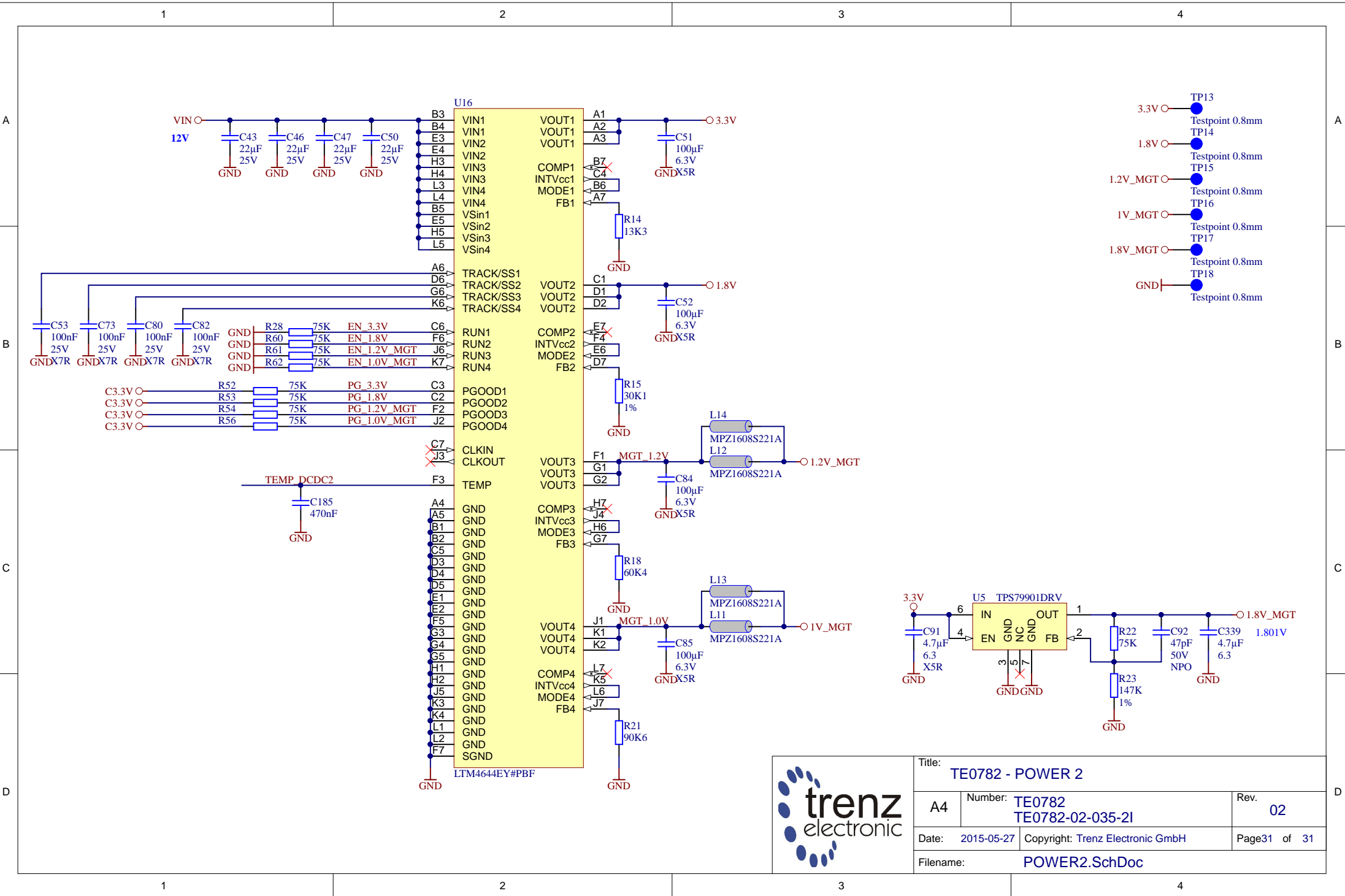
Title: TE0782 - ETH_PHY1		
A4	Number: TE0782 TE0782-02-035-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 28 of 31
Filename: ETH1.SchDoc		





- TP7 1V ○ ● Testpoint 0.8mm
- TP8 GND ○ ● Testpoint 0.8mm
- TP10 1.5V ○ ● Testpoint 0.8mm
- TP11 VTT ○ ● Testpoint 0.8mm
- TP12 VTTREF ○ ● Testpoint 0.8mm

	Title: <b>TE0782 - POWER</b>	
	A4	Number: <b>TE0782 TE0782-02-035-21</b>
	Date: <b>2015-05-27</b>	Copyright: <b>Trenz Electronic GmbH</b>
	Filename: <b>POWER.SchDoc</b>	Page <b>30</b> of <b>31</b>



Title: TE0782 - POWER 2		
A4	Number: TE0782 TE0782-02-035-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 31 of 31
Filename: POWER2.SchDoc		