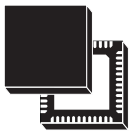
L5965

Datasheet

Power management for automotive vision and radar systems



VFQFPN-48 (7x7 mm)

Features

- AEC-Q100 qualified
- Pre SMPS BUCK1 regulator controller, adjustable via OTP to 0.8 V, 1.0 V, 1.1 V, 1.2 V, 1.8 V, 3.3 V, 3.8 V, 5.0 V @ 0.4 MHz
- Pre SMPS BUCK2 regulator, adjustable via OTP to 1.0 V, 1.1 V, 1.2 V, 1.35 V, 1.5 V, 3.3 V, 3.6 V, 5.0 V @ 1.35/2.6 A min peak current limit, 0.4/2.4 MHz
- Post SMPS BUCK3 regulator, adjustable via OTP to 1.0 V, 1.2 V, 1.35 V, 1.8 V, 2.0 V, 2.3 V, 2.5 V, 3.3 V @ 1.4 A min peak current limit, 2.4 MHz
- Post SMPS BUCK4 regulator, adjustable via OTP to 1.1 V, 1.12 V, 1.2 V, 1.25 V, 1.3 V, 1.35 V, 1.8 V, 3.3 V @ 1 A min peak current limit, 2.4 MHz
- Post SMPS BOOST regulator, adjustable via OTP to 5.0 V @ 0.3 A max load current, 7.0 V @ 0.2 A max load current, 2.4 MHz
- Post Linear regulator LDO, adjustable via OTP to 1.2 V, 1.25 V, 1.3 V, 1.8 V, 2.5 V, 2.8 V, 3.3 V, 5.0 V @ 300/600 mA max load current
- Precise Voltage reference, adjustable via OTP to 1.8 V, 2.5 V, 3.3 V, 4.1 V @ 20 mA max load current
- SPI interface with CRC
- Programmable slew rate/soft start
- Voltage supervisors
- Spread frequency spectrum
- Reset and reset activation list
- Adjustable window watchdog supervisors
- Power up phase programmable via OTP
- Short circuit protected outputs and Fault detection pin to Microcontroller
- Low external components number
- Thermal shutdown junction temperature 175 °C

Product status link
L5965

Product summary		
Order code	Package	Packing
L5965SQ-V0Y	VFQFPN-48	Tray
L5965SQ-V0T		Tape and reel

Description

L5965 is a multiple voltage regulator composed by two battery compatible BUCK pre-regulators (one of which is a controller), two BUCK post regulators with internal compensation, one BOOST, one LDO and a precise voltage reference regulator. All the regulators, except the BUCK1 pre-regulator, have internal power switches.

OTP (One Time Programmable) cells are used for the main device parameters programming (output voltages and currents, switching frequencies) and to configure power up sequence.

An SPI interface can be used to enable or disable the single voltage regulators, for diagnostic information and to program internal blocks parameters (monitor and Power Good thresholds, slew rate, etc.).

The device offers a set of features to support applications that need to fulfill functional safety requirements as defined by Automotive Safety Integrity Level (ASIL) A-B-C-D.

1 Overview

L5965 is a multichannel voltage regulator able to offer flexibility and ease to use, together with a set of features that make it compliant to car passenger applications that require a certain level of safety. The product includes input and output monitors, independent band-gaps, ground loss monitors, internal compensation networks, that also help reduce the BOM, digital and analog BIST, fault pin.

In this product, there are 7 different regulators. A first battery-compatible regulator, a controller that can supply several current flow thanks to the use of external MOSs. A second regulator with integrated MOS that can be used as a pre-regulator for currents up to about 2.6 A. Two bucks, post regulators, one boost that can be used to supply, for example, a CAN bus, one LDO and a 1% accurate reference voltage for the microcontroller.

All output voltages can be selected via memory cells (OTP) that can be programmed before using the PMIC. This guarantees precision and safety, since output voltages are not susceptible to variations due to the external environment. It also contributes to reducing the number of external components. Through the OTP it is also possible to decide the switching frequency of some regulators, the current limitation, select the main buck and the system power-on sequence.

Programming can also be done at customer's production line.

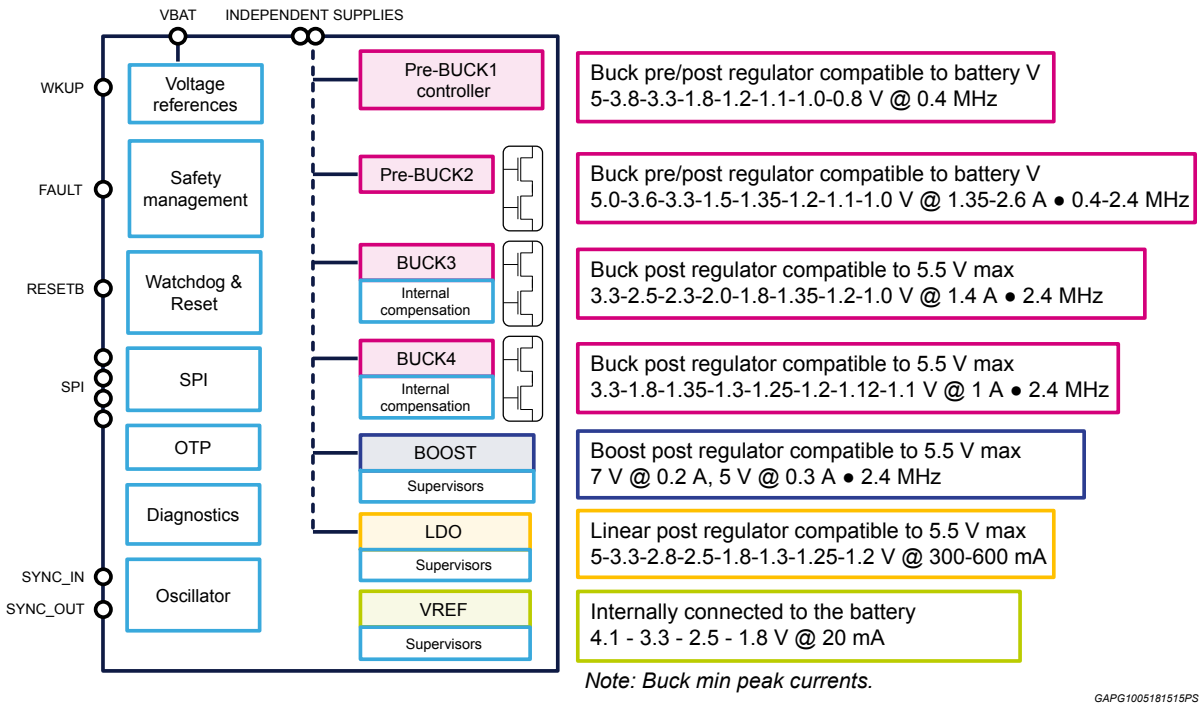
There is also an SPI bus, used to program the PMIC and to communicate with the microcontroller. Through this bus it is possible to set overvoltage and undervoltage thresholds, enable the spread spectrum, select the soft start time and many other things. The SPI is also used to communicate the status of the bucks in case of fault, over-temperature or other events.

The maximum free run switching frequency of the bucks is 2.4 MHz, modifiable through external synchronization signals.

The PMIC can manage watchdog and reset signals.

1.1 Simplified block diagram

Figure 1. Simplified block diagram



Note: Buck min peak currents.

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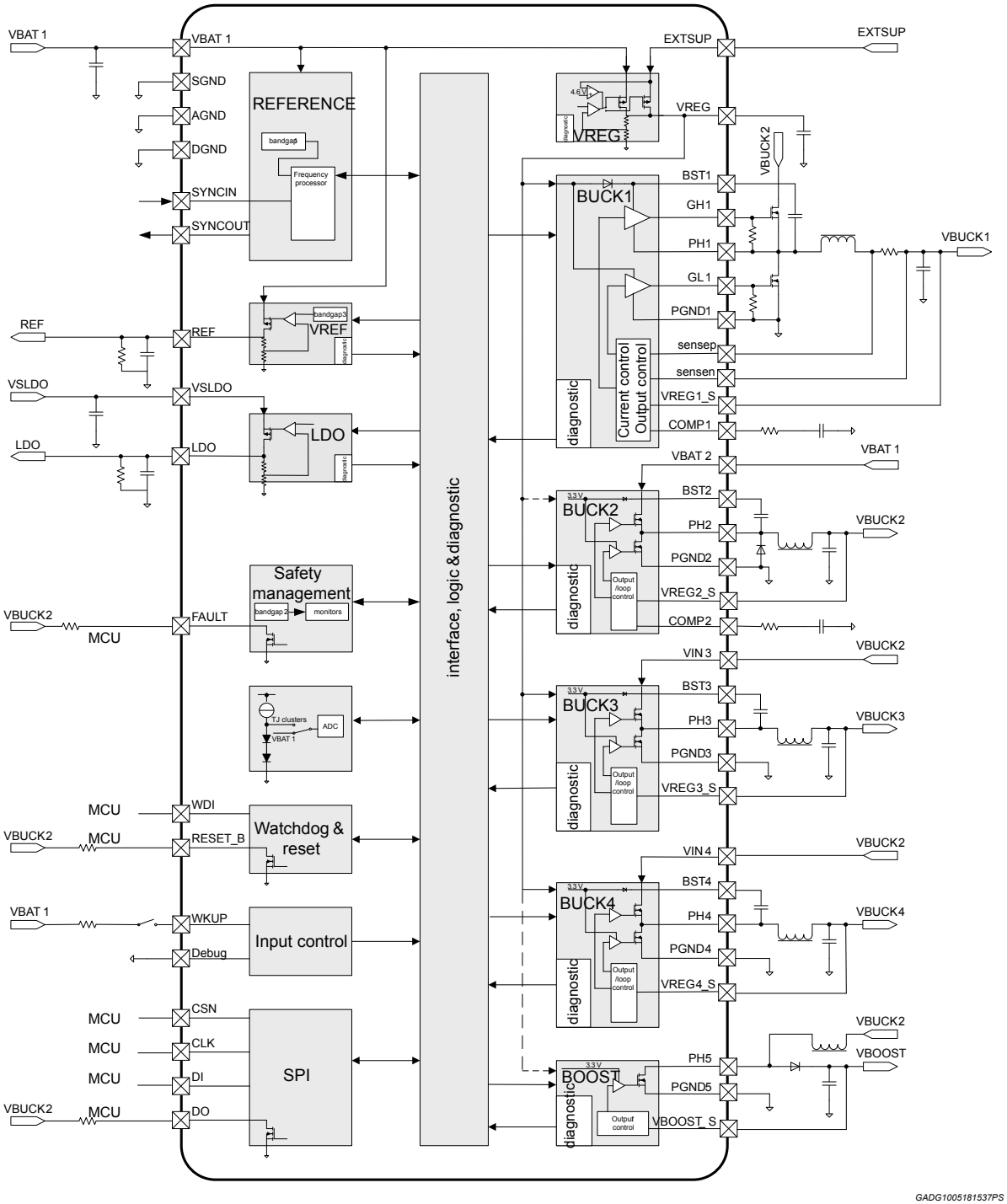
1.2 Functional block diagram

Figure 2. Functional block diagram

Application example with BUCK2 as main buck.



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2 Pins description

Figure 3. **Pin out (top view)**

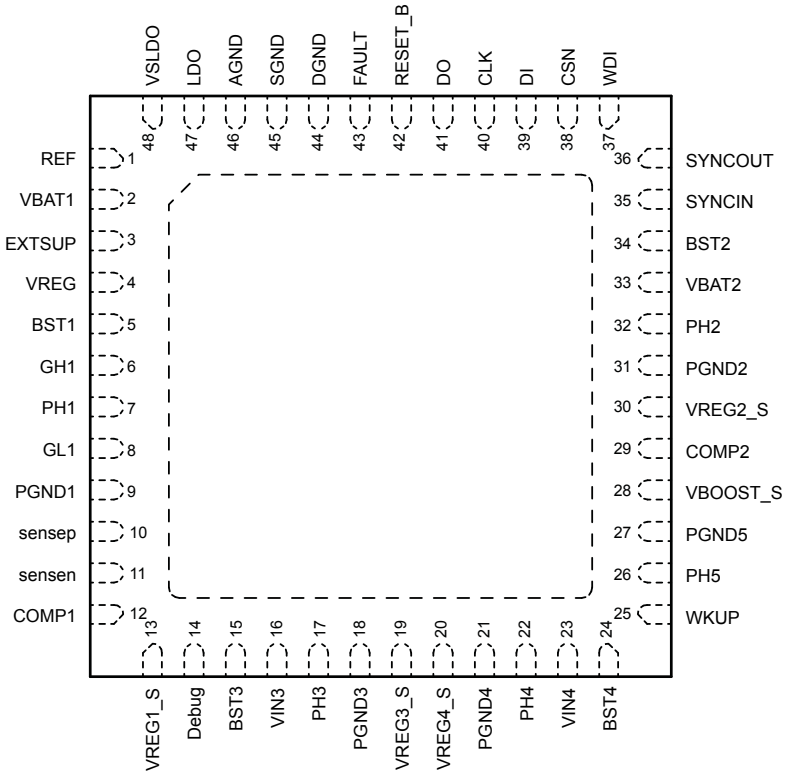

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Table 1. **Pin description and functions**

No.	Pin name	Pin type	Description
1	REF	O	Accurate reference voltage output
2	VBAT1	S	VBAT1 for inner reference and supply for pre-BUCK1 external HS MOS
3	EXTSUP	S	Optional LV input for BUCK1, BUCK3, BUCK4 gate driver supply
4	VREG	O	Internal regulator for BUCK1, BUCK3, BUCK4 gate driver supply (decoupling)
5	BST1	I/O	Boot-strap capacitor to supply BUCK1 high-side MOS gate-driver circuitry
6	GH1	O	Gate driver of external high-side MOS
7	PH1	O	Switching node BUCK1
8	GL1	O	Gate driver of external low-side MOS
9	PGND1	G	Ground for external low-side MOS driver circuitry
10	sensep	I	Positive differential current sense input for BUCK1
11	sensen	I	Negative differential current sense input for BUCK1
12	COMP1	I/O	BUCK1 Error Amplifier compensation network
13	VREG1_S	I	BUCK1 regulated voltage output (to internal voltage monitors)
14	Debug	I	Device debug. Keep floating or connect to ground when not used

No.	Pin name	Pin type	Description
15	BST3	I/O	Boot-strap capacitor to supply BUCK3 high-side MOS gate-driver circuitry
16	VIN3	S	Input voltage supply for BUCK3
17	PH3	O	Switching node BUCK3
18	PGND3	G	BUCK3 Power ground
19	VREG3_S	I	BUCK3 regulated voltage output (to internal voltage monitors)
20	VREG4_S	I	BUCK4 regulated voltage output (to internal voltage monitors)
21	PGND4	G	BUCK4 Power ground
22	PH4	O	Switching node BUCK4
23	VIN4	S	input voltage supply for BUCK4
24	BST4	I/O	Boot-strap capacitor to supply BUCK4 high-side MOS gate-driver circuitry
25	WKUP	I	Wake up input. Internal 200 kΩ pull-down
26	PH5	O	BOOST switching node
27	PGND5	G	BOOST Power ground
28	VBOOST_S	I	BOOST regulated voltage output (to internal voltage monitors)
29	COMP2	I/O	BUCK2 Error Amplifier compensation network
30	VREG2_S	I	BUCK2 regulated voltage output (to internal voltage monitors)
31	PGND2	G	BUCK2 Power ground
32	PH2	O	Switching node BUCK2
33	VBAT2	S	Input voltage supply for BUCK2
34	BST2	I/O	Boot-strap capacitor to supply BUCK2 high-side MOS gate-driver circuitry
35	SYNCIN	I	PWM input frequency for synchronization purpose. Internal current pull-down
36	SYNCOUT	O	PWM output frequency of inner 2.4M oscillator, or SYNCIN if used
37	WDI	I	Watchdog input. WDI is trigger input from MCU. Internal current pull-down
38	CSN	I	SPI: chip select input. Active low. Internal current pull-up
39	DI	I	SPI: serial data input. Internal current pull-down
40	CLK	I	SPI: serial clock input. Internal current pull-down
41	DO	OD	SPI: serial data output
42	RESET_B	OD	Reset
43	FAULT	OD	Fault pin detection to MCU
44	DGND	G	Digital GND
45	SGND	G	Signal ground for low noise circuitry
46	AGND	G	Analog GND
47	LDO	O	Linear regulated output
48	VSLDO	S	Input voltage supply for LDO

3 Electrical specifications

3.1 Absolute maximum ratings & operating voltage

Table 2. Absolute maximum ratings & operating voltage

Pin name	Absolute maximum rating			Operating voltage		
	Min	Max	Unit	Min	Max	Unit
VBAT1	-0.3	42	V	-0.3	32	V
SGND	-0.3	0.3	V	0	0	V
AGND	-0.3	0.3	V	0	0	V
DGND	-0.3	0.3	V	0	0	V
REF	-0.3	6.5	V	-0.3	5.5	V
VSLDO	-0.3	13	V	-0.3	6	V
LDO	-0.3	7	V	-0.3	6	V
WKUP	-0.3	42	V	-0.3	32	V
RESET_B	-0.3	6.5	V	-0.3	5.5	V
WDI	-0.3	6.5	V	-0.3	5.5	V
CSN	-0.3	6.5	V	-0.3	5.5	V
CLK	-0.3	6.5	V	-0.3	5.5	V
DI	-0.3	6.5	V	-0.3	5.5	V
DO	-0.3	6.5	V	-0.3	5.5	V
FAULT	-0.3	6.5	V	-0.3	5.5	V
SYNCOUT	-0.3	4.6	V	-0.3	3.6	V
SYNCIN	-0.3	6.5	V	-0.3	5.5	V
EXTSUP	-0.3	13	V	-0.3	12	V
VREG	-0.3	8	V	-0.3	6.6	V
BST1	PH1-0.3	PH1+10	V	PH1-0.3	PH1+8	V
GH1	PH1-0.3	PH1+10	V	PH1-0.3	PH1+8	V
PH1	-1	42	V	-1	32	V
GL1	PGND1-0.3	PGND1+10	V	PGND1-0.3	PGND1+8	V
sensep	-0.3	6.5	V	-0.3	5.5	V
	sensen-2	sensen+2	V	sensen-2	sensen+2	V
sensen	-0.3	6.5	V	-0.3	5.5	V
VREG1_S	-0.3	6.5	V	-0.3	5.5	V
PGND1	-0.3	0.3	V	-0.3	0.3	V
VBAT2	-0.3	42	V	-0.3	32	V
BST2	PH2-0.3	PH2+4.6	V	PH2-0.3	PH2+3.6	V
PH2	-1	42	V	-1	32	V
VREG2_S	-0.3	6.5	V	-0.3	5.5	V
PGND2	-0.3	0.3	V	-0.3	0.3	V

Pin name	Absolute maximum rating			Operating voltage		
	Min	Max	Unit	Min	Max	Unit
VIN3	-0.3	6.5	V	-0.3	5.5	V
BST3	PH3-0.3	PH3+4.6	V	PH3-0.3	PH3+3.6	V
PH3	-1	6.5	V	-1	5.5	V
VREG3_S	-0.3	4.6	V	-0.5	3.6	V
PGND3	-0.3	0.3	V	-0.3	0.3	V
VIN4	-0.3	6.5	V	-0.3	5.5	V
BST4	PH4-0.3	PH4+4.6	V	PH4-0.3	PH4+3.6	V
PH4	-1	6.5	V	-1	5.5	V
VREG4_S	-0.3	4.6	V	-0.5	3.6	V
PGND4	-0.3	0.3	V	-0.3	0.3	V
PH5	-0.3	9	V	-0.3	8	V
VBOOST_S	-0.3	13	V	-0.3	7.5	V
PGND5	-0.3	0.3	V	-0.3	0.3	V
Debug	-0.3	42	V	-0.3	20	V
COMP1	-0.3	4.6	V	-0.3	3.6	V
COMP2	-0.3	4.6	V	-0.3	3.6	V

3.2 Thermal data

3.2.1 Thermal resistance

Table 3. Operation junction temperature

Symbol	Parameter	Board	Value unit	Unit
$R_{th\ j\text{-}a\text{-}2s}$	Thermal resistance junction-to-ambient	2s	66	°C/W
$R_{th\ j\text{-}a\text{-}2s2p}$		2s2p	32	°C/W
$R_{th\ j\text{-}a\text{-}2s2pv}$		2s2p+vias	26	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-to-case		2.2	°C/W

3.2.2 Thermal warning and protection

Table 4. Temperature thresholds

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{SD_TH}	Thermal Shutdown	–	160	175	190	°C
T_{SD_hys}		Hysteresis	0.5	4	8	°C
$T_{OT\_THx\ (x=1\text{-}7)}$	Over temperature warning	–	140	155	170	°C
$T_{OT\_hysx\ (x=1\text{-}7)}$		Hysteresis	3	7	11	°C
T_{SD_filter}	Thermal Filter time	–	–	16	–	µs
T_j	Junction temperature	T_j	-40		150	°C
T_{stg}	Storage temperature	T_{stg}			150	°C

According to the below formula and considering T_{SD_TH} thermal shutdown minimum threshold at 160 °C, the maximum suggested power dissipation is:

$P_{DISS\_suggested} = (T_{SHD} - T_{AMB}) / R_{THJ-A}$

Table 5. Maximum suggested power

Symbol	T_{amb} 125 ° C	T_{amb} 105 ° C	T_{amb} 80 ° C
$R_{th\ j-a-2s}$	0.53 W	0.9 W	1.2 W
$R_{th\ j-a-2s2p}$	1.1 W	1.8 W	2.6 W
$R_{th\ j-a-2s2pvias}$	1.35 W	2.3 W	3.2 W

3.3 Electrical characteristics

V_{BAT1} supplies pre-BUCK1 circuitry the inner reference circuit (band-gap and oscillator) and VREF.

V_{BAT2} supplies BUCK2, VSLDO supplies the LDO, VIN3 supplies BUCK3 and VIN4 supplies BUCK4.

$V_{BAT1,2}$ = 14 V, T_{amb} = –40 °C to 125 °C, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
General characteristics						
V_{BAT1}	Operating range	–	4	14	32	V
V_{BAT2}	Operating range	–	4	14	32	V
$I_{STANDBY1}$	STANDBY mode total current consumption on VBAT1	All regulators off, V_{BAT1} = 14 V, non-supply inputs floating, current consumption from the supplies	–	–	50	µA
$I_{STANDBY2}$	STANDBY mode total current consumption on VBAT2	All regulators off, V_{BAT2} = 14 V, non-supply inputs floating, current consumption from the supplies	–	–	1	µA
I_{ACTIVE}	ACTIVE mode total current consumption	Main BUCK only, V_{BAT1-2} = 14 V, EXTSUP = 0 V	–	10	–	mA
I_{ACTIVE_ALL}	ACTIVE mode total current consumption	All regulators ON, V_{BAT1-2} = 14 V, Rising slope < 0.1V*ms, EXTSUP=0 V	–	40	–	mA
Supply monitors						
V_{UV}	Under-voltage threshold for V_{BAT1} and V_{BAT2}	Supply decreasing	5.3	5.8	6.3	V
V_{UV_HYS}	Under-voltage hysteresis	–	–	0.2	0.4	V
V_{OK}	OK threshold for VBAT1 or VBAT2, depending on which is the main regulator	Supply increasing	5.5	6	6.5	V
V_{OK_HYS}	OK-voltage hysteresis	-	-	0.2	0.4	V
V_{OV}	Over-voltage threshold for V_{BAT1} and V_{BAT2}	Supply increasing	30	32	34	V
V_{OV_HYS}	Over-voltage hysteresis	–	–	2	2.4	V
t_{UVOV_filter}	Over/under voltage filter time	–	10	16	–	µs
V_{RESETB}	RESETB pin low output voltage	I_{RESET} = 1 mA		0.1	0.25	V
T_{RESETB}	RESETB pulse duration	–	4	10	16	µs
V_{FAULT}	FAULT pin low output voltage	I_{FAULT} = 1 mA		0.1	0.25	V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Power on reset						
V_{POR_R}	V_{BAT1} threshold	V_{BAT1} rising	3	3.4	3.8	V
V_{POR_F}	V_{BAT1} threshold	V_{BAT1} falling	2.8	3.2	3.6	V
Oscillator						
f_{osc}	Oscillator frequency	–	4.08	4.8	5.52	MHz
f_{IN}	Input frequency at SYNCIN pin	–	1.8	–	2.76	MHz
VH_{SYNC}	SYNCIN high threshold	–	2.1	–	–	V
VL_{SYNC}	SYNCIN low threshold	–	–	–	1	V
VREG						
V_{VREG}	BUCK1 gate driver inner regulated supply	I_{VREG}= 0 mA~50 mA, EXTSUP = 6.3~12 V	5.8	6.0	6.2	V
V_{EXTSUP_TH}	Switch over threshold	I_{VREG} = 5 mA~50 mA, EXTSUP rising, in ACTIVE mode	–	4.7	–	
V_{EXTSUP_HYS}	Switch over hysteresis	–	–	0.2	–	V
V_{DROP_VREG}	Drop out voltage at VREG	I_{load} = 50 mA, supplied by VBAT1	–	–	0.25	V
		I_{load} = 50 mA, supplied by EXTSUP	–	–	0.4	V
I_{LIM_REG}	VREG current limitation	Supplied by VBAT1/EXTSUP	60	85	-	mA
C_{VREG}	Capacitive load	–	–	2.2	–	µF
V_{REG_OK}	VREG under voltage threshold	VREG rising	–	4	–	V
V_{REG_OK}	VREG under voltage threshold	Hysteresis	–	0.26	–	V
BUCK1						
V_{IN_BUCK1}	Input voltage range	–	4	–	32	V
V_{OUT_BUCK1}	Output voltage (> 200 mA, static)	OTP = 000	-2.5%	5.0	+2.5 %	V
		OTP = 001		3.8		V
		OTP = 010		3.3		V
		OTP = 011		1.8		V
		OTP = 100		1.2		V
		OTP = 101		1.1		V
		OTP = 110		1.0		V
		OTP = 111		0.8		V
Vsense	Cycle by cycle current limitation sense voltage	–	–	80	–	mV
F_{SW_BUCK1}	Switching frequency	–	340	400	460	kHz
F_{spread_BUCK1}	Spread spectrum range	Fsw = 400 kHz	-20	–	20	%

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{programming\_dead\_BUCK1}$	Dead time (Blanktime: non-overlap time plus programming time)	SPI = 000 default	–	50	–	ns
		SPI = 001	–	40	–	ns
		SPI = 010	–	30	–	ns
		SPI = 011	–	0	–	ns
		SPI = 100	–	60	–	ns
		SPI = 101	–	70	–	ns
		SPI = 110	–	100	–	ns
		SPI = 111	–	200	–	ns
t_{on_min}	–	–	–	208	–	ns
BUCK1 GATE Driver						
Ron HS1	Ron @ Buck1_curr_max	SPI = '0' (1.0 A)	–	1.75	–	Ω
		SPI = '1' (2.0 A)	–	0.85	–	Ω
Ron LS1	Ron @ Buck1_curr_max	SPI = '0' (1.0 A)	–	3.20	–	Ω
		SPI = '1' (2.0 A)	–	1.60	–	Ω
$V_{CLAMP\_VGS\_HS}$	Clamp protection for Vgs of external transistor	–	9	–	11	V
$V_{CLAMP\_VGS\_LS}$	Clamp protection for Vgs of external transistor	–	9	–	11	V
$t_{SOFTSTART\_BUCK1}$	Soft start time when start up, Vref from 0 V to 1 V	SPI = 00	0.3	0.42	0.55	ms
		SPI = 01	0.7	1	1.3	ms
		SPI = 10	1.6	2	2.4	ms
BUCK2						
V_{IN_BUCK2}	Input voltage range	–	3.3	–	32	V
V_{OUT_BUCK2}	Output voltage (no load, static)	OTP = 000	-2.5%	5.0	+2.5 %	V
		OTP = 001		3.6		V
		OTP = 010		3.3		V
		OTP = 011		1.5		V
		OTP = 100		1.35		V
		OTP = 101		1.2		V
		OTP = 110		1.1		V
		OTP = 111		1.0		V
t_{on_min}	Min T_{on} internal FET	–	–	100	–	ns
F_{SW}	Free running frequency	OTP = 0	0.34	0.4	0.46	MHz
		OTP = 1	2.04	2.4	2.76	MHz
$\Delta V_{BUCK2}/V_{BUCK2}$ (2)	Undershoot &overshoot	Load = 0.3 A to 1.8 A, Δt = 10 µs, V_{IN} = 5 V	-5	–	5	%
$\Delta V_{LINER-LOADR\_VBUCK2}$	Static line + load regulation	V_{IN} = 6 V to 32 V, V_{OUT} = 5 V I_{Load} = 0.3 A to 1.8 A	–	-0.45	–	%
I_{LIMIT}	Peak switching current limitation	OTP = 0	1.35	1.8	2.3	A
		OTP = 1	2.6	3.4	4.2	A
Ron_{HS}	High side switch on resistance	–	–	120	190	mΩ

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Ron_{LS}	Low side switch on resistance	–	–	110	190	mΩ
η(2)	Efficiency	FSW =400 kHz, V_{IN}=14 V, V_{OUT} = 5 V/3.3 V, I_{load} = 2 A	–	86	–	%
		F_{SW} = 2.4 MHz, V_{IN} = 5 V, V_{OUT} = 3.3 V, I_{load} = 1 A	–	88	–	%
$t_{SOFTSTART\_BUCK2}$	Soft start time when start up, Vref from 0 V to 1 V	SPI = 00 default	0.35	0.45	0.5	ms
		SPI = 01	0.8	1.1	1.4	ms
		SPI = 10	1.8	2.2	2.6	ms
F_{spread_BUCK2}	Spread spectrum range	Fsw=400 kHz	-20	–	20	%
		Fsw=2.4 MHz	-4	–	4	%
Phi_{BUCK2}	Phase shift to BUCK1	–	–	180	–	deg
t_{SR_PH2}(2)	Output stage slew rate when F_{SW} = 400 kHz	V_{IN} = 14 V, I_{load} = 1.8 A, V_{OUT} = 3.3 V SPI = 00	–	10	–	ns
		SPI = 01	–	20	–	ns
	Output stage slew rate when F_{SW} = 2.4 MHz	V_{IN} = 5 V, I_{load} = 1 A, V_{OUT} = 3.3 V	–	10	–	ns
BUCK3						
V_{IN_BUCK3}	Input voltage range	–	3.0	–	5.5	V
V_{OUT_BUCK3}	Output voltage (no load, static)	OTP = 000 V_{IN_BUCK3} > 4.5 V	-2.5%	3.3	+2.5 %	V
		OTP = 001		2.5		V
		OTP = 010		2.3		V
		OTP = 011		2.0		V
		OTP = 100		1.8		V
		OTP = 101		1.35		V
		OTP = 110		1.2		V
		OTP = 111		1.0		V
t_{on_min}	–	–	–	70	-	ns
$\Delta V_{BUCK3}/V_{BUCK3}$(2)	Undershoot	Load = 0.3 A to 0.8 A Δt = 10 µs, V_{IN}= 3.3 V	-5	–	5	%
$\Delta V_{LINEAR-LOADR\_VBUCK3}$	Static line + load regulation	Load = 0.3 A to 0.8 A	–	0.1	–	%
I_{LIMIT}	Peak switching current limitation	–	1.4	1.8	2.3	A
Ron_{HS}	High side switch on resistance	–	–	150	250	mΩ
Ron_{LS}	Low side switch on resistance	–	–	110	200	mΩ
F_{sw_BUCK3}	Free-run switching frequency	–	2.04	2.4	2.76	MHz
η(2)	Efficiency	FSW = 2.4 MHz, V_{IN} = 3.3 V, V_{OUT} = 1. 2 V, I_{load} = 0.7 A	–	80	–	%

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{SOFTSTART\_BUCK3}$	Soft start time when start up, Vref from 0 V to 1 V	SPI = 00	0.35	0.45	0.55	ms
		SPI = 01	0.8	1.1	1.4	ms
		SPI = 10	1.8	2.2	2.6	ms
F_{spread_BUCK3}	Spread spectrum range	Fsw=2.4 MHz	-4		4	%
Phi_{BUCK3}	Phase shift to BUCK1	–	–	90	–	deg
t_{SR_PH3}(2)	Ouptut stage slew rate, F_{SW}=2.4 MHz	V_{IN} = 3.3 V, I_{load} = 0.8 A, V_{OUT} = 1.2 V	–	10	–	ns
BUCK4						
VIN_BUCK4	Input voltage range	–	3.0	–	5.5	V
VOUT_BUCK4	Output voltage (no load, static)	OTP = 000 V_{IN_BUCK4} > 4.5 V	-2.5%	3.3	+2.5 %	V
		OTP = 001		1.8		V
		OTP = 010		1.35		V
		OTP = 011		1.3		V
		OTP = 100		1.25		V
		OTP = 101		1.2		V
		OTP = 110		1.12		V
		OTP = 111		1.1		V
t_{on_min}	–	–	–	70	–	ns
$\Delta V_{BUCK4}/V_{BUCK4}$(2)	Undershoot	Load = 0.3 A to 0.6 A Δt = 10 µs, V_{IN} = 3.3 V	-5	–	5	%
$\Delta V_{LINER-LOADR\_VBUCK4}$	Static line + load regulation	Load = 0.3 A to 0.6 A	–	0.1	–	%
I_{LIMIT}	Peak switching current limitation	–	1	1.35	1.9	A
Ron_{HS}	High side switch on resistance	–	–	150	250	mΩ
Ron_{LS}	Low side switch on resistance	–	–	120	220	mΩ
η(2)	Efficiency	F_{SW} = 2.4 MHz, V_{IN} = 3.3 V, V_{OUT} = 1.8 V, I_{load} = 0.6 A	–	85	–	%
$t_{SOFTSTART\_BUCK4}$	Soft start time when start up, Vref from 0 V to 1 V	SPI = 00	0.35	0.45	0.55	ms
		SPI = 01	0.8	1.1	1.4	ms
		SPI = 10	1.8	2.2	2.6	ms
F_{spread_BUCK4}	Spread spectrum range	Fsw=2.4 MHz	-4%	–	4%	–
Phi_{BUCK4}	Phase shift to BUCK1	–	–	270	–	deg
F_{sw_BUCK4}	Free-run switching frequency	–	2.04	2.4	2.76	MHz
t_{SR_PH4}(2)	Output stage slew rate when f_{SW} = 2.4 MHz	V_{IN} = 3.3 V, I_{load} = 0.6 A, V_{OUT} = 1.8 V	–	10	–	ns
BOOST						
V_{IN_BOOST}	Input voltage range	–	3.0	–	5.5	V
V_{BOOST}	Output voltage	OTP = 0	-2.5%	5	+2.5 %	V
		OTP = 1		7		V
I_{BOOST_limit}	Switch current limitation	–	500	–	1200	mA

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
F_{SW_BOOST}	Switching frequency	–	2.04	2.4	2.76	MHz
PhS_{BOOST}	Phase shift to BUCK1	–	–	270	–	deg
F_{spread_BOOST}	Spread spectrum range	F_{SW} = 2.4 MHz	-4%	–	4%	*f_{SW}
t_{SS_BOOST}	Soft start time	SPI = 00 default	0.4	0.5	0.6	ms
		SPI = 01	0.9	1.2	1.5	ms
		SPI = 10	1.8	2.4	3	ms
RDS_{ON_BOOST}	LS RDS_{ON}	–	–	400	700	mΩ
η_{BOOST}(2)	Efficiency	F_{SW} = 2.4 MHz, V_{IN} = 3.3 V, V_{OUT} = 5 V, Load = 200 mA	–	87	–	%
LDO						
VSLDO	Input voltage range	–	1.8	–	6	V
V_{LDO}	Output voltage	OTP = 000	-2.5%	5.0	+2.5 %	V
		OTP = 001		3.3		V
		OTP = 010		2.8		V
		OTP = 011		2.5		V
		OTP = 100		1.8		V
		OTP = 101		1.3		V
		OTP = 110		1.25		V
		OTP = 111		1.2		V
I_{load}	Load current range	OTP = 0	1	–	300	mA
I_{load}	Load current range	OTP = 1	1	–	600	mA
V_{drop}	I_{out} = 600 mA	–	–	–	0.6	V
C_{load}	–	–	10	–	–	µF
C_{ESR}	–	–	-	–	100	mΩ
VREF						
V_{REF}	REF Output voltage, I_{VREF} = 5 mA	OTP = 00	1.78	1.8	1.82	V
		OTP = 01	2.47	2.5	2.53	V
		OTP = 10	3.27	3.3	3.33	V
		OTP = 11	4.06	4.1	4.14	V
I_{load}	Load current range	–	1	–	20	mA
I_{REF_TOT}	Reference voltage current limit	–	23	35	–	mA
C_{VREF}	VREF load capacitor	–	0.22	–	–	µF
C_{ESR}	Load capacitor ESR	–	–	–	30	mΩ
Toc_filter	Filter for over current flag of VREF	-	–	4	–	ms
SYNC IN/OUT						
$V_{SYNCOUTL}$	Output low level	$I_{SYNCOUT}$ = -1 mA	–	–	0.2	V
$V_{SYNCOUTH}$	Output high level	$I_{SYNCOUT}$ = 200 µA	3.0	–	3.3	V
$C_{SYNCOUT}$	Pin capacitance inside silicon	(1)	–	10	15	pF
C_L	Load capacitor at application level	(2)	–	–	200	pF

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$T_{SYNCOUT}$	SYNCOUT cycles/seconds	Aligned with SYNCIN frequency range	-	–	370	ns
$T_{delay\_SYNC\_in\text{-}out}$	Delay between SYNCIN rising edge and SYNCOUT rising edge	No load on SYNCOUT pin	–	–	20	ns
DC_{SYNCIN}	Duty cycle of SYNCIN	-	30%		70%	
T_{det}	SYNCIN rising edge detection time	SYNCIN frequency >1.6 MHz.	10	14	18	µs
WKUP						
V_{WAKE_ON}	–	–	3	–	4	V
V_{WAKE_OFF}	–	–	2	–	3	V
I_{LEAK_WKUP}	Leakage current	V_{WKUP} = 5 V, active mode	10	–	40	µA
t_{WAKE_filter}	–	–	–	60	–	µs
R_{PD_WAKE}	Internal pull-down resistor	–	–	200	–	kΩ
Twk_rec	WKUP high duration in REC	SPI = 00 default	8	10	11	ms
		SPI = 01	17	20	22	ms
		SPI = 10	26	30	33	ms
		SPI = 11	35	40	44	ms
GND loss comparator						
V_{GL_TH}	GND loss threshold	SGND to PGNDx	0.18	0.27	0.34	V
t_{GL_filter}	GND loss filter	–	–	16	–	µs
Power output UV/OV monitor						
VUV_L_ BUCKx, BOOST, LDO, V_{ref}	Under voltage threshold at falling edge of output (as % of output). Referred to the output relative value	SPI = 0 default	-	91	-	%
		SPI = 1	-	86	-	%
VUV_HYS_ BUCKx, BOOST, LDO, V_{ref}	Hysteresis of UV	–	–	2	3	%
VOV_H_BUCK2 VOV_H_BOOST, LDO VOV_H_VREF, $BUCK_{1/3/4}$	Over voltage threshold at rising edge of output (as % of output). Referred to the output relative value	SPI = 0 (default)	-3.5	107 108 107.5	+3.5	%
VOV_H_BUCK2 VOV_H_BOOST, LDO VOV_H_VREF, $BUCK_{1/3/4}$	Over voltage threshold at rising edge of output (as % of output). Referred to the output relative value	SPI = 1	-3.5	112 113 112.5	+3.5	%
VOV_HYS_ BUCKx, BOOST, LDO, V_{ref}	Hysteresis of OV	–	–	2	3	%
$t_{UV\_filter\_BUCK3,4}$, BOOST, LDO, V_{ref}	Under voltage threshold filter time	–	–	16	–	µs
$t_{OV\_filter\_BUCK3,4}$, BOOST, LDO, V_{ref}	Over voltage threshold filter time	–	–	16	–	µs
$t_{UV\_filter\_BUCK1}$ $t_{UV\_filter\_BUCK2}$	Under voltage threshold filter time	–	–	40	–	µs
$t_{OV\_filter\_BUCK1}$ $t_{OV\_filter\_BUCK2}$	Over voltage threshold filter time	–	–	40	–	µs
Power Good						

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{TH\_PGx\ (x=1,2,3,4)}$	PGx Threshold as output voltage percentage. Referred to the output relative value	SPI = 0 default	-	95	99	%
		SPI = 1	-	90	94	%
t_{GLITCH_PG}	Glitch Filter Time for PG	–	–	60	–	µs
Watchdog trigger time						
VH_{WDI}	WDI pin threshold high	–	2.3	–	–	V
VL_{WDI}	WDI pin threshold low	–	–	–	1	V
T_{LW}	Long open window	–	160	200	240	ms
T_{EFW1}	Early Failure Window 1	SPI = 00	–	–	6.4	ms
T_{LFW1}	Late Failure Window 1	SPI = 00	15.6	–	–	ms
T_{SW1}	Safe Window 1	SPI = 00	7.8	–	12.7	ms
T_{EFW2}	Early Failure Window 2	SPI = 01	–	–	12.7	ms
T_{LFW2}	Late Failure Window 2	SPI = 01	31.1	–	–	ms
T_{SW2}	Safe Window 2	SPI = 01	15.6	–	25.5	ms
T_{EFW3}	Early Failure Window 3	SPI = 10	–	–	25.5	ms
T_{LFW3}	Late Failure Window 3	SPI = 10	62.2	–	–	ms
T_{SW3}	Safe Window 3	SPI = 10	31.1	–	50.9	ms
T_{EFW4}	Early Failure Window 4	SPI = 11	–	–	50.9	ms
T_{LFW4}	Late Failure Window 4	SPI = 11	124.4	–	–	ms
T_{SW4}	Safe Window 4	SPI = 11	62.2	–	101.8	ms

1. *Guaranteed by design*
2. *Guaranteed by bench tests*

3.3.1 Electrical characteristic curves

Figure 4. Efficiency of Buck2 with Vin = 14 V and Vout = 3.3 V

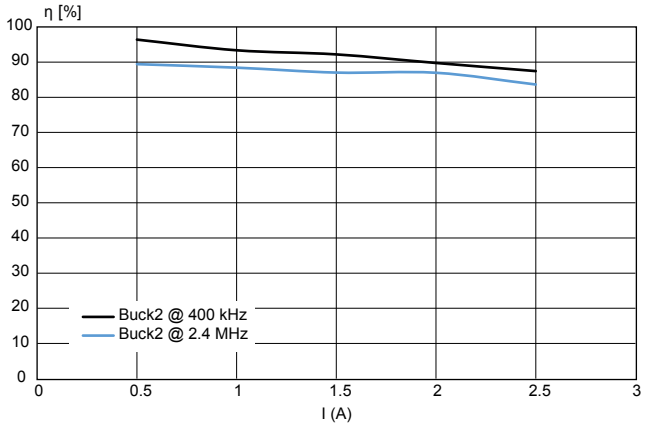


Figure 5. Efficiency of Buck3 with Vin = 3.3 V and Vout = 2 V

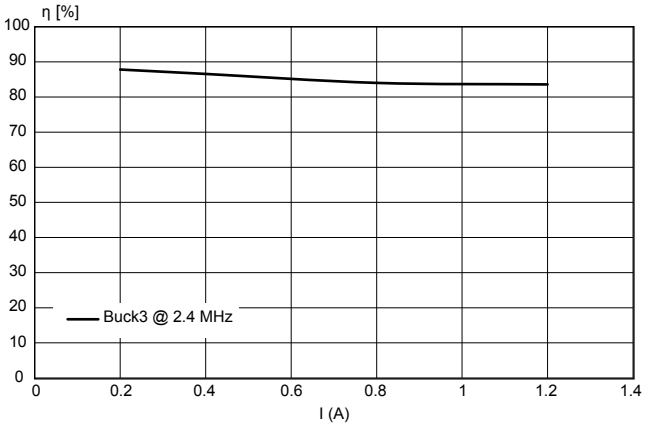


Figure 6. Efficiency of Buck4 with Vin = 3.3 V and Vout = 1.8 V

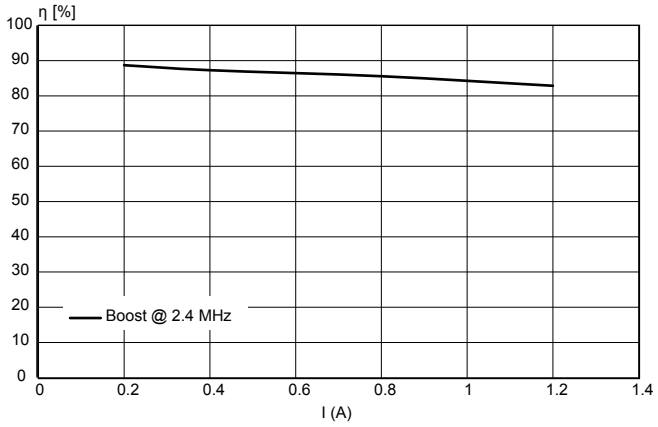
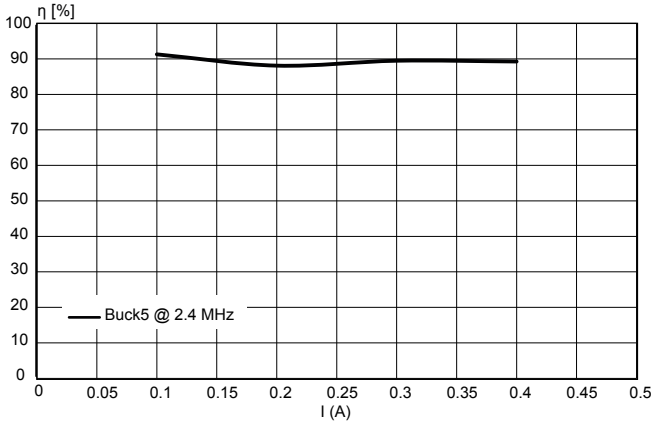


Figure 7. Efficiency of Boost with Vin = 3.3 V and Vout = 5 V



4 Functional description

4.1 Programming by OTP

OTP cells are used to program all regulators output voltages and running frequencies, together with additional device features. Programmable values are:

- BUCK1 output values : 5.0 V, 3.8 V, 3.3 V, 1.8 V, 1.2 V, 1.1 V, 1.0 V or 0.8 V (3 bits)
- BUCK2 output values : 5.0 V, 3.6 V, 3.3 V, 1.5 V, 1.35 V, 1.2 V, 1.1 V or 1.0 V (3 bits)
- BUCK2 current limit value: 1.35 A or 2.6 A (1 bit)
- BUCK2 free running frequency: 0.4 or 2.4 MHz (1 bit)
- BUCK3 output values : 3.3 V, 2.5 V, 2.3 V, 2.0 V, 1.8 V, 1.35 V, 1.2 V, or 1.0 V (3 bits)
- BUCK4 output values : 3.3 V, 1.8 V, 1.35 V, 1.3 V, 1.25 V, 1.2 V, 1.12 V or 1.1 V (3 bits)
- LDO output values : 5.0 V, 3.3 V, 2.8 V, 2.5 V, 1.8 V, 1.3 V, 1.25 V or 1.2V (3 bits)
- LDO output current limitation: 300 or 600 mA (1 bit)
- BOOST output voltage: 7.0 V or 5.0 V (1 bit)
- VREF output voltage: 4.1 V, 3.3 V, 2.5 V or 1.8 V (2 bits)
- Watchdog selection: by WDI pin or through SPI (2 bits)
  - if OTP "WD_cfg" bits is "00" or "01": Use Watch Dog;
  - if OTP "WD_cfg" bits is "10" : No watch dog;
  - if OTP "WD_cfg" bits is "11": Use SPI as Watch Dog;
- Effect of WD failure on FSM. If SPI_WD_REC_en=0 and OTP_WD_REC_en=0, a WD failure asserts RESET_B but not FSM: the device keeps active state with regulators running. If one of these bits is “1”, RESET_B is asserted and FSM goes to REC state.
- Main BUCK selection: BUCK1 or BUCK2 (3 bit)
- Other regulators turning on order: from the second to the seventh one (3 bits per each regulator)
- Regulators turning on delay after Power Good of the previous regulator: 0, 2, 5 or 10 ms (2 bits)
- Reset activation after Power Good signal of a specific regulator (3 bits), with the possibility to add a delay from 0 (no delay) to 10 ms (2 bits)
- Reset activation by the over-voltage of regulators in reset activation list (1 bit)

The approach used in L5965 device is the following:

- L5965 OTP cells must be programmed before first device turning on:
  - No default status is present for OTP programmed parameters
  - Customer can program OTP by itself
- If all OTP cells are not written, the device automatically moves to OTP program mode.
- OTP programming can be done only one time:
  - It is not possible additional writing procedure after the first one:
    - 3 bits stored inside OTP means OTP written (USR Area Protection)
  - If OTP programming procedure fails or it is wrong, device is discarded

If a regulator is not used (disabled), it is recommended to set to “0” its enable and SeqId (post regulator activation) bits. PGNDx, VREGx_S and VBOOST_S pins should be connected to ground, while other pins can be left floating. If the internal VREG is not used, EXSUP pin should be connected to ground.

4.2 Voltage regulators and features description

4.2.1 VREG

VREG is an internal regulator used to supply Buck1, Buck3 and Buck4. Its output (6.0 V typical) is available at VREG pin and decoupled by using a ceramic capacitor (2.2 µF suggested). The regulator has an internal current limitation protection.

An external supply can be provided at EXTSUP pin, in parallel to VBAT1. In ACTIVE mode, if EXTSUP is higher than a fixed threshold (typically 4.6 V), VREG supply is automatically switched to EXTSUP. It helps to improve efficiency and save power dissipation when VBAT1 is higher than EXTSUP.

In case of over-temperature detection on VREG, the PMIC enters REC mode.

When the PMIC is in RAMPUP MAIN or SECUP mode, in case of fail of “vreg ok" on VREG, the IC enters REC mode.

When the PMIC is in other modes, in case of fail of “vreg ok" on VREG, the IC provides a "vreg not ok" status via SPI bit and asserts the FAULT pin.

VREG output value influences the PMIC power-up phase when BUCK2 is configured as main buck.

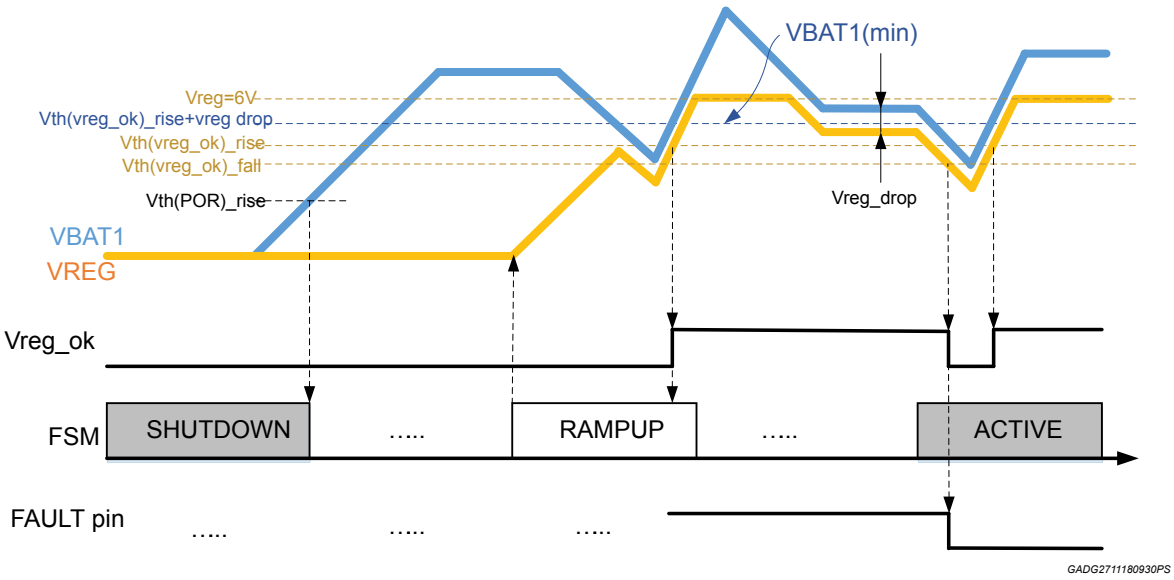
The minimum value of VBAT1 required to switch-on the IC can be calculated as Vth(VREG_OK)_rising + VREG drop.

In RAMPUP MAIN and SECUP modes, if VBAT1 has not reached the minimum required value and VREG is not ok, then FSM moves to REC state.

In ACTIVE mode, if VBAT1 has not reached the minimum required value and VREG is not ok, all related analog blocks (buck1, buck3, buck4) are active, but the SPI bit and FAULT pin are asserted. To make sure that BUCK1, BUCK3 and BUCK4 fully work, VREG should be higher than 3.5 V.

If this regulator is disabled and not used, EXSUP pin should be connected to ground.

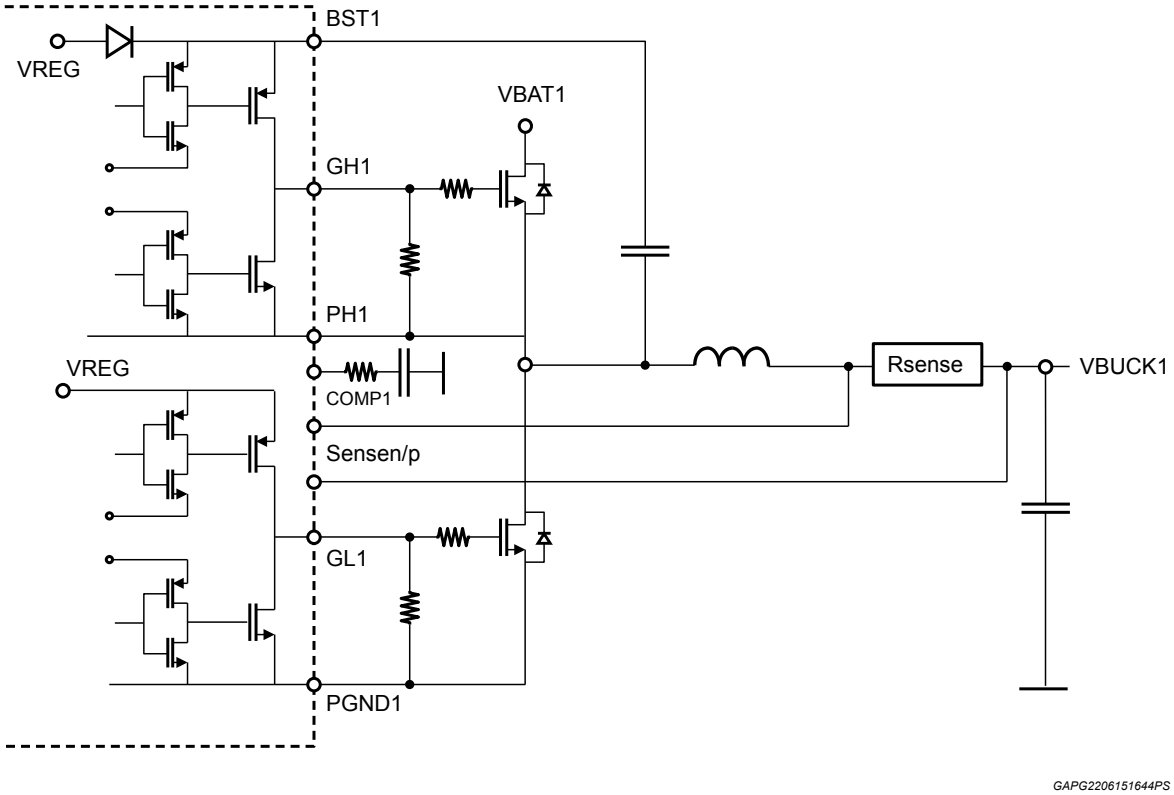
Figure 8. VREG influence on PMIC behavior



4.2.2 Pre regulator BUCK1

BUCK1 controller operates using constant frequency peak current mode control. According to OTP selection, it can work as Main BUCK pre-regulator (enabled by WKUP pin signal) or as post-regulator. The input voltage (VBAT1) is compatible to battery level and the overvoltage detection of VBAT1 (typ 32 V, available via SPI and enabled by default) can be disabled via SPI (enabled by default). The switching frequency is set to 400 kHz with the possibility to have Spread Spectrum (enabled by default and disabled via SPI). Driving stage maximum output current is programmable via SPI to 1 A or 2 A. Output voltage is programmable via OTP to 8 possible values (5.0 V, 3.8 V, 3.3 V, 1.8 V, 1.2 V, 1.1 V, 1.0 V or 0.8 V). The inductor current is monitored by a Sense Amplifier, sensing the drop on an external resistor, then the current limit value depends on the resistor value. Output power stage dead time (to avoid Cross Conduction) is programmable via SPI on 8 different levels. Soft Start time is programmable via SPI. Compensation network is external.

Figure 9. **Pre regulator BUCK1**



In dropout operation the external high-side MOSFET is kept always on; every fourth clock cycle it has to be turned off for 180ns to recharge bootstrap capacitor. This allows a maximum duty cycle of 98%.

BUCK1 controller provides the following diagnostic:

- Monitor of the output voltage is monitored by an independent circuit for UV/OV detection: thresholds are set via SPI.
- Monitor of the Power Good thresholds: are set via SPI (at 5/10% of VBUCK1) and the status is provided via SPI bit.
- Over Current Protection via current sense amplifier.
- Over Temperature detection by a local thermal sensor.
- PGND1 loss detection.

If BUCK1 is set as Main BUCK pre-regulator:

- If a UV/OV fault occurs, then Fault pin is asserted and the corresponding fault bit is set inside the SPI register, where can be read and cleared. RESET_B is always asserted in case of UV. In case of OV, it is possible to enable or disable the reset for all regulators together by OTP. The reset moves the device to REC state.
- If OT occurs, the power stage is switched OFF with a 16 µs filter time. The output decreases until UV is detected. The regulator goes in REC state and can restart only when OT flag is reset. The corresponding SPI bit is set and FAULT pin is asserted.
- Over current limitation is a cycle by cycle protection: when a fault happens for 7 consequent cycles, the FAULT pin is asserted and the corresponding fault bit is set inside SPI register.
- If PGND1 ground loss occurs, all regulators are turned OFF, FAULT and RESET_B pins are asserted and device goes back to REC state. Until the fault is present, any tentative of turning on the regulator is ignored.

If BUCK1 is set as BUCK post-regulator we have the same behavior as above, except that:

- In case of UV fault, RESET_B is asserted according to OTP reset activation and power up sequence. If PGND1 ground loss occurs, the regulator is turned OFF and the FAULT pin is asserted. RESET_B is

asserted according to OTP reset activation and power up sequence. Until the fault is present and stored any tentative of turning on the regulator is ignored. BUCK1 can be turned on again after the fault removal and a Read & Clear cycle.

If this regulator is disabled and not used, VREG1_S and PGND1 pins should be connected to ground.

4.2.3 Pre regulator BUCK2

BUCK2 regulator operates using constant frequency peak current mode control. According to OTP selection about Main BUCK, it can work as Main BUCK pre-regulator (enabled by WKUP pin signal) or as post-regulator. The input voltage (VBAT2) is compatible to battery level (up to 32 V) and the overvoltage detection of VBAT2 (typ 32 V, available via SPI and enabled by default) can be disabled via SPI (enable by default condition). The switching frequency is set via OTP to 0.4/2.4 MHz with the possibility to have Spread Spectrum (enabled by default and disabled via SPI); a phase shift of 180° versus BUCK1 is internally generated. Output voltage is programmable with internal OTP cells to 8 possible values (5.0 V, 3.6 V, 3.3 V, 1.5 V, 1.35 V, 1.2 V, 1.1 V or 1.0 V). Over current protection can be set via OTP to 1.5 A or to 3 A. Soft start time and power stage driver slew rates (change in T_{rise} and T_{fall}) can be independently set via SPI. Compensation network is external.

BUCK2 regulator provides the following diagnostic:

- Monitor of the output voltage by an independent circuit for UV/OV detection: thresholds are set via SPI.
- Monitor of the Power Good thresholds is set via SPI (at 5/10% of VBUCK2) but the information is not available on the bus in active mode.
- Over Current Protection (with 2 selectable values by OTP) on High Side FET.
- Over Temperature detection by a local thermal sensor.
- PGND2 loss detection. An external schottky diode is necessary to protect the power stage in case of ground loss.

If BUCK2 is set as Main BUCK pre-regulator:

- If a UV/OV fault occurs then Fault pin is asserted and the corresponding fault bit is set inside the SPI register, where it can be read and cleared. RESET_B is always asserted in case of UV. In case of OV, it is possible to enable or disable the reset for all regulators together by OTP. The reset moves the device to REC state.
- If OT occurs, the power stage is switched OFF with a 16 µs filter time. The output decreases until UV is detected. The regulator goes in REC state and can restart only when OT flag is reset. The corresponding SPI bit is set and FAULT pin is asserted.
- The over current limitation is a cycle by cycle protection: when a fault happens for 7 consequent cycles, the FAULT pin is asserted and the corresponding fault bit is set inside the SPI register.
- If PGND2 ground loss occurs, all regulators are turned OFF, FAULT and RESET_B pins are asserted and the device goes back to REC state. Until the fault is present any tentative of turning on the regulator is ignored.

If BUCK2 is set as BUCK post-regulator we have the same behavior as above, except that:

- In case of UV fault, RESET_B is asserted according to OTP reset activation and power up sequence.
- If PGND2 ground loss occurs, the regulator is turned OFF and Fault pin is asserted. RESET_B is asserted according to OTP reset activation and power up sequence. Until the fault is present and stored any tentative of turning on the regulator is ignored. BUCK2 can be turned on again after the fault removal, Read & Clear cycle.

If this regulator is disabled and not used, VREG2_S and PGND2 pins should be connected to ground.

4.2.4 Post regulator BUCK3

BUCK3 regulator operates using constant frequency peak current mode control. The input voltage (VIN3) is compatible to the Main regulator output (up to 5.5 V). The switching frequency is 2.4 MHz with the possibility to have Spread Spectrum (enabled by default and disabled via SPI); a phase shift of 90 ° versus BUCK1 is internally generated. Output voltage is programmable via OTP cells to 8 possible values (3.3 V, 2.5 V, 2.3 V, 2.0 V, 1.8 V, 1.35 V, 1.2 V, or 1.0 V). The soft start time can be set via SPI. Compensation network is internal.

BUCK3 regulator provides the following diagnostic:

- Monitor of the output voltage by an independent circuit for UV/OV detection: thresholds are set via SPI.
- Monitor of the Power Good thresholds: are set via SPI (at 5/10% of VBUCK3) and the status is provided via SPI bit.

- Over Current Protection on High Side FET.
- Over Temperature detection by a local thermal sensor.
- PGND3 loss detection.

BUCK3 fault management:

- If a UV/OV fault occurs then the FAULT pin is asserted and the corresponding fault bit is set inside the SPI register, where it can be read and cleared. RESET_B is asserted in case of UV, according to OTP reset activation and power up sequence. In case of OV, it is possible to enable or disable the reset for all regulators together by OTP. The reset moves the device to REC state.
- If OT occurs, the power stage is switched OFF with a 16us filter time. The output decreases until UV is detected. The regulator goes in REC state and can restart only when OT flag is reset. The corresponding SPI bit is set and FAULT pin is asserted.
- The over current limitation is a cycle by cycle protection: if a fault happens for 7 consequent cycles, the FAULT pin is asserted and the corresponding fault bit is set in the SPI register.
- If PGND3 ground loss occurs, the regulator is turned OFF and the FAULT pin is asserted. RESET_B is asserted according to OTP reset activation and power up sequence. The device moves to REC state. Until the fault is present and stored any tentative of turning on the regulator is ignored. BUCK3 can be turned on again after the fault removal and a Read & Clear cycle.

If this regulator is disabled and not used, VREG3_S and PGND3 pins should be connected to ground.

4.2.5 Post regulator BUCK4

BUCK4 regulator operates using constant frequency peak current mode control. The input voltage (VIN4) is compatible to the Main regulator output up to 5.5 V. The switching frequency is 2.4 MHz with the possibility to have Spread Spectrum (enabled by default and disabled via SPI); a phase shift of 270 ° versus BUCK1 is internally generated. Output voltage is programmable with internal OTP cells to 8 possible values (3.3 V, 1.8 V, 1.35 V, 1.3 V, 1.25 V, 1.2 V, 1.12 V or 1.1 V). The soft start time can be set via SPI. Compensation network is internal.

BUCK4 regulator provides the following diagnostic:

- Monitor of the output voltage by an independent circuit for UV/OV detection: thresholds are set via SPI.
- Monitor of the Power Good thresholds: are set via SPI (at 5/10% of VBUCK4) and the status is provided via SPI bit.
- Over Current Protection on High Side FET.
- Over Temperature detection by a local Thermal sensor.
- PGND4 loss detection.

BUCK4 Fault management:

- If a UV/OV fault occurs then the FAULT pin is asserted and the corresponding fault bit is set inside the SPI register, where can be read and cleared. RESET_B is asserted in case of UV, according to OTP reset activation and power up sequence. In case of OV, it is possible to enable or disable the reset for all regulators together by OTP. The reset moves the device to REC state.
- If OT occurs, the power stage is switched OFF with a 16 µs filter time. The output decreases until UV is detected. The regulator goes in REC state and can restart only when OT flag is reset. The corresponding SPI bit is set and FAULT pin is asserted.
- Over current limitation is a cycle by cycle protection: if a fault happens for 7 consequent cycles the FAULT pin is asserted and the corresponding fault bit is set in the SPI register.
- If PGND4 ground loss occurs, the regulator is turned OFF and the FAULT pin is asserted. RESET_B is asserted according to OTP reset activation and power up sequence. The device moves to REC state. Until the fault is present and stored any tentative of turning on the regulator is ignored. BUCK4 can be turned on again after the fault removal, Read & Clear cycle.

If this regulator is disabled and not used, VREG4_S and PGND4 pins should be connected to ground.

4.2.6 BOOST

BOOST regulator is a converter running at 2.4 MHz that provides a nominal voltage of 5 V/7 V (selectable via OTP). Spread Spectrum on PWM is enabled by default and disabled via SPI; a phase shift of 270° versus BUCK1 is internally generated. Soft start time is programmed via SPI. Compensation network is internal.

BOOST regulator provides the following diagnostic:

- Monitor of the output voltage by an independent circuit for UV/OV detection.
- Monitor of the Power Good: thresholds status provided via SPI bit.
- Over Current Protection.
- Over Temperature detection by a local thermal sensor.
- PGND5 loss detection.

BOOST Fault management:

- If a UV/OV fault occurs the FAULT pin is asserted and the fault bit is set in the SPI register, where it can be read and cleared.
- If OT occurs, the power stage is switched OFF with a 16 µs filter time. The output decreases until UV is detected. The regulator goes in REC state and can restart only when OT flag is reset. The corresponding SPI bit is set and FAULT pin is asserted.
- Over current limitation is a cycle by cycle protection: if the fault happens for 7 consequent cycles, the FAULT pin is asserted and the corresponding fault bit is set in the SPI register.
- If PGND5 ground loss occurs, the BOOST is turned OFF and FAULT pin is asserted. Until the fault is present and stored any tentative of turning on the regulator is ignored. BOOST can be turned on again after the fault removal, and a Read & Clear cycle.

If this regulator is disabled and not used, VBOOST_S and PGND5 pins should be connected to ground.

4.2.7 LDO

LDO is a low drop out linear regulator with 8 programmable output voltages (5.0 V, 3.3 V, 2.8 V, 2.5 V, 1.8 V, 1.3 V, 1.25 V or 1.2 V) through OTP cell. The input voltage (VSLDO) is compatible to main regulator output (up to 5.5 V).

LDO regulator provides the following diagnostic:

- Programmable Over Current limitation in case of over-load or short to ground. Programmable.
- Monitor of the output voltage is monitored by an independent circuit for UV/OV detection.
- Over Temperature detection by a local thermal sensor.

LDO Fault management:

- In case of OV, the power stage is turned off, the fault SPI bit is set and the FAULT pin is asserted. The power stage is turned on again after a Read & Clear cycle. RESET_B is asserted if enabled by OTP, and it moves the device to REC state.
- In case of UV, the SPI bit is set and the FAULT pin is asserted. RESET_B is asserted, according to OTP reset activation and power up sequence, and moves the device to REC state.
- If OT occurs, the LDO is switched OFF with a 16 µs filter time. The output decreases until UV is detected. The regulator goes in REC state and can restart only when OT flag is reset. The corresponding SPI bit is set and FAULT pin is asserted.

4.2.8 VREF

L5965 includes a 1% precise voltage reference output to supply a system ADC. Output voltage can be selected via OTP cell (4.1 V, 3.3 V, 2.5 V or 1.8 V).

VREF provides the following diagnostic:

- Over Current limitation in case of over-load or short to ground.
- Monitor of the output voltage by an independent circuit for UV/OV detection.

VREF Fault management:

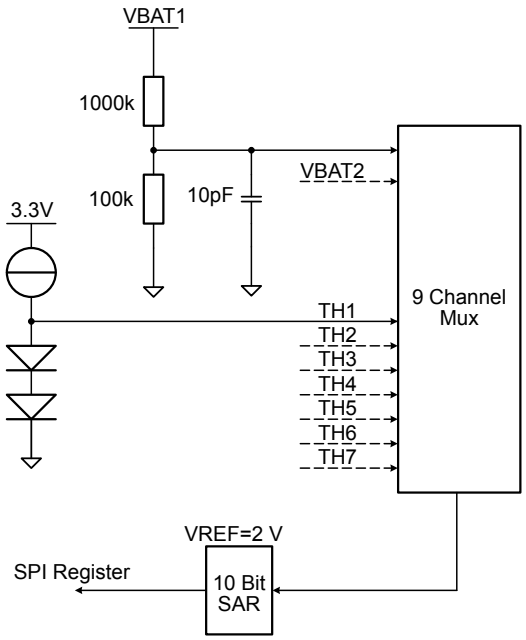
- In case of OV, the power stage is turned off, the fault SPI bit is set and the FAULT pin is asserted. The power stage is turned on again after a Read & Clear cycle.
- In case of UV, the fault SPI bit is set and the FAULT pin is asserted.
- In case of OC on VREF for 4 ms, the SPI register fault bit is set and VREF turns off. The FAULT pin is asserted. VREF turns on again when OC is removed.

4.2.9 ADC

L5965 includes an Analog to Digital converter (10 bit SAR) to provide via SPI a digital information on internal local thermal sensors (divided in Thermal Clusters THCL) VBAT1 and VBAT2. The voltages are provided sequentially by an analog multiplexer and converted with a t_{con} conversion time: therefore, an update of the ADC value is available every t_{con}*9.

The ADC works only in ACTIVE mode. Out of active mode, ADC value of thermal sensors is 10'b1, ADC value of VBAT1/VBAT2 is 10'b0.

Figure 10. ADC circuit



The Thermal Clusters are seven: six are dedicated to every regulators (TH1 → VREG, TH2 → BUCK1, TH3 → BUCK2, TH4 → BUCK3, TH5 → BUCK4 and BOOST, TH6 → LDO) and one at the center of the die, TH7.

In case of OT, the FAULT pin is asserted.

4.2.10 Wake up pin (WKUP)

The WKUP pin has an internal pulldown resistance. The maximum voltage this pin can sustain is limited to 40 V. A higher voltage compliance level in the application can be achieved by applying an external series resistor between the WKUP pin and the external wake-up signal.

- When the device is in STANDBY mode, it can be activated by a voltage above V_{WAKE_ON} threshold, with a minimum duration of t_{WAKE_FILTER}.
- The device can be moved to STANDBY mode, applying a voltage below V_{WAKE_OFF} threshold, with a minimum pulse width of t_{WAKE_FILTER}.

4.2.11 Synchronizing pin (SYNC in/out)

The user can provide an external clock on SYNCIN pin (higher than 1.8 MHz) in order to change the switching frequency of the internal regulators (Buck1,Buck2, Buck3, Buck4 and Boost).

In case an external clock is not provided, SYNCIN can be left floating (with inner pull-down resistor). All regulators work at their default switching frequency or, for Buck2, the frequency selected by OTP.

When a clock at f_{syncin} frequency is provided on SYNCIN pin:

- Buck1 works at $f_{syncin}/6$ if f_{syncin}>1.8 MHz or 400 kHz (default switching frequency) if f_{syncin}<1.2 MHz.
- Buck3, Buck4 and Boost work at f_{syncin} if f_{syncin}>1.8 MHz or 2.4 MHz (default switching frequency) if f_{syncin}<1.2 MHz.
- When the frequency of Buck2 is set to 2.4 MHz by OTP, Buck2 works at f_{syncin} if f_{syncin}>1.8 MHz or 2.4 MHz (default switching frequency) if f_{syncin}<1.2 MHz.
- When frequency of Buck2 is set to 400 kHz by OTP, Buck2 works at $f_{syncin}/6$ if f_{syncin}>1.8 MHz or 400 kHz (default switching frequency) if f_{syncin}<1.2 MHz.

Figure 11. **SYNC IN/OUT in Active mode**

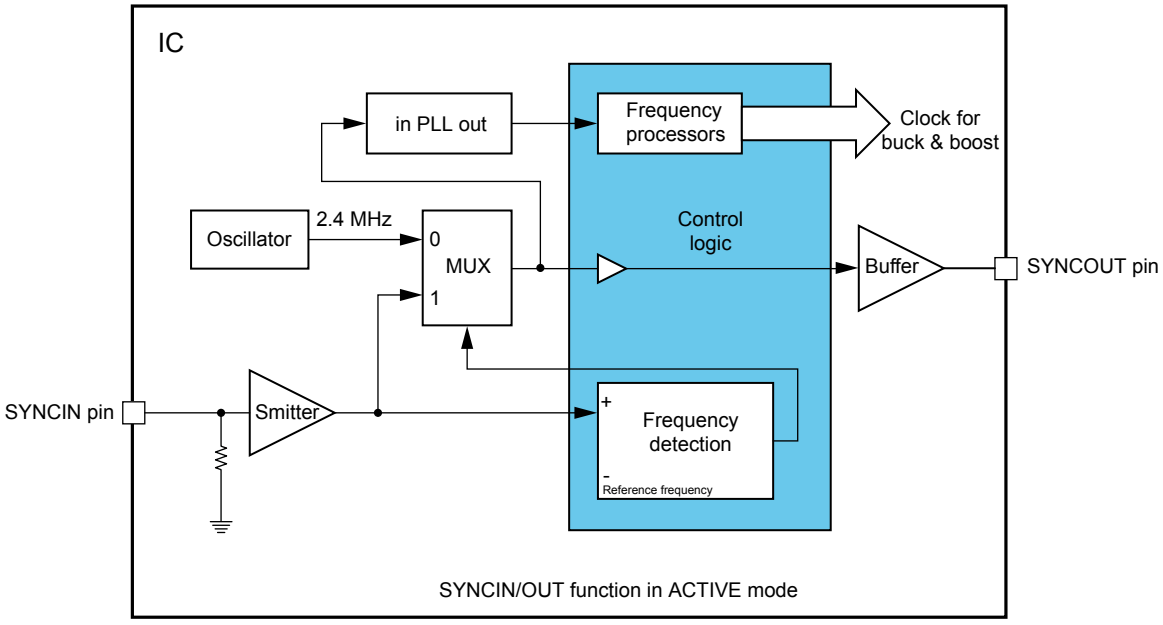


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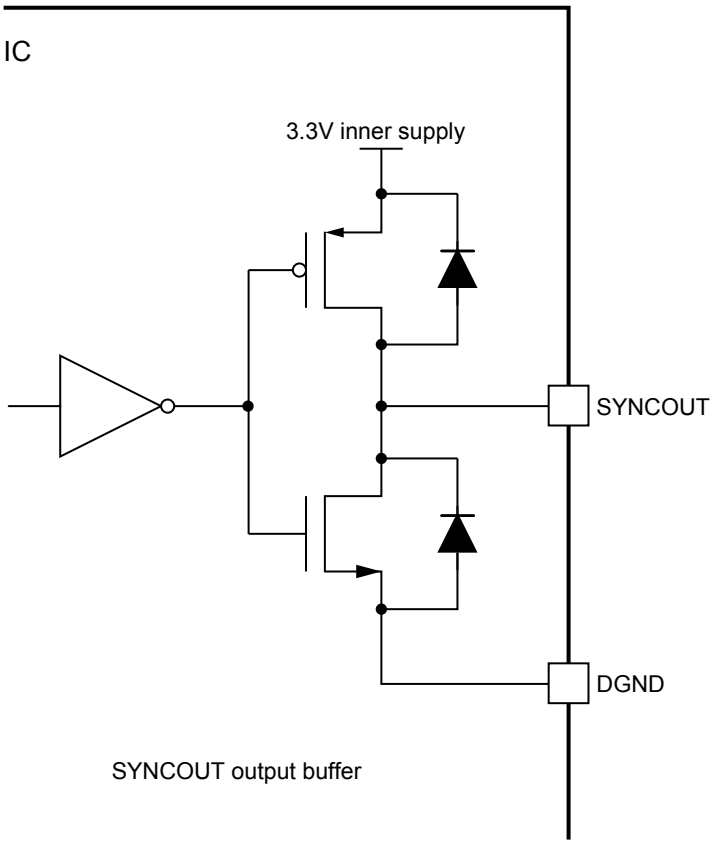
Figure 12. **SYNCOUT output buffer**



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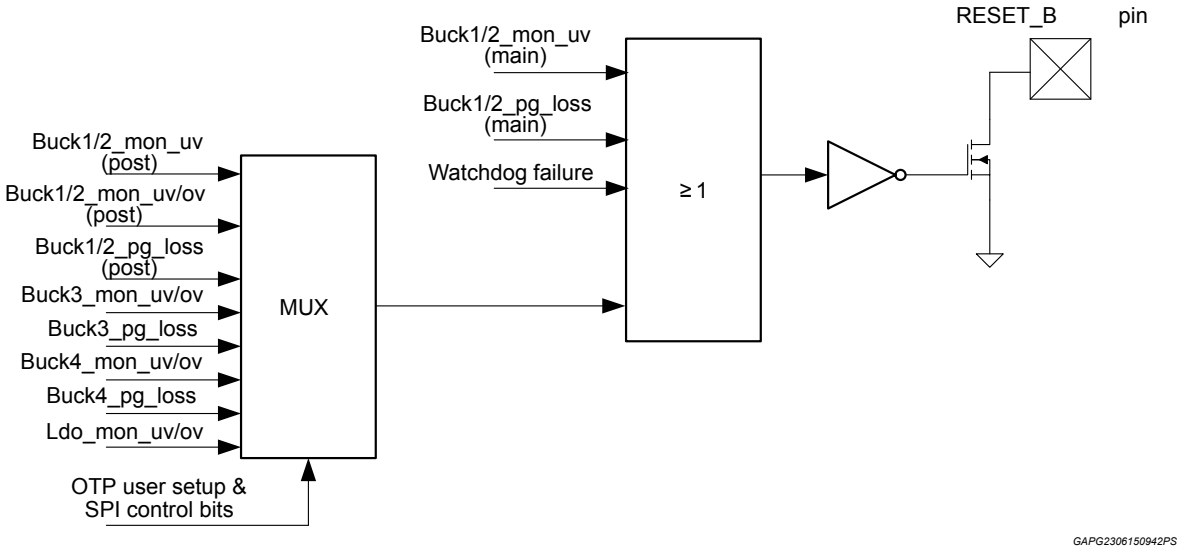
4.2.12 Reset and Fault

In ACTIVE mode, a reset signal is generated by L5965 at RESET_B pin in case of UV, OV if enabled by OTP, PG loss on Main regulator and Watchdog failure (wrong trigger of WD). Every regulator that can issue a reset, moves the device to REC state. Reset behavior at Power Up phase is fully described in Section 6 Device operating mode.

Figure 13. Reset circuit diagram in ACTIVE mode



A loss of ground (PGLOSS) asserts RESET_B with the following rules:

1. if the regulator is disabled by OTP, PGLOSS cannot assert RESET_B;
2. if the regulator is enabled by OTP, but it is not in the Reset Activation list, PGLOSS cannot assert RESET_B;
3. if the regulator is enabled by OTP and it is in the Reset Activation list, no matter if it is disabled by SPI, PGLOSS can assert RESET_B.

The undervoltage (UV) asserts RESET_B with the following rules:

- if the regulator is disabled by OTP, UV cannot assert RESET_B;
- if the regulator is enabled by OTP, but it is not in the Reset Activation list, UV cannot assert RESET_B;
- it the regulator is enabled by OTP and it is in the Reset Activation list, but it is disabled by SPI, UV cannot assert RESET_B;
- if the regulator is enabled by OTP, it is in the Reset Activation list and it is not disabled by SPI, UV can assert RESET_B.

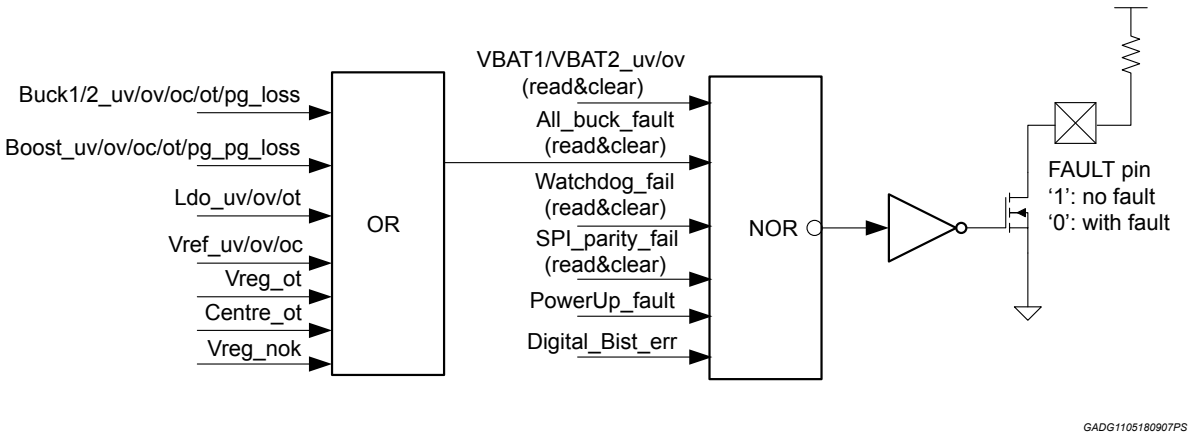
The overvoltage (OV) asserts RESET_B in a similar way as the undervoltage, with this additional condition:

- if OvRst_EN is set to 0 through OTP, the OV cannot assert RESET_B.

A FAULT signal is generated in active mode in case of a fault, as shown in Figure 14.

- "SPI_parity_fail" refers SPI_PAR_FAIL, Bit2 of SPI fault STAT
- "PowerUp fault" is an error generated by regulators during power-up phase:
  - each regulator should complete its own power-up phase up to the power good signal within 20 ms
- "Digital_Bist_err" is an error generated by one of the following checks:
  - Buck clock generation
  - Logic diagnostics circuit
  - Main State Machine

Figure 14. **Fault function in active mode**



In order to avoid triggering RESET and FAULT during the soft start time, the UV is masked when regulators (BUCK1/2/3/4, BOOST, LDO and VREF) are going to be enabled. The masking time is given by the following table.

Table 7. **UV masking time**

Regulator	Masking time (ms typ.)
BUCK1	5
BUCK2	5
BUCK3	5
BUCK4	5
BOOST	5
VREF	0.5
LDO	0.5
VREG	0.5

4.2.13 Configurable watchdog and reset

During normal operation, the watchdog monitors the microcontroller within a programmable trigger cycle. When the device is in ACTIVE mode, which means the power up phase has been correctly performed and RESET_B signal has been released, the watchdog is started with a timeout (long open window TLW) to allow the microcontroller to run its own setup and then to start the window watchdog by setting an inner signal TRIG = 1. Subsequently, the micro controller has to serve the watchdog by providing the watchdog trigger bit TRIG within the safe trigger area TSW. The trigger time is configurable by SPI. A correct watchdog trigger signal immediately starts the next cycle. A wrong watchdog trigger causes a watchdog failure.

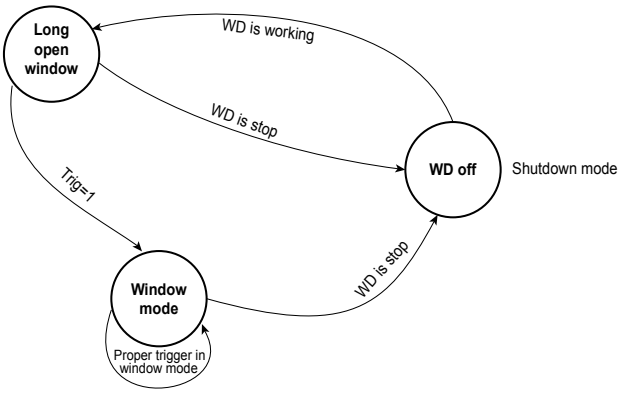
WDI signal can be ignored (by setting OTP bit) and SPI can be used as watchdog: in this case, a specific SPI register must be accessed and toggled by SPI within the watchdog window. If the register is not refreshed at the right time, a watchdog failure happens. In case of a watchdog failure, a RESET_B is always asserted, and the device goes to REC mode or keeps in ACTIVE mode depending on WD_REC_en OTP configuration.

If OTP_WD_REC_en = 1 the device goes to REC mode in case of WD failure, and WD is not more active until the ACTIVE mode is reached.

If OTP_WD_REC_en = 0, the device keeps in ACTIVE mode in case of WD failure, and WD is inactive for 280 ns (1 system clock cycle, not significant), then active again in Long open window, and RESET_B asserts a small pulse (typ 8 µs). Moving SPI_WD_REC_en = 1, the device behavior is the same as OTP_WD_REC_en = 1. Configuration with OTP_WD_REC_en = 0 is useful if voltages should be immediately active in order to initialize the system, regardless of the WD signal.

The following picture illustrates the watchdog behavior.

Figure 15. Watchdog behavior



WD is working when in ACTIVE mode and OTP bit is enabled

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The watchdog trigger time is configured by setting SPI. The change of this time is not limited to the Long Open Window. It can be changed also in "Window mode" state. However, it is suggested to write these bits only during the long window, in order to avoid watchdog failures. Besides, the first trigger time should be < TLW (160 ms), after that, next trigger should happen between (previous _Trigger_ time + TSW_min) and (previous _Trigger_ time + TSW_max).

Figure 16. Watchdog timing if WD_REC_en = 1

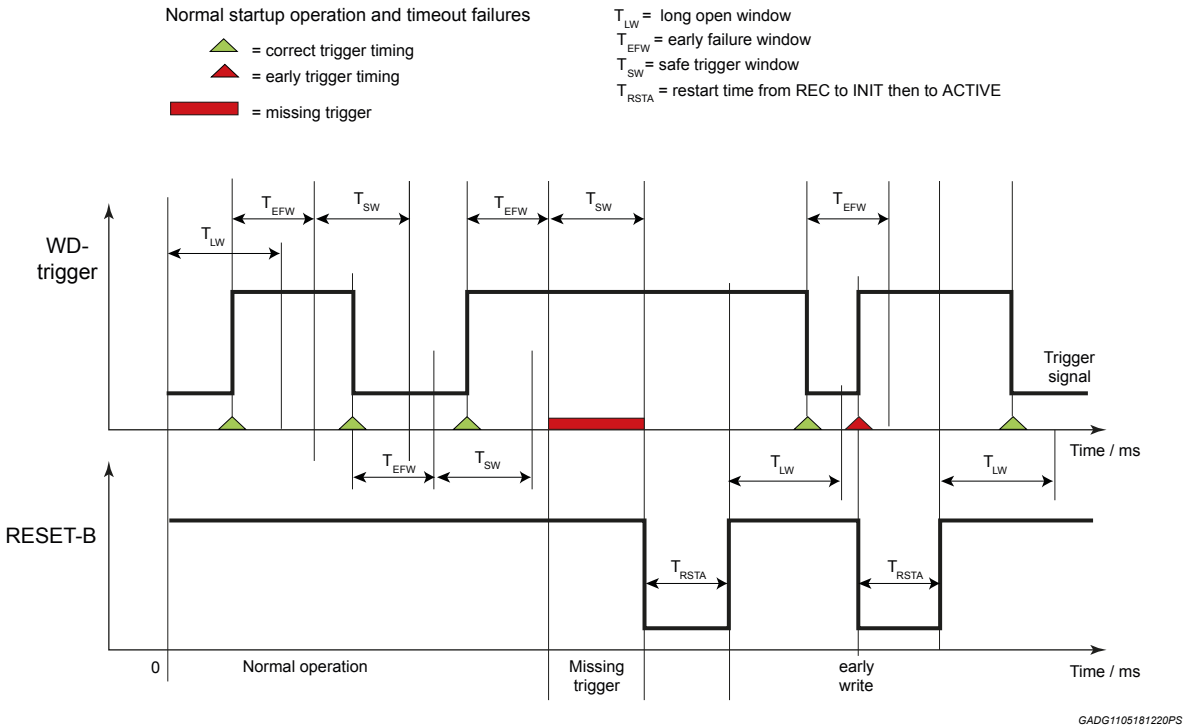

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Figure 17. Watchdog timing if WD_REC_en = 0

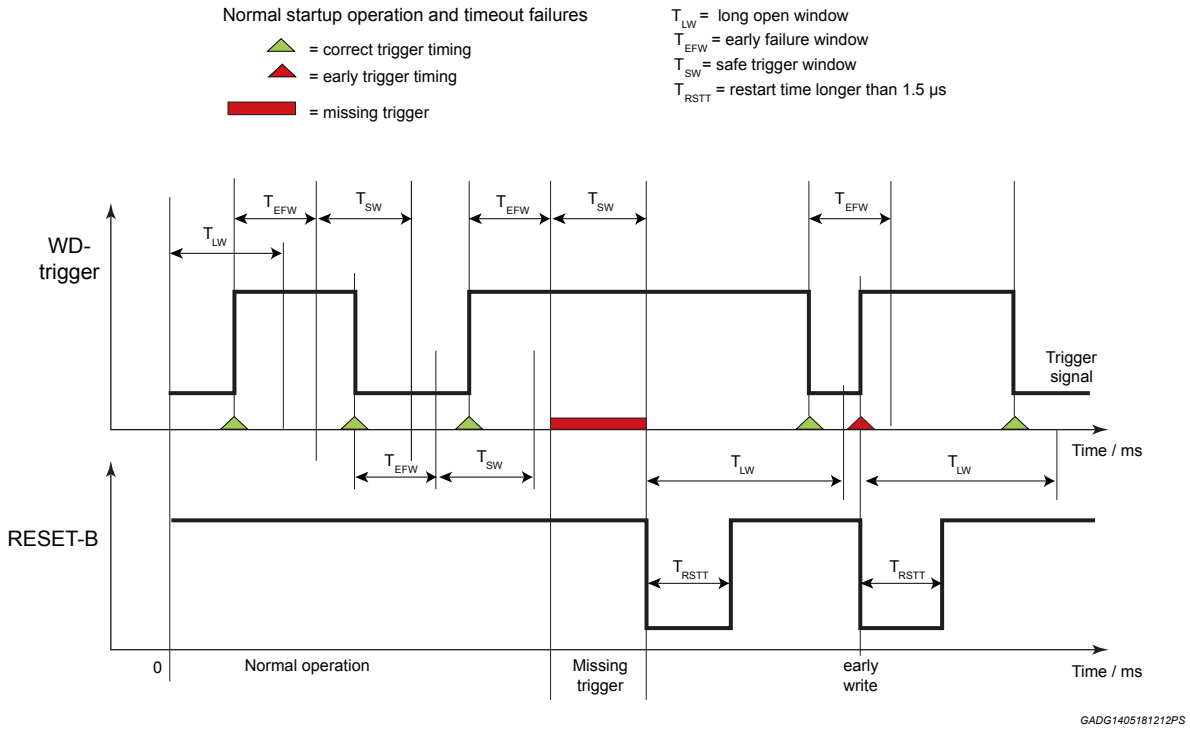
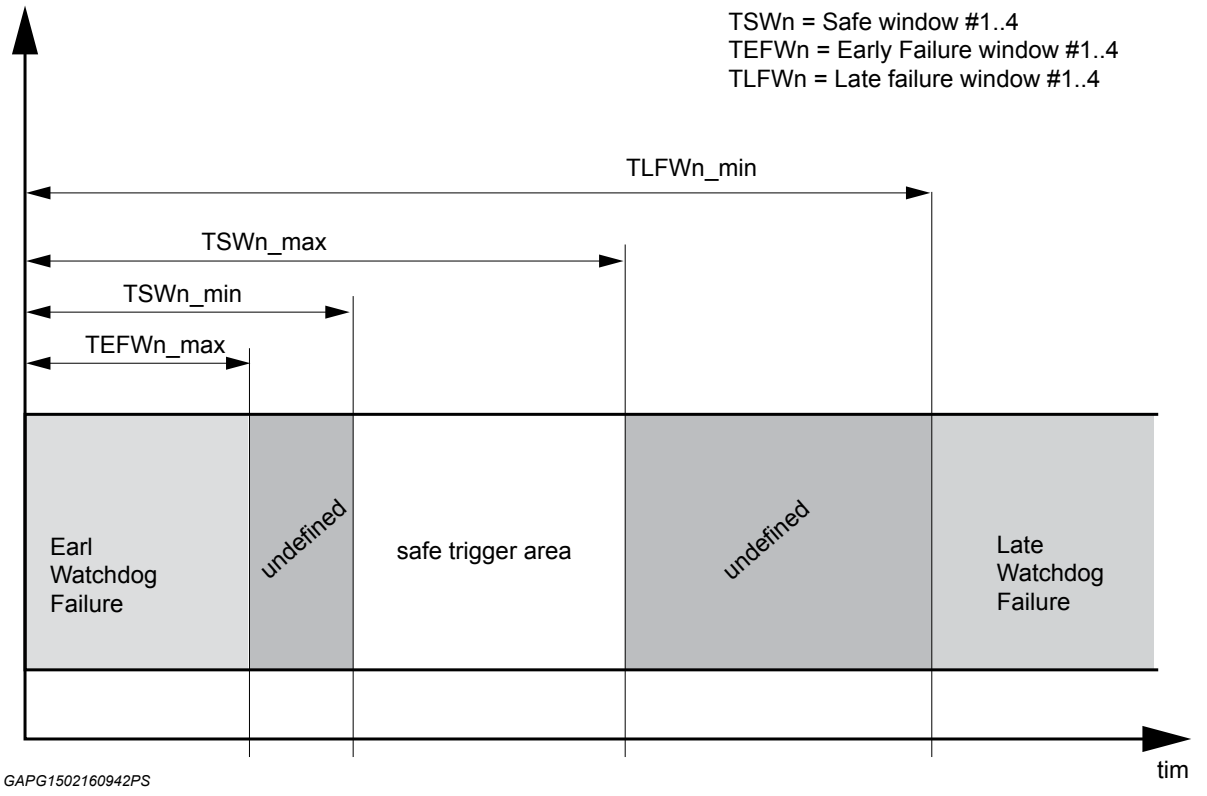


Figure 18. Watchdog Early, Safe and Late window diagram



4.2.14 Under-Voltage, Over-Voltage and Power-Good

All regulators are monitored, and Power-Good, Over-Voltage and Under-Voltage information is provided through SPI.

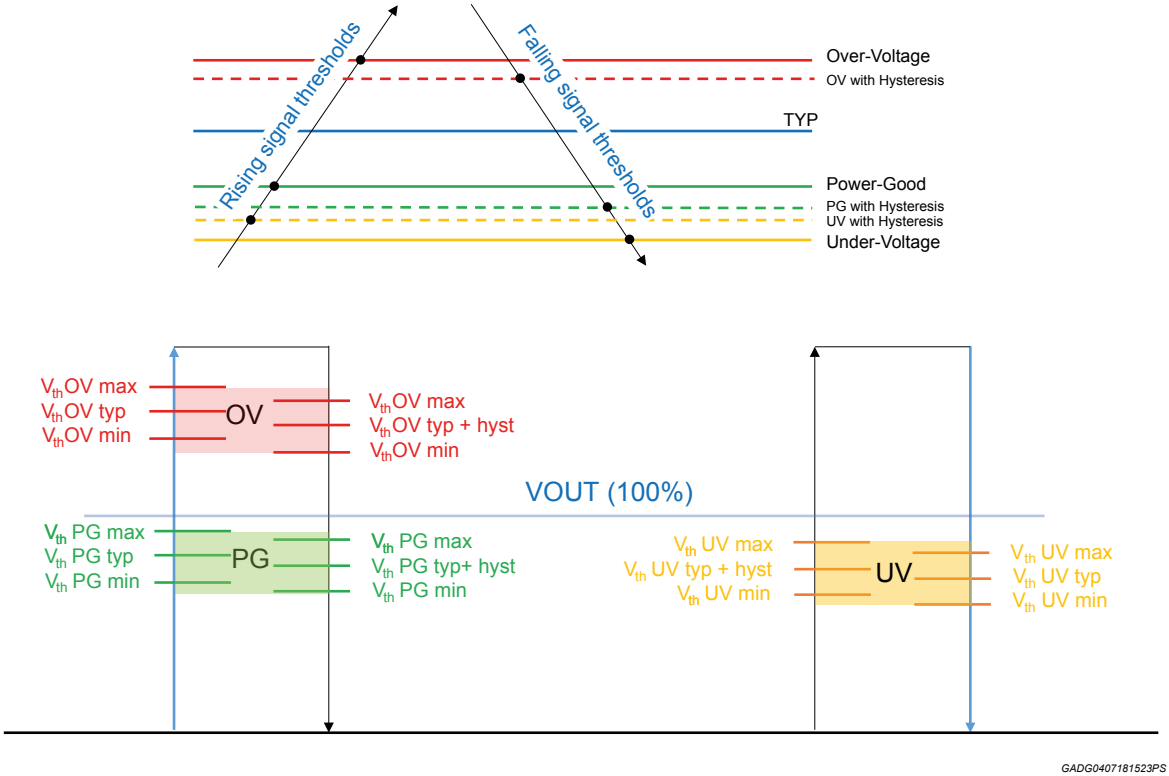
One SPI bit allows to select between two threshold options:

- UV/PG/OV of 91%, 95%, 108%
- UV/PG/OV of 86%, 90%, 113%

Over-voltage and Power-Good are checked when the signal is rising, the Under-Voltage is valid when the signal is falling.

The next figure shows the relationships among these monitors.

Figure 19. Output voltage and monitors



4.2.15 Temperature control and VBATx voltage through internal ADC

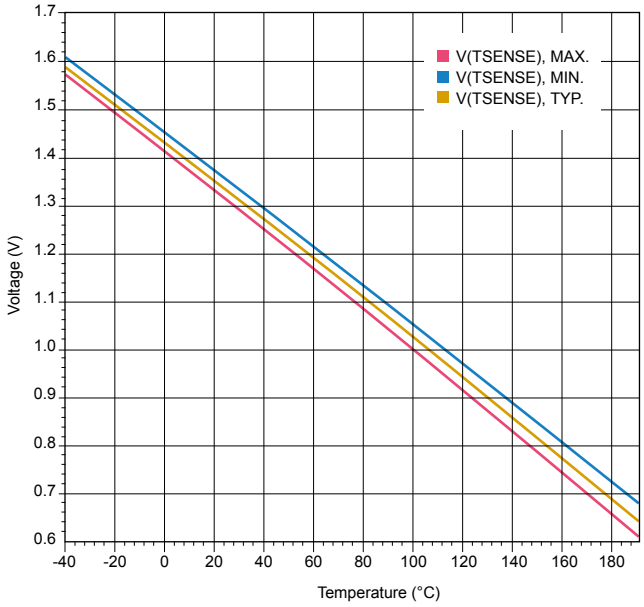
In order to provide an advanced on-chip temperature control, power outputs are grouped in 7clusters with dedicated thermal sensors. The sensors are suitably located on the device. In case the temperature of a cluster reaches the thermal shutdown threshold, the outputs assigned to this cluster are shut down (all other outputs remain active). The central cluster only asserts the FAULT pin. Each output cluster has a dedicated temperature warning and shutdown flag and the cluster temperature can be read out by SPI.

Next table shows voltages referred to ground and currents are assumed positive when the current flows into the pin. T_j = -40 °C to 130 °C.

Table 8. Temperature diode characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{TROOM1-7}$	T_{SENSE} output voltage at 25 °C	T = 25 °C		1.335		V
$TC_{TSENSE1-7}$	Temperature coefficient for T_{SENSE} output voltage	T = 25 °C; T = 130 °C; T = -40 °C		-4		mV/K

Figure 20. VTSENSE vs. temperature



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Cluster temperatures information is available in SPI registers and can be calculated from the binary coded register value using the following formula:

$$Decimal = V_{TSENSE} \times \left(\frac{1024}{V_{REFADC}}\right) - 1 \quad (1)$$

$$V_{TSENSE} = V_{TROOM} + \left(T_j - 25\right) \times TC_{TSENSE} \quad (2)$$

Starting from the following values:

$$Decimal = \frac{\left(358.26 - T_j\right)}{0.488} \quad (3)$$

$$T_j = 358.26 - Decimal \times 0.488 \quad (4)$$

We can get this information:

T = -40 °C → decimal code is 816 (0x330, read out from SPI register)

T = 25 °C → decimal code is 683 (0x2AB, read out from SPI register)

Read out SPI register 0x330, means the decimal is 816 → T = -40 °C

Read out SPI register 0x2AB, means the decimal is 683 → T = 25 °C

Also VBATx can be read from 0 to 22 V (above 22 V the ADC output doesn't change):

$$Decimal = 46.55 \times V_{BATx(x=1,2)} - 1 \quad (5)$$

$$V_{BATx} = \frac{decimal + 1}{46.55} \quad (6)$$

Example:

V_{BAT1} = 14 V→ decimal code is 651 (0x28B, read out from SPI register)

Read out SPI register 0x28B, means the decimal is 65 → V_{BAT1} = 14 V

4.2.16 Maximum Duty Cycle and Refresh Mode for Buck

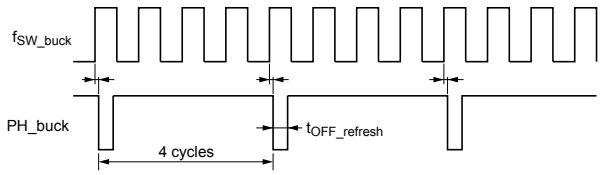
The high-side N-channel MOSFET is turned on at the beginning of each clock cycle and kept on until the inductor current reaches its peak value as set by the regulation loop. Once the high side power is turned OFF, and after a small delay (shoot-through delay), the lower N-channel MOSFET is turned on until the start of the next clock cycle.

In dropout operation the high-side MOSFET can stay on 100%. To ensure the bootstrap capacitor is recharged, the buck low-side power is forced off time (140ns) per 4 cycles. It is called “refresh mode”. This forced OFF time limits the maximum duty cycle of the buck to:

$$D_{\max} = 1 - f_{sw} \cdot t_{OFF} \cdot 0.25 \quad (7)$$

The actual maximum duty cycle varies with the switching frequency.

Figure 21. Refresh mode in bucks



4.2.17 Frequency-Hopping Spread Spectrum

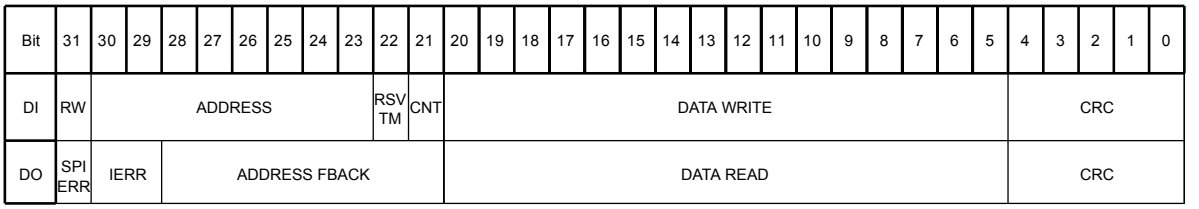
L5965 features a pseudo-random spectrum for 2.4 MHz switching frequency, and a triangular spread architecture for 400 kHz switching frequency. The frequency shifts only by one step at each cycle to avoid large jumps in bucks and boost switching frequencies.

5 SPI format and register mapping

A 32-bit SPI bus is used for bi-directional communication with the microcontroller, for functional and test purpose. A write operation leads to a modification of the addressed data by the payload if a write access is allowed (e.g. control register, valid data). A read operation (based on previous communication request) shifts out the data present in the addressed register (out of frame data exchange protocol).

A Read & Clear Operation will lead to a clear of addressed status bits. The bits to be cleared are defined first by payload bits set to 0. The SPI word is represented in the below figure.

Figure 22. SPI word representation



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DI Stream:

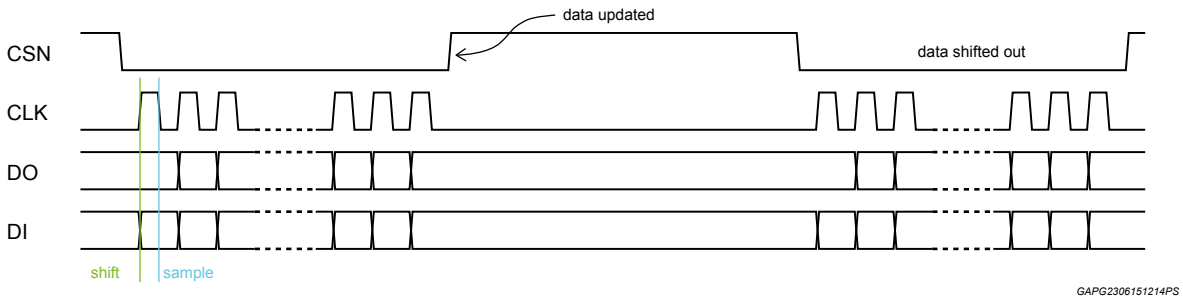
- Bit 31: R/W flag. To select read (0) or write (1) operation
- Bit 30-23: SPI register address
- Bit 22: Test Mode flag
- Bit 21: Frame counter (0/1). After Power-on reset, this bit must be '0'. The bit must be toggled according to the previous SPI CNT bit.
- Bit 20-5: Data to be written at selected address
- Bit 4-0: CRC code

DO Stream:

- Bit 31: Previous SPI communication Error (CRC error, Too long frame, Too short frame, frame count error, SPI error, CSN low time out)(*)
- Bit 30:RSTB(*)
- Bit 29: FAULT(*)
- Bit 28:21: SPI register address (related to the previous transmission)
- Bit 20-5: Data read at selected address (related to previous transmission)
- Bit 4-0: CRC code

Note: (*) bit 29 and bit 30 reflect the current status of RSTB pin and FAULT pin. Every time the relevant SPI register is accessed, an internal register will sample the current status of RSTB and FAULT pins, store them, then shift them out on SPI DO frame at next SPI access. If RSTB and Fault bits in ACTIVE mode are `1' , it means there's no reset and no fault.

Figure 23. **SPI diagram**

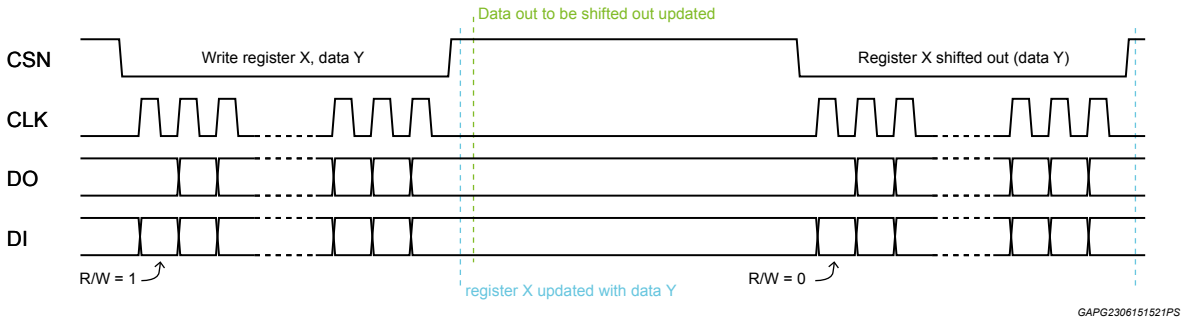


DO is sampled by the microcontroller on CLK falling edge, DI is sampled by L5965 on CLK falling edge. In case of writing operation selected, internal register is updated at CSN rising edge.

In the below figure SPI protocol is shown:

- 1st Frame: Write Access on RW Register X → Register X is updated at the end of the frame.
- After the update of register X, the data out shift register is updated too.
- 2nd Frame: Read Access → Register X with data Y is shifted out on MISO.
- Register X is not updated because the R/W bit is LOW.
- The data out shift register is updated with the same data.

Figure 24. **SPI protocol diagram**



To detect frame losses/non-refreshment, Bit21 of DI frame must have opposite values in sequential frames. If a static fault (stuck-at) or cross-talk occurs, the communication data received would not pass the CRC check and will be discarded: FAULT pin is asserted.

If SPI communication has some errors (no matter to which register), the write in data is discarded. In the next SPI communication, DO will automatically read out 0x1D register address and data-in order to give details on SPI error.

Table 9. **Input CSN**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CSNLOW}	Input voltage low level	Normal mode	–	–	1	V
$V_{CSNHIGH}$	Input voltage high level	Normal mode	2.3	–	–	V
V_{CSNHYS}	$V_{CSNHIGH}$ - V_{CSNLOW}	Normal mode	0.2	0.4	–	V
I_{CSNPU}	Internal pull up resistor	Normal mode	–	800	–	kΩ

Table 10. Input CLK, DI

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{in\ L}$	Input low level	–	–	–	1	V
$V_{in\ H}$	Input high level	–	2.3	–	–	V
$V_{in\ Hyst}$	Input hysteresis	–	0.2	0.4	–	V
I_{in}	Pull down current at input	V_{in} = 1.5 V	3	7	12	µ A
C_{in}	Input capacitance at input pins CSN, CLK, DI	Guaranteed by design	–	–	15	pF
f_{CLK}	SPI input frequency at CLK	–	–	–	1	MHz

Table 11. DI, CLK and CSN timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{CLK}	Clock period	–	1000	–	–	ns
t_{CLKH}	Clock high time	–	400	–	–	ns
t_{CLKL}	Clock low time	–	400	–	–	ns
$t_{set\ CSN}$	CSN setup time, CSN low before rising edge of CLK	–	500	–	–	ns
$t_{set\ CLK}$	CLK setup time, CLK high before rising edge of CSN	–	500	–	–	ns
$t_{set\ DI}$	DI setup time	–	25	–	–	ns
$t_{hold\ DI}$	DI hold time	–	25	–	–	ns
$t_{r\ in}$	Rise time of input signal DI, CLK, CSN	–	–	–	25	ns
$t_{f\ in}$	Fall time of input signal DI, CLK, CSN	–	–	–	25	ns

Table 12. Output DO

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DOL}	Output low level	I_{DO} = -4 mA	–	–	0.3	V
I_{DOLK}	Open Drain leakage current	When DO output=high	-5	–	5	µA
C_{DO}	Open Drain input capacitance	Guaranteed by design	–	10	15	pF

Table 13. CSN timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{CSN\_HI,min}$	Minimum CSN high time Active mode	Transfer of SPI-command to Input Register	6	–	–	µs
$t_{CSNfail}$	CSN low timeout	–	20	35	50	ms

5.1 SPI frame CRC generator

The SPI protocol is defined by frames of 32 bits with 5 bits of CRC (Cyclic Redundancy Check) in both input and output directions. The polynomial calculation implemented is:

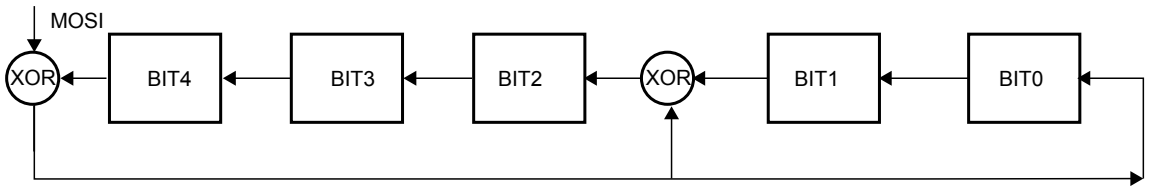
g(x)= x^5 + x^2 + 1

the structure of CRC generator is shown in Figure 25. Structure of CRC generator.

Here are the rules:

1. For DI, CNT=DI[21] is ignored when calculating CRC, it means only {DI[31:22],DI[20:5]} is used to calculate CRC. For example, if DI[31:5]=27‘b1000_0010_1011_1111_1111_1111_111, the CRC[4:0]= 5‘b0_0011
2. For DO, DO[21] is ignored when calculating CRC, it means only {DO[31:22],DO[20:5]} is used to calculate CRC.
3. The initial value of CRC generator is 5'b1_1111.
4. MSB (DI[31]) is shift in CRC generator at first.

Figure 25. Structure of CRC generator



5.2 SPI registers mapping

When registers are not written, their default state is the one shown in the respective map.

5.2.1 SPI REG BUCK1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					BUCK1_SSCLK_SEL		RESERVED		BUCK1_BLANKTIME			BUCK1_SPREAD_EN	BUCK1_XTH	BUCK1_CUR_MAX	RESERVED
R	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Address 0x00

BUCK1_CUR_MAX: Driver max output current (see BUCK1 GATE Driver)

BUCK1_XTH: OV/UV/PG threshold setting (see Power output UV/OV monitor, Power Good)

BUCK1_SPREAD_EN: Spread spectrum enable

BUCK1_BLANKTIME: Output power stage blanking time (see tprogramming_dead_BUCK1)

BUCK1_SSCLK_SEL: SoftStart time selection (see tSOFTSTART_BUCK1)

5.2.2 SPI REG BUCK2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					BUCK2_SSCLK_SEL		RESERVED			BUCK2_OUTPUT_SR		BUCK2_SPREAD_EN	BUCK2_XTH	RESERVED	RESERVED
R	R	R	R	R	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Address 0x01

BUCK2_XTH: OV/UV/PG threshold setting (see Power output UV/OV monitor, Power Good)

BUCK2_SPREAD_EN: Spread spectrum enable

BUCK2_OUTPUT_SR: Output stage slew rate (see tSR_PH2)

BUCK2_SSCLK_SEL: SoftStart time selection (see tSOFTSTART_BUCK2)

5.2.3 SPI REG WD_REC_EN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											SPI_WD_REC_EN	RESERVED			
R	R	R	R	R	R	R	R	R	R		R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Address 0x02

SPI_WD_REC_EN: In case OTP_WD_REC_EN=1, WD failure asserts RESET_B and makes FSM go to REC state.

5.2.4 SPI REG BUCK4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					BUCK4_SSCLK_SEL		RESERVED					BUCK4_SPREAD_EN	BUCK4_XTH	RESERVED	RESERVED
R	R	R	R	R	R/W	R/W	R	R	R	R	R	R/W	R/W	R	R
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Address 0x03

BUCK4_XTH: OV/UV/PG threshold setting (see Power output UV/OV monitor, Power Good)

BUCK4_SPREAD_EN: Spread spectrum enable

BUCK3_SSCLK_SEL: SoftStart time selection (see tSOFTSTART_BUCK4)

5.2.5 SPI REG BOOST VREF

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					BOOST_SSCLK_SE		RESERVED	LDO_XTH	RESERVED			BOOST_SPREAD_EN	BOOST_XTH	VREF_XTH	RESERVED
R	R	R	R	R	R/W	R/W	R	R/W	R	R	R	R/W	R/W	R/W	R
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Address 0x04

VREF_XTH: OV/UV/PG threshold setting (see Power output UV/OV monitor, Power Good)

BOOST_XTH: OV/UV/PG threshold (see Power output UV/OV monitor, Power Good)

BOOST_SPREAD_EN: Boost spread spectrum enable

LDO_XTH: OV/UV/PG threshold setting (see Power output UV/OV monitor, Power Good)

BOOST_SSCLK_SEL: Boost SoftStart time selection (see tSS_BOOST)

5.2.6 SPI REG BUCK EN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VBAT2_EN	VBAT1_EN	RESERVED							VREF_EN	LDO_EN	BOOST_EN	BUCK4_EN	BUCK3_EN	BUCK2_EN	BUCK1_EN
R/W	R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address 0x05

VBAT1/2_EN: VBAT UV/OV detection Enable

(Others)_EN SPI Regulators Enable/Disable (only in ACTIVE Mode)

5.2.7 SPI REG WD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI_WDI	RESERVED							FAULT_TOGGLE			INF_RETRIAIL_EN	TWK_REC		WD_TWIN	
R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Address 0x06

WD_TWIN: WatchDog Window timer selection (see Watchdog trigger time)

TWK_REC: WKUP high duration timer selection (see WKUP)

INF_RETRIAL_EN: 0: finite restart trials
1: infinite restart trials (default)

FAULT_TOGGLE: fault pin toggle test bits

101: set fault pin 'low';
110: set fault pin 'high';

others: keep fault pin as original fault output.

SPI_WDI: If SPI bit is used as WatchDog Input, SPI need to toggle this bit in WatchDog time windows. This bit has default value 0.

5.2.8 SPI REG BUCK STAT1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VREF_UV_STAT	LDO_UV_STAT	BOOST_UV_STAT	BUCK4_UV_STAT	BUCK3_UV_STAT	VREF_OC_4MS_STAT	BUCK2_OT_STAT	BUCK2_OC_STAT	BUCK2_UV_STAT	BUCK2_OV_STAT	BUCK2_GLOSS_STAT	BUCK1_OT_STAT	BUCK1_OC_STAT	BUCK1_UV_STAT	BUCK1_OV_STAT	BUCK1_GLOSS_STAT
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address 0x10

[15:0] '0' means no fault present: read&clear bits

5.2.9 SPI REG BUCK STAT2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CENTER_OT_STAT	LDO_OT_STAT	VREG_OT_STAT	BUCK4_OT_STAT	BUCK3_OT_STAT	BOOST_OC_STAT	BUCK4_OC_STAT	BUCK3_OC_STAT	VREF_OV_STAT	LDO_OV_STAT	BOOST_OV_STAT	BUCK4_OV_STAT	BUCK3_OV_STAT	BOOST_GLOSS_STAT	BUCK4_GLOSS_STAT	BUCK3_GLOSS_STAT
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address 0x11

[15:0] 0: means no fault present: read & clear bits

5.2.10 SPI REG Fault Table PWUP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LBIST_ERR	SAF_CRC_FAILED	ABSIT_ERR	WD_FAIL	RESERVED	REC_CNT		VREG_NOK_STAT	RESERVED	VREF_POWERUP_FAULT	BOOST_POWERUP_FAULT	LDO_POWERUP_FAULT	BUCK4_POWERUP_FAULT	BUCK3_POWERUP_FAULT	BUCK2_POWERUP_FAULT	BUCK1_POWERUP_FAULT
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address 0x12

XX_POWERUP_FAULT: 1: means Power-on failed
0: means Power-on succeeded or regulator disabled by OTP

VREG_NOK_STAT: Vreg not ok state; read and clear.

0: vreg ok;
1: vreg not ok

REC_CNT: the counter of times that FSM into REC; will be cleared in STANDBY. If inf_retrail_en=1, REC_CNT is always 0.

RESERVED (Bit11): this bit is reporting the internal PLL locking status. When "1", the output frequency of the PLL is locked and stable. When "0", the PLL is not yet stable or off.

WD_FAIL: watchdog fail flag, read and clear; Include normal WDI WD or SPI WD.

0: no fail
1: fail

ABIST_ERR: ABist fail flag, read only.

0: no fail
1: fail

SAF_CRC_FAILED: read only.

0: no fail
1: fail

LBIST_ERR: read only.

0: no fail
1: fail

5.2.11 SPI REG ADC TH1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						ADC_TH1									
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Address 0x13

ADC_TH1: ADC bits output for TH1 cluster (VREG); read only

5.2.12 SPI REG ADC TH2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						ADC_TH2									
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Address 0x14

ADC_TH2: ADC bits output for TH2 cluster (BUCK1); read only

5.2.13 SPI REG ADC TH3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						ADC_TH3									
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Address 0x15

ADC_TH3: ADC bits output for TH3 cluster (BUCK2); read only

5.2.14 SPI REG ADC TH4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						ADC_TH4									
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Address 0x16

ADC_TH4 ADC bits output for TH4 cluster (BUCK3); read only

5.2.15 SPI REG ADC TH5

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						ADC_TH5									
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Address 0x17

ADC_TH5: ADC bits output for TH5 cluster (BUCK4 and BOOST); read only

5.2.16 SPI REG ADC TH6

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						ADC_TH6									
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Address 0x18

ADC_TH6: ADC bits output for TH6 cluster (LDO); read only

5.2.17 SPI REG ADC TH7

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						ADC_TH7									
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Address 0x19

ADC_TH7: ADC bits output for TH7 cluster (Center of the DIE); read only

5.2.18 SPI REG ADC VBAT1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				VBAT1_UV_STAT	VBAT1_OV_STAT	ADC_VBAT1									
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address 0x1A

ADC_VBAT1: ADC output for VBAT1 voltage (see Figure 10. ADC circuit); read only

VBAT1_OV_STAT: VBAT1 status; read & clear

VBAT1_UV_STAT: VBAT1 status; read & clear

5.2.19 SPI REG ADC VBAT2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				VBAT2_UV_STAT	VBAT2_OV_STAT	ADC_VBAT2									
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address 0x1B

ADC_VBAT2: ADC output for VBAT2 voltage (see Figure 10. ADC circuit); read only

VBAT2_OV_STAT: VBAT2 status; read&clear

VBAT2_UV_STAT: VBAT2 status; read&clear

5.2.20 SPI REG OT Warning

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									ADC_TH7_OT_Warning	ADC_TH6_OT_Warning	ADC_TH5_OT_Warning	ADC_TH4_OT_Warning	ADC_TH3_OT_Warning	ADC_TH2_OT_Warning	ADC_TH1_OT_Warning
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address 0x1C

[6:0] Thermal warning from all the Thermal Clusters; read & clear

5.2.21 SPI Fault STAT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										CSN_LOW_TIMEOUT_FAIL	SPI_ADDRESS_ERR	SPI_FRAME_CNT_FAULT	SPI_PAR_FAIL	SPI_FRAME_SHORT	SPI_FRAME_LONG
R										R	R	R	R	R	R
0										0	0	0	0	0	0

Address 0x1D

SPI_FRAME_LONG: SPI frame length error; read & clear

SPI_FRAME_SHORT: SPI frame length error; read & clear

SPI_PAR_FAIL: SPI frame CRC fail; read & clear

SPI_FRAME_CNT_FAULT: SPI frame error on Count bit; read & clear

SPI_ADDRESS_ERR: SPI frame address error; read & clear

CSN_LOW_TIMEOUT_FAIL: 0: Csn right;

1: Csn low time longer than 35 ms; read & clear

5.2.22 SPI Silicon Version

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSM_STATUS				FSM2REC			TOREC_REASON_FLAG					SILVERSION			
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address 0x20

SILVERSION: read only ("0000" means 'AA' version)

FSM_STATUS: read only

0001: Shutdown
0010: StandBy

0011: INIT
0100: RampUP_Main

0101: Secup
0110: Active

0111: Rec
1000: Test

1001: OTP_Prog

FSM2REC: read & clear. State machine status before going into REC mode.

000: default value after reset release or R&C;

001: INIT, means the state machine moved from INIT mode to REC mode;
010: RAMPUP MAIN, means the state machine moved from RAMPUP MAIN mode to REC mode;

011: SECUP, means the state machine moved from SECUP mode to REC mode;
100: ACTIVE, means the state machine moved from ACTIVE mode to REC mode;

TOREC_REASON_FLAG: read & clear. The reason that make state machine jump to REC.

When FSM2REC is INIT:

Bit4 = 1: lbist_fail flag makes state machine from INIT to REC.
Bit5 = 1: abist_fail flag makes state machine from INIT to REC.

Bit6 = 1: mbuck_pgndloss flag makes state machine from INIT to REC.
Bit7 = 1: saf_crc_fail flag makes state machine from INIT to REC.

When FSM2REC is RAMPUP MAIN:

Bit4 = 1: lbist_fail flag makes state machine from RAMPUP MAIN to REC.
Bit5 = 1: main_buck_fail flag (main PG=0 & timer expired) makes state machine fromRAMPUP MAIN to REC.

Bit6 = 1: main_buck_pg_loss makes state machine from RAMPUP MAIN to REC.

When FSM2REC is SECUP:

Bit4 = 1: lbist_fail flag makes state machine from SECUP to REC.

Bit5 = 1: mbuck_PG=0 flag makes state machine from SECUP to REC.

Bit6 = 1: mbuck_pgndloss flag makes state machine from SECUP to REC.
Bit7 = 1: vreg_ot flag makes state machine from SECUP to REC.

When FSM2REC is ACTIVE:

Bit4 = 1: lbist_fail flag makes state machine from ACTIVE to REC.

Bit5 = 1: mbuck_PG=0 or vreg_ot flag makes state machine from ACTIVE to REC.
Bit6= '1' => mbuck_pgndloss flag makes state machine from ACTIVE to REC.

Bit7 = 1: SECUP fail=3 flag makes state machine from ACTIVE to REC.
Bit8 = 1: Rstb fail.

5.2.23 SPI Device Identification

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									OTP_DEVICE_IDENTIFICATION						OTP_WD_REC_EN
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address 0x21

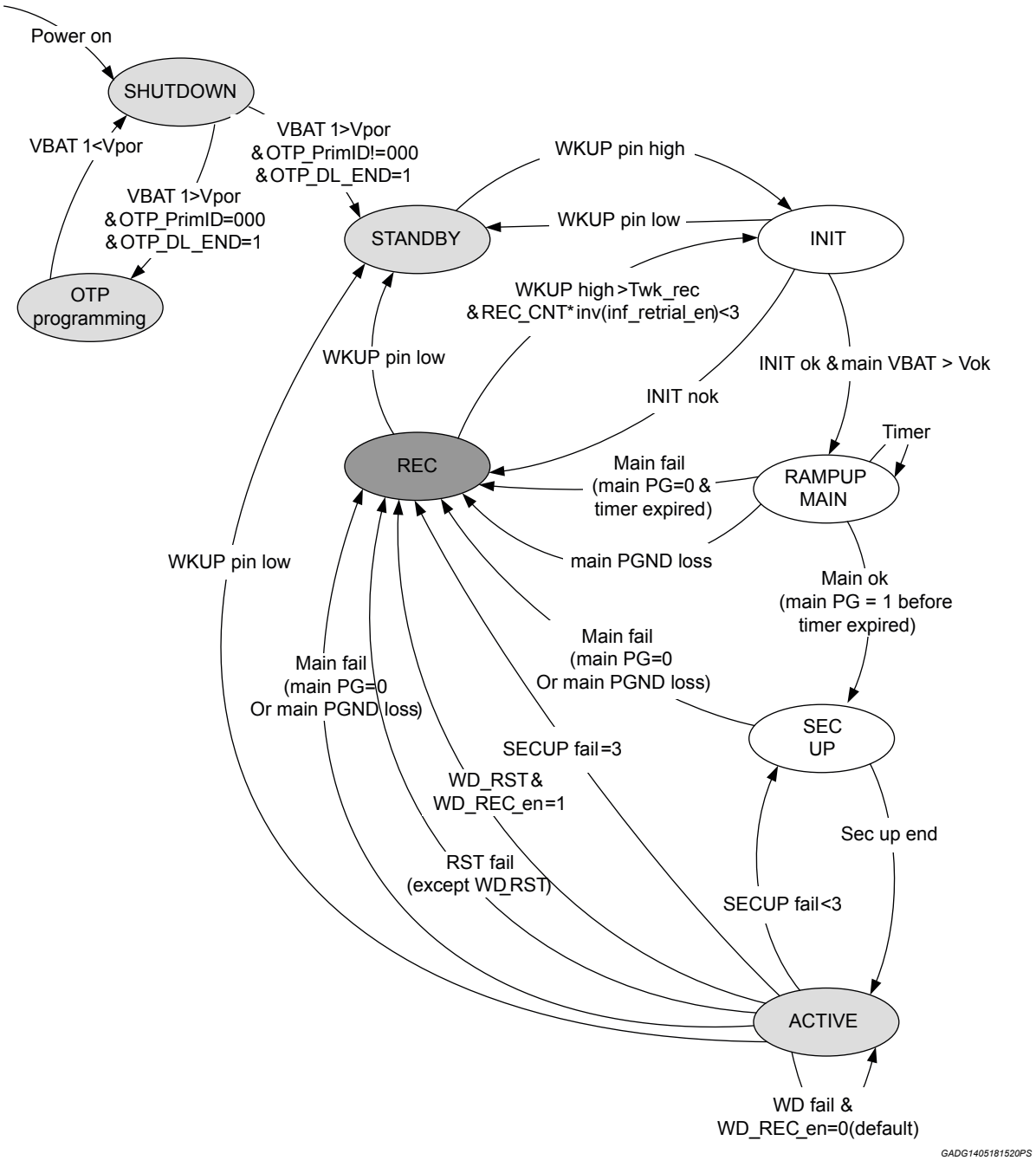
OTP DEVICE IDENTIFICATION: Digital circuit auto download the information from OTP to this register when chip power up. Read only. The default value will be all 0 if OTP is not configured.

OTP_WD_REC_EN: Digital circuit auto download the information from OTP to this register when chip power up. Read only. The default value will be all 0 if OTP is not configured.

6 Device operating mode

L5965 can work in different operative modes according to input/SPI signals, OTP/SPI settings, fault management and regulators status.

Figure 26. State machine



6.1 Shutdown mode

In Shutdown Mode supply batteries (VBAT1/VBAT2/VINx) are not present and all regulators are OFF.

A rising edge on VBAT1 line (higher than Power On Reset threshold) moves L5965 to STANDBY Mode.

6.2 Standby mode

In Standby mode, all the regulators are OFF, RESET_B is asserted and current consumption is very low. A low to high transition on WKUP pin moves the IC to INIT Mode. If VBAT1 falls below POR threshold, the device goes back to Shutdown Mode.

6.3 INIT mode

In INIT mode all the functional checks on analog and digital circuitry are performed:

- OTP program checksum: data integrity is verified and OTP WR bit is checked
- Analog BIST on Voltage monitors (UV/OV)
- Analog BIST on Temperature monitors
- RESET_B assertion and path is checked
- Digital BIST
- Check if main VBAT is ok

Main regulator GND LOSS comparator is active.

DBIST is always active, not only in INIT mode. In INIT mode, in case of issues during DBIST, the IC moves to REC mode. Outside INIT mode, in case of issues during DBIST, the FAULT pin is asserted.

Besides, DBIST includes:

1. Buck clock generation check;
2. Logic diagnostics;
3. Main State Machine check.

If all the checks are completed without any fail, L5965 moves to RAMPUP mode. In case of fail, the device moves from INIT to REC state and the FAULT pin is asserted. A transition (High to Low) on WKUP moves the state machine back to STBY, where the FAULT pin is de-asserted.

6.4 REC mode

L5965 goes to REC mode (recovery state) in case the Main Regulator or a regulator associated with the reset activation fails. When the IC moves from active to stand-by state, the power down phase is activated. When the IC moves from the active to REC state, all regulators switch off at the same time.

In this state, the FAULT pin is asserted and RESET_B is kept low. There are 2 ways to move the device out of REC:

1. A transition High to Low on WKUP pin moves the IC back to STANDBY, where the FAULT pin is de-asserted.
2. If WKUP pin is kept High for a time longer than Twk_rec and the IC goes in REC mode less than a number of times (3 times if inf_retrial_en = 0, infinite times if inf_retrial_en = 1), then the device moves from REC to INIT and restarts again.

When the chip enters the REC mode, the IC is switched off. The outputs of the SMPS decrease slowly in order to be ready for next power up phase. The outputs of the SMPS are pulled down to 0 V by an inner pull-down current. The pull-down current of each regulator is typically 12 mA.

6.5 RAMPUP MAIN and SEC_UP

In RAMPUP MAIN status, the main regulator (selected by OTP bit) is turned on: when this phase ends, the state machine moves to SEC_UP status where all secondary regulators are turned ON following the Power Up sequence programmed by OTP. When the last regulator has finished its power up phase, device moves to ACTIVE Mode, where SPI communication is allowed: all regulators that have to be turned on by SPI command can now be enabled.

WKUP pin is not monitored in these transition phases.

Reset signal release is programmed via OTP: three OTP bits associate the reset signal to a regulator.

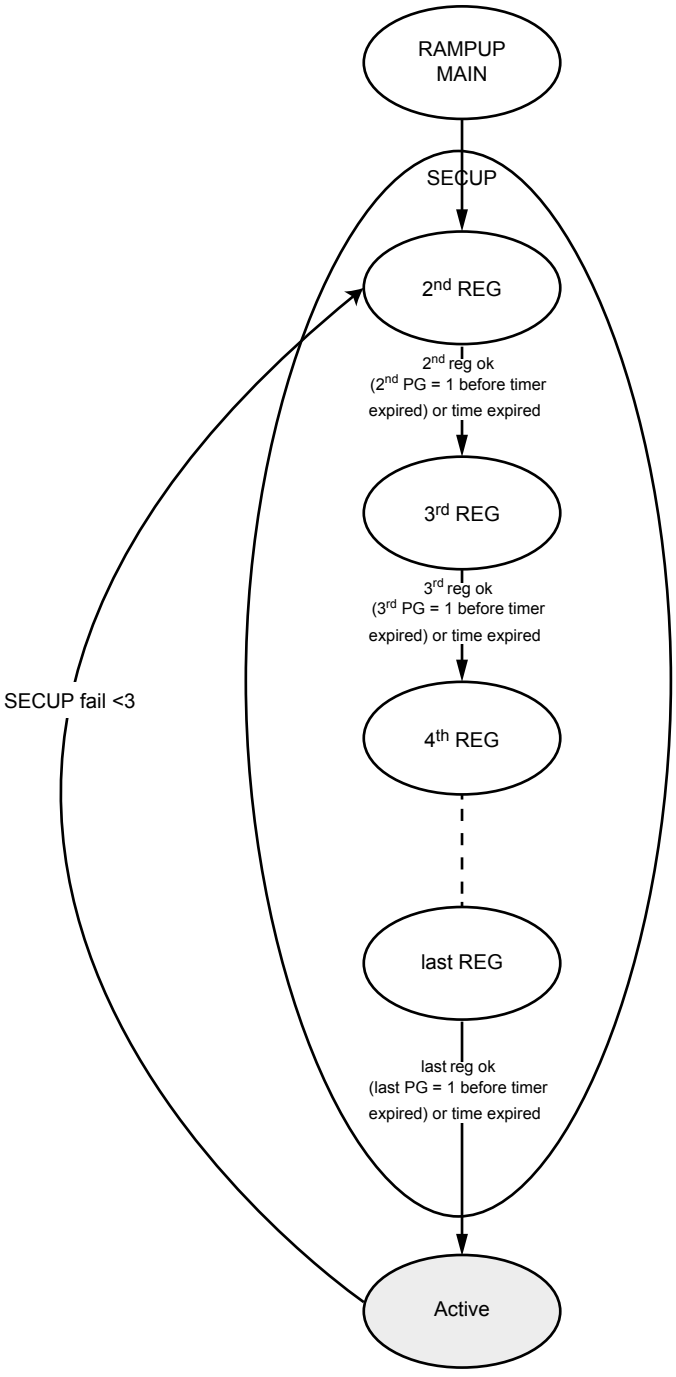
A regulator is a “reset associated regulator” if it can issue a reset signal. This is decided by OTP. RESET_B de-asserts only when the Power Good signals of all the “reset associated regulators” are high.

When a regulator starts the power up phase, a dedicated timer, whose duration is typically of 20ms, is started: if the Power Good signal goes high before the time expires, then the state machine moves to the next regulator in the sequence (after the OTP programmed delay). If the time expires and the Power Good is still low, then the correspondent regulator power up phase is considered failed.

We can have two possible scenarios, depending on the regulator type (Main, or reset associated, or Post):

- Main BUCK power up phase fails: the FAULT pin is asserted, RESET_B is kept low and the device goes to a safe state (called REC state) waiting for a WKUP falling down transition to go back to STANDBY.
- Reset associated regulator or Post regulator power up phase fails: the FAULT pin is asserted, RESET_B signal is kept low and SEC_UP phase is completed for the other regulators. Once the device has moved to the ACTIVE state, it immediately goes back to SEC_UP state to retry to turn on the failed regulator. The retry phase is done three times: if the fail is still present, then the device moves to REC state.

Figure 27. **State machine for SEC UP**



6.6 ACTIVE mode

In ACTIVE Mode the regulators are ON and the device is controlled by SPI: SPI communication is active only in this state. All the regulators, except the Main regulator and the ones disabled via OTP (ENx = 0), can be turned on and off via SPI; if the device goes out from ACTIVE mode, OTP power up phase is recovered.

If a fault occurs, the device can stay in ACTIVE Mode or move to REC, depending on the regulator involved and the kind of fault.

- A fault that asserts RESET_B moves the IC to the REC phase. WD failure asserting RESET_B depends on OTP bit WD_REC_en: if WD_REC_en=1, L5965 moves to REC phase;
- if WD_REC_en=0, L5965 keeps in ACTIVE mode.

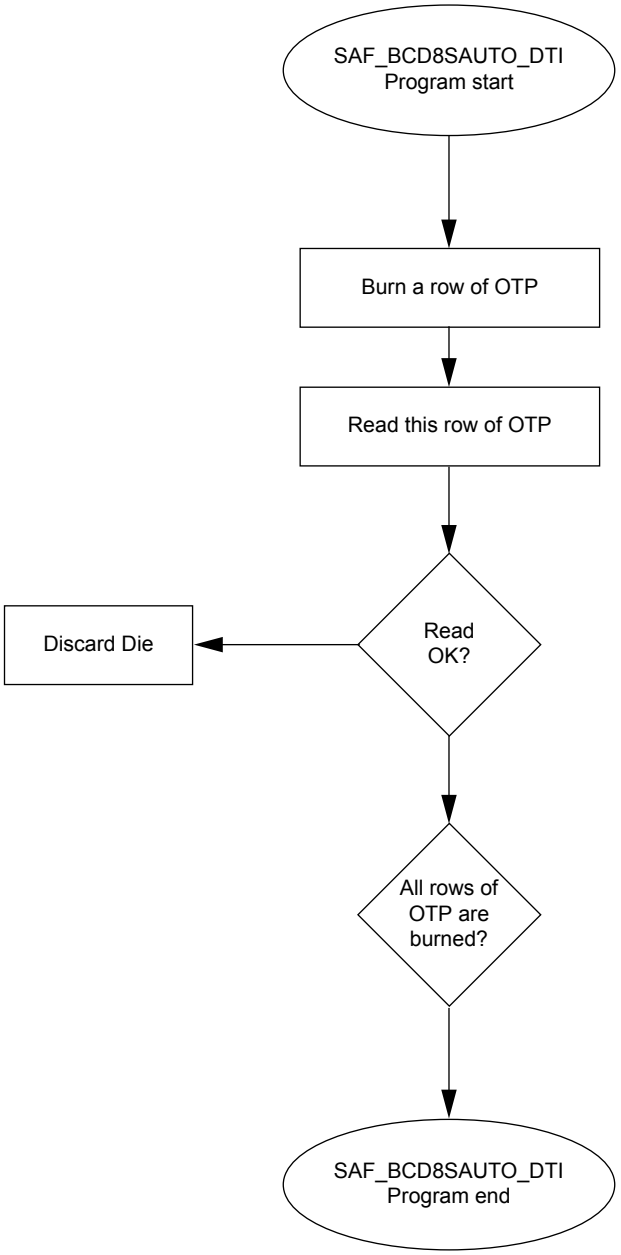
WKUP pin is continuously monitored: if the signal goes low after a filtering time, then L5965 goes back to STANDBY state after proper Power Down phase.

When the IC is switched on for the first time, supplying VBAT1 and/or VBAT2, a fault is asserted by VBAT1_uv or VBAT2_uv. That's not a real fault, and it can be cleared by an SPI read&clear command.

6.7 OTP program mode

L5965 needs a programming phase of OTP (One Time Programmable) cells before starting any operation: this is allowed by providing battery line higher than 17 V (~20 V) at VBAT1 pin, together with a dedicated SPI word.

Figure 28. **OTP program flow chart**



After power-on release, the SAF (Antifuse cell) FSM (Finite State Machine) starts to download all SAF rows to internal DFFs. When the auto download has finished, if Prim Id (bit15~13, ROW9) are “000”, the FSM will go to OTP program mode for customer usage.

In this mode, the user could program/burn SAF rows:

- Write data to SAF_REG_DI via SPI
- Set SAF parameter in SAF_REG_CFG via SPI

The program/burn command should be sent to SAF_REG_OP via SPI, then the data in SAF_REG_DI will be burned in SAF cells.

USR_ Area _PROTECTION (bit15~13 of ROW12) is used to protect SAF rows from re-burning; when the bits are “111”, the burning command for USR SAF rows can’t be executed. So the Row12 must be the last one to be burned in the USR Area.

In OTP program mode, the saf_addr should be from 8~12; otherwise the saf_opration_error flag will be set.

Table 14. OTP row programming shows the detailed instructions on how to program an OTP row.

Table 14. OTP row programming

Step	Description	Action	SPI Frame
Enter OTP prog mode	Power on device. If OTP has not been burned yet, the device goes to OTP program mode	Power on device.	--
Burn OTP	In this step, selected words (indicated as data1) must be written to a selected row of OTP (address indicated as row_addr)	Write register SAF_REG_DI = “data1” via SPI. Note: bit15~13 of this register is crc of data1, it is auto calculated by digital circuit.	DI frame: Bit31=’1’, bit30~23 =“0x32”, Bit22=’1’, bit21=’0’, bit20~5=data1, bit4~0=CRC.
		Write register SAF_REG_CFG=“0x7000” via SPI; note: saf_hv_en_force_decoding (bit14~bit12 of this register) should be set to "111", otherwise the burn operation is forbidden.	DI frame: Bit31=’1’, bit30~23 =“0x31”, Bit22=’1’, bit21=’1’, bit20~5=“0x7000”, bit4~0=CRC.
		Send burn command and address of selected row of OTP. Write register SAF_REG_OP=“0x001[row_addr]” via SPI	DI frame: Bit31=’1’, bit30~23 =“0x30”, Bit22=’1’, bit21=’0’, bit20~11=“0x000”, Bit10~9=”01”, Bit8~5=”row_addr”, bit4~0=CRC.
		Wait end of write procedure, then read register SAF_REG_STAT via SPI. For first reading, don’t care DO frame.	DI frame: Bit31=’0’, bit30~23 =“0x34”, Bit22=’1’, bit21=’1’, bit20~5=”--”, bit4~0=CRC.
		Read register SAF_REG_STAT via SPI again. Saf_busy (bit4 of this register)=’1’ indicates burn operation is not finished, then wait a moment and read this register again. Saf_busy =’0’ indicates burn operation is finished. Saf_opration_error (bit6 of this register) =’0’ indicates the burn operation is valid, otherwise invalid.	DI frame: Bit31=’0’, bit30~23 =“0x34”, Bit22=’1’, bit21=’0’, bit20~5=”--”, bit4~0=CRC. DO frame: Check if bit28~21=“0x34”, If bit9=’0’, if bit11=’0’.

Step	Description	Action	SPI Frame
Read OTP	In this step, read the selected row of OTP	Write register SAF_REG_CFG="0xXXXX" via SPI; This is not necessary, you can skip it if you keep saf_r_code default.	--
		Send read command and address of selected row of OTP. Write register SAF_REG_OP="0x002[row_addr]" via SPI	DI frame: Bit31='1', bit30~23 ="0x30", Bit22='1', bit21='1', bit20~11="0x000", Bit10~9="10", Bit8~5="row_addr", bit4~0=CRC.
		Read register SAF_REG_STAT via SPI. For first reading, don't care DO frame. Get read back data on next DO frame, and then check if reading operation is finished (saf_busy=0) and crc of OTP is ok (saf_crc_ok=1/ status_crc_glb=1).	DI frame: Bit31='0', bit30~23 ="0x34", Bit22='1', bit21='0', bit20~5="--", bit4~0=CRC.
		Read register SAF_REG_DO_Bit_Ts via SPI. For first reading, don't care DO frame.	DI frame: Bit31='0', bit30~23 ="0x33", Bit22='1', bit21='1', bit20~5="--", bit4~0=CRC. DO frame (read back data of SAF_REG_STAT): Check if bit28~21="0x34", If bit9='0', if bit8='1', if bit7='1'.
		Read register SAF_REG_DO_Bit_Ts via SPI again, then get the read back data of this register on DO frame. Note: bit15~13 of this register is crc of data1, it needs to be checked.	DI frame: Bit31='0', bit30~23 ="0x33", Bit22='1', bit21='0', bit20~5="--", bit4~0=CRC. DO frame: Check if bit28~21="0x33", If bit20~5=""data1".

6.8 OTP bit mapping and register configuration

Figure 29. OTP bit mapping

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
8	Reset activation			Device identification						OTP_WD_REC_en	BUCK1 CFG			CRC		
9	Prim Id			Non Prim SeqId			BUCK2 CFG					EnBUCK4	EnBUCK3	CRC		
10	SeqId BUCK4			SeqId BUCK3			BUCK4 CFG			OvRst EN	BUCK3 CFG			CRC		
11	SeqId LDO			SeqId BOOST			EnLDO	EnBOOST	LDO CFG				BOOST CFG	CRC		
12	USR Area Protection			SeqId VREF			PowrOn Delay		EnVREF	WDG CFG		VREF CFG		CRC		

Figure 30. Programmed configuration

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
8	Reset activation			Device identification						OTP_WD_REC_en	BUCK1 CFG			CRC		
9	Prim Id			Non Prim SeqId			BUCK2 CFG					EnBUCK4	EnBUCK3	CRC		
10	SeqId BUCK4			SeqId BUCK3			BUCK4 CFG			OvRst EN	BUCK3 CFG			CRC		
11	SeqId LDO			SeqId BOOST			EnLDO	EnBOOST	LDO CFG				BOOST CFG	CRC		
12	USR Area Protection			SeqId VREF			PowrOn Delay		EnVREF	WDG CFG		VREF CFG		CRC		

Table 15. Reset activation OTP

Bit Nb	Name	Description
Row 8 Bit15:13	Reset_activation<2:0>(1)	Reset release 000: Reset release after PGOOD of Main BUCK with a delay set by PowrOn Delay 001: Reset release after PGOOD of the 2nd regulator with a delay set by PowrOn Delay 010: Reset release after PGOOD of the 3rd regulator with a delay set by PowrOn Delay 011: Reset release after PGOOD of the 4th regulator with a delay set by PowrOn Delay 100: Reset release after PGOOD of the 5th regulator with a delay set by PowrOn Delay 101: Reset release after PGOOD of the 6th regulator with a delay set by PowrOn Delay 110: Reset release after PGOOD of the last regulator with a delay set by PowrOn Delay 111: Reset release when ACTIVE state is reached (unconditional Reset release)

1. *All regulators switched on before the Reset is released are considered part of the "Reset activation list"*

Table 16. Device identification OTP

Bit Nb	Name	Description
Row 8 Bit12:7	Device_id<5:0>	Custom information. It can be read out by SPI.

Table 17. WD_REC_en OTP

Bit Nb	Name	Description
Row 8 Bit6	OTP_WD_REC_en<0>	When OTP bit = 0, SPI bit = 0 make a WD failure to assert RESET_B but not affect the FSM. All regulators keep running in active mode. If the SPI bit = 1 WD failure asserts RESET_B and makes FSM go to REC state. When OTP bit = 1, a WD failure asserts RESET_B and makes FSM go to REC state.

Table 18. Buck1 CFG

Bit num	Name	Description
Row 8 Bit5:3	vsel<2:0>	Output Voltage selection 000: 5.0 V 001: 3.8 V 010: 3.3 V 011: 1.8 V 100: 1.2 V 101: 1.1 V 110: 1.0 V 111: 0.8 V

Table 19. Primary activation OTP

PrimId	Non Prim SeqId	EnBuck1	EnBuck2	Note
"101"	[001:110]	1	FSM=ON, SPI=CH	Buck1 is primary, Buck2 is enabled by FSM
"101"	"111"	1	FSM=OFF, SPI=CH	Buck1 is primary, Buck2 can be enabled by SPI
"101"	“000”	1	0	Error
"110"	[001:110]	FSM=ON SPI=CH	1	Buck2 is primary, Buck1 can be enabled by FSM
"110"	“111”	FSM=OFF SPI=CH	1	Buck2 is primary, Buck1 can be enabled by SPI
“110”	“000”	0	1	Error
"001"	any	0	1	Buck2 is primary, Buck1 is disabled
"010"	any	1	0	Buck1 is primary, Buck2 is disabled
"000 | 011 | 100 | 111"	any	0	0	Error

Table 20. Buck2 CFG

Bit num	Name	Description
Row 9 Bit9	freqsel<0>	Free Running Frequency selection 0: 0.4 MHz 1: 2.4 MHz
Row 9 Bit8	cursel<0>	Max current selection 0: 1.5 A 1: 3.0 A
Row 9 Bit7:5	vsel<2:0>	Output Voltage selection 000: 5.0 V 001: 3.6 V 010: 3.3 V 011: 1.5 V 100: 1.35 V 101: 1.2 V 110: 1.1 V 111: 1.0 V

Table 21. Enables

EnBuck4	EnBuck3	EnLDO	EnBoost	EnVREF
enable of buck4 0: disable 1: enable	enable of buck3 0: disable 1: enable	enable of LDO 0: disable 1: enable	enable of Boost 0: disable 1: enable	enable of VREF 0: disable 1: enable

Table 22. SeqId Buck4, Buck3, LDO, Boost, Vref OTP

Bit Nb	Name	Description
–	SeqID_x<2:0> (x=buck4, buck3, ldo, boost, vref)	000: regulator is turned on only by SPI enable signal 001: regulator is turned on after Main regulator (second regulator) 010: regulator is turned on as third one 011: regulator is turned on as fourth one 100: regulator is turned on as fifth one 101: regulator is turned on as sixth one 110: regulator is turned on as seventh one 111: regulator is turned on only by SPI enable signal

Table 23. Buck4 CFG

Bit num	Name	Description
Row 10 Bit9:7	vsel<2:0>	Output voltage selection 000: 3.3 V 001: 1.8 V 010: 1.35 V 011: 1.3 V 100: 1.25 V 101: 1.2 V 110: 1.12 V 111: 1.1 V

Table 24. OvRst_EN

Bit num	Name	Description
Row 10 Bit6	OvRst_EN<0>	OV assert RESET_B enable for all regulators except BOOST and VREF 0: no OV of regulator can assert RESET_B; 1: the OV of regulator that is in the reset activation list can assert RESET_B.

Table 25. Buck3 CFG

Bit num	Name	Description
Row 10 Bit5:3	vsel<2:0>	Output voltage selection 000: 3.3 V 001: 2.5 V 010: 2.3 V 011: 2.0 V 100: 1.8 V 101: 1.35 V 110: 1.2 V 111: 1.0 V

Table 26. LDO CFG OTP

Bit num	Name	Description
Row 11 Bit7	cursel<0>	Maximum current selection 0: 0.299 A 1: 0.599 A
Row 11 Bit6:4	vsel<2:0>	Output Voltage selection 000: 5.0 V 001: 3.3 V 010: 2.8 V 011: 2.5 V 100: 1.8 V 101: 1.3 V 110: 1.25 V 111: 1.2 V

Table 27. Boost CFG OTP

Bit num	Name	Description
Row 11 Bit3	vsel<0>	Output Voltage selection 0: 5.0 V 1: 7.0 V

Table 28. USR Area Protection OTP

Bit num	Name	Description
Row 12 Bit15:13	Usr_area_protection<2:0>	Rewrite protection. 111: the User SAF rows couldn't be burned or simulated; Others: the User SAF rows could be burned or simulated

Table 29. PowrOn Delay OTP

<1:0>	time (ms)
00	0
01	2 (min 1.49, max 2.3)

<1:0>	time (ms)
10	5 (min 4.04 max 5.75)
11	10 (min 8.29 max 11.5)

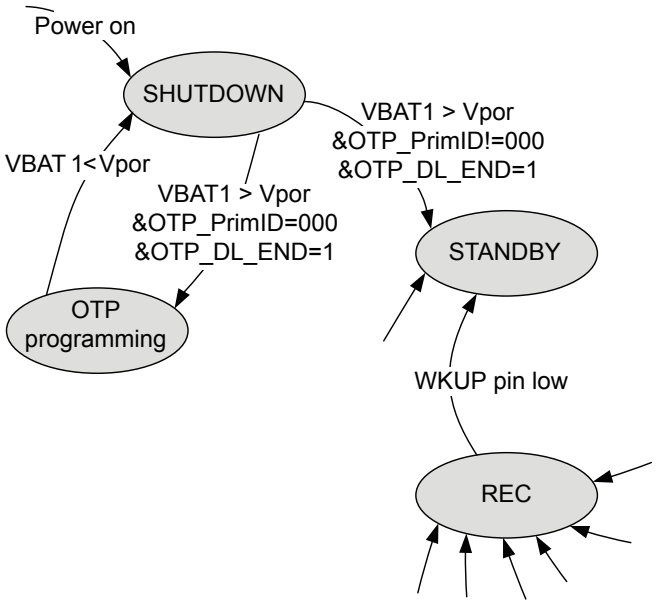
Table 30. WDG CFG OTP

Bit num	Name	Description
Row 12 Bit6:5	Wd_cfg<1:0>	Output Voltage selection 00, 01: use hardware watchdog (WDI pin) 10: no watchdog 11: use SPI as watchdog

Table 31. VREF CFG OTP

Bit num	Name	Description
Row 12 Bit4:3	vsel<1:0>	Output Voltage selection 00: 1.8 V 01: 2.5 V 10: 3.3 V 11: 4.1 V

Figure 31. OTP start-up state check



GAPG2302160823PS

6.9 OTP (SAF) registers

6.9.1 SAF_REG_OP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			SAF_AUTO_DL_FORCE	RESERVED						SAF_CMD		SAF_ADDR			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address 0x30

[3:0] SAF_ADDR: SAF row address

[5:4] SAF_CMD: SAF opt command

01: burn / write

10: read

11: simulation

[11:6] RESERVED

[12] SAF_AUTO_DL_FORCE: SAF auto download bit. When auto download is finished, this bit will be cleared to '0'. This register is only accessible in TM and OTP Program mode.

Note: In OTP program mode, 8/9/10/11/12 (USR ROWs) are valid for SAF_ADDR;

Writing operation to this register generates SAF_TRIG pulse (if SAF_CMD is valid op);
The auto download has higher priority.

6.9.2 SAF_REG_CFG

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			SAF_HV_EN_FORCE DECODING	RESERVED		SAF_HV_MAN		RESERVED				SAF_T_WR		SAF_R_CODE	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Address 0x31

[1:0] SAF_R_CODE: SAF reading time;

[3:2] SAF_T_WR: SAF programming time;

[7:4] RESERVED

[9:8] SAF_HV_MAN: SAF burning configuration;

[10:11] RESERVED

[12] SAF_HV_EN_FORCE_DECODING: When the bits are set to "111", the SAF write/burn operation is activated. This register is only accessible in OTP program mode (High voltage connection for burning operation is implemented).

[13:15] RESERVED

6.9.3 SAF_REG_DI

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC CODE			SAF_DIN												
R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address 0x32

[15:13] CRC_CODE: the CRC checksum for SAF din. These bits can be set to '000' in SAF_REG_DI word, since they are read only.

[12:0 SAF_DIN: SAF writing data; (for burning).

Note: The CRC_CODE is only readable and is generated automatically by HW; This register is only accessible in OTP program mode.

6.9.4 SAF_REG_D0_Bit_Ts

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC CODE			SAF_BIT_TS												
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address 0x33

[15:13] CRC CODE: CRC checksum for SAF din.

[12:0] SAF_BIT_TS: read data from SAF bit_ts port, 3 state bus.

Note: The register will return the data from SAF_BIT_TS bus after the SAF read command.

6.9.5 SAF_REG_STAT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CRC_BUSY	SAF_OPERATION_ERROR	SAF_AUTO_DL_END	SAF_BUSY	SAF_CRC_OK	STATUS_CRC_GLB	SAF_RES_PROTECT_STAT	SAF_USR_PROTECT_STAT
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Address 0x34

[0] SAF_USR_PROTECT_STAT: SAF protection status for usr region; '1' means the SAF rows in user region can't be burned or simulated;

[1] SAF_TRIM_PROTECT_STAT: SAF protection status for usr region; '1' means the SAF rows in trim region can't be burned or simulated;

[2] SAF_BUSY: SAF is busy for reading/program or CRC checking;

[3] SAF_AUOT_DL_END: '1' means saf auto download is ended;

[4] CRC_STATUS_GLB: CRC checksum status for all rows;

[5] CRC_OK: CRC checksum status for current SAF row reading operation;

[6] SAF_OPERATION_ERROR: Invalid SAF operation in OTP programing mode;

[7] CRC_BUSY: CRC busy flag;

[15:8] RESERVED

Note: This register is only accessible in OTP program mode.

6.10 Power down phase

When WKUP signal goes low, the device moves from any state to STANDBY status turning off all the regulators: at first all the active regulators are switched off, then, after a delay time (T_{delay}), the internal VREG is switched off too.

6.11 Power up programming

According to the data written in OTP cells, we can have different power up phases. The meaning of OTP bits code is the following:

- Main BUCK selection : main regulator, BUCK1 (OTP = 101) or BUCK2 (OTP = 110), is turned on only by WKUP signal
- Other regulators (BUCK1 or BUCK2, BUCK3, BUCK4, BOOST, LDO and VREF) turning on order, from second to the seventh one:
  - 000 = regulator is never turned on
  - 001 = regulator is turned on after Main regulator (second regulator)
  - 010 = regulator is turned on as third one
  - 011 = regulator is turned on as fourth one
  - 100 = regulator is turned on as fifth one
  - 101 = regulator is turned on as sixth one
  - 110 = regulator is turned on as seventh one
  - 111 = regulator is turned on only by SPI enable signal

Two regulators with the same order number is not allowed, except for 000 or 111 code. Enable bit in OTP cells (EnBuck3/4, EnLDO, EnBoost and EnVref) must be set to '1' too, to have the regulator ON in ACTIVE phase. All the regulators with 111 code can be turned on in ACTIVE mode, when the SPI is available.

Regulators turning on delay after Power Good: the delay is the same for all the regulators.

- 00 = no delay
- 01 = 2 ms after PGOOD of previous regulator
- 10 = 5 ms after PGOOD of previous regulator
- 11 = 10 ms after PGOOD of previous regulator
- Reset activation related to the right regulator Power Good (3 bits)
  - 000 = Reset release after PGOOD of Main BUCK with a delay from 0 (no delay) to 10 ms (2bits)
  - 001 = Reset release after PGOOD of the second regulator with a delay from 0 (no delay) to 10 ms (2bits)
  - …
  - 110 = Reset release after PGOOD of the last regulator with a delay from 0 (no delay) to 10 ms (2bits)
  - 111 = Reset release when ACTIVE state is reached (unconditional Reset release)

Figure 32. Power up sequence

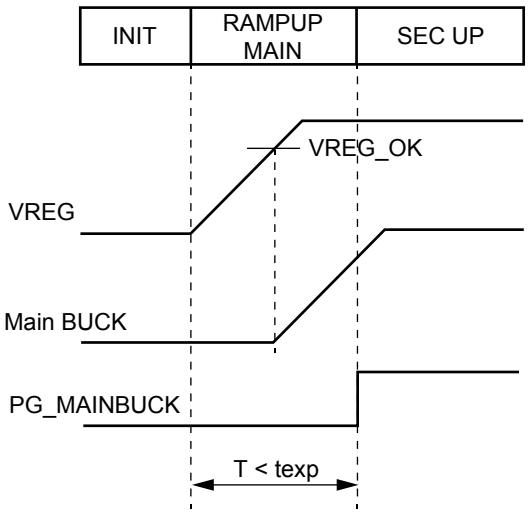
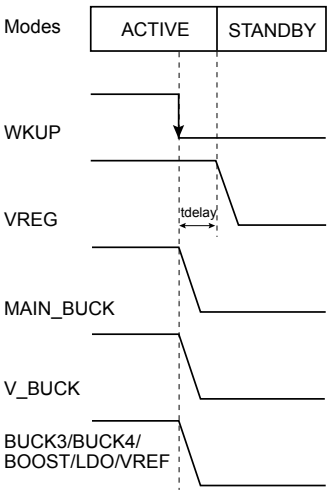


Figure 33. Power down sequence



GAPG2306151452PS

7 Functional safety requirements

The device has been designed taking into account the following Top Level Safety Requirements:

Table 32. Top level safety requirements

ID	Description	Safe State
TLSR1	All regulators output voltages must remain within programmed range when RESET_B and FAULT pins are not asserted	REC state with RESET_B and FAULT pin asserted
TLSR2	Operation of the voltage regulators is allowed till over temperature limit	REC state with RESET_B and FAULT pin asserted; all regulators OFF

7.1 Functions and safety mechanism related to safety requirements

Table 33. Functions and safety mechanism

ID	Description	TLSR
1	Two independent voltage references (VBG1-VBG2) for voltage monitor comparators	TLSR1
2	Ground loss comparators	TLSR1
3	Built In Self Test (Analog BIST) of Under/Over voltage and overtemperature comparators at INIT status	TLSR1
4	Built In Self Test (Digital BIST) on internal logic block at INIT status	TLSR1
5	OTP integrity Check at INIT status	TLSR1
6	Over temperature monitoring (via 7 different sensors) at ACTIVE state	TLSR2
7	Thermal sensors value readable via SPI	TLSR2
8	Built In Self Test on Thermal Comparators	TLSR2

7.2 System safety mechanism

Table 34. System safety mechanism

ID	Description
1	Window Watchdog (via WDI pin or SPI communication)
2	Failure Status pin FAULT (open drain) indicating a generic failure on the device
3	SPI command to read device diagnosis via SPI fault registers
4	SPI communication check via CRC and CNT bit

8 Application information

8.1 External components calculation

8.1.1 BUCK1 controller

8.1.1.1 *R_{SENSE}*

An external resistor senses the current through the inductor. R_{SENSE} must be chosen so that the maximum forward peak current in the inductor generates a voltage (V_{SENSE}) across the sense pins. The typical value of V_{SENSE} is 75 mV.

$$R_{SENSE} = \frac{V_{SENSE}}{I_{PEAK\_LIM}} \quad (8)$$

8.1.1.2 *BUCK1 output inductor*

The value of the output inductor is usually calculated to satisfy the peak-to-peak ripple current requirement. For the best compromise of cost, size and performance, it is suggested to keep the inductor current ripple between 20% and 40% of maximum load current.

For example, if $\Delta I_L = I_{Ripple} = 0.3 x I_{OUT(max)}$

Where, $I_{OUT(max)}$ is the maximum output current.

Then, the inductor value can be estimated by the following equation:

$$L > \frac{1}{f_{SW} \times \Delta I_L} \times V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN(\max)}}\right) \quad (9)$$

Where, f_{SW} is the switching frequency, $V_{IN(max)}$ is the maximum input voltage.

The peak current flowing in Inductor is:

$$I_{L(PEAK)} = I_{OUT}(\max) + \frac{\Delta I_L}{2} \quad (10)$$

If the Inductor value decreases, the peak current increases. The peak current has to be lower than the current limit of the device.

The inductor should have a saturation current higher than the device current limit.

Note: in order to meet slope compensation, L needs to meet the following equation:

$$L > \frac{1}{2} \times \frac{V_{OUT}}{I_{slope}} \quad (11)$$

$$I_{slope} = 30\mu A \times f_{SW} \quad (12)$$

8.1.1.3 *BUCK1 output capacitor*

Output capacitors are selected to support load transients and output ripple current, as well as loop stability.

The amount of the voltage ripple can be calculated by the output ripple current flowing in the inductor:

$$\Delta V_{OUT(RIPPLE)} = \Delta I_L \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (13)$$

Usually the first term is dominant. However, if the ceramic capacitor (which is recommended) is adopted, the first term on the above equation can be neglected, as the ESR value is very low.

$$C_{OUT}(\min) = \frac{\Delta I_L}{8 \times f_{SW} \times \left(V_{OUT(RIPPLE)} - \Delta I_L \times ESR\right)} \quad (14)$$

For example, in case V_{OUT} = 3.3 V, V_{IN} = 14 V, f_{SW} = 250 kHz, ΔI_L = 0.3 x 3.5 A = 1.05 A, in order to have a ΔV_{OUT} = 5% x V_{OUT} = 0.165 V, a 4.7 µF ceramic capacitor is needed. In case of not negligible ESR (electrolytic or tantalum capacitors), the capacitor is chosen taking into account its ESR value.

In the above example, if a 100 µF with ESR = 100 mΩ electrolytic capacitor is chosen, the voltage drop on ESR dominates and the voltage ripple 1.05 A × 100 mΩ = 105 mV

The output capacitor is also important to sustain the output voltage during a load transient. In general, minimizing the ESR value and increasing the output capacitance results in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel, or by using higher quality capacitors.

The minimum output capacitance needed is determined by the maximum energy stored in the inductor when a high current to low current transition occurs. The capacitance must be sufficient to absorb the change in inductor current.

$$C_{OUT(\min)} = \frac{L}{2} \times \frac{Iout(max)^2 - Iout(min)^2}{Vout \times \Delta Vout} \quad (15)$$

Where:

$I_{OUT(max)}$, $I_{OUT(min)}$ refer to the worst case load step in the system and ΔV_{OUT} is the tolerance of regulated output voltage.

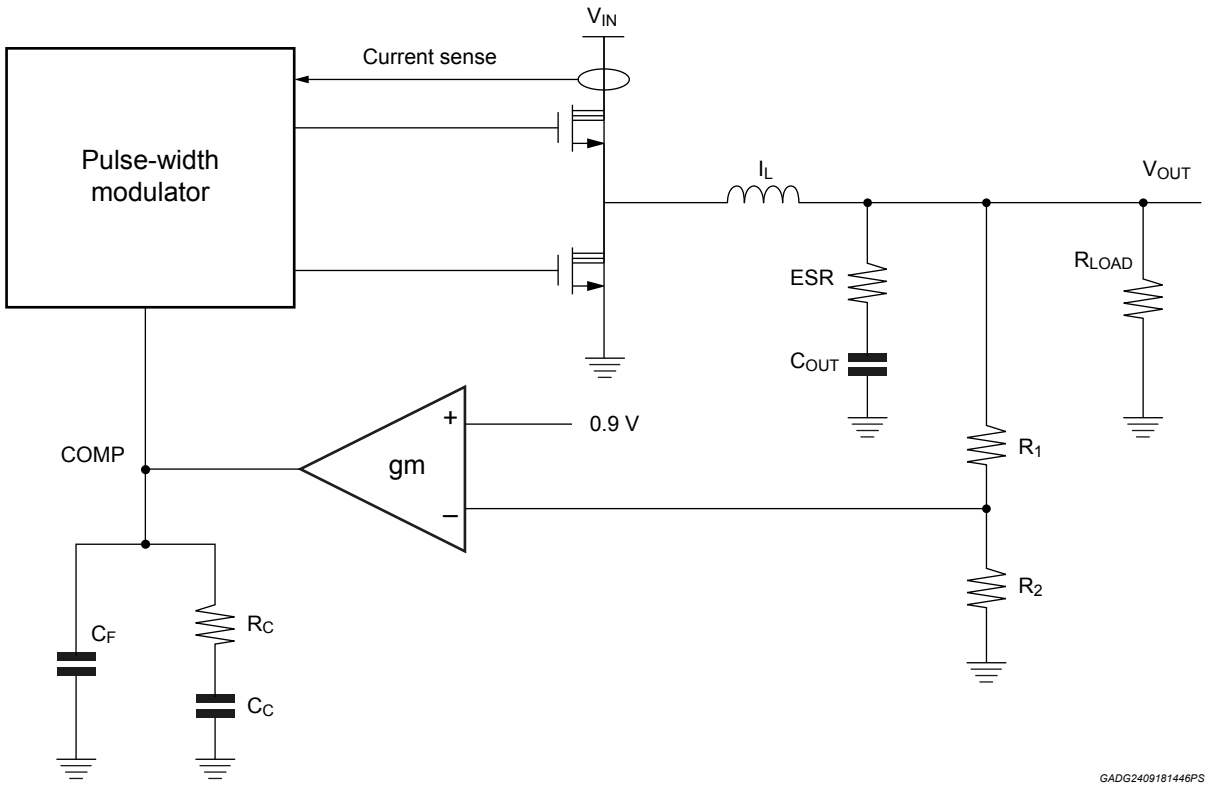
8.1.1.4 BUCK1 bootstrap capacitor

The bootstrap capacitor is put between PH1 and BS1, and is 100 nF. The voltage rating of the capacitor is at least 9 V. The bootstrap capacitor should be a high-quality ceramic type with good temperature stability.

8.1.1.5 BUCK1 compensation network

The compensation network has to assure stability and good dynamic performance. The loop of the device is based on the peak current mode control, compatible with external RC compensation network. The error amplifier is a trans-conductance amplifier with large bandwidth, which is much larger than the closed-loop one.

Figure 34. Basic control loop block diagram



The above figure shows the closed loop system with a RC compensation network. The basic regulator loop is modeled as a power modulator, an output feedback divider and an error amplifier. The loop transfer function is:

$$L(s) = \frac{V_{REF}}{V_{OUT}} \times G_{MOD}(s) \times G_{EA}(s) \quad (16)$$

Where:

s is the angular frequency.

V_{REF} is the internal reference voltage, 0.8 V.

V_{OUT} is the output voltage of the converter.

$G_{MOD}(s)$ is the transfer function of the error amplifier with RC compensation network.

$G_{MOD}(s)$ forms a pole and a zero by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR as expressed in the below equation:

$$G_{MOD}(s) = \frac{g_{mMOD} \times R_{LOAD} \times (1 + sESR \times C_{OUT})}{(1 + sR_{LOAD} \times C_{OUT})} \quad (17)$$

g_{mMOD} = 1/(10 x R_{sense})

$$R_{LOAD} = \frac{V_{OUT}}{I_{OUT,MAX}} \quad (18)$$

The dominant pole is:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times (R_{LOAD} \times ESR)} \quad (19)$$

The zero is:

$$f_{zMOD} = \frac{1}{2\pi \times C_{OUT} \times ESR} \quad (20)$$

GEA(s) is the transfer function of the buck converter from control to output. It forms two poles and a zero as expressed in the below equation:

$$G_{EA}(s) \approx \frac{g_{mEA} \times r_O(1 + sR_C \times C_C)}{(1 + sr_O \times C_C)(1 + sR_C \times C_F)} \quad (21)$$

Where:

g_{mEA} is the trans-conductance of the error amplifier, 1 mS.

r_O is the output resistance of the error amplifier.

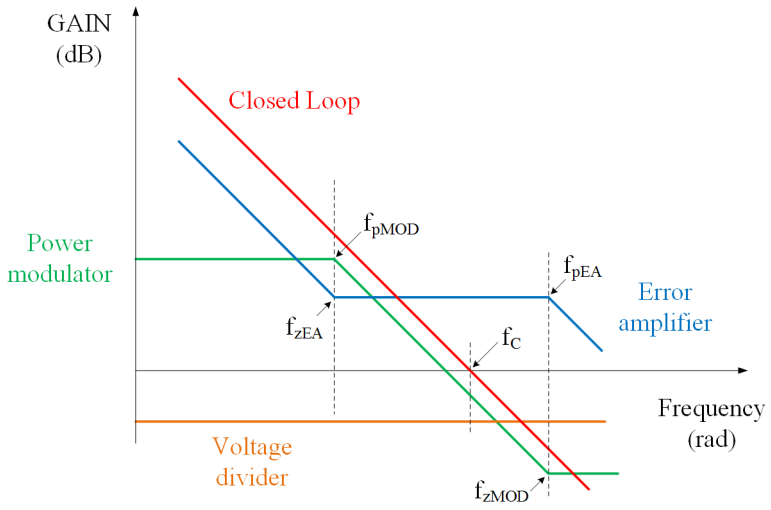
The zero is:

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C} \quad (22)$$

The optional pole is:

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C} \quad (23)$$

Figure 35. Simplified gain plot



The zero f_{zEA} set by C_C and R_C cancels the pole f_{pMOD} set by R_{LOAD} and C_{OUT}.

The optional pole f_{pEA} is set by C_F and R_C in order to cancel the output capacitor ESR zero if it occurs near the crossover frequency f_C, where the loop gain equals 1 (0 dB).

The power modulator has a DC gain set by g_{mMOD} x R_{LOAD}.

g_{mMOD} is trans-conductance of modulator, it is about 3.6 S. The following equations allow to approximate the value for the gain of the power modulator $GAIN_{MOD(DC)}$.

$$GAIN_{MOD(fC)} = g_{mMOD} \times R_{LOAD} \quad (24)$$

The total loop gain as the product of the modulator gain, the feedback voltage-divider gain, and the error-amplifier gain at f_C should be equal to 1.

Then:

$$GAIN_{MOD(fC)} = GAIN_{MOD(DC)} \times \frac{f_{pMOD}}{f_C} \quad (25)$$

The guidelines for calculating the external network are the following ones.

1. Choose a value for f_C , usually between $f_{SW}/5$ and $f_{SW}/10$.
2. Choose resistor divider R_1 and R_2 that set the required V_{OUT}.
3. Calculate the value of RC as follows:

$$R_C = \frac{V_{OUT}}{g_{mEA} \times V_{FB} \times GAIN_{MOD(fC)}} \quad (26)$$

4. Set the error-amplifier compensation zero formed by R_C and C_C (f_{zEA}) at the f_{pMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C} \quad (27)$$

5. If f_{zMOD} is less than $5f_C$, add a second capacitor, C_F, from COMP to GND and set the compensation pole formed by R_C and C_F (f_{pEA}) at the f_{zMOD}. Calculate the value of C_F as follows:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C} \quad (28)$$

8.1.2 BUCK2 controller

8.1.2.1 *BUCK2 output inductor*

The value of the output inductor is usually calculated to satisfy the peak-to-peak ripple current requirement. For the best compromise of cost, size and performance, it is suggested to keep the inductor current ripple between 20% and 40% of maximum load current.

For example, if $\Delta I_L = I_{Ripple} = 0.3xI_{OUT(max)}$

Where, $I_{OUT(max)}$ is the maximum output current.

Then, the inductor value can be estimated by the following equation:

$$L > \frac{1}{f_{SW} \times \Delta I_L} \times V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN(\max)}}\right) \quad (29)$$

Where, f_{SW} is the switching frequency, $V_{IN(max)}$ is the maximum input voltage.

The peak current flowing in the Inductor is:

$$I_{L(PEAK)} = I_{OUT}(\max) + \frac{\Delta I_L}{2} \quad (30)$$

If the Inductor value decreases, the peak current increases. The peak current has to be lower than the current limit of the device.

The inductor should have a saturation current higher than the device current limit.

Note: in order to meet slope compensation, L needs to meet the following equation:

$$L > \frac{1}{2} \times \frac{V_{OUT}}{I_{slope}} \quad (31)$$

$$I_{slope} = 45\mu A \times f_{SW} \quad (32)$$

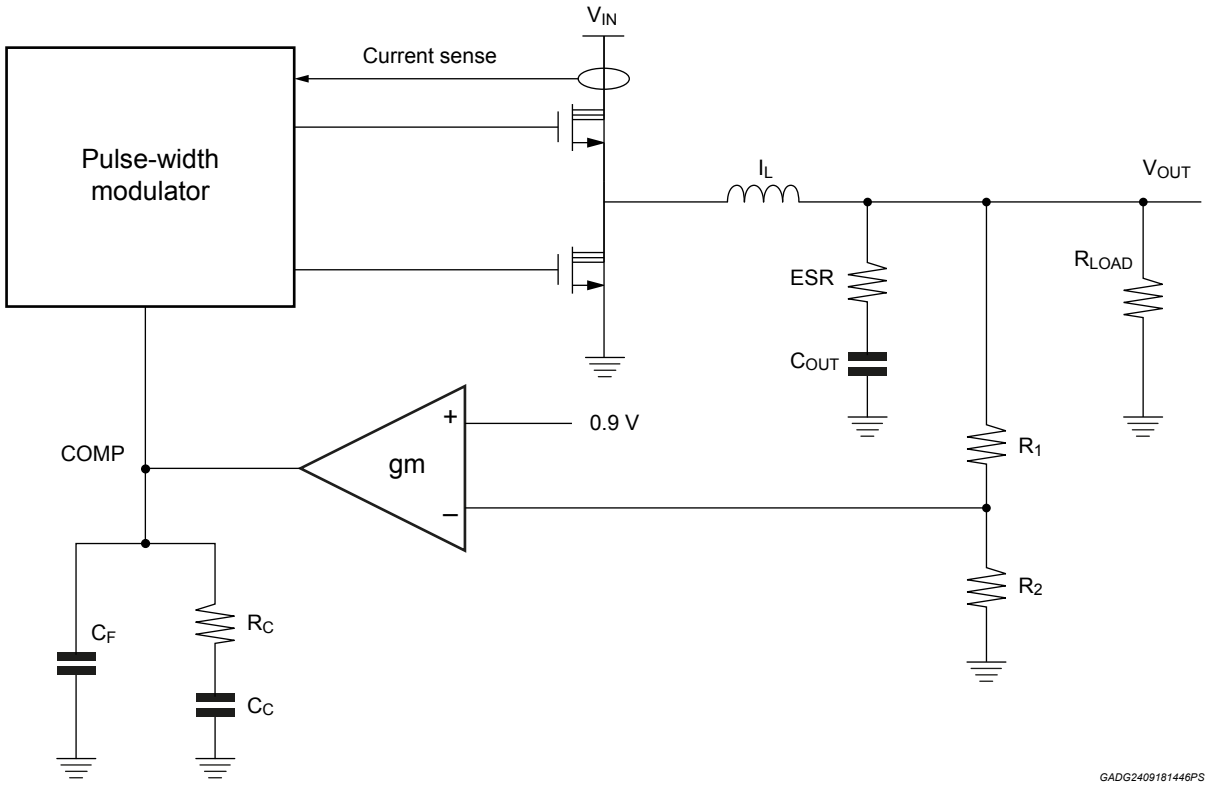
8.1.2.2 *BUCK2 output capacitor*

Refer to BUCK1 output capacitor for BUCK2 output capacitor selection.

8.1.2.3 BUCK2 compensation network

The compensation network has to assure stability and good dynamic performance. The loop of the device is based on the peak current mode control, compatible with external RC compensation network. The error amplifier is a trans-conductance amplifier with large bandwidth, which is much larger than the closed-loop one.

Figure 36. Basic control loop block diagram



The above figure shows the closed loop system with a RC compensation network. The basic regulator loop is modeled as a power modulator, an output feedback divider and an error amplifier. The loop transfer function is:

$$L(s) = \frac{V_{REF}}{V_{OUT}} \times G_{MOD}(s) \times G_{EA}(s) \quad (33)$$

Where:

s is the angular frequency.

V_{REF} is the internal reference voltage, 1 V.

V_{OUT} is the output voltage of the converter.

$G_{MOD}(s)$ is the transfer function of the error amplifier with RC compensation network.

$G_{MOD}(s)$ forms a pole and a zero by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR as expressed in the below equation:

$$G_{MOD}(s) = \frac{g_{mMOD} \times R_{LOAD} \times (1 + sESR \times C_{OUT})}{(1 + sR_{LOAD} \times C_{OUT})} \quad (34)$$

g_{mMOD} = 2.2 S

$$R_{LOAD} = \frac{V_{OUT}}{I_{OUT,MAX}} \quad (35)$$

The dominant pole is:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times (R_{LOAD} \times ESR)} \quad (36)$$

The zero is:

$$f_{zMOD} = \frac{1}{2\pi \times C_{OUT} \times ESR} \quad (37)$$

GEA(s) is the transfer function of the buck converter from control to output. It forms two poles and a zero as expressed in the below equation:

$$G_{EA}(s) \approx \frac{g_{mEA} \times r_o(1 + sR_C \times C_C)}{(1 + sr_O \times C_C)(1 + sR_C \times C_F)} \quad (38)$$

Where:

g_{mEA} is the trans-conductance of the error amplifier, 1 mS.

r_O is the output resistance of the error amplifier.

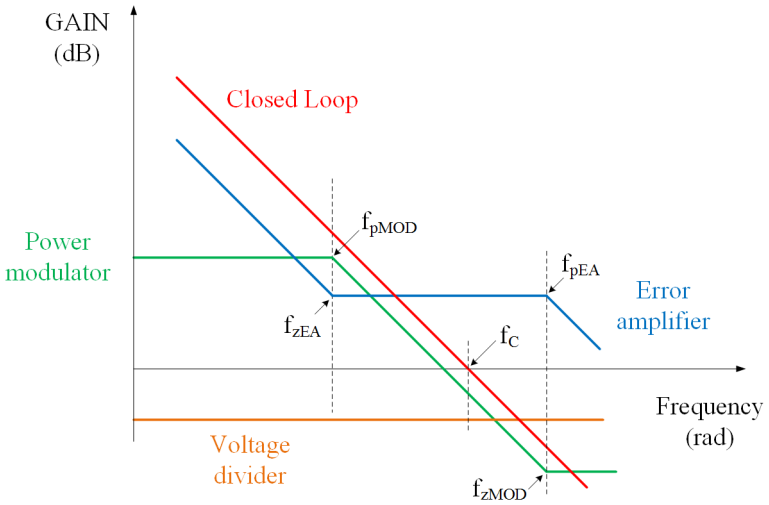
The zero is:

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C} \quad (39)$$

The optional pole is:

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C} \quad (40)$$

Figure 37. Simplified gain plot



The zero f_{zEA} set by C_C and R_C cancels the pole f_{pMOD} set by R_{LOAD} and C_{OUT}.

The optional pole f_{pEA} is set by C_F and R_C in order to cancel the output capacitor ESR zero if it occurs near the crossover frequency f_C, where the loop gain equals 1 (0 dB).

The power modulator has a DC gain set by g_{mMOD} x R_{LOAD}.

g_{mMOD} is trans-conductance of modulator, it is about 3.6 S. The following equations allow to approximate the value for the gain of the power modulator $GAIN_{MOD(DC)}$.

$$GAIN_{MOD(fC)} = g_{mMOD} \times R_{LOAD} \quad (41)$$

The total loop gain as the product of the modulator gain, the feedback voltage-divider gain, and the error-amplifier gain at f_C should be equal to 1.

Then:

$$GAIN_{MOD(fC)} = GAIN_{MOD(DC)} \times \frac{f_{pMOD}}{f_C} \quad (42)$$

The guidelines for calculating the external network are the following ones.

1. Choose a value for f_C , usually between f_{SW}/5 and f_{SW}/10 .
2. Choose resistor divider R_1 and R_2 that set the required V_{OUT}.
3. Calculate the value of RC as follows:

$$R_C = \frac{V_{OUT}}{g_{mEA} \times V_{FB} \times GAIN_{MOD(fC)}} \quad (43)$$

4. Set the error-amplifier compensation zero formed by R_C and C_C (f_{zEA}) at the f_{pMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C} \quad (44)$$

5. If f_{zMOD} is less than $5f_C$, add a second capacitor, C_F, from COMP to GND and set the compensation pole formed by RC and CF (f_{pEA}) at the f_{zMOD}. Calculate the value of CF as follows:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C} \quad (45)$$

8.1.3 BUCK3, BUCK4

8.1.3.1 *Output inductor and capacitor*

Buck3 and BUCK4 have an inner compensation. Here below are the recommendations for selecting the external inductor and capacitor:

- When output voltage >1.2 V, the L recommended value is 2.2 µH; when output voltage ≤ 1.2 V, the L recommended value is 1.5 µF.
- The output capacitor is recommended to be 4.7 µF~20 µF.

To select output inductor and capacitor, please refer to BUCK1 output inductor and BUCK1 output capacitor explanation.

8.1.3.2 Bootstrap capacitor for BUCK3 and BUCK4

A bootstrap capacitor must be connected between the BSx and PHASEx pins to provide a floating gate drive to the high-side MOSFET. For most applications 47 nF is sufficient. This should be a ceramic capacitor with a voltage rating of at least 6 V.

8.1.3.3 Input capacitor

Because of their nature, the buck converter has a pulsating input current. The device requires a low-ESR input capacitor to prevent large voltage transients that can cause misbehavior of the device or interference with other circuits in the system. An input capacitor of 4.7 µF~10 µF is sufficient for BUCK3 and BUCK4.

8.1.4 BOOST

8.1.4.1 *BOOST output inductor*

The inductor value depends on the allowed ripple current in the coil, related to VIN, VOUT and FSW.

The peak to peak ripple could be selected to be 30%, for instance. In this case:

$$IL_{RIPPLE}(\max) = 0.3 \times \frac{I_{OUT(MAX)}}{1 - D_{MIN}} \quad (46)$$

$$L_{MIN} \approx \frac{V_{INmax}}{I_{RIPPLEmax}} \times D_{MIN} \times \frac{1}{f_{SW}} \quad (47)$$

The maximum inductor value (L) acceptable by the Boost is limited by RHP, as explained later.

The output inductor is recommended to be 4.7 µH.

8.1.4.2 *BOOST output capacitor*

Output capacitors should be selected to meet the required output ripple and transient specifications for $V_{OUT(ripple)}$. Low ESR (equivalent series resistance) capacitors should be used at the output to minimize the output ripple voltage.

$$C_{OUT} = 8 \times \frac{I_{OUT} \times D}{V_{OUT(ripple)}} \times \frac{1}{f_{SW}} \quad (48)$$

Because BOOST employs inner compensation, which is fixed, the maximum acceptable output capacitor needs to be selected based on compensation, bandwidth and phase margin.

8.1.4.3 *BOOST compensation network*

The BOOST works in current mode, then the compensation principle can refer to the compensation of the buck, as explained before. The RHP (Right-Half-Plane) zero limits the cross frequency.

$$f_{Z,RHP} = \frac{R_{LOAD} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2}{2\pi \times L} \quad (49)$$

The inner compensation of BOOST is, R_{COMP} = 42 kΩ, C_{COMP} =240 pF, C_f = 1 pF. REA is the output resistor of error amplifier, which has MΩ of magnitude.

If a different output capacitor is needed, the cross over frequency f_C needs to be checked in order to assure that $f_C < \frac{1}{5} \times f_{SW}$. When a bigger output inductor is required, the $f_{Z,RHP}$ should be decreased and the inductance needs to be selected in order to have $f_C < f_{Z,RHP}$.

8.1.4.4 *Output diode for the BOOST converter*

The selected diode must have a reverse voltage rating >1.25 V_{OUT} of the boost.

The peak current rating of the diode must be greater than the maximum inductor current.

To reduce the power losses, the diode is usually a schottky diode. The power dissipation of the diode is estimated as below:

$$P_{Dmax} \approx V_{FD} \times I_{OUT} \quad (50)$$

where V_{FD} is the forward drop voltage of the diode.

8.1.4.5 *Input capacitor selection*

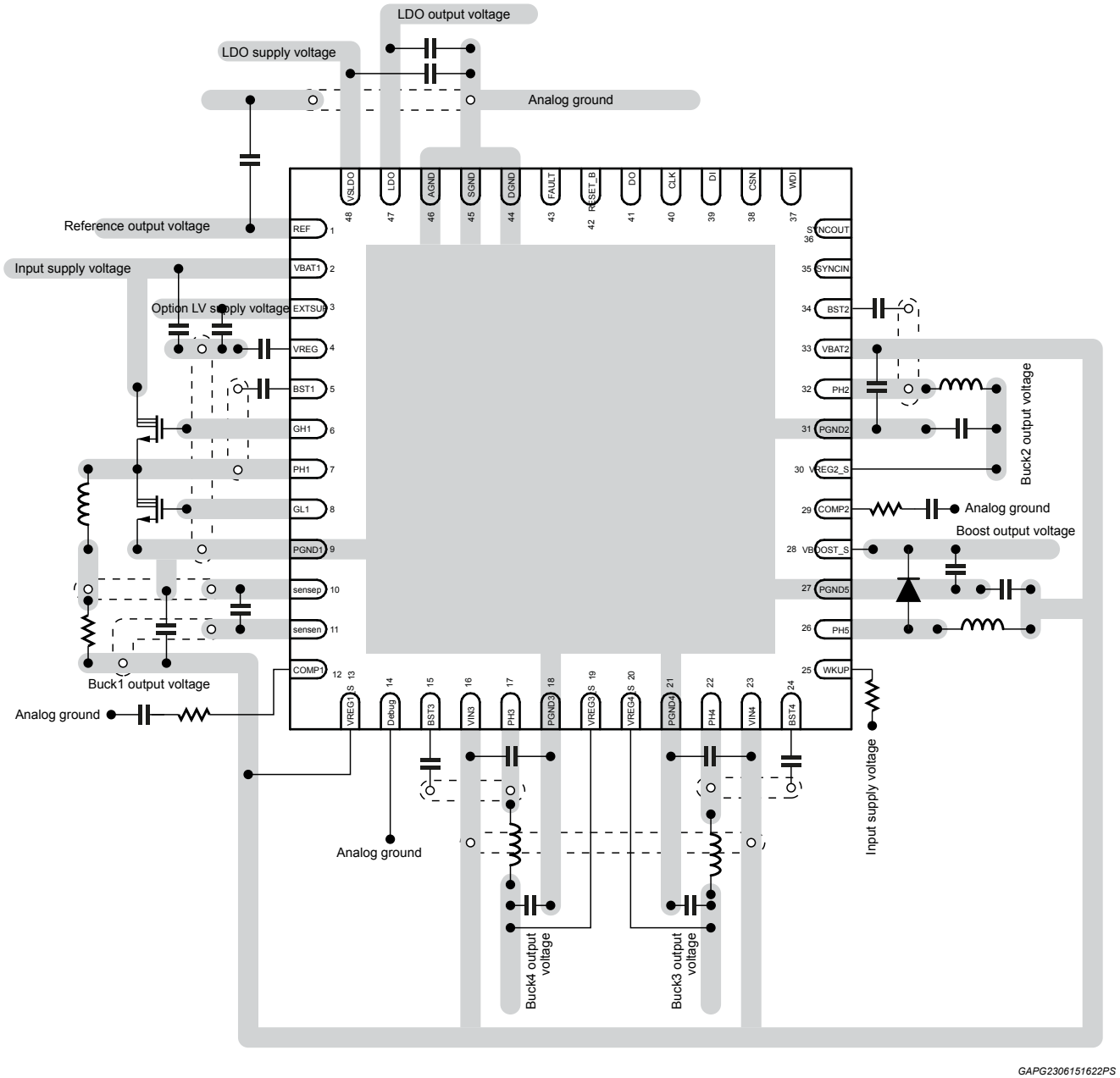
The input capacitor is chosen based on VIN(RIPPLE), and can be calculated as below:

$$C_{IN} > \frac{I_{RIPPLE}}{4 \times V_{IN(RIPPLE)} \times f_{SW}} \quad (51)$$

$$ESR < \frac{V_{IN(RIPPLE)}}{2 \times I_{IN(RIPPLE)}} . \quad (52)$$

8.2 PCB Layout example (BUCK1 as main regulator)

Figure 38. **PCB Layout example**



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 VFQFPN-48 (7x7x1.0 mm - opt. D) package information

Figure 39. **VFQFPN-48 (7x7x1.0 mm - opt. D) package outline**

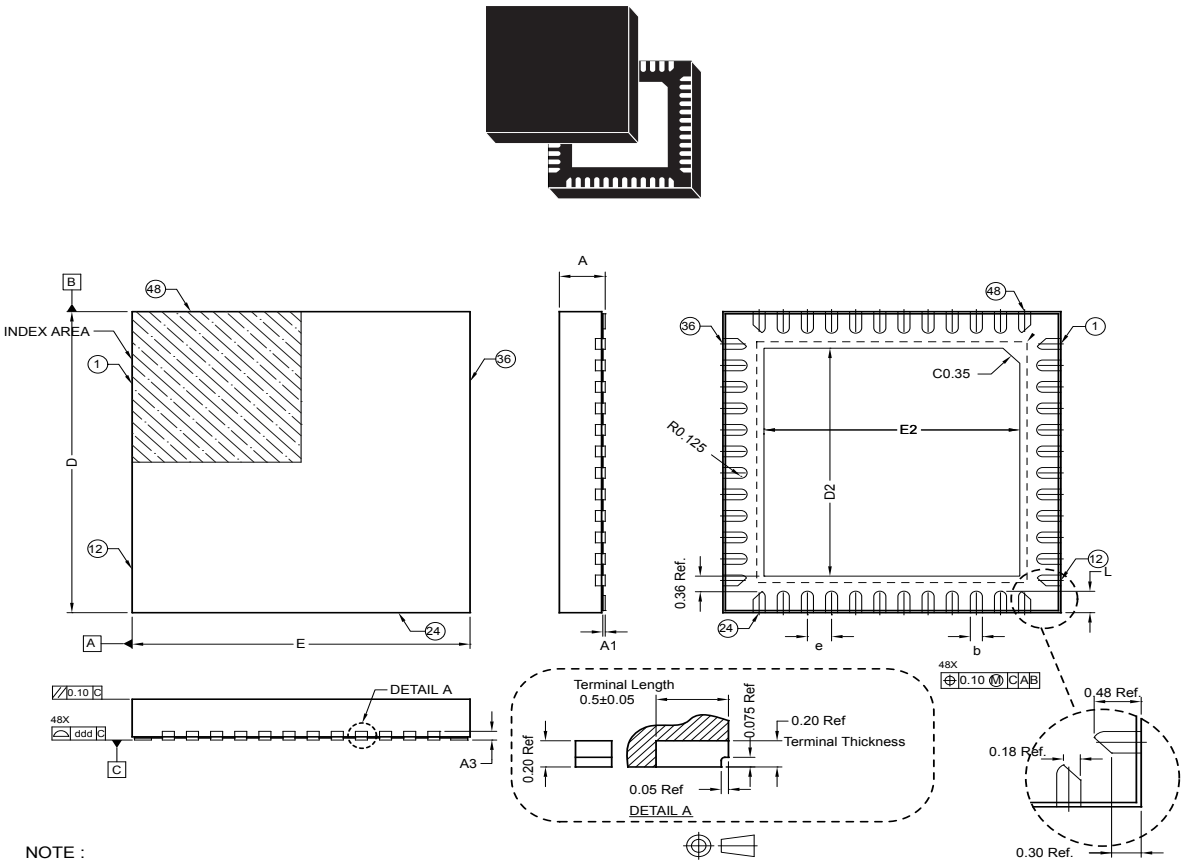


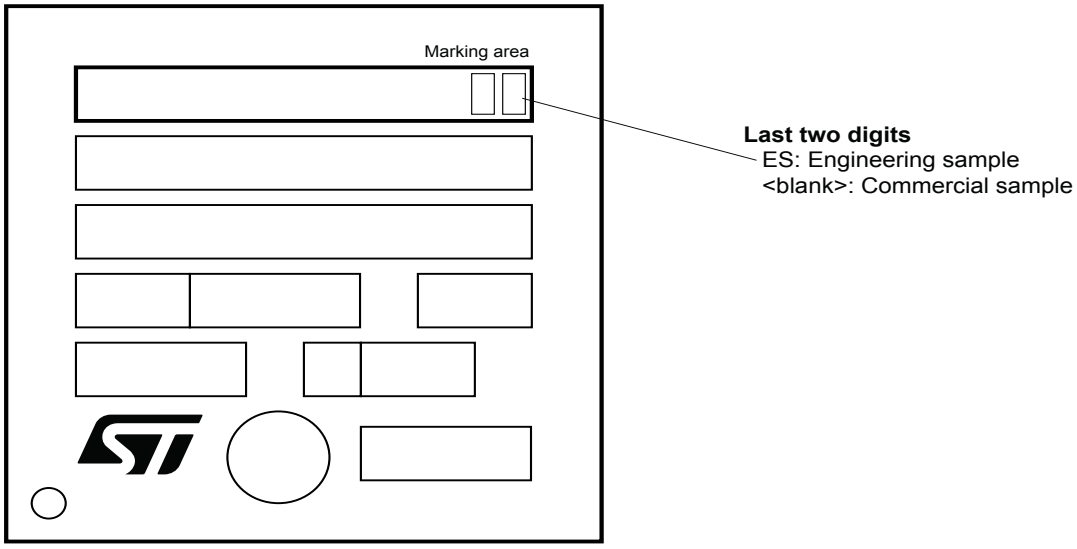
Table 35. **VFQFPN-48 (7x7x1.0 - opt. D) package mechanical data**

Ref	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.85	0.95	1.05
A1	-	-	0.05
A2	-	0.75	-

Ref	Dimensions (mm)		
	Min.	Typ.	Max.
A3	-	0.200	-
b	0.15	0.25	0.35
D	6.80	7.00	7.15
D2	5.15	5.30	5.45
E	6.85	7.00	7.15
E2	5.15	5.30	5.45
e	0.45	0.50	0.55
L	0.45	0.50	0.55
ddd	-	-	0.08

9.2 VFQFPN-48 (7x7x1.0) marking information

Figure 40. **VFQFPN-48 (7x7x1.0) marking information**



Parts marked as 'ES' are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

Revision history

Table 36. **Document revision history**

Date	Revision	Changes
04-Dec-2018	1	Initial release.
09-May-2019	2	Updated: Features; Section 4 Functional description; Electrical characteristics; Table 32. Top level safety requirements and Table 33. Functions and safety mechanism; INIT mode, OTP bit mapping and register configuration; From SPI REG ADC TH1 to SPI REG ADC TH7.

Contents

1 **Overview** 2
1.1 Simplified block diagram 2
1.2 Functional block diagram 2
2 **Pins description** 4
3 **Electrical specifications** 6
3.1 Absolute maximum ratings & operating voltage 6
3.2 Thermal data 7
3.2.1 Thermal resistance 7
3.2.2 Thermal warning and protection 7
3.3 Electrical characteristics 8
3.3.1 Electrical characteristic curves 16
4 **Functional description** 17
4.1 Programming by OTP 17
4.2 Voltage regulators and features description 17
4.2.1 VREG 17
4.2.2 Pre regulator BUCK1 18
4.2.3 Pre regulator BUCK2 20
4.2.4 Post regulator BUCK3 20
4.2.5 Post regulator BUCK4 21
4.2.6 BOOST 21
4.2.7 LDO 22
4.2.8 VREF 22
4.2.9 ADC 22
4.2.10 Wake up pin (WKUP) 23
4.2.11 Synchronizing pin (SYNC in/out) 23
4.2.12 Reset and Fault 24
4.2.13 Configurable watchdog and reset 26
4.2.14 Under-Voltage, Over-Voltage and Power-Good 28
4.2.15 Temperature control and VBATx voltage through internal ADC 29
4.2.16 Maximum Duty Cycle and Refresh Mode for Buck 31

4.2.17 Frequency-Hopping Spread Spectrum . . . 31
5 SPI format and register mapping . . . 32
5.1 SPI frame CRC generator . . . 34
5.2 SPI registers mapping . . . 35
5.2.1 SPI REG BUCK1 . . . 35
5.2.2 SPI REG BUCK2 . . . 36
5.2.3 SPI REG WD_REC_EN . . . 36
5.2.4 SPI REG BUCK4 . . . 37
5.2.5 SPI REG BOOST VREF . . . 37
5.2.6 SPI REG BUCK EN . . . 38
5.2.7 SPI REG WD . . . 38
5.2.8 SPI REG BUCK STAT1 . . . 39
5.2.9 SPI REG BUCK STAT2 . . . 39
5.2.10 SPI REG Fault Table PWUP . . . 40
5.2.11 SPI REG ADC TH1 . . . 41
5.2.12 SPI REG ADC TH2 . . . 41
5.2.13 SPI REG ADC TH3 . . . 41
5.2.14 SPI REG ADC TH4 . . . 41
5.2.15 SPI REG ADC TH5 . . . 42
5.2.16 SPI REG ADC TH6 . . . 42
5.2.17 SPI REG ADC TH7 . . . 42
5.2.18 SPI REG ADC VBAT1 . . . 43
5.2.19 SPI REG ADC VBAT2 . . . 43
5.2.20 SPI REG OT Warning . . . 44
5.2.21 SPI Fault STAT . . . 44
5.2.22 SPI Silicon Version . . . 44
5.2.23 SPI Device Identification . . . 46
6 Device operating mode . . . 47
6.1 Shutdown mode . . . 48
6.2 Standby mode . . . 48
6.3 INIT mode . . . 48
6.4 REC mode . . . 48

6.5 RAMPUP MAIN and SEC_UP 48
6.6 ACTIVE mode 51
6.7 OTP program mode 51
6.8 OTP bit mapping and register configuration 54
6.9 OTP (SAF) registers 60
6.9.1 SAF_REG_OP 60
6.9.2 SAF_REG_CFG 61
6.9.3 SAF_REG_DI 62
6.9.4 SAF_REG_D0_Bit_Ts 62
6.9.5 SAF_REG_STAT 63
6.10 Power down phase 63
6.11 Power up programming 64
7 Functional safety requirements 66
7.1 Functions and safety mechanism related to safety requirements 66
7.2 System safety mechanism 66
8 Application information 67
8.1 External components calculation 67
8.1.1 BUCK1 controller 67
8.1.2 BUCK2 controller 70
8.1.3 BUCK3, BUCK4 74
8.1.4 BOOST 75
8.2 PCB Layout example (BUCK1 as main regulator) 75
9 Package information 77
9.1 VFQFPN-48 (7x7x1.0 mm - opt. D) package information 77
9.2 VFQFPN-48 (7x7x1.0) marking information 78
Revision history 79

List of tables

Table 1. Pin description and functions . . . 4
Table 2. Absolute maximum ratings & operating voltage . . . 6
Table 3. Operation junction temperature . . . 7
Table 4. Temperature thresholds . . . 7
Table 5. Maximum suggested power . . . 8
Table 6. Electrical characteristics . . . 8
Table 7. UV masking time . . . 26
Table 8. Temperature diode characteristics . . . 29
Table 9. Input CSN . . . 33
Table 10. Input CLK, DI . . . 34
Table 11. DI, CLK and CSN timing . . . 34
Table 12. Output DO . . . 34
Table 13. CSN timing . . . 34
Table 14. OTP row programming . . . 53
Table 15. Reset activation OTP . . . 55
Table 16. Device identification OTP . . . 55
Table 17. WD_REC_en OTP . . . 55
Table 18. Buck1 CFG . . . 56
Table 19. Primary activation OTP . . . 56
Table 20. Buck2 CFG . . . 56
Table 21. Enables . . . 57
Table 22. SeqId Buck4, Buck3, LDO, Boost, Vref OTP . . . 57
Table 23. Buck4 CFG . . . 57
Table 24. OvRst_EN . . . 57
Table 25. Buck3 CFG . . . 58
Table 26. LDO CFG OTP . . . 58
Table 27. Boost CFG OTP . . . 58
Table 28. USR Area Protection OTP . . . 58
Table 29. PowrOn Delay OTP . . . 58
Table 30. WDG CFG OTP . . . 59
Table 31. VREF CFG OTP . . . 59
Table 32. Top level safety requirements . . . 66
Table 33. Functions and safety mechanism . . . 66
Table 34. System safety mechanism . . . 66
Table 35. VFQFPN-48 (7x7x1.0 - opt. D) package mechanical data . . . 77
Table 36. Document revision history . . . 79

List of figures

Figure 1. Simplified block diagram . . . 2
Figure 2. Functional block diagram . . . 3
Figure 3. Pin out (top view) . . . 4
Figure 4. Efficiency of Buck2 with Vin = 14 V and Vout = 3.3 V . . . 16
Figure 5. Efficiency of Buck3 with Vin = 3.3 V and Vout = 2 V . . . 16
Figure 6. Efficiency of Buck4 with Vin = 3.3 V and Vout = 1.8 V . . . 16
Figure 7. Efficiency of Boost with Vin = 3.3 V and Vout = 5 V . . . 16
Figure 8. VREG influence on PMIC behavior . . . 18
Figure 9. Pre regulator BUCK1 . . . 19
Figure 10. ADC circuit . . . 23
Figure 11. SYNC IN/OUT in Active mode . . . 24
Figure 12. SYNCOUT output buffer . . . 24
Figure 13. Reset circuit diagram in ACTIVE mode . . . 25
Figure 14. Fault function in active mode . . . 26
Figure 15. Watchdog behavior . . . 27
Figure 16. Watchdog timing if WD_REC_en = 1 . . . 27
Figure 17. Watchdog timing if WD_REC_en = 0 . . . 28
Figure 18. Watchdog Early, Safe and Late window diagram . . . 28
Figure 19. Output voltage and monitors . . . 29
Figure 20. VTSENSE vs. temperature . . . 30
Figure 21. Refresh mode in bucks . . . 31
Figure 22. SPI word representation . . . 32
Figure 23. SPI diagram . . . 33
Figure 24. SPI protocol diagram . . . 33
Figure 25. Structure of CRC generator . . . 35
Figure 26. State machine . . . 47
Figure 27. State machine for SEC UP . . . 50
Figure 28. OTP program flow chart . . . 52
Figure 29. OTP bit mapping . . . 54
Figure 30. Programmed configuration . . . 55
Figure 31. OTP start-up state check . . . 59
Figure 32. Power up sequence . . . 64
Figure 33. Power down sequence . . . 65
Figure 34. Basic control loop block diagram . . . 68
Figure 35. Simplified gain plot . . . 69
Figure 36. Basic control loop block diagram . . . 71
Figure 37. Simplified gain plot . . . 72
Figure 38. PCB Layout example . . . 76
Figure 39. VFQFPN-48 (7x7x1.0 mm - opt. D) package outline . . . 77
Figure 40. VFQFPN-48 (7x7x1.0) marking information . . . 78