



# **Dynamic Threshold Adjustment on ZeroPower Listening™ Microphone**

**Application Note  
Rev1.0  
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## 1. Introduction

Vesper's ZeroPower Listening™ (ZPL) microphone harvests sound energy in the environment using an external resistor to set the energy threshold at which the microphone switches from Wake on Sound (WoS) mode to full power normal mode. This Application note provides techniques to dynamically adjust the energy threshold using circuitry external to the VM1010 ZPL microphone.

## 2. General guidelines

The following key constraints are considered to design the circuitry to adjust the threshold dynamically for the different techniques in below sections.

- 1) Capacitive load on GA1 / GA2 pins used to adjust the threshold should be kept to minimum. Large capacitive load on either pin can cause significant degradation of frequency response in WoS mode and decreases the bandwidth in WoS mode.
- 2) Balance the load between GA1 and GA2 wherever possible, so that more of the capacitance can be moved to common mode with minimal impact to WoS frequency response.

### 2.1 External Resistor method

WoS Threshold can be adjusted by connecting a resistor between pins *GA1* and *GA2*. As can be seen in Figure 1, these pins provide access to the feedback network of an instrumentation amplifier in the WoS signal path:

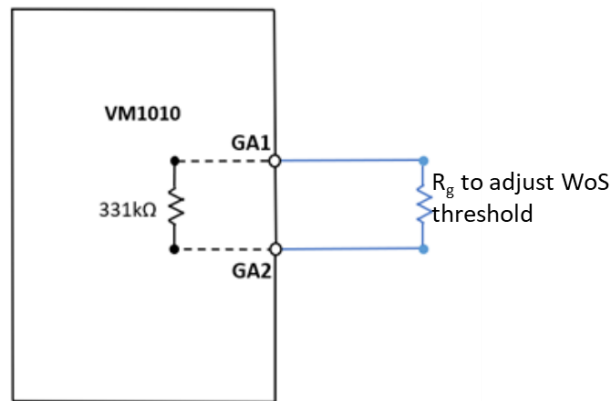


Figure 1: Fixed adjusted WoS threshold, implemented with external resistor (R<sub>g</sub>) between GA1 and GA2 pins

The smaller the resistor between GA1 and GA2, the higher the gain of the instrumentation amplifier. The resulting WoS threshold follows this formula:

$$WoS\ threshold = \left[ 89 - 20 \cdot \log_{10} \left( 1 + \left( \frac{331k\Omega}{R_g} \right) \right) \right] dBSPL$$

This formula holds true to a minimum threshold of 65dBSPL, as shown in Figure 2:

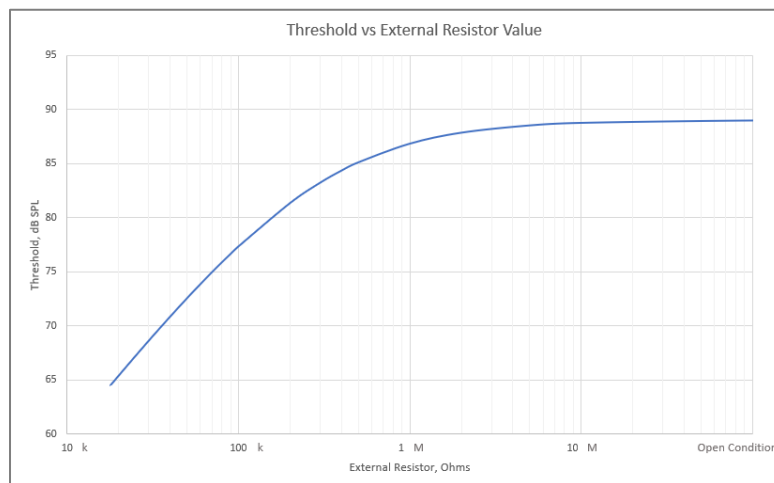


Figure 2: Graph of WoS threshold versus external gain resistor (R<sub>g</sub>)

GA1 and GA2 pins can each tolerate a maximum load capacitance of 5pF to GND. Therefore, it is best practice to keep the wires connecting R<sub>g</sub> to GA1 and GA2 as short as possible.

## 2.2 Analog Switch method

A resistor switch circuit can be used to adjust the threshold to three different WoS levels. By combining external resistors connected to GA1/GA2 pin on the ZPL microphone, the analog switch SW1/SW2 provide the three threshold levels. Circuit is designed to keep the capacitive loading on the GA1 and GA2 pins to a minimum of 5pf. Therefore, the key metric to look for when choosing an analog switch is the capacitance in the OFF position. The lower the value of this capacitance, the lower the impact on WoS frequency response. The threshold levels that correspond to the different switching positions for the resistor combination in Figure below is shown in Table 1.

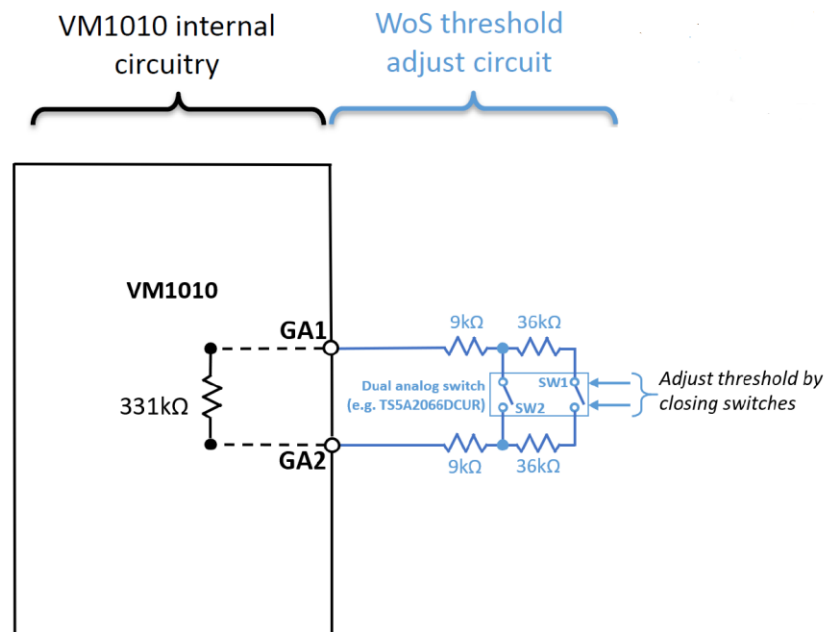


Figure 3: Threshold adjust circuit with Analog switch / resistor combination

| SW2 State<br>(high=closed) | SW1 State<br>(high=closed) | Rg<br>External<br>Resistance | GA1-GA2<br>Effective<br>Impedance<br>(331kΩ    Rg) | WoS<br>threshold |
|----------------------------|----------------------------|------------------------------|--|------------------|
| Low                        | Low                        | Open                         | 331 kΩ   | 89 dB SPL        |
| Low                        | High                       | 90 kΩ                        | 69 kΩ  | 77 dB SPL        |
| High                       | Low                        | 18 kΩ                        | 17 kΩ  | 65 dB SPL        |
| High                       | High                       | 18 kΩ                        | 17 kΩ  | 65 dB SPL        |

Table 1: WoS threshold levels achieved with circuit in Figure 3

An example of an analog switch is Texas Instruments TS5A2066 Single Pole Single Throw (SPST) switch ( <https://www.ti.com/lit/ds/symlink/ts5a2066.pdf> ) . The capacitance of this switch in the open position is 5.5 pF at  $V_{dd} = 5V$ . A typical schematic of the switch-resistor combination with the example of TS5A2066 is shown below.

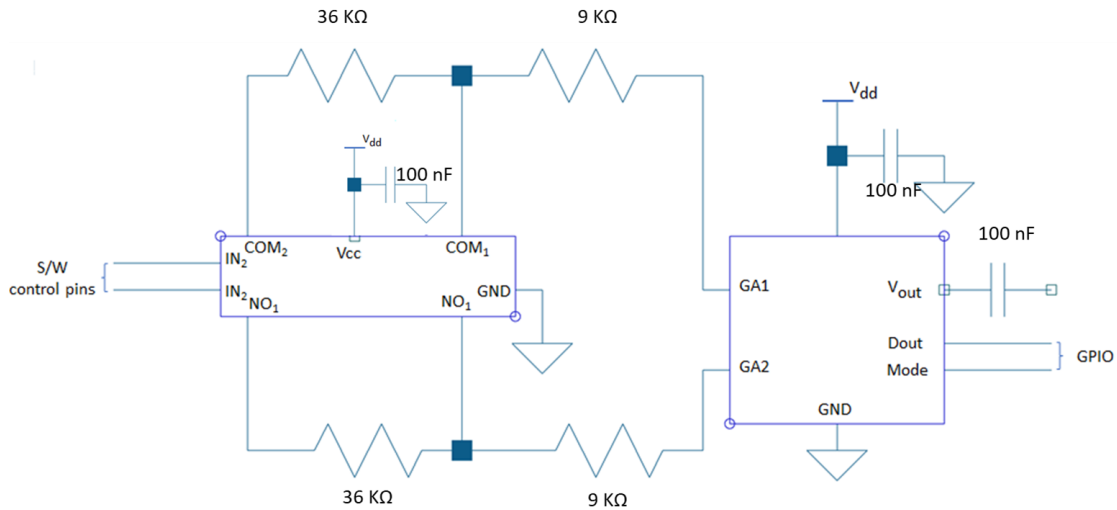


Figure 4: Example schematic with TS5A2066 SPST Switch and VM1010

In the schematic, you can see the resistor combination symmetrically connected on the COM and NO pins on the switch. The pins IN1 and IN2 control the switch using software interrupts. For reference, an incorrect implementation of the schematic is also shown in Figure 5 below.

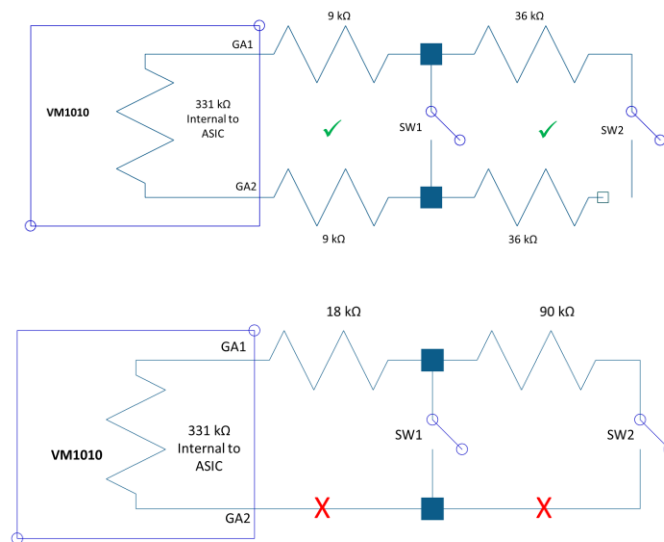


Figure 5: Analog switch method: Correct (top) and incorrect(bottom) implementation

Resistor values can be changed in the above circuit to vary the WoS threshold levels. In order to achieve the threshold levels 71 and 83 dB SPL

- a) Refer to the resistor vs. Threshold graph to obtain the external resistor value for each threshold – 30 kΩ for 71 dB SPL and 50 kΩ for 83 dB SPL.
- b) Split the resistor values to balance the load on either side of the switch as shown in figure.

| SW2 state<br>(high = closed) | SW1 state<br>(high = closed) | Rg External Resistance | GA1-GA2 Effective Impedance<br>(331kΩ    Rg) | WoS Threshold |
|------------------------------|------------------------------|------------------------|--|---------------|
| Low                          | Low                          | Open                   | 331 kΩ                                       | 89 dB SPL     |
| Low                          | High                         | 50 kΩ                  | 43 kΩ  | 83 dB SPL     |
| High                         | Low                          | 30 kΩ                  | 28 kΩ  | 71 dB SPL     |
| High                         | High                         | 30 kΩ                  | 28 kΩ  | 71 dB SPL     |

Table 2: Resistor values to implement 71, 83, 89 dB SPL thresholds

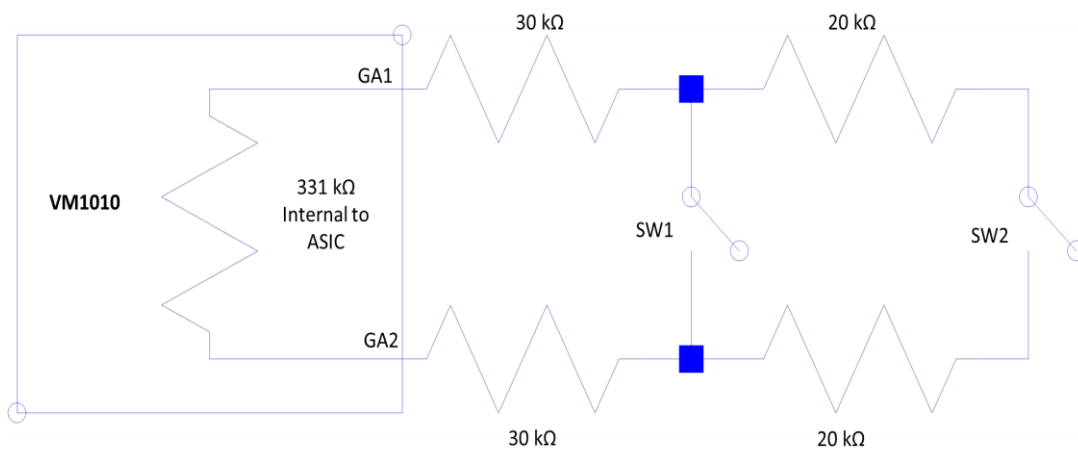


Figure 6: Switch Resistor circuit for 71, 83, 89 dB SPL thresholds



SPST switch is recommended to avoid any impact on WoS frequency response due to unbalanced load on GA1/GA2 pins. In case of substituting an SPST with SPDT switch, it is recommended to split the resistive load on either side of the switch to balance the load on the pins.

Note that a resistor can be added between GA1-GA2 pins to eliminate the 89-dB threshold, while still using the above resistor switch circuit. This means, the combination would still provide 3 different threshold configurations, but the maximum threshold setting can be below 89 dB SPL.

### 2.3 Digital Potentiometer method

A digital potentiometer can also be used as an alternative to external resistor method to adjust the WoS thresholds. Potentiometers with I2C control can be used to program the thresholds to vary from 65 – 89 dB SPL. Manual for programming TPL0102 is available at the link <http://www.ti.com/lit/ds/symlink/tpl0102-100.pdf>. TPL0102 is a widely available, low cost, small QFN package with a built-in shutdown switch. Dual 100 kΩ potentiometer in a single package allows to design a differential circuit with relatively low capacitance.

A typical circuit implementation for this method using TPL0102 is shown in Figure 7 below.

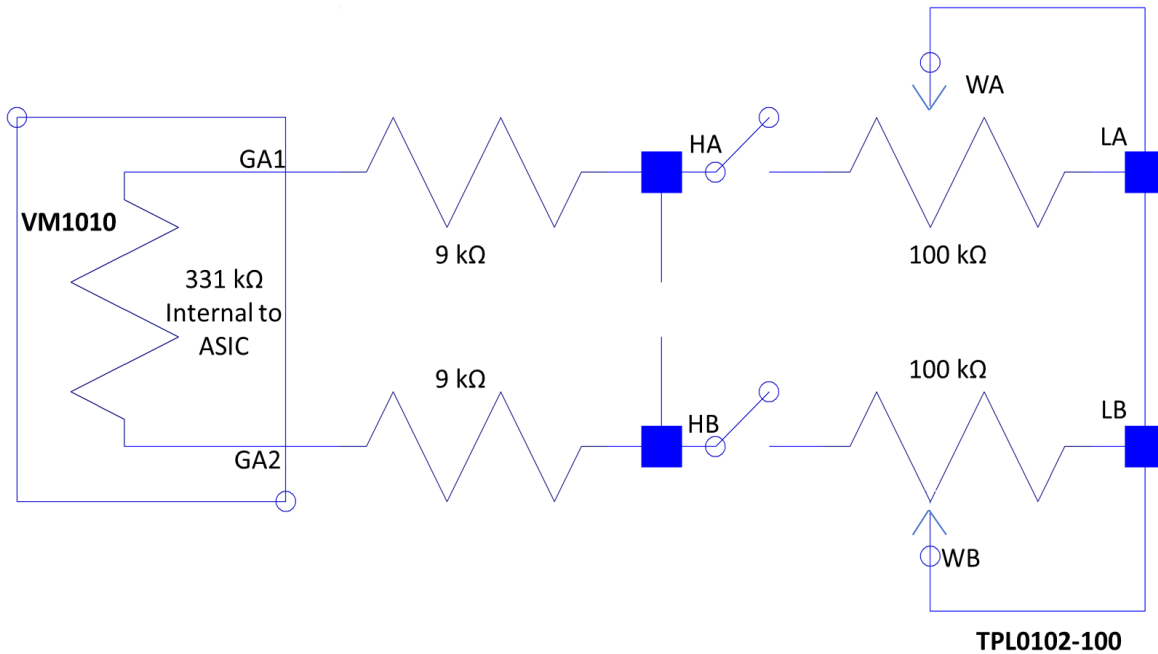


Figure 7: Digital Potentiometer circuit to adjust WoS Threshold

Potentiometer values can be changed to adjust GA1-GA2 impedance continuously from 18kOhm to 218kOhm. This corresponds to continuous threshold adjustment from 65 – 82 dB SPL. Shutdown switches inside the TPL0102-100 can be opened, to set GA1-GA2 impedance to infinity. This corresponds to a threshold setting of 89 dB SPL.

The resistance on each side between GA1/GA2 pins can be programmed by changing the wiper code from 0 to 255 using the below formula -

$$R_g = 18 \text{ k}\Omega + 2 * 100 \text{ k}\Omega * (255 - X) / 255$$

When the code is 255, W is at voltage of H since the output voltage is high. Therefore, the resistance is zero. When the code is 0, W is at voltage of L and resistance on one side is 100 KΩ. The resulting WoS threshold can then be calculated using the formula given in section 1.1 above.

This circuit minimizes the load capacitance on GA1/GA2 pins using the following mechanism:

- a) 9 kΩ Resistors separate CH (~ 22Pf) from GA1 and GA2 to reduce loading. These resistor values also enforce the minimum impedance of 18 KΩ between the pins.
- b) CW (~16pF) and CL (~22pF) are positioned symmetrically, so that they experience no voltage change when GA1 and GA2 move differentially. Thus, they have no impact on the differential load experienced by GA1 and GA2.

TPL0102 can also be put in a shutdown mode by executing proper command in the Access Control Register (ACR). Shutdown mode operates with a sleep current of 0.2 μA and wakes up within 35 μsec.

Note that TPL0102 is only compatible for systems that operate above 2.5V given the IC cannot operate below 1.8V. For systems that operate at 1.8V, alternative recommendation is to use MAXIM 5391 low voltage linear taper digital potentiometer. Below is a comparison of the pros and cons of the two parts -

| Part number / metric  | TI TPL0102                         | MAXIM 5931                  |
|---|------------------------------------|-----------------------------|
| Voltage supply  | 2.7 - 5.5 V                        | 1.7 – 5.5 V                 |
| Interface   | I2C interface                      | SPI interface               |
| Shutdown option (high impedance required for 89 dB threshold) | Shutdown option                    | No                          |
| Standby current   | 0.2 μA at 2.7V                     | 12 μA at 1.7V               |
| Adjustable threshold range with VM1010                        | 65 dB SPL – 89 dB SPL (full range) | 65 – 81 dB SPL              |
| Cost  | Cheaper                            | More expensive than TI part |

Table 3: Comparison of digital potentiometers

### 3. Supporting documentation

Application Note AN2 - Introducing ZeroPower Listening™ using VM1010

TI TPL0102 datasheet , <http://www.ti.com/lit/ds/symlink/tpl0102-100.pdf>

Maxim 5391 datasheet, <https://www.digikey.com/product-detail/en/maxim-integrated/MAX5391NATE-T/MAX5391NATE-TCT-ND/2272307>

For additional information on Vesper's latest roadmap of microphone products, reach out to [sales@vespermems.com](mailto:sales@vespermems.com).