16-Bit, 10 MSPS ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **High-Speed, Wide Bandwidth ΔΣ ADC**
- **10MSPS Output Data Rate**
- **4.9MHz Signal Bandwidth**
- **86dBFS Signal-to-Noise Ratio**
- **–94dB Total Harmonic Distortion**
- **95dB Spurious-Free Dynamic Range**
- **On-Chip Digital Filter Simplifies Anti-Alias Requirements**
- **$\overline{\text{SYNC}}$ Pin for Simultaneous Sampling with Multiple ADS1610s**
- **Low 3μs Group Delay**
- **Parallel Interface**
- **Directly Connects to TMS320 DSPs**
- **Out-of-Range Alert Pin**

APPLICATIONS

- **Scientific Instruments**
- **Test Equipment**
- **Communications**

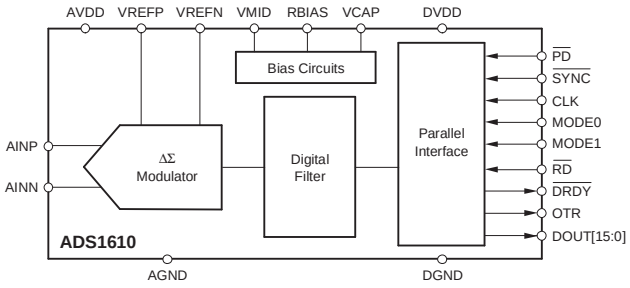
DESCRIPTION

The ADS1610 is a high-speed, high-precision, delta-sigma (ΔΣ) analog-to-digital converter (ADC) with 16-bit resolution operating from a 5V analog and a 3V digital supply. Featuring an advanced multi-stage analog modulator combined with an on-chip digital decimation filter, the ADS1610 achieves 86 dBFS signal-to-noise ratio (SNR) in a 5MHz signal bandwidth; while the total harmonic distortion is -94dB.

The ADS1610 ΔΣ topology provides key system-level design advantages with respect to anti-alias filtering and clock jitter. The design of the user's front-end anti-alias filter is simplified since the on-chip digital filter greatly attenuates out-of-band signals. The ADS1610s filter has a *brick wall* response with a very flat passband (±0.0002dB of ripple) followed immediately by a very wide stop band (5MHz to 55MHz). Clock jitter becomes especially critical when digitizing high frequency, large-amplitude signals. The ADS1610 significantly reduces clock jitter sensitivity by an effective averaging of clock jitter as a result of oversampling the input signal.

Output data is supplied over a parallel interface and easily connects to TMS320 digital signal processors (DSPs). The power dissipation can be adjusted with an external resistor, allowing for reduction at lower operating speeds.

With its outstanding high-speed performance, the ADS1610 is well-suited for demanding applications in data acquisition, scientific instruments, test and measurement equipment, and communications. The ADS1610 is offered in a TQFP64 package and is specified from –40°C to 85°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ADS1610 passes 1.5K CDM testing. ADS1610 passes 1kV human body model testing (TI Standard is 2kV).

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	VALUE	UNIT
AVDD to AGND	–0.3 to +6	V
DVDD to DGND	–0.3 to +3.6	V
AGND to DGND	–0.3 to +0.3	V
Input current, I_I	100, Momentary	mA
	10, Continuous	
Analog I/O to AGND	-0.3 to AVDD + 0.3	V
Digital I/O to DGND	-0.3 to DVDD + 0.3	V
Maximum junction temperature, T_J	150	°C
Operating free-air temperature range, T_A	-40 to +105	°C
Storage temperature range, T_{stg}	-60 to +150	°C
Lead temperature (soldering, 10s)	260	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

All specifications at –40°C to 85°C, AVDD = 5V, DVDD = 3V, f_{CLK} = 60MHz, V_{REF} = 3V, MODE = 00, V_{CM} = 2.5V, and RBIAS = 19kΩ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
$V_{ID(AINP - AINN)}$	Differential input voltage (AINP-AINN)			$\pm V_{REF}$		V
$V_{IC(AINP + AINN)/2}$	Common-mode input voltage			2.5		V
V_{IHA}	Absolute input voltage (AINP or AINN with respect to AGND)		–0.1		4.2	V
DYNAMIC SPECIFICATIONS						
	Data rate			$10\left(\frac{f_{CLK}}{60\ MHz}\right)$		MSPS
SNR	Signal-to-noise ration relative to full-scale (1)	f_{IN} = 100kHz, –2dBFS	83	86		dBFS

(1) For reference, this dynamic specification is extrapolated to full-scale and is thus dBFS. Subsequent dynamic specifications are dBc (dB), which is: Specification (in dBc) = Specification (in dBFS) + AIN (input amplitude in dBFS). For more information see Understanding and comparing datasheets for high-speed ADCs.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at –40°C to 85°C, AVDD = 5V, DVDD = 3V, f_{CLK} = 60MHz, V_{REF} = 3V, MODE = 00, V_{CM} = 2.5V, and RBIAS = 19kΩ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	f_{IN} = 100kHz, –2dBFS	81	84		dB
		f_{IN} = 100kHz, –6dBFS	77	80		
		f_{IN} = 100kHz, –20dBFS		66		
		f_{IN} = 1MHz, –2dBFS		83		
		f_{IN} = 1MHz, –6dBFS		80		
		f_{IN} = 1MHz, –20dBFS		66		
		f_{IN} = 4MHz, –2dBFS	79.5	83		
		f_{IN} = 4MHz, –6dBFS	76	79		
		f_{IN} = 4MHz, –20dBFS		65		
THD	Total harmonic distortion	f_{IN} = 100kHz, –2dBFS		–90	–83	dB
		f_{IN} = 100kHz, –6dBFS		–95	–85	
		f_{IN} = 100kHz, –20dBFS		–95		
		f_{IN} = 1MHz, –2dBFS		–91		
		f_{IN} = 1MHz, –6dBFS		–93		
		f_{IN} = 1MHz, –20dBFS		–95		
		f_{IN} = 4MHz, –2dBFS		–109	–100	
		f_{IN} = 4MHz, –6dBFS		–105	–100	
		f_{IN} = 4MHz, –20dBFS		–95		
SINAD	Signal-to-noise and distortion	f_{IN} = 100kHz, –2dBFS		83		dB
		f_{IN} = 100kHz, –6dBFS		79		
		f_{IN} = 100kHz, –20dBFS		65		
		f_{IN} = 1MHz, –2dBFS		82		
		f_{IN} = 1MHz, –6dBFS		79		
		f_{IN} = 1MHz, –20dBFS		65		
		f_{IN} = 4MHz, –2dBFS		83		
		f_{IN} = 4MHz, –6dBFS		79		
		f_{IN} = 4MHz, –20dBFS		65		
SFDR	Spurious-free dynamic range	f_{IN} = 100kHz, –2dBFS	85	90		dB
		f_{IN} = 100kHz, –6dBFS	90	96		
		f_{IN} = 100kHz, –20dBFS		96		
		f_{IN} = 1MHz, –2dBFS		94		
		f_{IN} = 1MHz, –6dBFS		94		
		f_{IN} = 1MHz, –20 dBFS		96		
		f_{IN} = 4MHz, –2dBFS	100	109		
		f_{IN} = 4MHz, –6dBFS	100	105		
		f_{IN} = 4MHz, –20dBFS		95		
	Aperture jitter	Excludes jitter of CLK source		2		ps, rms
	Aperture delay			4		ns

ELECTRICAL CHARACTERISTICS (Continued)

All specifications at –40°C to 85°C, AVDD = 5V, DVDD = 3V, f_{CLK} = 60MHz, V_{REF} = 3V, MODE = 00, V_{CM} = 2.5V, and RBIAS = 19kΩ (unless otherwise noted).

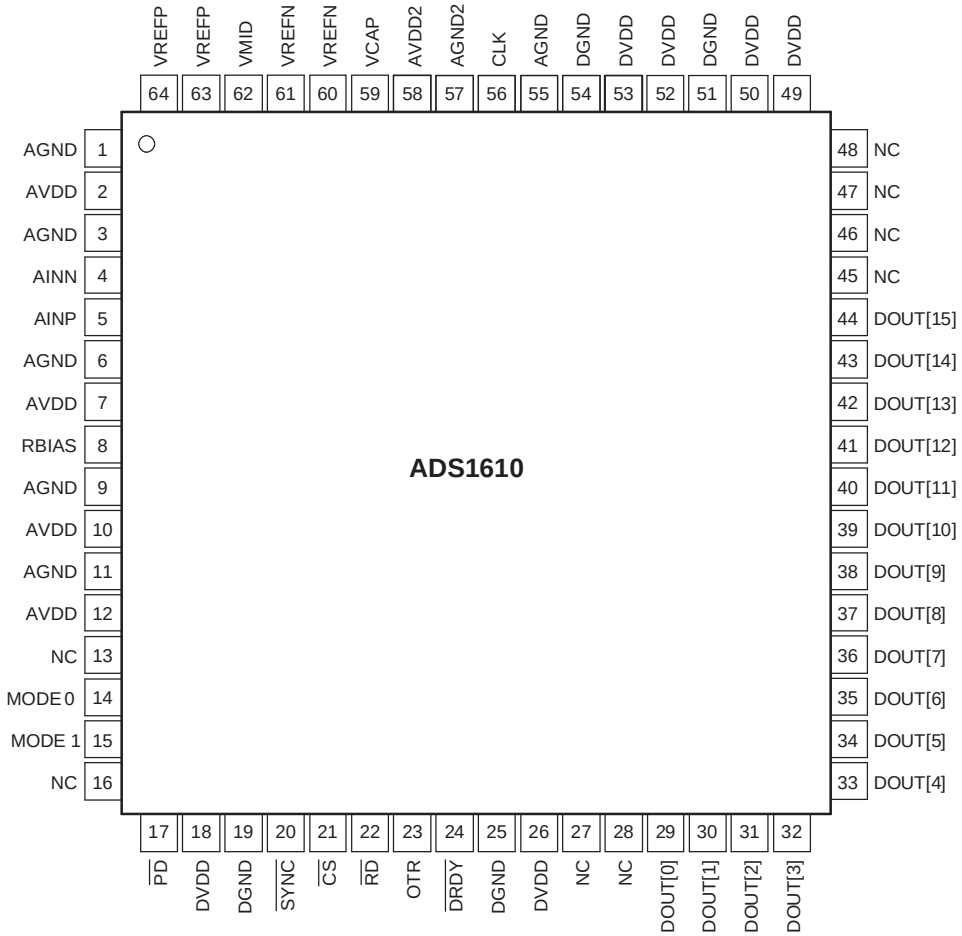
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL FILTER CHARACTERISTICS						
	Passband		0		$4.4\left(\frac{f_{CLK}}{60\ MHz}\right)$	MHz
	Passband ripple				±0.0002	dB
	Passband transition	–0.1dB attenuation		$4.6\left(\frac{f_{CLK}}{60\ MHz}\right)$		MHz
		–3.0dB attenuation		$4.9\left(\frac{f_{CLK}}{60\ MHz}\right)$		
	Stop band		5.6		54.4	MHz
	Stop band attentuation		80	See Figure 34		dB
$t_{d(grp)}$	Group delay			$3.0\left(\frac{60\ MHz}{f_{CLK}}\right)$		µs
t_s	Settling time	To ±0.001%		$5.5\left(\frac{60\ MHz}{f_{CLK}}\right)$		µs
STATIC SPECIFICATIONS						
	Resolution	No missing codes	16			Bits
	Input rms noise	Shorted input		1.0	1.4	LSB (rms)
	Integral nonlinearity	1V input		±0.4		LSB
		2.5V input		±1.5		LSB
	Differential nonlinearity			±0.5		LSB
V_{IO}	Offset error	T = 25°C		0.05		%FS
	Offset drift			5		ppm/°C
$G_{(ERR)}$	Gain error	T = 25°C		±0.3(1)		%FS
G	Gain drift	Excluding reference drift		10		ppm/°C
CMRR	Common-mode rejection ratio	At DC		60		dB
PSRR	Supply-voltage rejection ratiio	At DC		80		dB
VOLTAGE REFERENCE						
V_{ref}	Reference voltage, (VREFP - VREFN)		2.9	3.0	3.1	V
VREFP			3.6	4.0	4.4	V
VREFN			0.9	1.0	1.1	V
VMID			2.2	2.5	3.8	V
DIGITAL INPUT/OUTPUT						
V_{IH}	High-level input voltage		0.7DVDD		DVDD	V
V_{IL}	Low-level input voltage		DGND		0.3DVDD	V
V_{OH}	High-level output voltage	I_{OH} = –50µA	0.8DVDD			V
V_{OL}	Low-level output voltage	I_{OL} = 50µA			0.2DVDD	V
I_{lkg}	Input leakage current	DGND < $V_{DIGITAL\ INPUT}$ < DVDD			±10	µA
POWER-SUPPLY REQUIREMENTS						
V_{AVDD}	AVDD voltage		4.9	5.0	5.1	V
V_{DVDD}	DVDD voltage		2.7	3.0	3.6	V
I_{AVDD}	AVDD current			150	170	mA
I_{DVDD}	DVDD current			70	80	mA
P_D	Power dissipation			960	1100	mW
		$\overline{PD}$ = low		4		

(1) There is a constant gain error of 3.8% in addition to the variable gain eror of ±0.3%. Therefore, the gain error is 3.8 ±0.3%.

DEVICE INFORMATION

PIN CONFIGURATION

HTQFP
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION
NAME	NO.		
AGND	1, 3, 6, 9, 11, 55	Analog	Analog ground
AVDD	2, 7, 10, 12	Analog	Analog supply
AINN	4	Analog input	Negative analog input
AINP	5	Analog input	Positive analog input
RBIAS	8	Analog	Analog bias setting resistor
NC	13, 16, 27, 28, 45–48	—	Must be left unconnected.
MODE	14, 15	Digital input	Control for four output modes (See *MODE SELECTION* section)
$\overline{PD}$	17	Digital input; active low	Power-down
DVDD	18, 26, 49, 50, 52, 53	Digital	Digital supply
DGND	19, 25, 51, 54	Digital	Digital ground
$\overline{SYNC}$	20	Digital input; active low	Digital reset
$\overline{CS}$	21	Digital input; active low	Chip-select

TERMINAL FUNCTIONS (continued)

TERMINAL		ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION
NAME	NO.		
$\overline{RD}$	22	Digital input; Active low	Read enable
OTR	23	Digital output	Analog inputs out-of-range
$\overline{DRDY}$	24	Digital output	Data ready
DOUT[15:0]	29–44	Digital output	Data output. DOUT[15] is the MSB and DOUT[0] is the LSB.
CLK	56	Digital input	Clock input
AGND2	57	Analog	Analog ground for AVDD2
AVDD2	58	Analog	Analog supply for modulator clocking
VCAP	59	Analog	Bypass capacitor
VREFN	60, 61	Analog	Negative reference voltage
VMID	62	Analog	Midpoint voltage
VREFP	63, 64	Analog	Positive reference voltage

TIMING SPECIFICATIONS

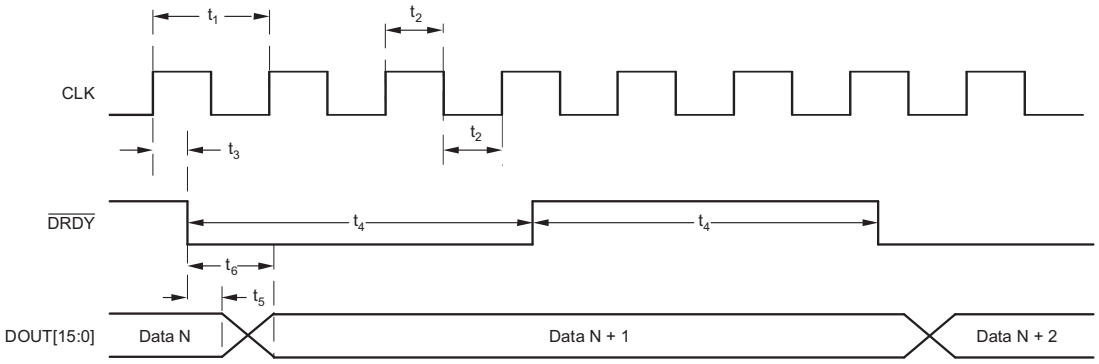


Figure 1. Data Retrieval Timing

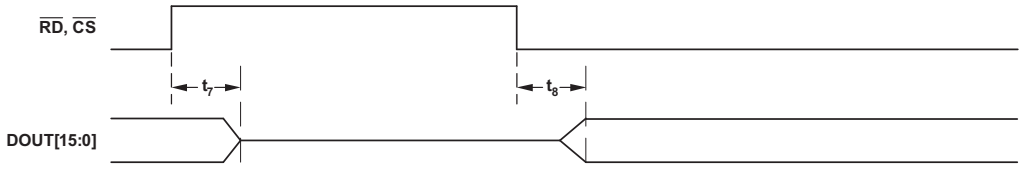


Figure 2. DOUT Inactive/Active Timing

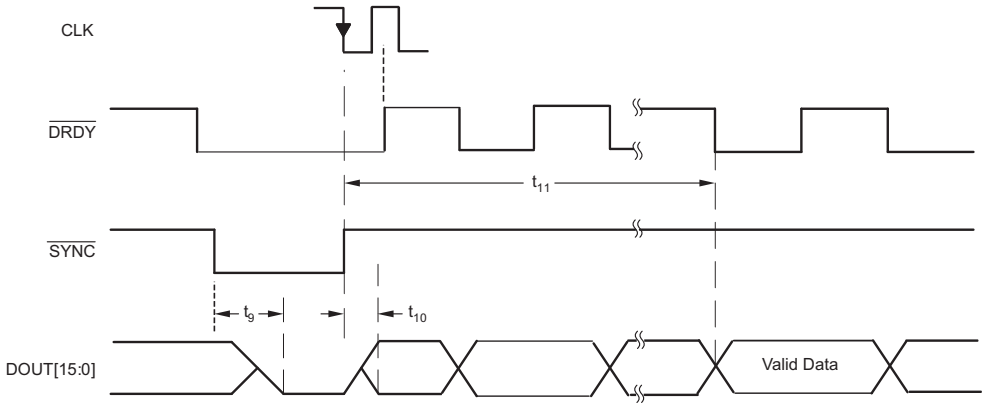


Figure 3. Reset Timing

Timing Specifications(1)

	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	CLK period ($1/f_{CLK}$)	16.667			ns
$1/t_1$	f_{CLK}	1		60	MHz
t_2	CLK pulse width, high or low	45%		55%	ns
t_3	CLK to $\overline{DRDY}$ high (propagation delay)		12		ns
t_4	$\overline{DRDY}$ pulse width, high or low		3 t_1		ns
t_5	Previous data valid (hold time)	0			ns
t_6	New data valid (setup time)			5	ns
t_7	$\overline{RD}$ and/or $\overline{CS}$ inactive (high) to DOUT high impedance		15		ns
t_8	$\overline{RD}$ and/or $\overline{CS}$ active (low) to DOUT active		15		ns
t_9	Delay from $\overline{SYNC}$ active (low) to all-zero DOUT[15:0]		12		ns
t_{10}	Delay from $\overline{SYNC}$ inactive (high) to non-zero DOUT[15:0]			21	DRDY
t_{11}	Delay from $\overline{SYNC}$ inactive (high)to valid DOUT[15:0] (time – 55 $\overline{DRDY}$ cycles; required for digital filter to settle).		55		DRDY

(1) Output load = 10pF|| 500kΩ.

TYPICAL CHARACTERISTICS

At T_A = 25°C, R_{BIAS} = 19kΩ, AVDD = 5V, DVDD = 3V, f_{CLK} = 60MHz, V_{REF} = 3V, MODE = 00,and V_{CM} = 2.5V (unless otherwise noted).

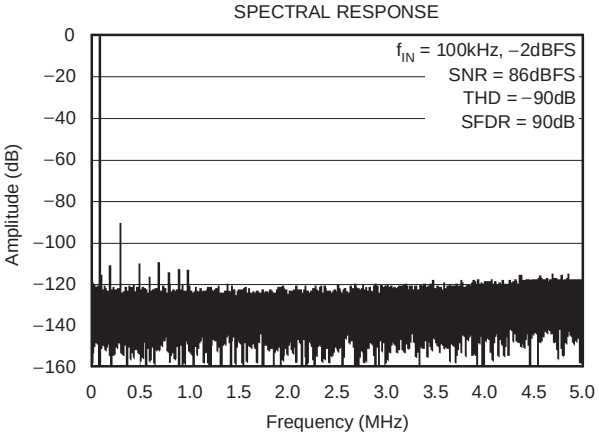


Figure 4.

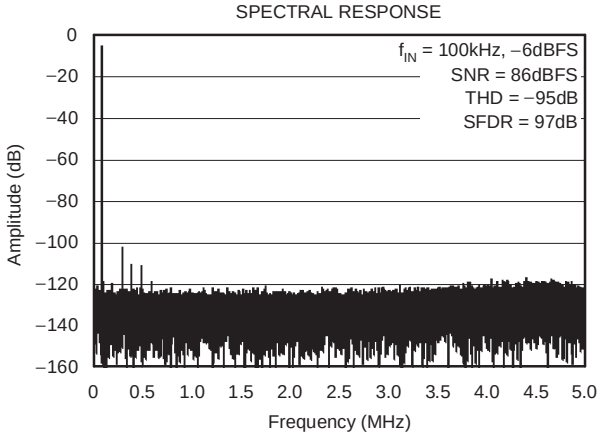


Figure 5.

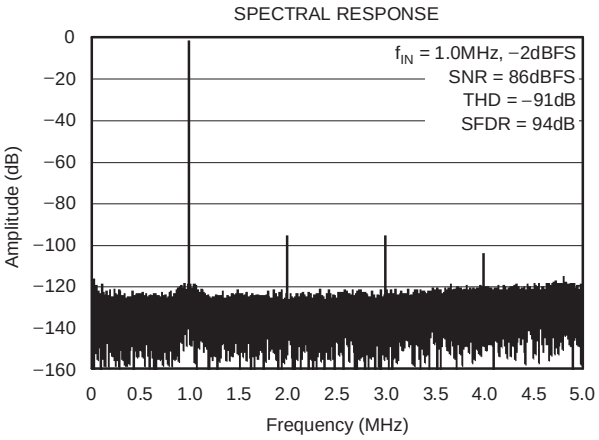
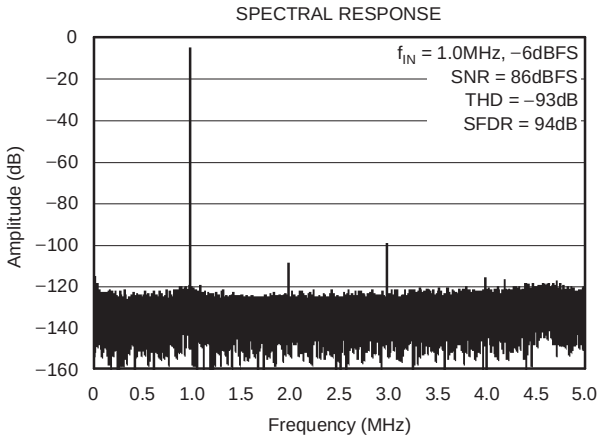


Figure 6.



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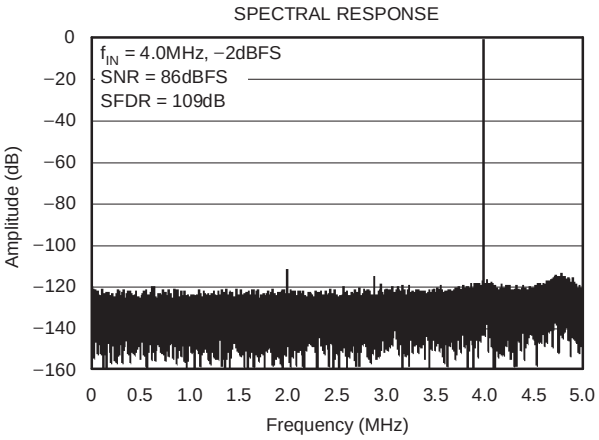


Figure 8.

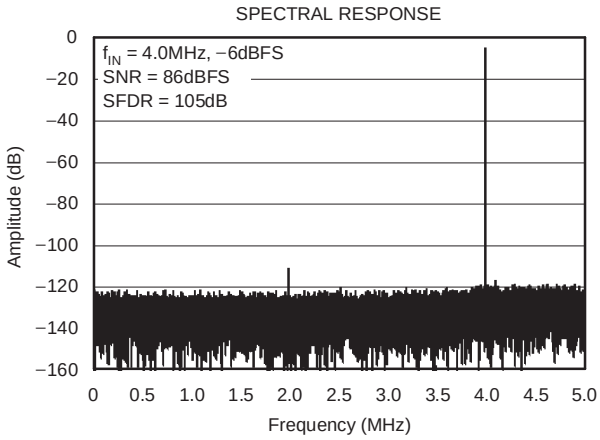


Figure 9.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, R_{BIAS} = 19kΩ, AVDD = 5V, DVDD = 3V, f_{CLK} = 60MHz, V_{REF} = 3V, MODE = 00,and V_{CM} = 2.5V (unless otherwise noted).

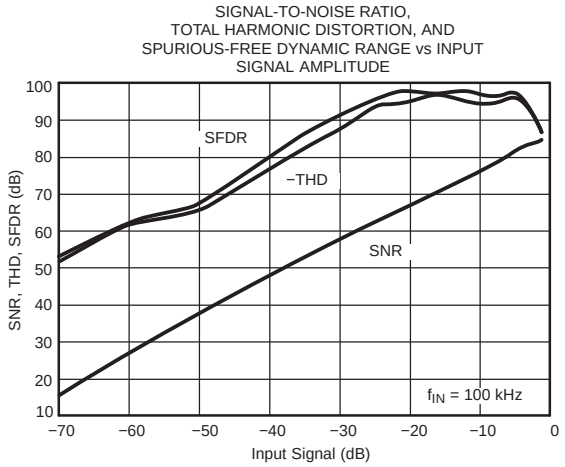


Figure 10.

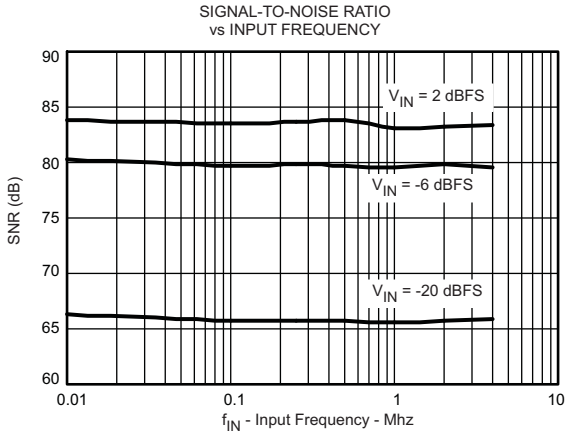


Figure 11.

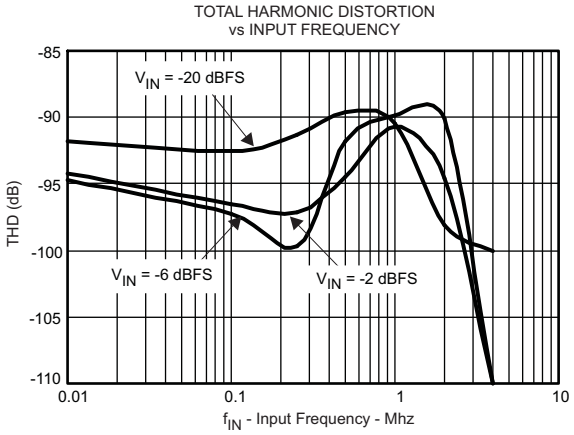


Figure 12.

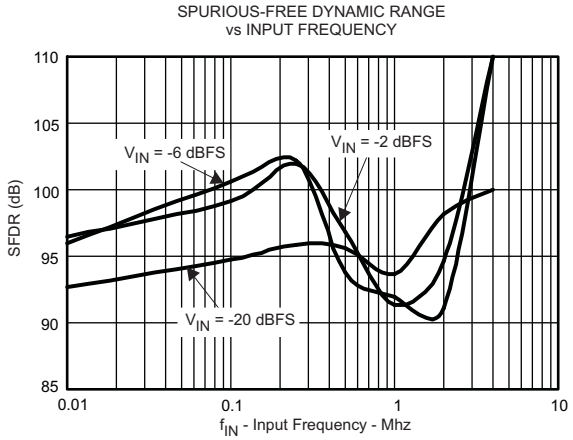


Figure 13.

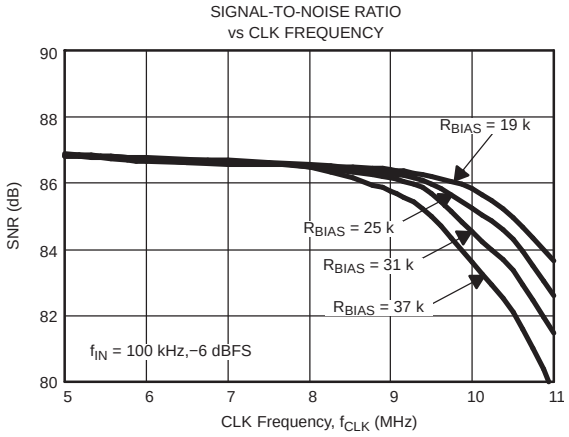


Figure 14.

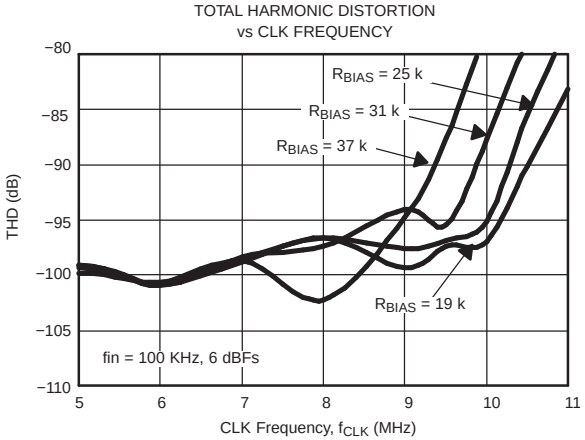


Figure 15.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, R_{BIAS} = 19kΩ, AVDD = 5V, DVDD = 3V, f_{CLK} = 60MHz, V_{REF} = 3V, MODE = 00,and V_{CM} = 2.5V (unless otherwise noted).

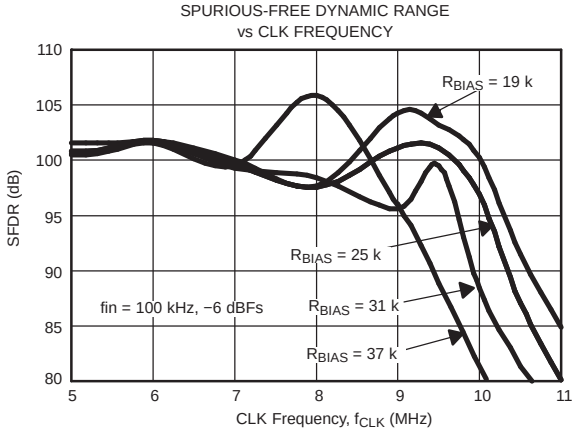


Figure 16.

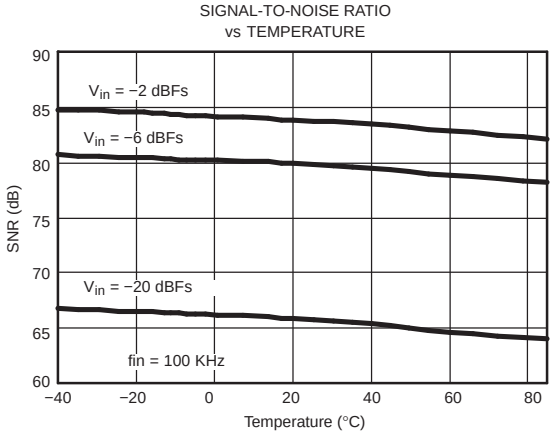


Figure 17.

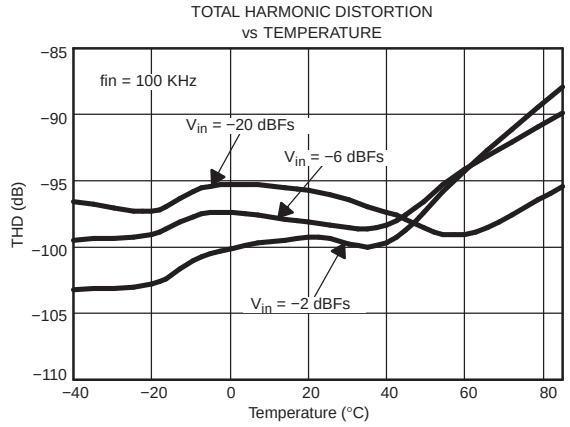


Figure 18.

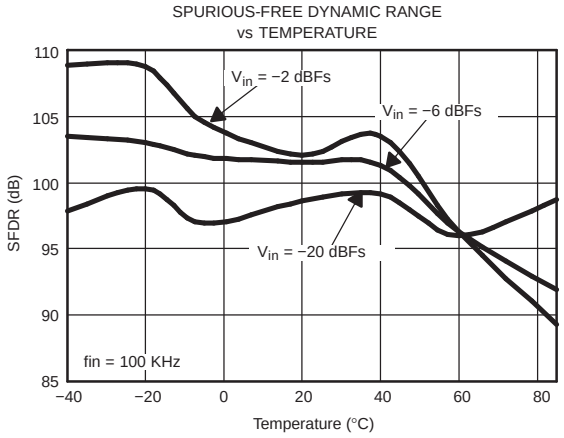


Figure 19.

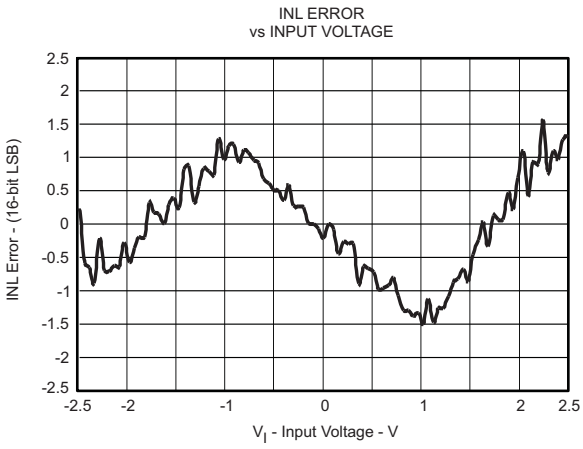


Figure 20.

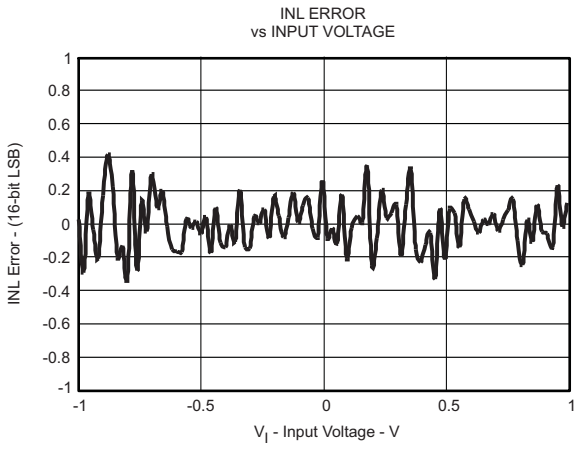


Figure 21.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, R_{BIAS} = 19kΩ, AVDD = 5V, DVDD = 3V, f_{CLK} = 60MHz, V_{REF} = 3V, MODE = 00,and V_{CM} = 2.5V (unless otherwise noted).

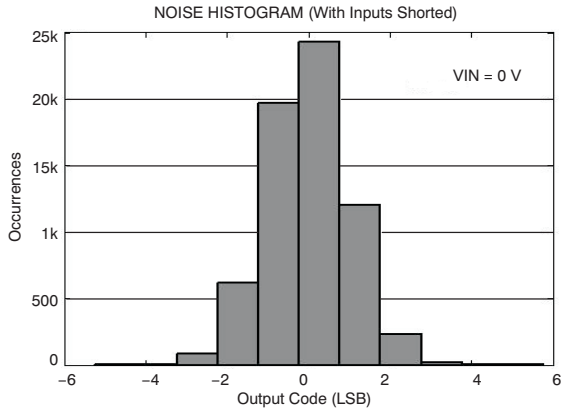


Figure 22.

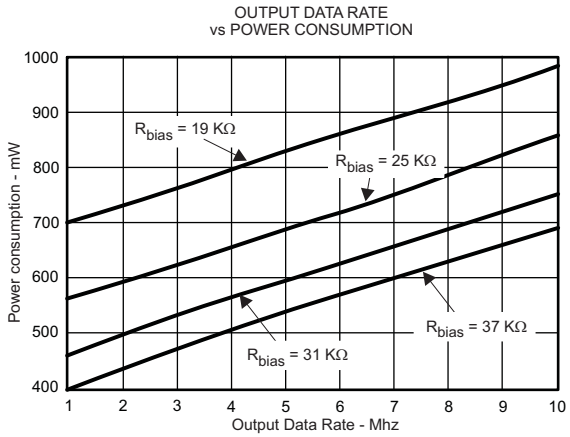


Figure 23.

OVERVIEW

The ADS1610 is a high-performance, delta-sigma ADC. The modulator uses an inherently stable, pipelined, delta-sigma modulator architecture incorporating proprietary circuitry that allows for very linear high-speed operation. The modulator samples the input signal at 60MSPS (when f_{CLK} = 60MHz). A low-ripple linear phase digital filter decimates the modulator output by 6 to provide data output word rates of 10MSPS with a signal passband out to 4.9MHz.

Conceptually, the modulator and digital filter measure the differential input signal, V_{ID} = (AINP – AINN), against the differential reference, V_{ref} = (VREFP – VREFN), as shown in Figure 11. A 16-bit parallel data bus, designed for direct connection to DSPs, outputs the data. A separate power supply for the I/O allows flexibility for interfacing to different logic families. Out-of-range conditions are indicated with a dedicated digital output pin. Analog power dissipation is controlled using an external resistor. This allows reduced dissipation when operating at slower speeds. When not in use, power consumption can be dramatically reduced using the $\overline{PD}$ pin.

ANALOG INPUTS (AINP, AINN)

The ADS1610 supports a very wide range of input signals. Having such a wide input range makes out-of-range signals unlikely. However, should an out-of-range signal occur, the digital output OTR will go high.

To achieve the highest analog performance, it is recommended that the inputs be limited to no greater than 0.891VREF (-1dBFS). For VREF = 3V, the corresponding recommended input range is 2.67V.

The analog inputs must be driven with a differential signal to achieve optimum performance. The recommended common-mode voltage of the input signal, $V_{CM} = \frac{AINP + AINN}{2}$ is 2.5V.

In addition to the differential and common-mode input voltages, the absolute input voltage is also important. This is the voltage on either input (AINP or AINN) with respect to AGND. The range for this voltage is:

$$-0.1\ V < (AINN \text{ or } AINP) < 4.2\ V \quad (1)$$

If either input is taken below –0.1V, ESD protection diodes on the inputs will turn on. Exceeding 4.2V on either input will result in linearity performance degradation. ESD protection diodes will also turn on if the inputs are taken above AVDD (+5V).

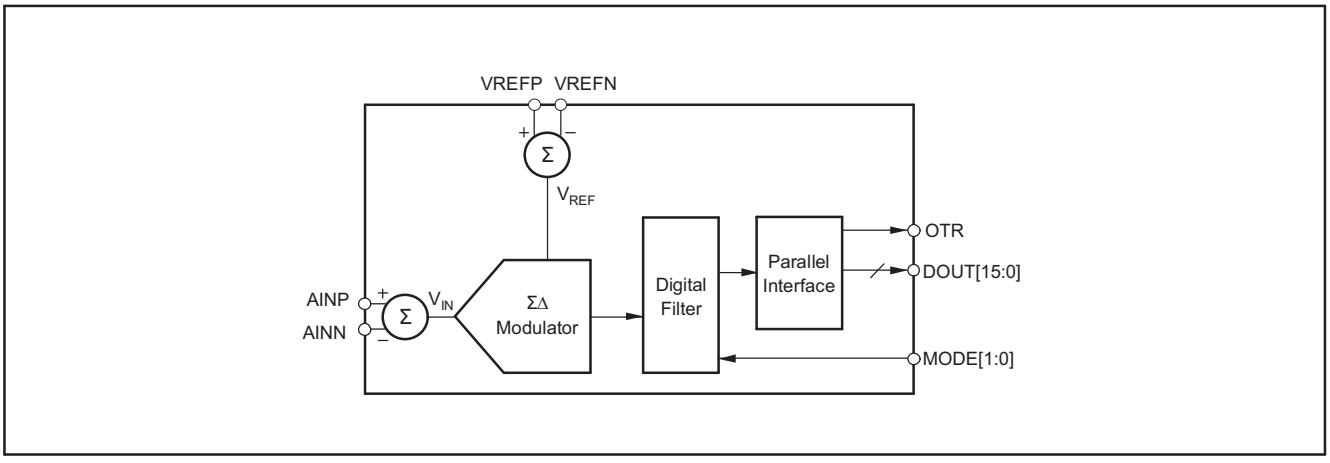


Figure 24. Conceptual Block Diagram

INPUT CIRCUITRY

The ADS1610 uses switched-capacitor circuitry to measure the input voltage. Internal capacitors are charged by the inputs and then discharged internally with this cycle repeating at the frequency of CLK. Figure 25 shows a conceptual diagram of these circuits. Switches S_2 represent the net effect of the modulator circuitry in discharging the sampling capacitors, the actual implementation is different. The timing for switches S_1 and S_2 is shown in Figure 26.

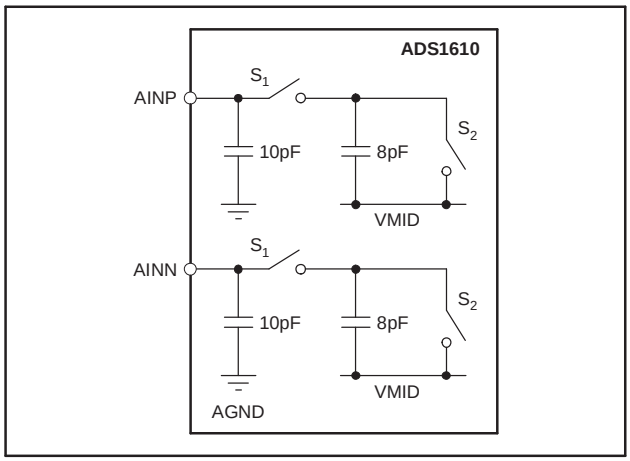


Figure 25. Conceptual Diagram of Internal Circuitry Connected to the Analog Inputs

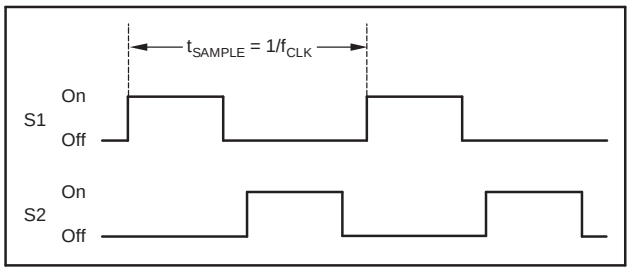


Figure 26. Timing for the Switches in Figure 25

DRIVING THE INPUTS

The external circuits driving the ADS1610 inputs must be able to handle the load presented by the switching capacitors within the ADS1610. The input switches S_1 in Figure 25 are closed approximately one half of the sampling period, t_{SAMPLE}, allowing only ~8 ns for the internal capacitors to be charged by the inputs, when f_{CLK} = 60MHz.

Figure 27 and Figure 28 show the recommended circuits when using single-ended or differential op amps, respectively. The analog inputs must be driven differentially to achieve optimum performance. If only a single-ended input signal is available, the configuration in Figure 27 can be used by shorting $-V_{IN}$ to ground.

This configuration would implement the single-ended to differential conversion.

The external capacitors, between the inputs and from each input to AGND, improve linearity and should be placed as close to the pins as possible. Place the drivers close to the inputs and use good capacitor bypass techniques on their supplies; usually a smaller high-quality ceramic capacitor in parallel with a larger capacitor. Keep the resistances used in the driver circuits low-thermal noise in the driver circuits degrades the overall noise performance. When the signal can be AC-coupled to the ADS1610 inputs, a simple RC filter can set the input common mode voltage. The ADS1610 is a high-speed, high-performance ADC. Special care must be taken when selecting the test equipment and setup used with this device. Pay particular attention to the signal sources to ensure they do not limit performance when measuring the ADS1610.

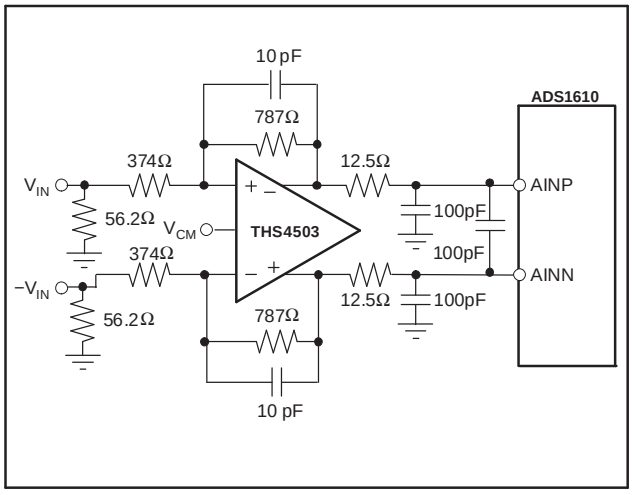


Figure 27. Recommended Single-Ended to Differential Conversion Circuit Using the THS4503 Differential Amplifier

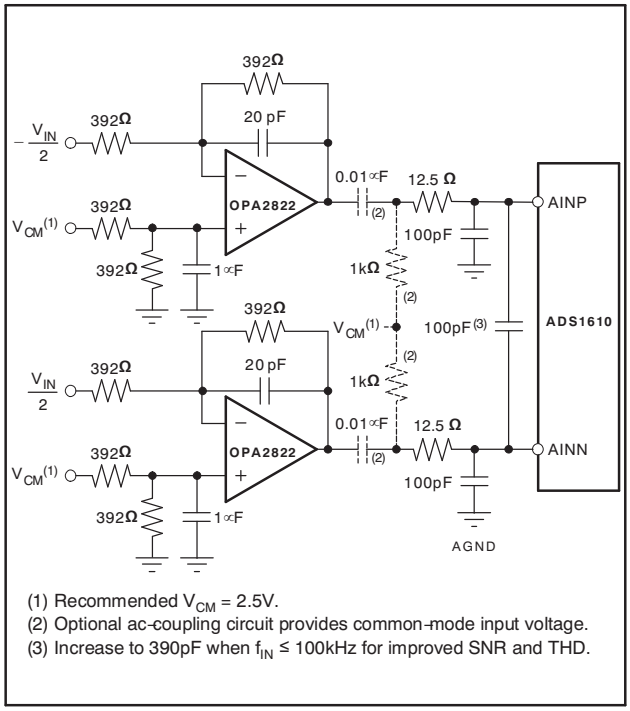


Figure 28. Recommended Driver Circuit Using the OPA2822

REFERENCE INPUTS (VREFN, VREFP, VMID)

The ADS1610 operates from an external voltage reference. The reference voltage (V_{ref}) is set by the differential voltage between VREFN and VREFP: V_{ref} = (VREFP – VREFN). VREFP and VREFN each use two pins, which should be shorted together. VMID, approximately 2.5V, is used by the modulator. VCAP connects to an internal node and must also be bypassed with an external capacitor.

The voltages applied to these pins must be within the values specified in the Electrical Characteristics table. Typically VREFP = 4V, VMID = 2.5V, and VREFN = 1V. The external circuitry must be capable of providing both a DC and a transient current. Figure 29 shows a simplified diagram of the internal circuitry of the reference. As with the input circuitry, switches S_1 and S_2 open and close as shown in Figure 26.

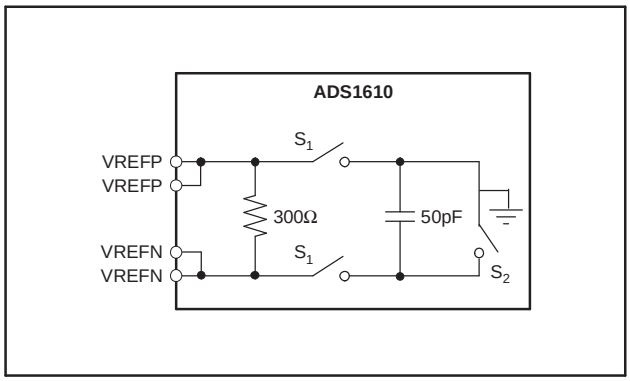


Figure 29. Conceptual Circuitry for the Reference Inputs

Figure 30 shows the recommended circuitry for driving these reference inputs. Keep the resistances used in the buffer circuits low to prevent excessive thermal noise from degrading performance. Layout of these circuits is critical, make sure to follow good high-speed layout practices. Place the buffers and especially the bypass capacitors as close to the pins as possible.

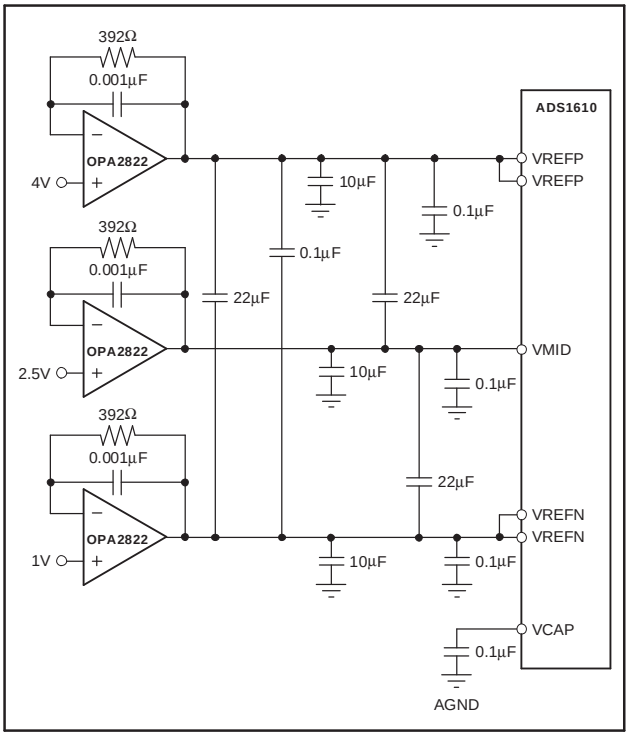


Figure 30. Recommended Reference Buffer Circuit

CLOCK INPUT (CLK)

The ADS1610 uses an external clock signal to be applied to the CLK input pin. The sampling of the modulator is controlled by this clock signal. As with any high-speed data converter, a high quality clock is essential for optimum performance. Crystal clock oscillators are the recommended CLK source; other sources, such as frequency synthesizers may not be adequate. Make sure to avoid excess ringing on the CLK input; keeping the trace as short as possible will help.

Measuring high-frequency, large-amplitude signals requires tight control of clock jitter. The uncertainty during sampling of the input from clock jitter limits the maximum achievable SNR. This effect becomes more pronounced with higher frequency and larger magnitude inputs. The ADS1610 oversampling topology reduces clock jitter sensitivity over that of Nyquist rate converters like pipeline and successive approximation converters by a factor of $\sqrt{6}$.

In order to not limit the ADS1610 SNR performance, keep the jitter on the clock source below the values shown in Table 1. When measuring lower frequency and lower amplitude inputs, more CLK jitter can be tolerated. In determining the allowable clock source jitter, select the worst-case input (highest frequency, largest amplitude) that will be seen in the application.

DATA FORMAT

The 16-bit output data is in binary two's complement format, as shown in Table 2. When the input is positive out-of-range, exceeding the positive full-scale value of V_{REF}, the output clips to all $7FFF_H$ and the OTR output goes high.

Table 1. Maximum Allowable Clock Source Jitter for Different Input Signal Frequencies and Amplitude

INPUT SIGNAL		MAXIMUM ALLOWABLE CLOCK SOURCE JITTER
MAXIMUM FREQUENCY	MAXIMUM AMPLITUDE	
4MHz	–1dB	1.6ps
4MHz	–20dB	14ps
2MHz	–1dB	3.3ps
2MHz	–20dB	29ps
1MHz	–1dB	6.5ps
1MHz	–20dB	58ps
100kHz	–1dB	65ps
100kHz	–20dB	581ps

Table 2. Output Code Versus Input Signal

INPUT SIGNAL (INP – INN)	IDEAL OUTPUT CODE(1)	OTR
≥ $+V_{ref}$ (> 0dB)	$7FFF_H$	1
V_{ref} (0dB)	$7FFF_H$	0
$\frac{+V_{REF}}{2^{15}-1}$	0001_H	0
0	0000_H	0
$\frac{-V_{REF}}{2^{15}-1}$	$FFFF_H$	0
$-V_{REF}\left(\frac{2^{15}}{2^{15}-1}\right)$	8000_H	0
$\le -V_{REF}\left(\frac{2^{15}}{2^{15}-1}\right)$	8000_H	1

(1)Excludes effects of noise, INL, offset and gain errors.

Likewise, when the input is negative out-of-range by going below the negative full-scale value of V_{ref}, the output clips to 8000_H and the OTR output goes high. The OTR remains high while the input signal is out-of-range.

OUT-OF-RANGE INDICATION (OTR)

If the output code on DOUT[15:0] exceeds the positive or negative full-scale, the out-of-range digital output (OTR) will go high on the falling edge of $\overline{DRDY}$. When the output code returns within the full-scale range, OTR returns low on the falling edge of $\overline{DRDY}$.

DATA RETRIEVAL

Data retrieval is controlled through a simple parallel interface. The falling edge of the $\overline{DRDY}$ output indicates new data is available. To activate the output bus, both $\overline{CS}$ and $\overline{RD}$ must be low, as shown in Table 3. Make sure the DOUT bus does not drive heavy loads (> 20pF), as this will degrade performance. Use an external buffer when driving an edge connector or cables.

Table 3. Truth Table for $\overline{CS}$ and $\overline{RD}$

$\overline{CS}$	$\overline{RD}$	DOUT [15:0]
0	0	Active
0	1	High impedance
1	0	High impedance
1	1	High impedance

SYNCHRONISING MULTIPLE ADS1610s

The ADS1610 is asynchronously reset when the $\overline{SYNC}$ pin is taken low. During reset, all of the digital circuits are cleared, DOUT[15:0] are forced low, and $\overline{DRDY}$ forced high. It is recommended that the $\overline{SYNC}$ pin be released on the falling edge of CLK. Afterwards, $\overline{DRDY}$ goes low on the second rising edge of CLK. Allow 55 $\overline{DRDY}$ cycles for the digital filter to settle before retrieving data. See Figure 3 for the timing specifications.

Reset can be used to synchronize multiple ADS1610s. All devices to be synchronized must use a common CLK input. With the CLK inputs running, pulse $\overline{SYNC}$ on the falling edge of CLK, as shown in Figure 31. Afterwards, the converters will be converting synchronously with the $\overline{DRDY}$ outputs updating simultaneously. After synchronization, allow 55 $\overline{DRDY}$ cycles (t_{11}) for output data to fully settle.

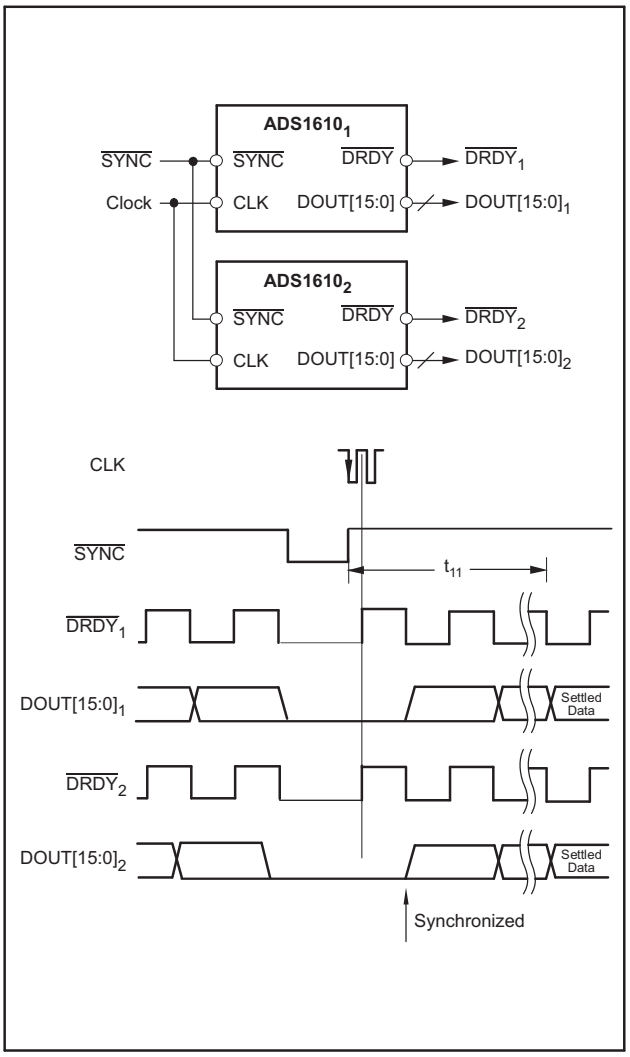


Figure 31. Synchronizing Multiple Converters

SETTLING TIME

The settling time is an important consideration when measuring signals with large steps or when using a multiplexer in front of the analog inputs. The ADS1610 digital filter requires time for an instantaneous change in signal level to propagate to the output.

Be sure to allow the filter time to settle after applying a large step in the input signal, switching the channel on a multiplexer placed in front of the inputs, resetting the ADS1610, or exiting the power-down mode.

Figure 32 shows the settling error as a function of time for a full-scale signal step applied at t = 0, with MODE = 00 (See Table 4). This figure uses $\overline{\text{DRDY}}$ cycles for the ADS1610 for the time scale (X-axis). After 55 $\overline{\text{DRDY}}$ cycles, the settling error drops below 0.001%. For f_{CLK} = 60MHz, this corresponds to a settling time of 5.5µs.

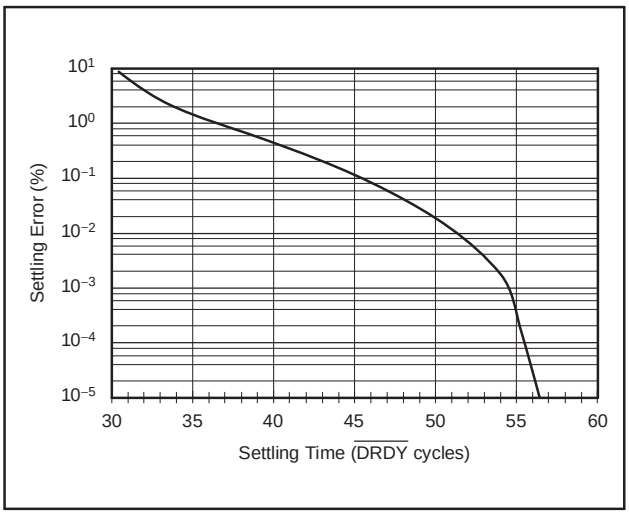


Figure 32. Settling Time

IMPULSE RESPONSE

Figure 33 plots the normalized response for an input applied at t = 0, with MODE = 00. The X-axis units of time are $\overline{\text{DRDY}}$ cycles for the ADS1610. As shown in Figure 33, the peak of the impulse takes 30 $\overline{\text{DRDY}}$ cycles to propagate to the output. For f_{CLK} = 60 MHz, a $\overline{\text{DRDY}}$ cycle is 0.1µs in duration and the propagation time (or group delay) is 30 × 0.1µs = 3.0 µs.

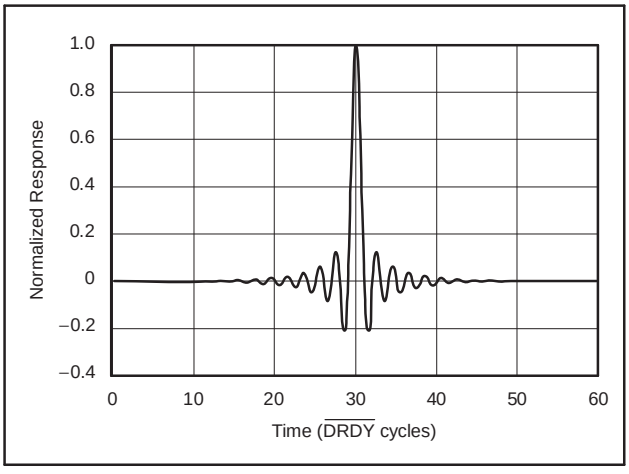


Figure 33. Impulse Response

FREQUENCY RESPONSE

The linear phase FIR digital filter sets the overall frequency response. The decimation rate is set to 6 (MODE = 00) for all the figures shown in this section. Figure 34 shows the frequency response from DC to 30 MHz for f_{CLK} = 60 MHz. The frequency response of the ADS1610 filter scales directly with CLK frequency. For example, if the CLK frequency is decreased by half (to 30 MHz), the values on the X-axis in Figure 34 would need to be scaled by half, with the span becoming DC to 15MHz.

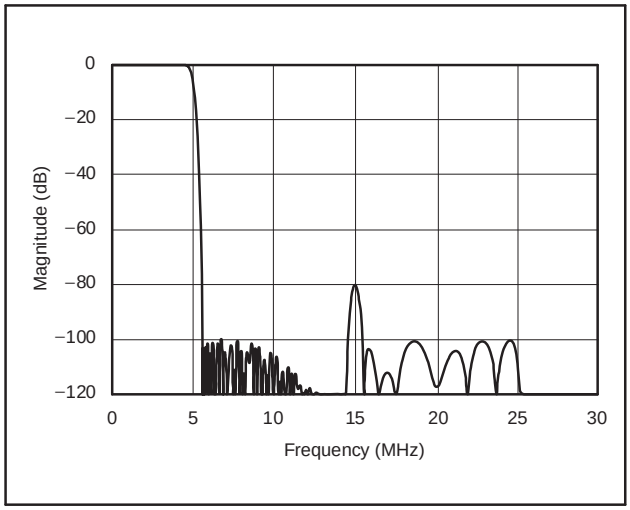


Figure 34. Frequency Response

Figure 35 shows the passband ripple from DC to 4.4MHz (f_{CLK} = 60MHz). Figure 36 shows a closer view of the passband transition by plotting the response from 4.0MHz to 5.0MHz (f_{CLK} = 60MHz).

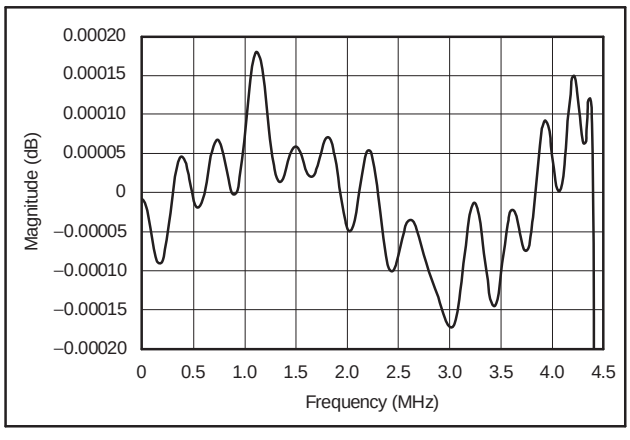


Figure 35. Passband Ripple

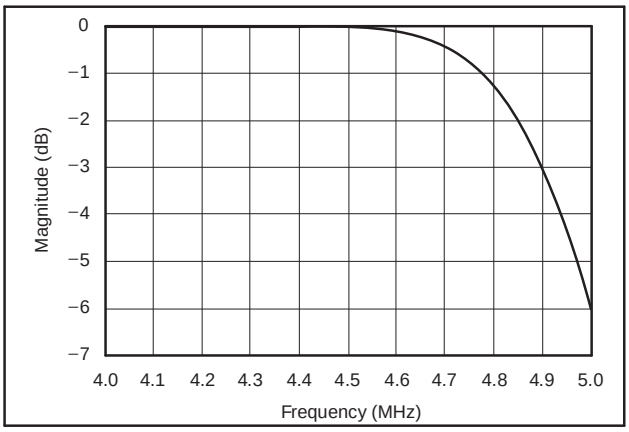


Figure 36. Passband Transition

The overall frequency response repeats at multiples of the CLK frequency. To help illustrate this, Figure 37 shows the response out to 180 MHz (f_{CLK} = 60MHz). Notice how the passband response repeats at 60MHz, 120MHz, and 180MHz; it is important to consider this sequence when there is high-frequency noise present with the signal. The modulator bandwidth extends to 100MHz. High-frequency noise around 60MHz and 120MHz will not be attenuated by either the modulator or the digital filter. This noise will alias back inband and reduce the overall SNR performance unless it is filtered out prior to the ADS1610. To prevent this, place an anti-alias filter in front of the ADS1610 that rolls off before 55MHz.

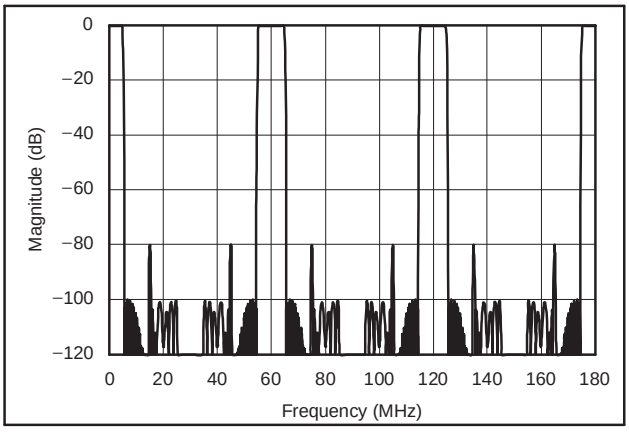


Figure 37. Frequency Response Out to 120MHz

NOISE FLOOR

The ADS1610 is a delta sigma ADC and it uses noise shaping to achieve superior SNR performance. The noise floor of a typical successive approximation (SAR) or a pipeline ADC remains flat until the nyquist frequency occurs. A gain of 3dB in SNR can be achieved by averaging two samples, thereby having a tradeoff between output data rate and achievable SNR. In contrast, the noise floor of the ADS1610 inside the bandwidth of interest is shaped. Hence, the gain in SNR that can be achieved by averaging two samples is more than 3dB. Figure 38 below shows the typical in-band noise spectral density of the ADS1610. The numbers in the bottom of the figure represent the noise distribution with respect to a full-scale signal in different bandwidths of interest. The shaded area represents the signal bandwidth in the default mode of operation (10MHz output data rate).

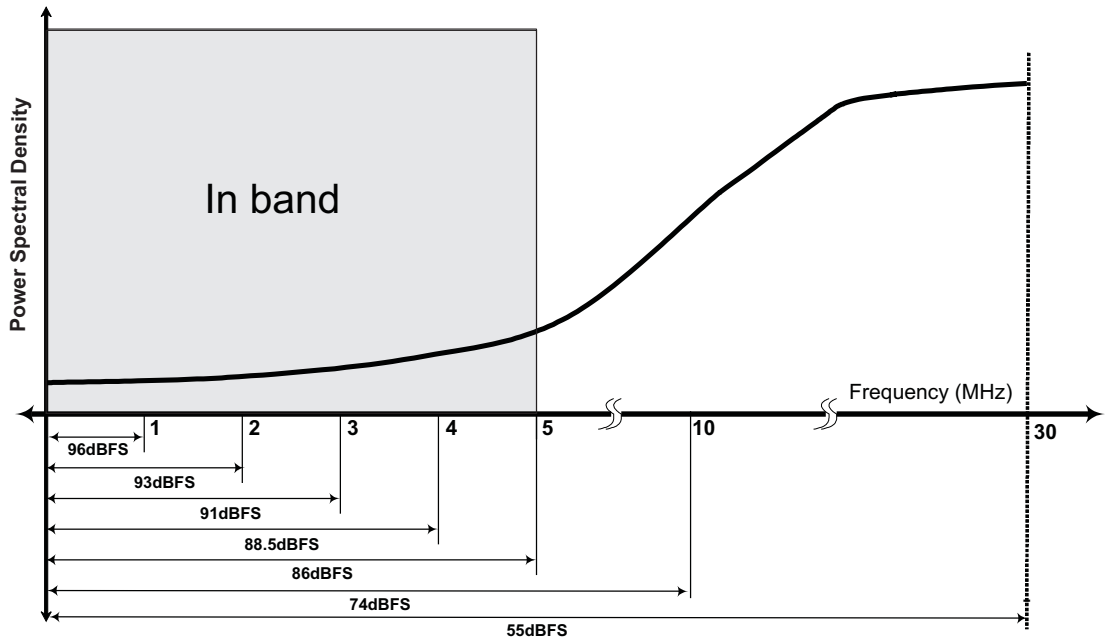


Figure 38. Typical Filter Bypass Mode Noise Spectral Density

By using appropriate filtering the user can achieve a tradeoff between speed and SNR. For ease of use, the ADS1610 provides four filtering modes as explained in the next section. Figure 39 shows a conceptual diagram of the available filtering modes. Custom filtering is achieved by taking the modulator output data and adding a filter externally.

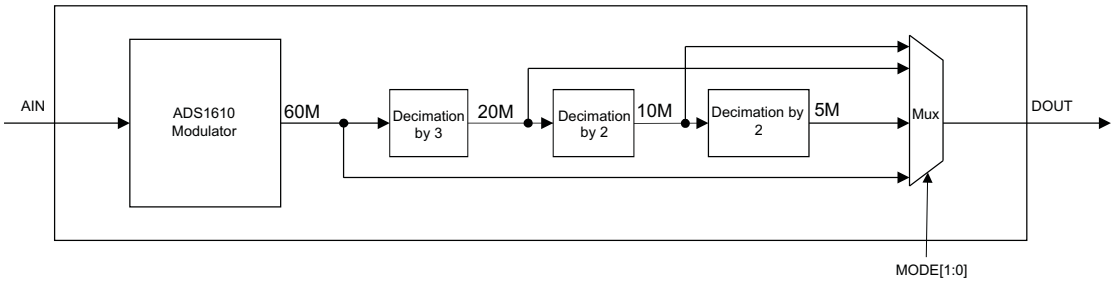


Figure 39. Conceptual Diagram of the ADS1610 Filtering Modes

MODE SELECTION

ADS1610 offers four different modes of operation each with different output data rates. This gives users the flexibility to choose the best output rate for their application. The outputs of all modes are MSB-aligned.

Table 4. Four Modes of Operation(1)

Mode 1	Mode 0	OUTPUT RATE	OSR	SNR (TYP)	BITS	SETTLING TIME (DRDY cycles)
0	0	Default 10MHz mode	6	86dBFS	16	55
0	1	20MHz	3	74dBFS	14	25
1	0	5MHz	12	91dBFS	16	55
1	1	60MHz bypass mode	1	55dBFS	12	NA

(1) There is a pull-down resistor of 170kΩ on both mode pins; however, it is recommended that this pin be reduced to either high or low.

20MHz MODE

In this mode, the oversampling ratio is three. Decreasing the OSR from 6 to 3 doubles the data rate, at the same time the performance is reduced from 16 bits to 14 bits. Note that all 16 bits of DOUT remain active in this mode. For f_{clk} = 60MHz, the data rate is 20MSPS. In addition, the group delay becomes 1 µs or 13 $\overline{DRDY}$ cycles. In this mode the noise increases. Typical SNR performance degrades by 14dB. THD remains approximately the same.

5MHz MODE

In this mode the OSR is 12 for f_{clk} = 60MHz and the data rate in 5MSPS. Typical SNR performance increases by 4dB. THD remains approximately the same.

60MHz MODE

In this mode, decimation filters are bypassed. This data output can be filtered externally by the user. For f_{clk} = 60MHz, the data rate is 60MSPS.

ANALOG POWER DISSIPATION

An external resistor connected between the RBIAS pin and the analog ground sets the analog current level, as shown in Figure 40. The current is inversely proportional to the resistor value. Table 5 shows the recommended values of RBIAS for different CLK frequencies. Notice that the analog current can be reduced when using a slower frequency CLK input because the modulator has more time to settle. Avoid adding any capacitance in parallel to RBIAS, since this will interfere with the internal circuitry used to set the biasing.

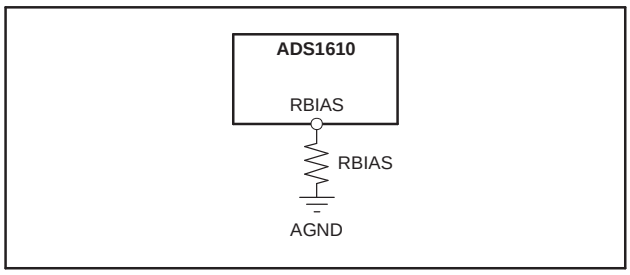


Figure 40. External Resistor Used to Set Analog Power Dissipation

Table 5. Recommended RBIAS Resistor Values for Different CLK Frequencies

f_{CLK}	DATA RATE	RBIAS	TYPICAL POWER DISSIPATION
42MHz	7MHz	45kΩ	550mW
48MHz	8MHz	37kΩ	640mW
54MHz	9MHz	31kΩ	720mW
60MHz	10MHz	19kΩ	960mW

POWER-DOWN ($\overline{PD}$)

When not in use, the ADS1610 can be powered down by taking the $\overline{PD}$ pin low. There is an internal pull-up resistor of 170kΩ on the $\overline{PD}$ pin, but it is recommended that this pin be connected to DVDD if not used. Once the $\overline{PD}$ pin is pulled high, allow at least t_{11} (see Timing Specification Table) $\overline{DRDY}$ cycles for the modulator and the digital filter to settle before retrieving data.

POWER SUPPLIES

Two supplies are used on the ADS1610: analog (AVDD), and digital (DVDD). Each supply (other than DVDD pins 49 and 50) must be suitably bypassed to achieve the best performance. It is recommended that a 1µF and 0.1µF ceramic capacitor be placed as close to each supply pin as possible. Connect each supply-pin bypass capacitor to the associated ground, as shown in Figure 41. Each main supply bus should also be bypassed with a bank of capacitors from 47µF to 0.1µF, as shown in Figure 41.

For optimum performance, insert a 10Ω resistor in series with the AVDD2 supply (pin 58); the modulator clocking circuitry. This resistor decouples switching.

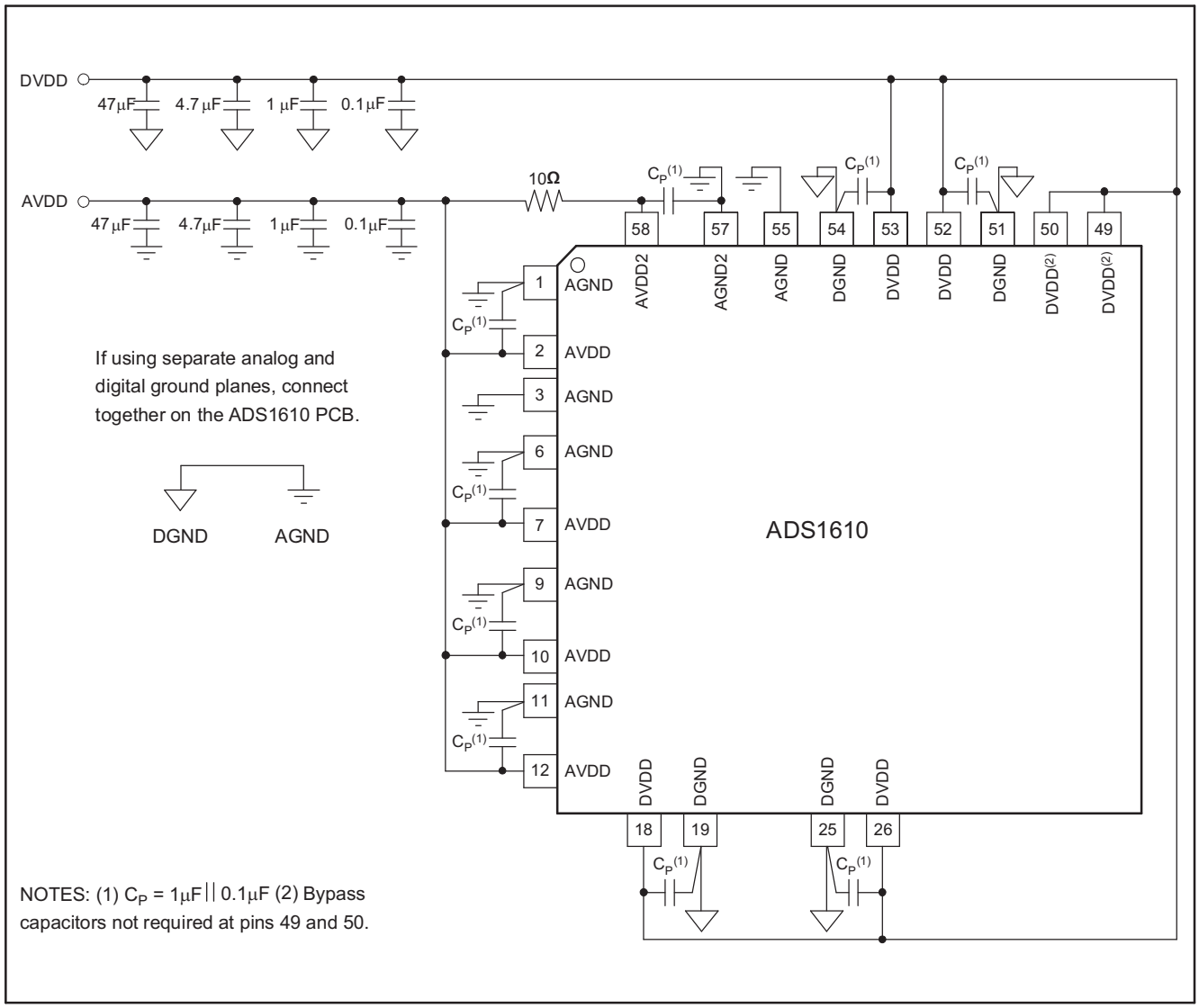


Figure 41. Recommended Power-Supply Bypassing

LAYOUT ISSUES

The ADS1610 is a very high-speed, high-resolution data converter. In order to achieve the maximum performance, careful attention must be given to the printed circuit board (PCB) layout. Use good high-speed techniques for all circuitry. Critical capacitors should be placed close to pins as possible. These include capacitors directly connected to the analog and reference inputs and the power supplies. Make sure to also properly bypass all circuitry driving the inputs and references.

Two approaches can be used for the ground planes: either a single common plane; or two separate planes, one for the analog grounds and one for the digital grounds. When using only one common plane, isolate the flow of current on AGND2 (pin 57) from pin 1; use breaks on the ground plane to accomplish this. AGND2 carries the switching current from the analog clocking for the modulator and can corrupt the quiet analog ground on pin 1. When using two planes, it is recommended that they be tied together right at the PCB. Do not try to connect the ground planes together after running separately through edge connectors or cables as this reduces performance and increases the likelihood of latch-up.

In general, keep the resistances used in the driving circuits for the inputs and reference low to prevent excess thermal noise from degrading overall performance. Avoid having the ADS1610 digital outputs drive heavy loads. Buffers on the outputs are recommended unless the ADS1610 is connected directly to a DSP or controller situated nearby. Additionally, make sure the digital inputs are driven with clean signals as ringing on the inputs can introduce noise.

The ADS1610 uses TI PowerPAD™ technology. The PowerPAD is physically connected to the substrate of the silicon inside the package and must be soldered to the analog ground plane on the PCB using the exposed metal pad underneath the package for proper heat dissipation. See application report SLMA002, located at www.ti.com, for more details on the PowerPAD package.

APPLICATION INFORMATION

INTERFACING THE ADS1610 TO THE TMS320C6000

Figure 42 illustrates how to directly connect the ADS1610 to the TMS320C6000 DSP. The processor controls reading using output $\overline{ARE}$. The ADS1610 is selected using the DSP control output, $\overline{CE2}$. The ADS1610 16-bit data output bus is directly connected to the TMS320C6000 data bus. The data ready output ($\overline{DRDY}$) from the ADS1610 drives interrupt $\overline{EXT\_INT7}$ on the TMS320C6000.

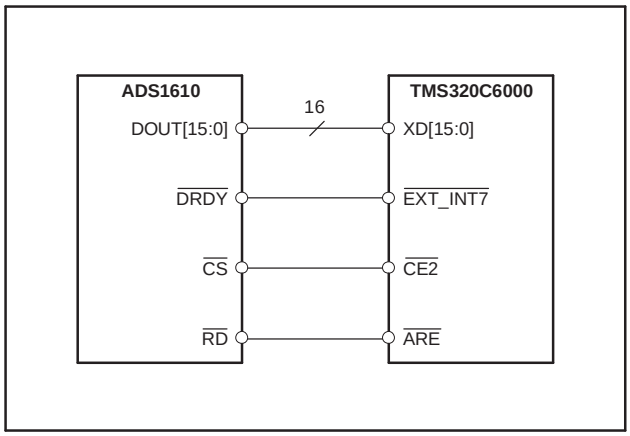


Figure 42. ADS1610 – TMS320C6000 Interface Connection

INTERFACING THE ADS1610 TO THE TMS320C5400

Figure 43 illustrates how to connect the ADS1610 to the TMS320C5400 DSP. The processor controls the reading using the outputs R/$\overline{W}$ and $\overline{IS}$. The I/O space-select signal ($\overline{IS}$) is optional and is used to prevent the ADS1610 $\overline{RD}$ input from being strobed when the DSP is accessing other external memory spaces (address or data). This can help reduce the possibility of digital noise coupling into the ADS1610. When not using this signal, replace NAND gate U1 with an inverter between R/$\overline{W}$ and $\overline{RD}$. Two signals, $\overline{IOSTRB}$ and A15, combine using NAND gate U2 to select the ADS1610. If there are no additional devices connected to the TMS320C5400 I/O space, U2 can be eliminated. Simply connect $\overline{IOSTRB}$ directly to $\overline{CS}$. The ADS1610 16-bit data output bus is directly connected to the TMS320C5400 data bus. The data ready output ($\overline{DRDY}$) from the ADS1610 drives interrupt $\overline{INT3}$ on the TMS320C5400.

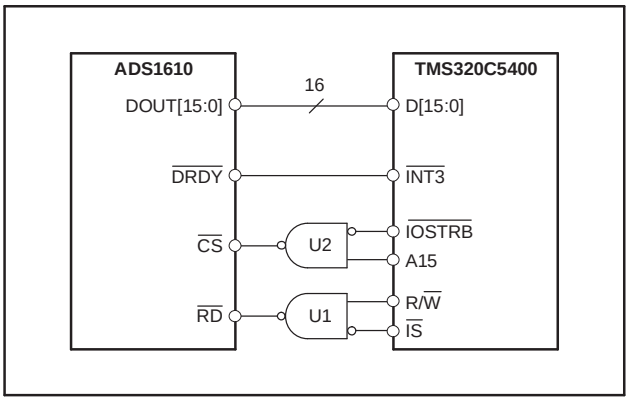


Figure 43. ADS1610 – TMS320C5400 Interface Connection

Code Composer Studio, available from TI, provides support for interfacing TI DSPs through a collection of data converter plug-ins. Check the TI website, located at www.ti.com/sc/dcplug-in, for the latest information on ADS1610 support.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1610IPAPR	NRND	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS1610I	
ADS1610IPAPT	NRND	HTQFP	PAP	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS1610I	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

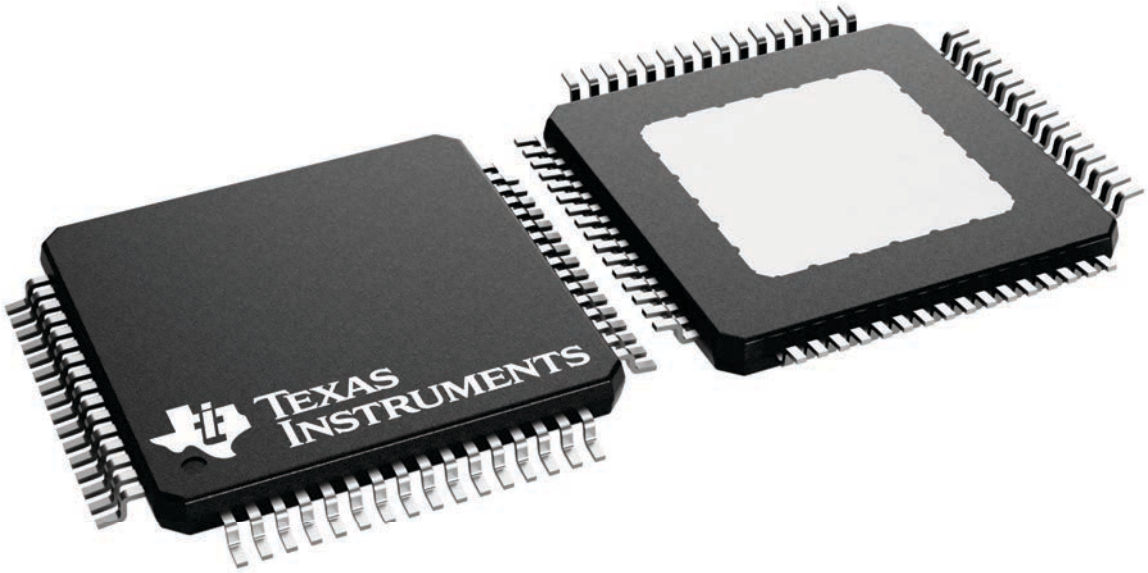
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



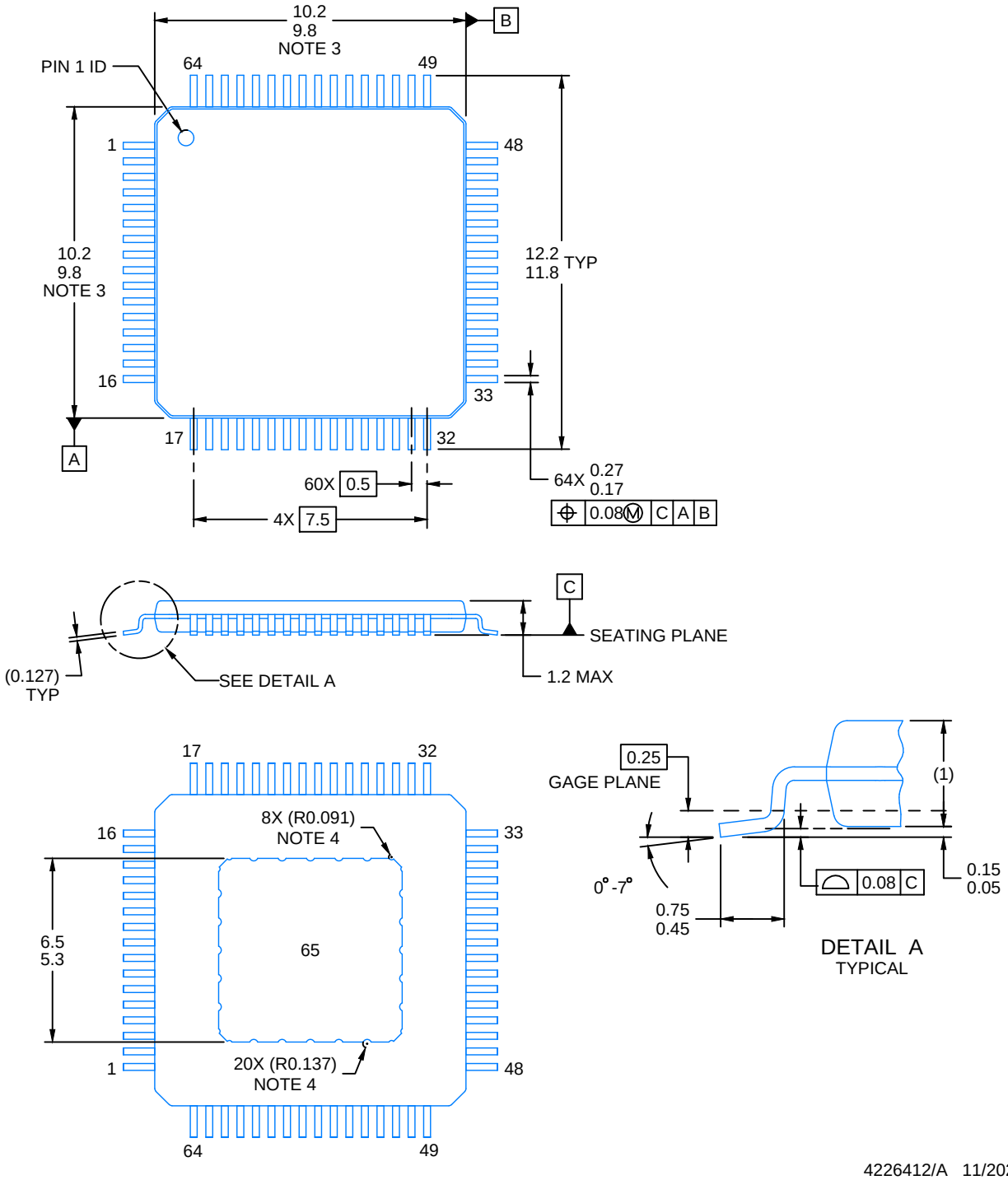
4226442/A

PACKAGE OUTLINE

PAP0064F

PowerPAD™ TQFP - 1.2 mm max height

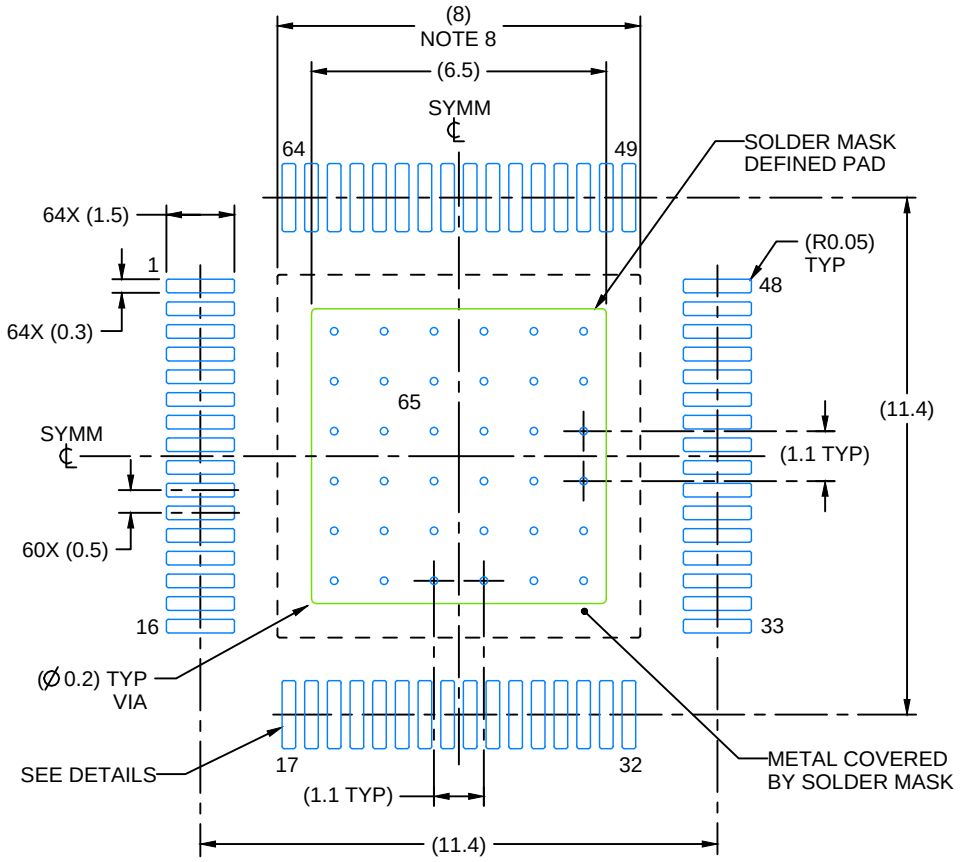
PLASTIC QUAD FLATPACK



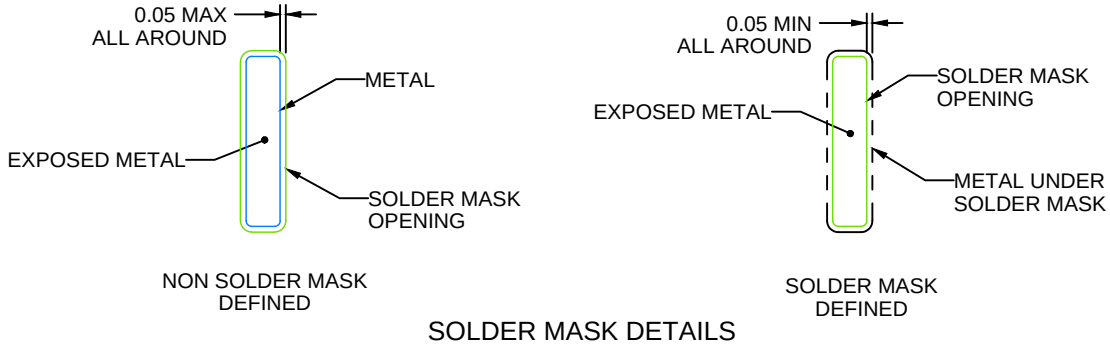
NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



NON SOLDER MASK
DEFINED

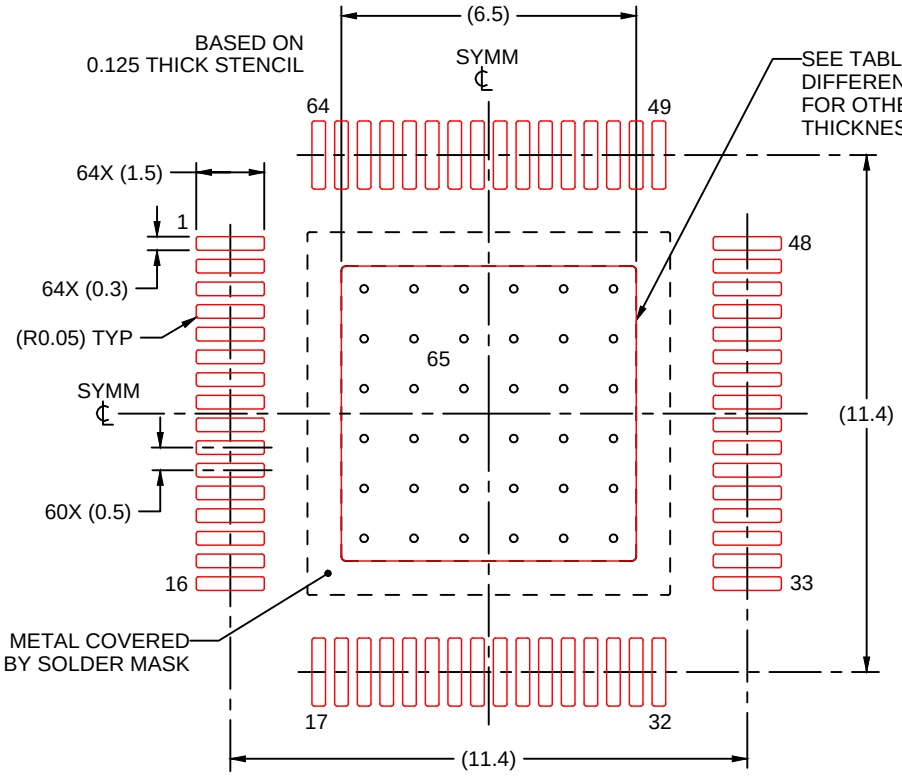
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4226412/A 11/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	7.27 X 7.27
0.125	6.5 X 6.5 (SHOWN)
0.15	5.93 X 5.93
0.175	5.49 X 5.49

4226412/A 11/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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