Jacinto7 EVM Infotainment Expansion

This document describes the hardware architecture of the Jacinto7 EVM – Infotainment Expansion (INFO) Boards. INFO is one of the expansion boards that will be interfaced with the Jacinto7 common processor board.

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Trademarks

1 Introduction

The Jacinto7 EVMs are development and evaluation systems that enable developers to write software and develop hardware around the Jacinto7 family of processors. The main elements of the system are available on the base board(s) of the EVM. This gives developers the basic resources needed for most general-purpose type projects that encompass the Jacinto7 processor.

The Jacinto7 EVM is comprised of two boards:

- Jacinto7 System on Module (SOM) – which includes Jacinto7 processor, its power solution, and non-volatile memory.
- Jacinto7 Common Processor Board (CPB) – which includes wide variety of memories, peripherals, and debug tools supporting by the Jacinto7 processor.

Beyond the basic resources provided, additional functionality can be added via expansion cards.

1.1 Key Features

Below are the key features of infotainment expansion board:

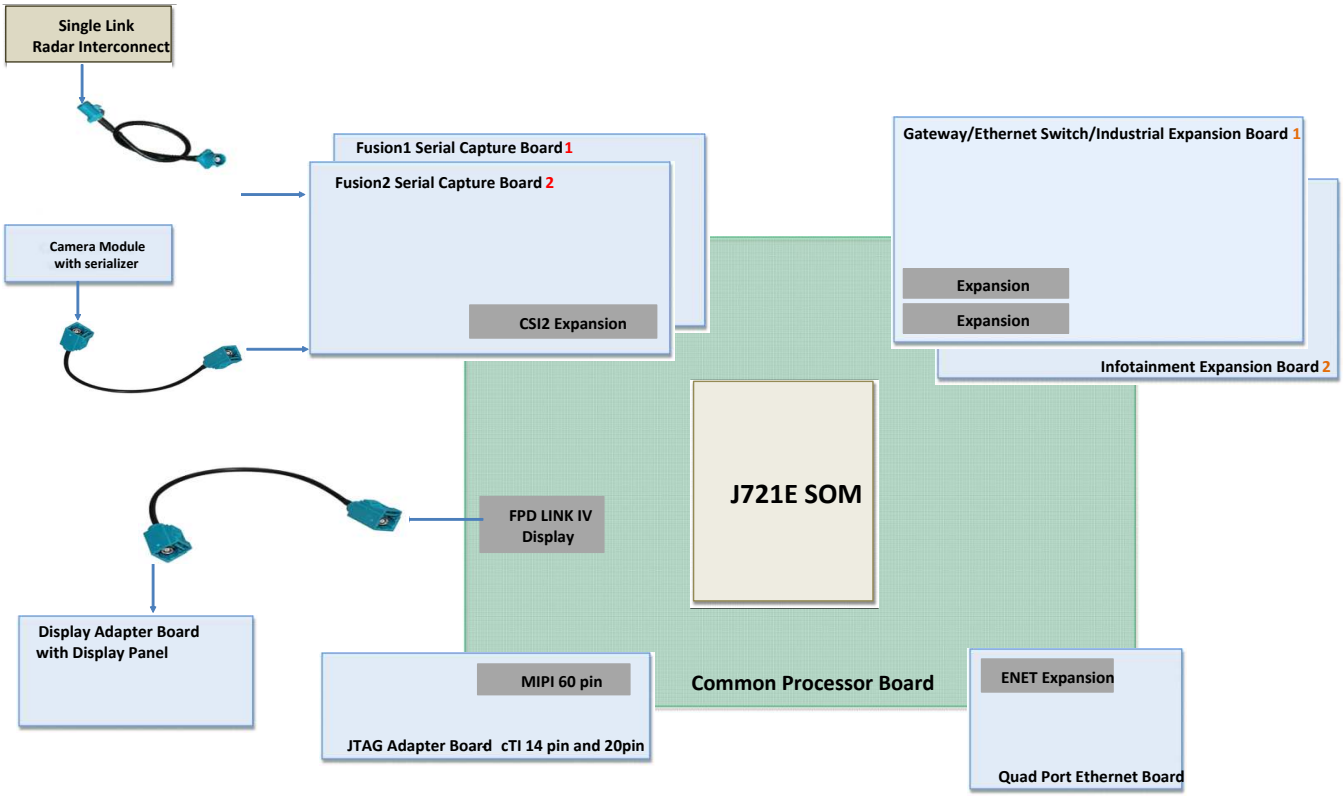
- Audio interfaces:
  - Two Audio codecs each with three Stereo Inputs and four Stereo Outputs
  - Audio input over FPD Link III
  - Digital Audio Interface Transmit
  - Digital Audio Interface Receiver
- Video interfaces:
  - HDMI/FPD LINK III Display out
  - LI/OV Camera input
- JAMR3 interface
- Board ID EEPROM

2 Infotainment Expansion Board Overview

Jacinto7 EVM can support different types of expansion boards, one of which is Infotainment. Not all the expansion boards may not be available on all Jacinto7 EVMs.

To determine version of the Jacinto7 EVM supports the Infotainment expansion board, see Appendix A.

Figure 1 shows the overall architecture of Jacinto7 EVM.



(1) Only one board can be connected to Expansion connector at a time.

(2) Only one board can be connected to CSI2 Expansion connector at a time.

Figure 1. System Architecture Interface

2.1 Infotainment Expansion Board Identification

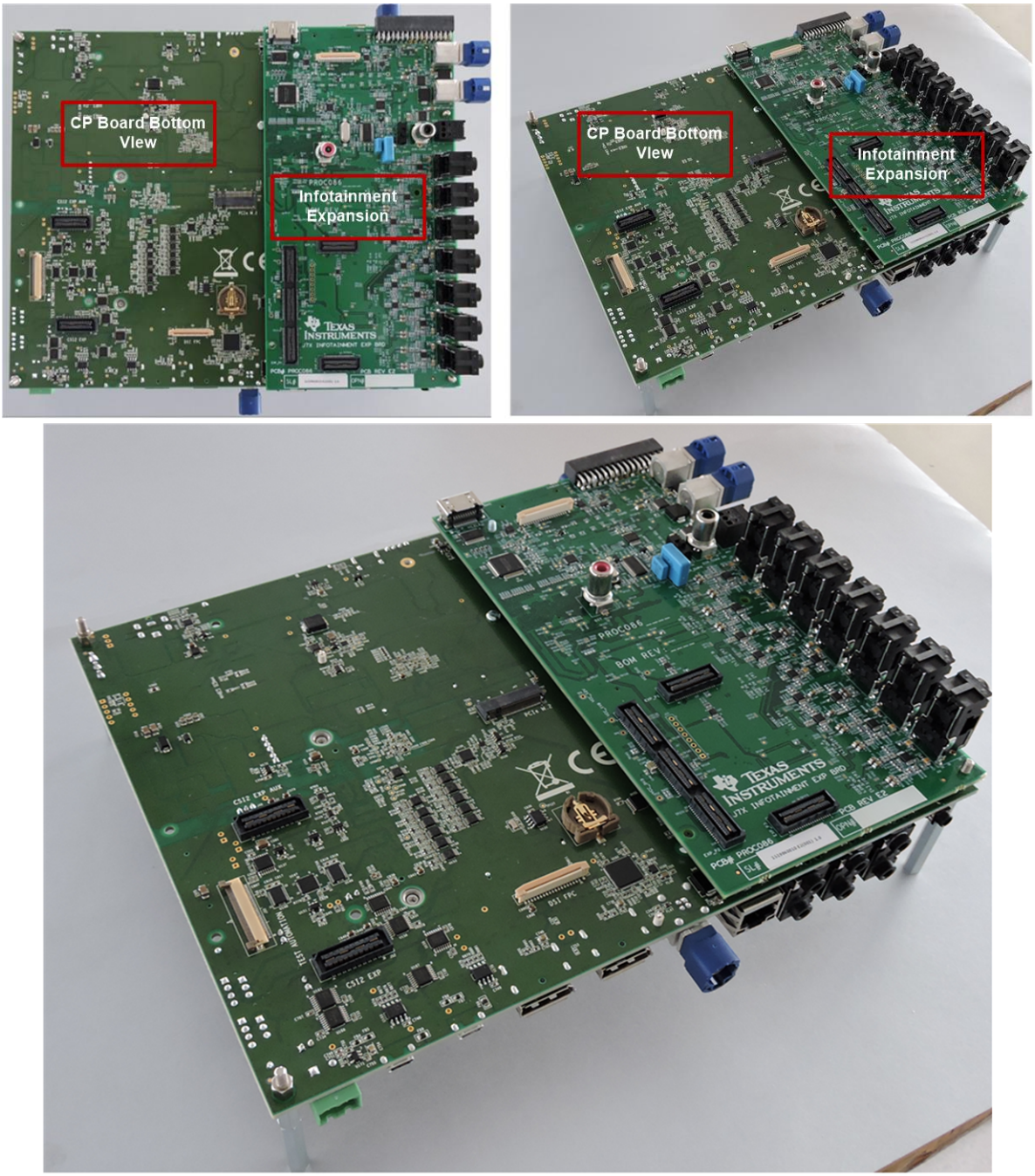


Figure 2. System Assembly Image

2.2 Infotainment Expansion Board Component Identification

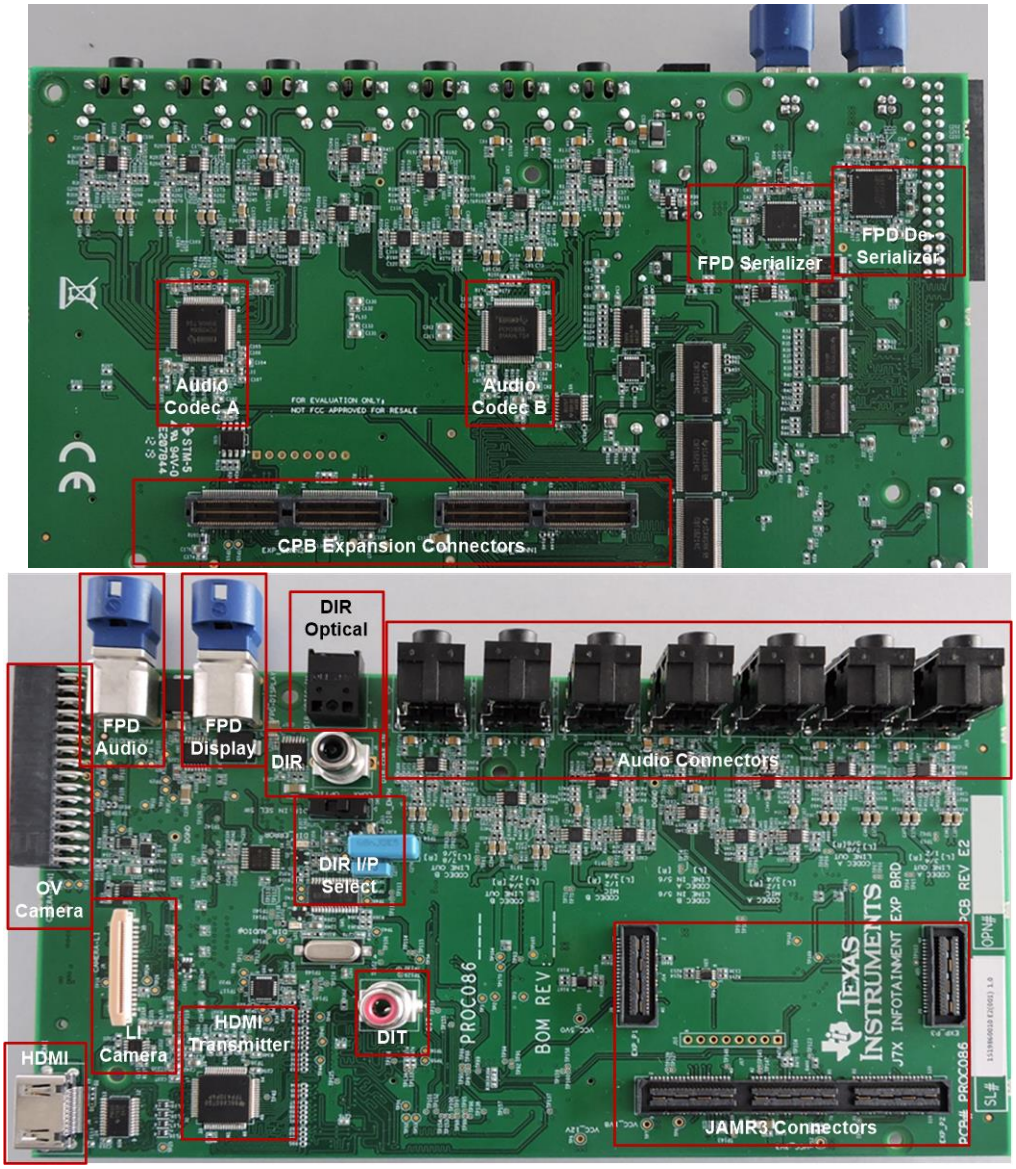


Figure 3. Infotainment Expansion Board Component Identification

3 Infotainment Expansion Board - User Setup/Configuration

3.1 Interfacing Infotainment Expansion Board With CP Board

Infotainment expansion boards interface with Jacinto7 EVM Common Processor Board (CPB). Expansion connectors J1 and J2 on the Infotainment will be mated to the EVM CPB Expansion connectors J46 and J51.

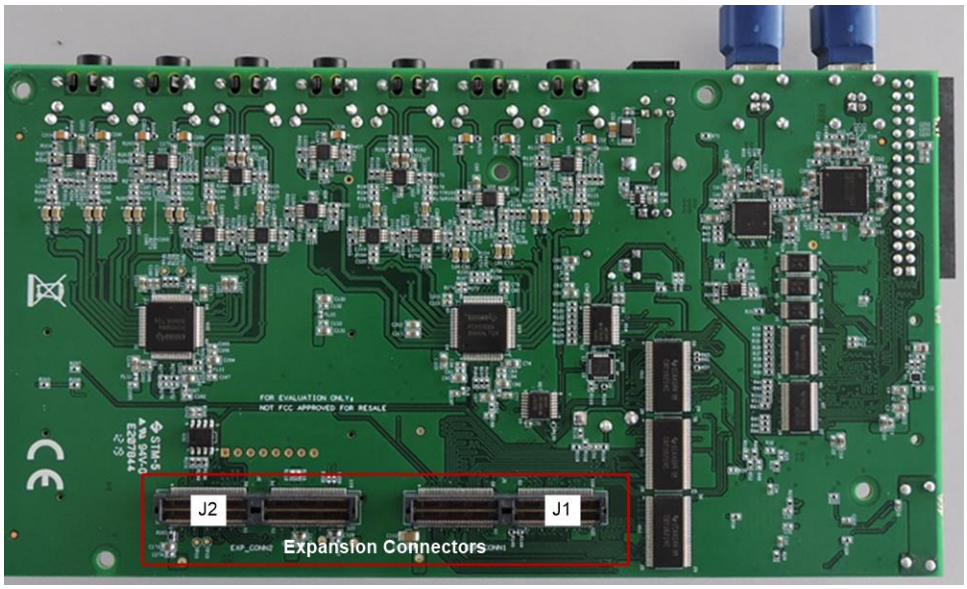


Figure 4. Expansion Connectors on INFO Exp Board Top Side

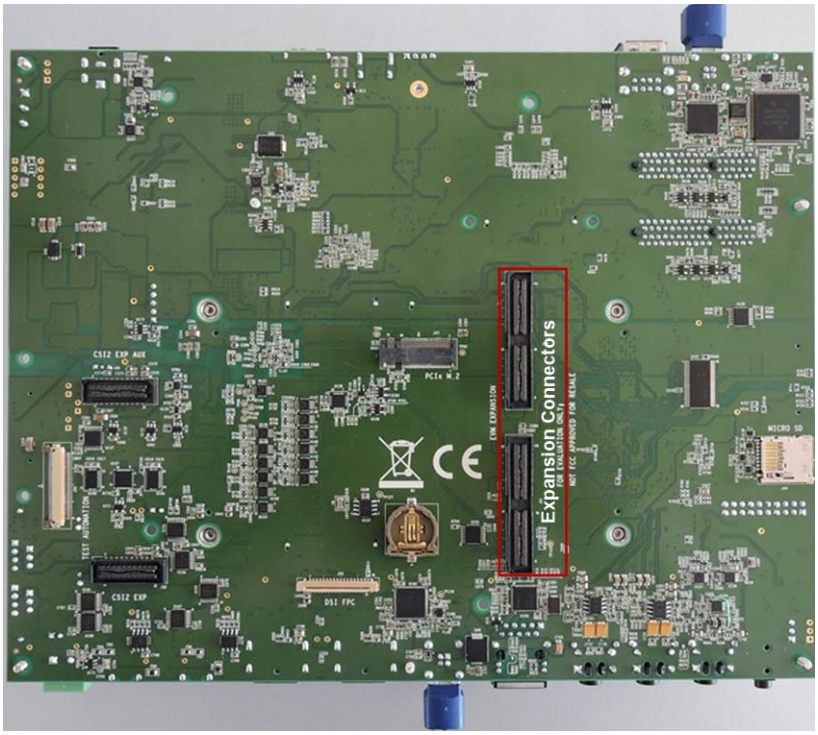


Figure 5. Expansion Connectors on Jacinto7 CP Board Bottom Side

3.1.1 Board Assembly Procedures

1. Take the Assembled CP board Kit
2. Remove the spacers from CP board and mate the infotainment board on CP board left side B-B connectors.
3. Add 2 mm thick washer (PART NUMBER : RWM100A) on the four stand offs in case no CSI Expansion Board connected.
4. Fix all the eight stand offs.

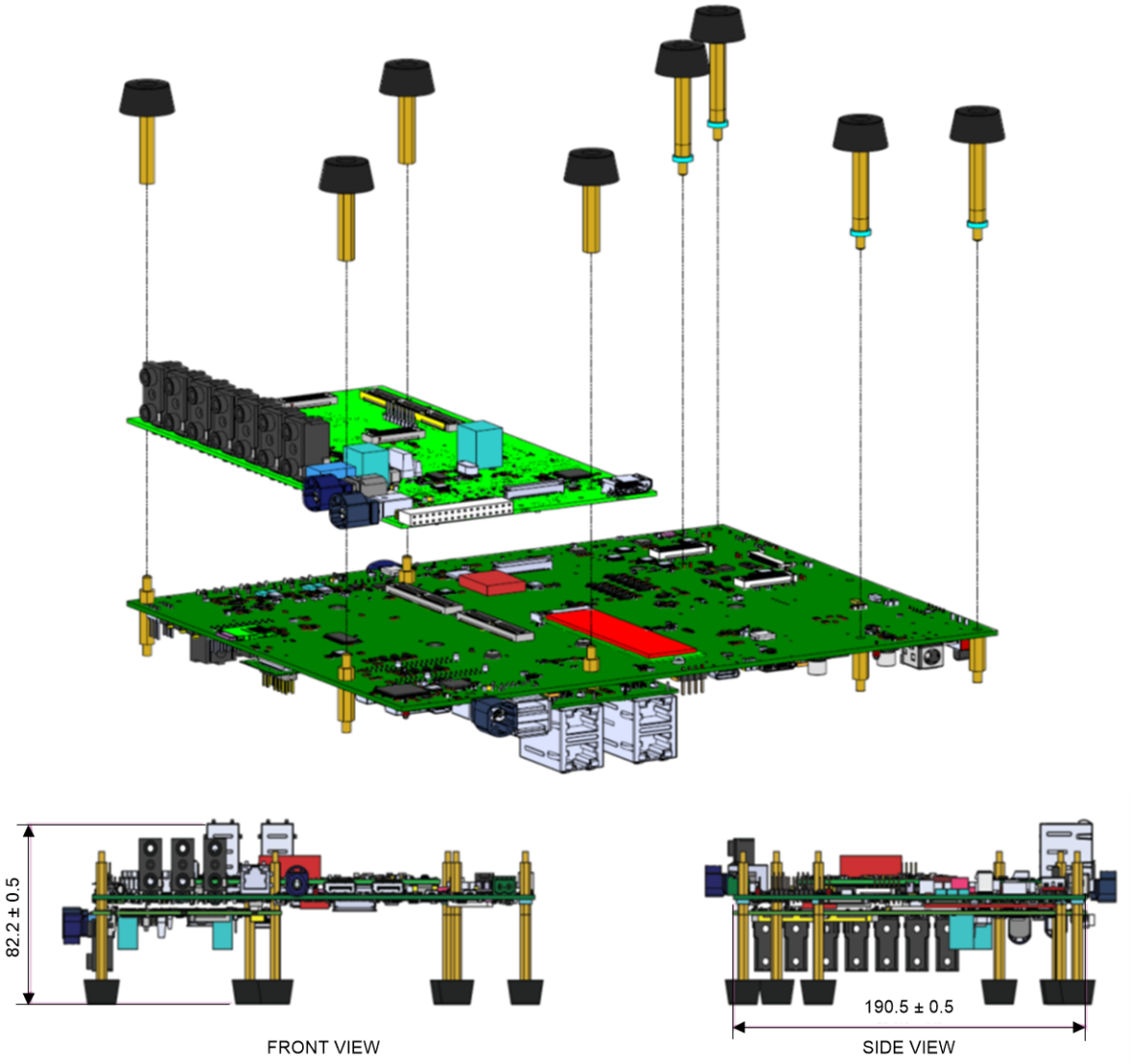


Figure 6. Board Assembly Procedure

3.2 Power Requirements

External power supply is not required since Infotainment board takes power from Jacinto7 EVM Common Processor Board. 12 V, 5 V, 3.3 V and 3.3 V_IO are tapped from CPB.

Power to the Camera Connectors (3.3 V/1.8 V) are generated locally on Infotainment Expansion board using LDO and the enable of LDO is controlled by a Switch from CPB.

No Power ON indication LEDs are provided in the Infotainment expansion board.

3.3 EVM Reset/Interrupt Push Buttons

Jacinto7 EVM supports multiple User Push buttons for providing Reset inputs and User Interrupts to the processor. For their location and function, see the device-specific user's manual.

There are no Specific Reset/Interrupt Push Buttons available on the infotainment expansion board.

3.4 EVM Configuration DIP Switch

Common processor board has dedicated EVM configuration switch (SW3) shown in Figure 7 to set the various functions of EVM peripherals. The Configuration DIP Switch (SW3) is placed on Top side of CPB right below the USB Type C port.

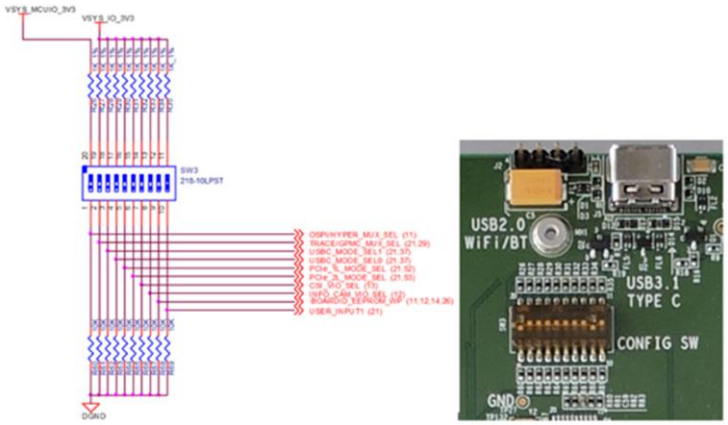


Figure 7. EVM Configuration DIP Switch

Table 1. Jacinto7 EVM Common Processor DIP Switches Used for Expansion Boards

Switch Name	Default Condition	Signal	Operation
SW3.8	ON	INFO_CAM_VIO_SEL	'1' (ON) =3.3V will be selected from LDO for camera IO voltage '0' (OFF) =1.8V will be selected from LDO for Camera IO Voltage
SW3.9	ON	BOARDID_EEPROM_WP	Sets EVM's configuration EEPROM Write Protection '0' (OFF) = Configuration EEPROM can be updated '1' (ON) = Configuration EEPROM cannot be updated/protected

4 Infotainment Expansion Board Hardware Architecture

This section explains the hardware architecture of infotainment expansion board in detail.

4.1 Infotainment Expansion Board Hardware Top Level Diagram

Figure 8 shows the functional block diagram of the infotainment expansion board

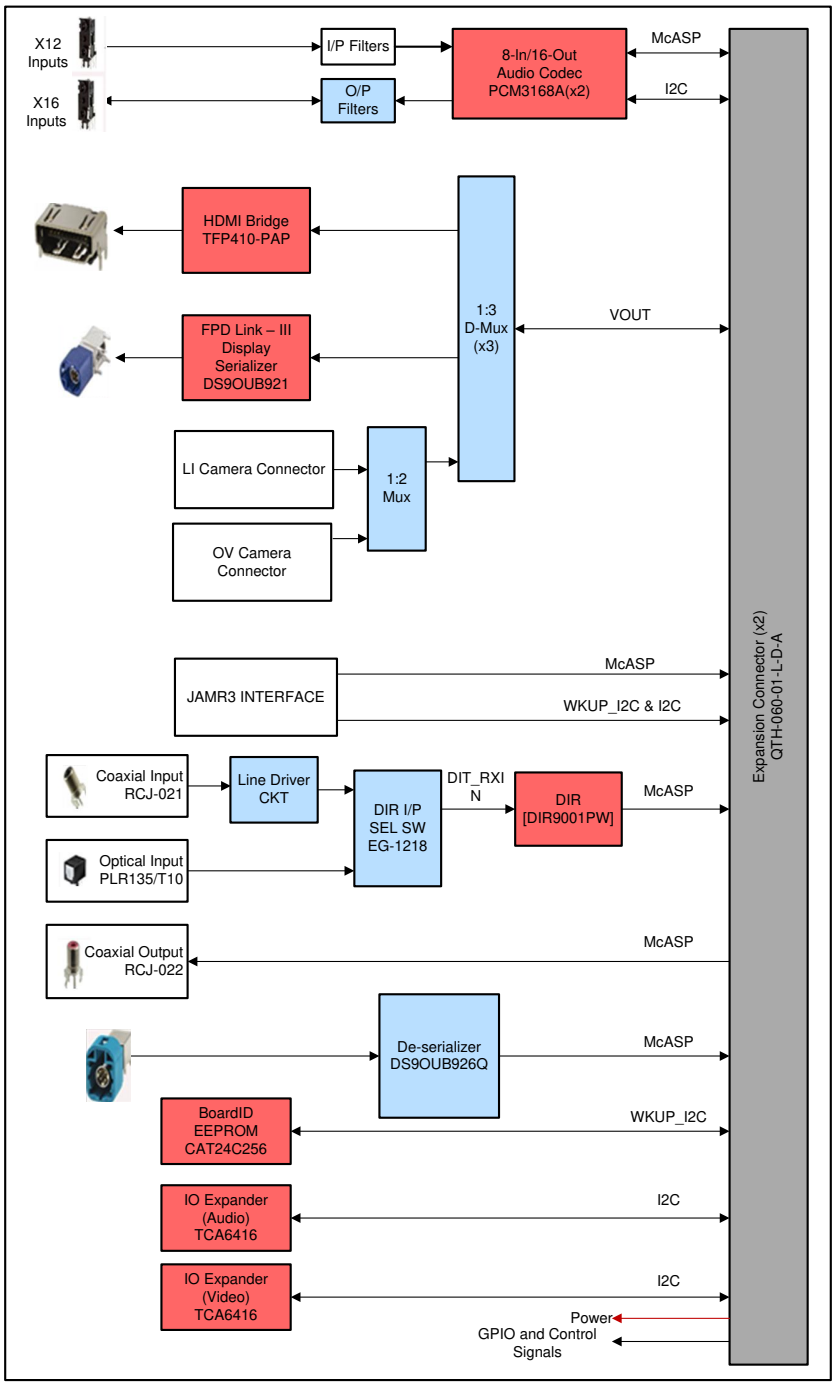


Figure 8. Functional Block Diagram of Infotainment Expansion Board

Few of the interfaces shown in the above diagram are specific EVM dependency. All may not be supported in all the Jacinto7 EVM.

For supported interfaces on the specific EVM platform, see Section A.1.

4.2 Expansion Connectors

There are two expansion connectors J1 and J2 (120 pin Samtec connector) on the Infotainment board for connecting it to Jacinto7 EVM Common processor board. All Infotainment Interfaces, power and control signals are provided with these connectors.

Table 2 and Table 3 contain the pin out/signal mapping INFO expansion connectors. The tables show only the primary function/net name.

Table 2. Pinouts of J1 Expansion Connector

Pin	Net Name	Pin	Net Name	Pin	Net Name	Pin	Net Name
1	DGND	31	VOUT0_DATA10	61	McASP0_AXR3	91	CAM_SEL_OV#
2	VCC_12V0	32	VOUT0_DATA23	62	NC	92	McASP6_ACLKR
3	DGND	33	VOUT0_VSYNC	63	WKUP_I2C0_SDA	93	McASP2_AXR0
4	VCC_12V0	34	VOUT0_DE	64	SOC_PORZ_OUT	94	MUX_McASP6_AXR0
5	DGND	35	NC	65	WKUP_I2C0_SCL	95	DGND
6	VCC_12V0	36	VOUT0_PCLK	66	NC	96	DGND
7	McASP1_AXR3	37	DGND	67	DGND	97	NC
8	VOUT0_DATA15	38	DGND	68	DGND	98	NC
9	JAMR3_GPIO1	39	VOUT0_DATA0	69	McASP0_AXR0	99	NC
10	VOUT0_DATA14	40	VOUT0_DATA19	70	McASP0_AXR8	100	JAMR3_I2S_DB
11	McASP1_AXR2	41	VOUT0_DATA2	71	McASP0_AXR2	101	SPI3_D0
12	VOUT0_HSYNC	42	VOUT0_DATA16	72	McASP0_AXR7	102	McASP0_AXR13
13	McASP1_AXR0	43	VOUT0_DATA1	73	McASP0_AXR4	103	SPI3_D1
14	VOUT0_DATA11	44	VOUT0_DATA20	74	McASP0_AXR11	104	NC
15	McASP1_AXR1	45	VOUT0_DATA3	75	UB926_GPIO2	105	SPI3_CLK
16	VOUT0_DATA13	46	VOUT0_DATA18	76	McASP0_AXR10	106	NC
17	JAMR3_GPIO0	47	VOUT0_DATA4	77	McASP0_AXR1	107	DGND
18	VOUT0_DATA12	48	VOUT0_DATA21	78	McASP0_AXR9	108	DGND
19	DGND	49	VOUT0_DATA6	79	UB926_GPIO3	109	I2C0_SCL
20	DGND	50	VOUT0_DATA17	80	McASP0_AXR12	110	McASP1_ACLKX
21	VOUT0_EXTPCLKIN	51	DGND	81	DGND	111	I2C0_SDA
22	CON_VPFE0_DATA6	52	DGND	82	DGND	112	SOC_I2C2_SCL
23	VOUT0_DATA5	53	McASP0_AXR5	83	McASP1_AXR8	113	I2C1_SCL
24	CON_VPFE0_DATA7	54	CON_VPFE0_DATA12	84	MUX_McASP6_ACLKX	114	SOC_I2C2_SDA
25	VOUT0_DATA7	55	McASP0_AXR6	85	McASP1_AXR7	115	I2C1_SDA
26	AUDIO_EXT_REFCLK1	56	CON_VPFE0_DATA11	86	McASP6_AFSR	116	NC
27	VOUT0_DATA8	57	McASP0_ACLKX	87	CON_UB921_INTB	117	NC
28	VOUT0_DATA22	58	SPI3_CS0	88	MUX_McASP6_AFSX	118	EXP_RSTz
29	VOUT0_DATA9	59	McASP0_AFSX	89	JAMR3_GPIO2	119	DGND
30	UB926_GPIO1	60	McASP1_AFSX	90	MUX_McASP6_AXR1	120	DGND

Table 3. Pinouts of J2 Expansion Connector

Pin	Net Name	Pin	Net Name	Pin	Net Name	Pin	Net Name
1	DGND	31	VOUT0_DATA10	61	McASP0_AXR3	91	CAM_SEL_OV#
2	VCC_12V0	32	VOUT0_DATA23	62	NC	92	McASP6_ACLKR
3	DGND	33	VOUT0_VSYNC	63	WKUP_I2C0_SDA	93	McASP2_AXR0
4	VCC_12V0	34	VOUT0_DE	64	SOC_PORZ_OUT	94	MUX_McASP6_AXR0
5	DGND	35	NC	65	WKUP_I2C0_SCL	95	DGND
6	VCC_12V0	36	VOUT0_PCLK	66	NC	96	DGND
7	McASP1_AXR3	37	DGND	67	DGND	97	NC
8	VOUT0_DATA15	38	DGND	68	DGND	98	NC
9	JAMR3_GPIO1	39	VOUT0_DATA0	69	McASP0_AXR0	99	NC
10	VOUT0_DATA14	40	VOUT0_DATA19	70	McASP0_AXR8	100	JAMR3_I2S_DB
11	McASP1_AXR2	41	VOUT0_DATA2	71	McASP0_AXR2	101	SPI3_D0
12	VOUT0_HSYNC	42	VOUT0_DATA16	72	McASP0_AXR7	102	McASP0_AXR13
13	McASP1_AXR0	43	VOUT0_DATA1	73	McASP0_AXR4	103	SPI3_D1
14	VOUT0_DATA11	44	VOUT0_DATA20	74	McASP0_AXR11	104	NC
15	McASP1_AXR1	45	VOUT0_DATA3	75	UB926_GPIO2	105	SPI3_CLK
16	VOUT0_DATA13	46	VOUT0_DATA18	76	McASP0_AXR10	106	NC
17	JAMR3_GPIO0	47	VOUT0_DATA4	77	McASP0_AXR1	107	DGND
18	VOUT0_DATA12	48	VOUT0_DATA21	78	McASP0_AXR9	108	DGND
19	DGND	49	VOUT0_DATA6	79	UB926_GPIO3	109	I2C0_SCL
20	DGND	50	VOUT0_DATA17	80	McASP0_AXR12	110	McASP1_ACLKX
21	VOUT0_EXTPCLKIN	51	DGND	81	DGND	111	I2C0_SDA
22	CON_VPFE0_DATA6	52	DGND	82	DGND	112	SOC_I2C2_SCL
23	VOUT0_DATA5	53	McASP0_AXR5	83	McASP1_AXR8	113	I2C1_SCL
24	CON_VPFE0_DATA7	54	CON_VPFE0_DATA12	84	MUX_McASP6_ACLKX	114	SOC_I2C2_SDA
25	VOUT0_DATA7	55	McASP0_AXR6	85	McASP1_AXR7	115	I2C1_SDA
26	AUDIO_EXT_REFCLK1	56	CON_VPFE0_DATA11	86	McASP6_AFSR	116	NC
27	VOUT0_DATA8	57	McASP0_ACLKX	87	CON_UB921_INTB	117	NC
28	VOUT0_DATA22	58	SPI3_CS0	88	MUX_McASP6_AFSX	118	EXP_RSTz
29	VOUT0_DATA9	59	McASP0_AFSX	89	JAMR3_GPIO2	119	DGND
30	UB926_GPIO1	60	McASP1_AFSX	90	MUX_McASP6_AXR1	120	DGND

4.3 Board ID EEPROM

The Infotainment Expansion board is identified by its version and serial number, which are stored in onboard EEPROM. The EEPROM CAT24C256WI-GT3 is accessible on the address 0x52 WKUP_I2C0 I2C BUS.

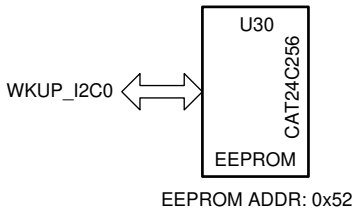


Figure 9. Board ID EEPROM

Table 4. Board ID Memory Header Information

Header	Field Name	Size (bytes)	Description	Value Written to EEPROM
	MAGIC	4	Magic Number	0xEE3355AA
	TYPE	1	Fixed length and variable position board ID header	0x1
		2	Size of payload	0xF7
BRD_ INFO	TYPE	1	payload type	0x10
	Length	2	offset to next header	0x002E
	Board_Name	16	Name of the board	“J7X-INFO-EXP”
	Design_Rev	2	Revision number of the design	Variable
	PROC_Nbr	4	PROC number	“0086”
	Variant	2	Design variant number	Variable
	PCB_Rev	2	Revision number of the PCB	Variable
	SCHBOM_Rev	2	Revision number of the schematic	Variable
	SWR_Rev	2	first software release number	Variable
	VendorID	2	Vendor ID	Variable
	Build_Week	2	week of the year of production	Variable
	Build_Year	2	year of production	Variable
	BoardID	6	Reserved. Not populated with any value	NA
	Serial_Nbr	4	incrementing board number	Variable

Above board ID details will be programmed on the EEPROM from the address 0x0h.

4.4 Audio Codec Interface

The infotainment expansion board has two TI ‘s Automotive Audio Codec IC Mfr. Part# PCM3168A-Q1, each supports three stereo Inputs and four stereo outputs. External Audio input and output signals are terminated to 3.5 mm stacked audio jack (stereo mode) Mfr. Part# STX-4235-3/3-N with appropriate filters circuitry.

TI’s Audio OPAMP Mfr. Part# OPA2322AI used to convert the single ended to differential as well as to convert the differential to single ended signals. The MODE pin is held LOW to select I2C as control interface and Codec is configured over I2C interface. Default I2C address is set to 0x46 &0x47 for Codec –B and Codec-A, respectively. The device reset is controlled by the I2C GPIO expander.

Microphone Input ports can be configured for active and passive microphones and also can be configured for Line Input. This Input port configuration can be set by the resistor option as shown in Table 5.

Table 5. MIC I/P Port Config for CODEC-A & CODEC-B

		Install	Remove
PASSIVE-MIC (default)	BIAS + PREAMP	R2, R3, R5, R6	R1, R4
ACTIVE-MIC	BIAS ONLY	R1, R2, R4, R5	R3, R6
LINE-INPUT	NO BIAS/PREAMP	R1, R4	R2, R3, R5, R6

4.4.1 Port Mapping

7x Standard 3.5 mm stacked 2by1 Stereo Audio Jack Mfr. Part# STX-4235-3/3-N is provided for:

- 4x – MIC IN
- 2x – Line IN
- 8x – Line OUT

The infotainment expansion board audio ports are mapped to audio codec as shown in Figure 10.

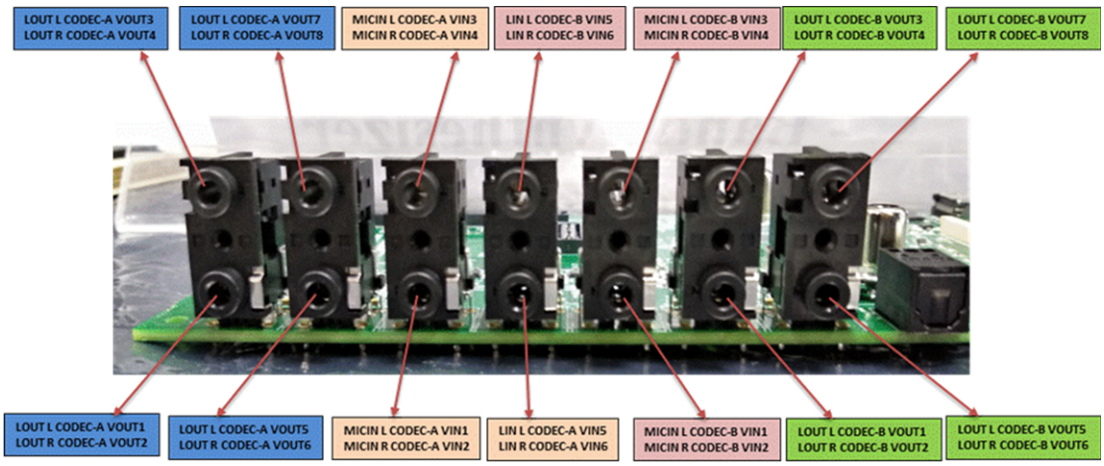


Figure 10. Audio Input and Outputs

4.5 FPD link De-Serializer Interface (Audio)

Infotainment expansion board uses FPD link III De-serializer IC Mfr. Part# DS90UB926QSQE for recover the audio signals from the FPD-Link interface. The de-serializer recovers up to eight digital audio channels, frame sync plus I2S channel across digital link. HSD connector Mfr. Part# D4S20G-400A5-C is used to receive the input signal.

The recovered eight audio data signal and AFSX connected directly to McASP port of J7 SoC through CP board B-B connector. And I2S signals from de-serializer are connected to McASP port of J7 SoC through DIR/FPDLink MUX selection IC(U17) on Infotainment board. For MUX channel selection through GPIO Expander, see Section A.2.

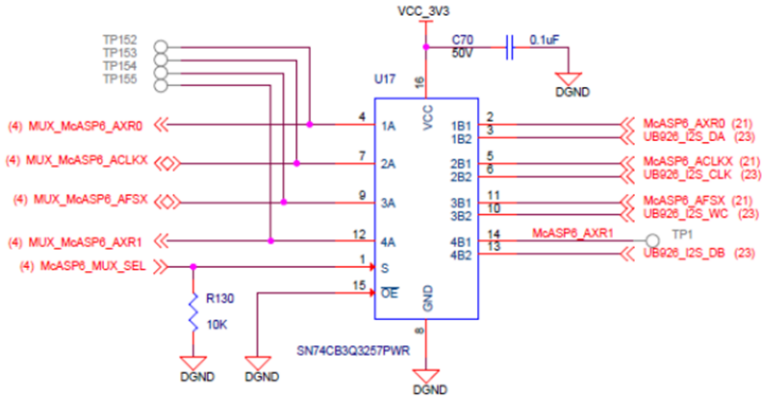


Figure 11. DIR/FPDLink Mux Selection

The I2C signals from SOC being used for controlling/configuring of the de-serializer and remote device. A 57.6KΩ Pull up and 121K Ω pull down is provided on ID[X] pin to set the 7'b I2C address to 0x3B.

The default mode set for the de-serializer is mode0. For the resistor population option to set different modes, see Figure 12.

Power +12 V is provided to the HSD connector using a power switch TPS1H100AQPWPRQ1 to power an external board. By default, power switch is OFF and it can be enabled by a GPIO expander signal (PWR_SW_UB926).

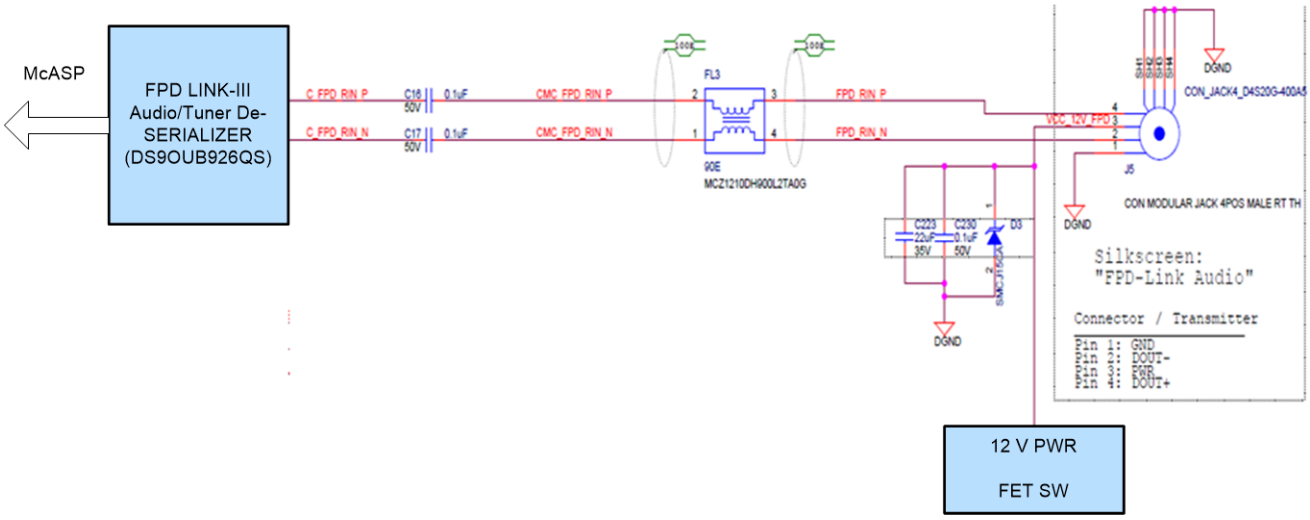


Figure 12. FPD Link De-Serializer Interface

4.6 DIR Interface

Infotainment expansion board is having a TI's Digital Audio Interface Receiver (DIR) IC Mfr. Part# DIR9001-Q1 to process the external digital audio input signal. The DOUT, SCKO, BCKO & LRCKO Outputs of DIR IC is connected to CP Board McASP signals Using a MUX/DMUX IC U14 Mfr. Part# SN74AVC8T245PWR and U17 IC Mfr. Part# SN74CB3Q3257PWR on INFO Board.

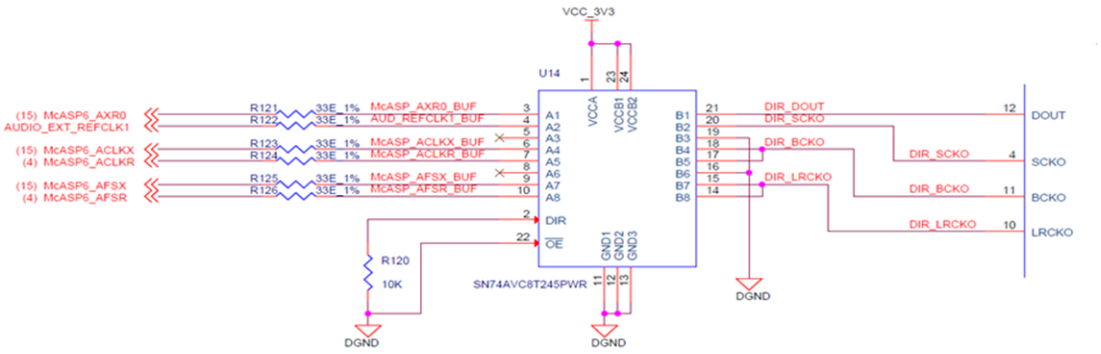


Figure 13. DIR 1:2 DeMux

RCA Jack Mfr. Part# RCJ-041 (Black) used to receive the external audio with buffer/filter circuitry. The input can be selected between DIR coaxial cable and a SPDIF optical input by using a switch (SW1).

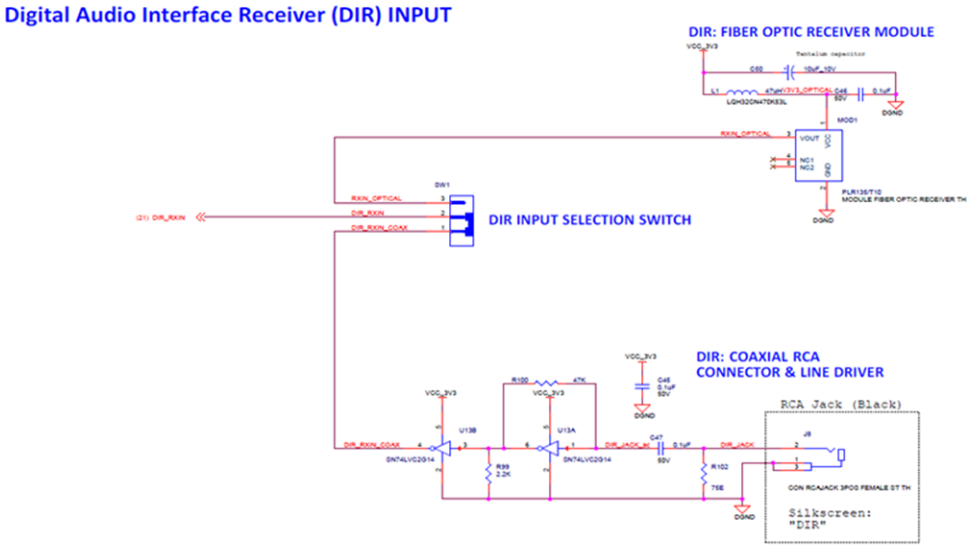


Figure 14. DIR Interface Selection Switch

Table 6. DIR Interface Selection Switch

SW1	Input Type
1-2	Co-Axial RCA
2-3	Fiber Optic Receiver

4.7 DIT Interface

Infotainment Expansion board includes an RCA Jack Mfr. Part# RCJ-042 (Red) to transmit the Digital Audio signal, one McASP Port data signal from SoC connected to RCA jack as shown in Figure 15.

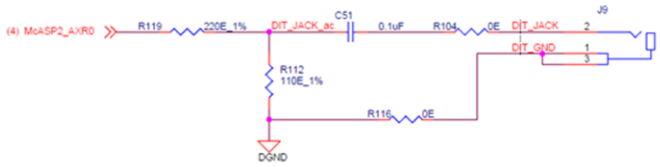


Figure 15. DIT Interface

4.8 Legacy Audio/JAMR3 Connectors

There are 3 B-B expansion connectors available on infotainment board to interface legacy audio/JAMR3 expansion board.

8 McASP data signals, frame sync and clock signals from the connector is directly connected to INFO-CP B-B expansion connector. WKUP_I2C0 & I2C3 signals from Infotainment board connected to the connector for accessing the board ID information and configuration. The device reset is controlled by the I2C GPIO expander on Infotainment Board.

The 12 V power supply is available from infotainment board for powering the expansion board. VCC_3V3 Supply is connected to the expansion connector to enable regulators on the expansion board.

Table 7. J14-Legacy Audio Interface Connector Pin Out

J14 connector Pin Out			
Pin No.	**Net Name**	**Pin No.**	**Net Name**
1	NC	21	NC
2	DGND	22	NC
3	NC	23	NC
4	DGND	24	NC
5	NC	25	NC
6	NC	26	NC
7	NC	27	NC
8	NC	28	NC
9	NC	29	DGND
10	DGND	30	DGND
11	EXP_I2C4_SCL	31	NC
12	EXP_I2C4_SDA	32	NC
13	NC	33	JAMR3_GPIO0
14	NC	34	JAMR3_GPIO1
15	NC	35	JAMR3_GPIO2
16	NC	36	NC
17	NC	37	NC
18	NC	38	NC
19	DGND	39	DGND
20	DGND	40	DGND

Table 8. J20-JAMR3 Interface Connector Pin Out

J20 connector Pin Out			
Pin No.	**Net Name**	**Pin No.**	**Net Name**
1	NC	21	EXP_I2C2_SDA
2	NC	22	EXP_I2C2_SCL
3	NC	23	NC
4	NC	24	NC
5	NC	25	NC
6	NC	26	NC
7	NC	27	NC
8	NC	28	NC
9	NC	29	NC
10	NC	30	NC
11	NC	31	NC
12	NC	32	NC
13	JAMR3_RESETn	33	NC
14	NC	34	NC
15	NC	35	NC
16	NC	36	NC
17	NC	37	NC
18	NC	38	NC
19	DGND	39	NC
20	DGND	40	NC

Table 9. J17-JAMR3 Interface Connector Pin Out

J17 connector Pin Out			
Pin No.	**Net Name**	**Pin No.**	**Net Name**
1	NC	61	NC
2	NC	62	NC
3	NC	63	NC
4	NC	64	NC
5	NC	65	NC
6	NC	66	NC
7	NC	67	NC
8	NC	68	NC
9	NC	69	NC
10	NC	70	NC
11	NC	71	NC
12	NC	72	NC
13	NC	73	NC
14	NC	74	NC
15	NC	75	NC
16	NC	76	APP_BD_PORz
17	NC	77	DGND
18	NC	78	DGND
19	NC	79	NC
20	NC	80	NC
21	NC	81	NC
22	McASP11_AXR6	82	NC

Table 9. J17-JAMR3 Interface Connector Pin Out (continued)

J17 connector Pin Out			
Pin No.	**Net Name**	**Pin No.**	**Net Name**
23	McASP11_AXR4	83	NC
24	McASP11_AXR5	84	NC
25	NC	85	NC
26	DGND	86	NC
27	DGND	87	NC
28	EXP_I2C1_SDA	88	NC
29	McASP11_ACLKX	89	NC
30	EXP_I2C1_SCL	90	NC
31	McASP11_AFSX	91	NC
32	NC	92	NC
33	McASP11_AXR1	93	NC
34	NC	94	NC
35	McASP11_AXR3	95	NC
36	NC	96	NC
37	McASP11_AXR0	97	NC
38	McASP11_AXR7	98	NC
39	McASP11_AXR2	99	NC
40	NC	100	NC
41	NC	101	NC
42	NC	102	JAMR3_I2S_WC
43	NC	103	JAMR3_I2S_DA
44	NC	104	JAMR3_I2S_CLK
45	NC	105	JAMR3_I2S_DB
46	NC	106	NC
47	NC	107	NC
48	NC	108	NC
49	VCC_12V	109	NC
50	VCC_12V	110	NC
51	VCC_12V	111	NC
52	VCC_12V	112	NC
53	VCC_12V	113	NC
54	VCC_12V	114	NC
55	NC	115	DGND
56	NC	116	DGND
57	EXP_DC_3V3	117	NC
58	EXP_DC_3V3	118	NC
59	EXP_DC_3V3	119	NC
60	EXP_DC_3V3	120	NC

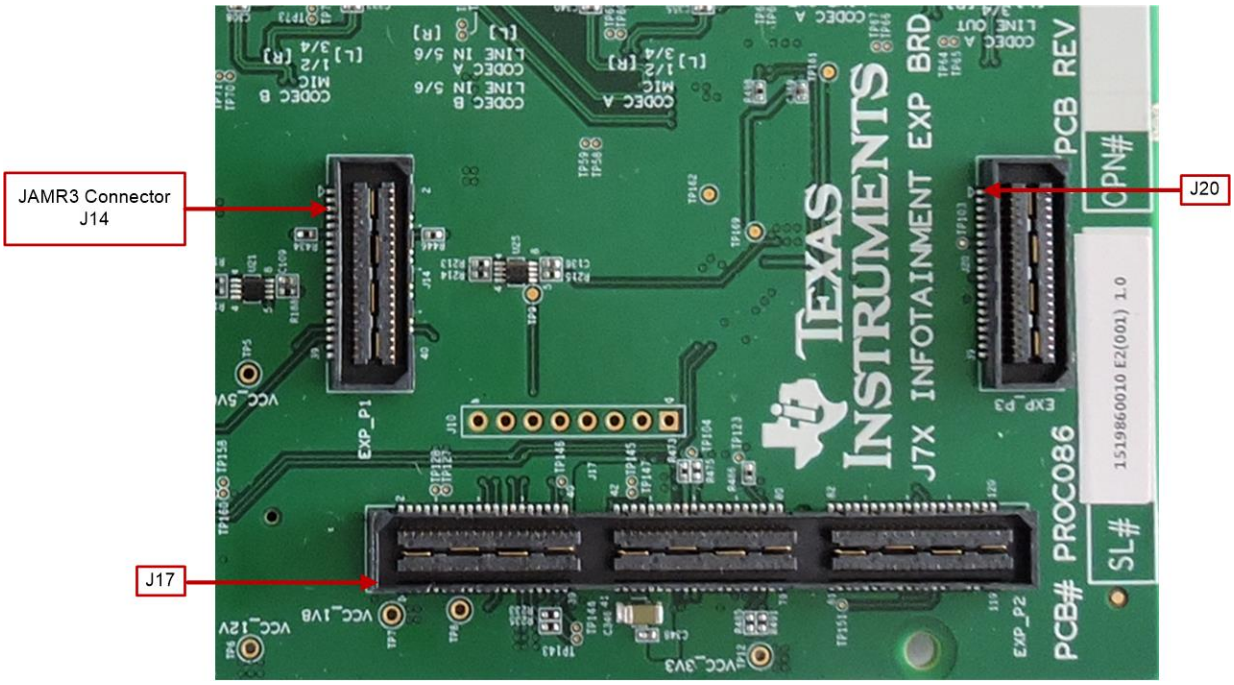


Figure 16. JAMR3 Interface Connectors

4.9 VIN/VOUT Mux Selection

The multiplexed video Input/Output signals from Expansion connector connected to three 12 bit 1:3 De-muxer U10, U11 and U12 IC Mfr. Part# SN74CBT16214CDGGR. One channel (Port B1) of the de-muxer interfaced with HDMI transmitter, the second channel (Port B2) interfaced with parallel camera interface and the third channel (Port B3) interfaced with FPD display port on the infotainment expansion board. For Mux selection GPIO details, see Section A.2.

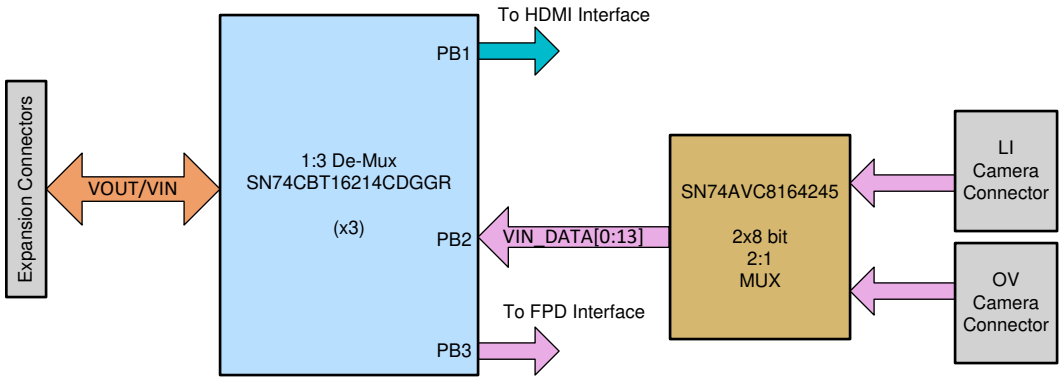


Figure 17. VIN/VOUT Mux Selection

Table 10. VIN/VOUT Mux Selection Table

Selection Inputs	Inputs/Outputs	
S2 S1 S0	A1	Function
H H L	VOUT	A1 port = B1 port (HDMI)- Default
H H H	VIN	A1 port = B2 port (Camera)
H L H	VOUT	A1 port = B3 port (FPD Link)

4.10 HDMI Interface Bridge

TI's HDMI transmitter IC Mfr. Part# TFP410-PAP is used for converting the 24-bit RGB video signals from VOUT port of SOC into HDMI output signals. The output of the HDMI transmitter chip terminated to a HDMI connector Mfr. Part# 10029449-001RLF by interfacing suitable filter and ESD circuitry.

Power +5 V is provided to the HDMI connector using current limit load switch TPD12S016PWR for current limiting and overall ESD protection for the HDMI controller. The current limit load switch is controlled by a GPIO expander signal (HDMI_DDC_OE). DDC signals are level translated using standard I2C level translator PCA9306DCT over TPD12S016 for improved drive strength.

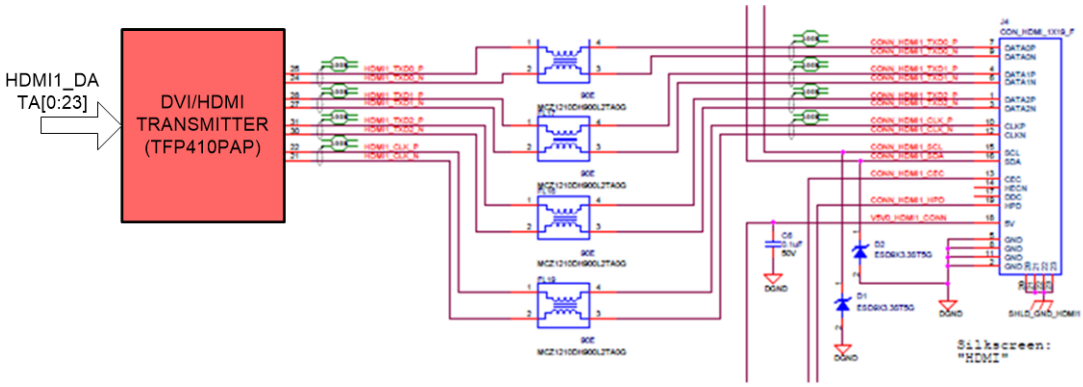


Figure 18. HDMI Interface Bridge

4.11 FPD Link Display Serializer Interface

FPD Link III serializer IC DS90UB921 is used for converting the 24 bit RGB signals Video signals from SOC into FPD link III signals. The serialized FPD link III output is terminated to HSD connector (Mfr Part# D4S20G-400A5-C). To route the VOUT signals from SOC to FPD link serializer from the default HDMI transmitter, see Table 10 and Section A.2.

I2C signals of J7 SOC being used for controlling and configuring the Display serializer. A 30.9 KΩ Pull up and 95.3K Ω pull down is provided on ID[X] pin to set the 7'b I2C address to 0x1A.

Power +12 V is provided to the HSD connector using a power switch TPS1H100AQPWPRQ1 to power the FPD Link-III display board. The power switch is controlled by a GPIO expander signal (PWR_SW_UB921). There is an optional clock cleaner circuit Mfr Part#:CDCE813-Q1 is available on infotainment board to clean the input clock signal coming from CP board and pass it to FPD link III Serializer.

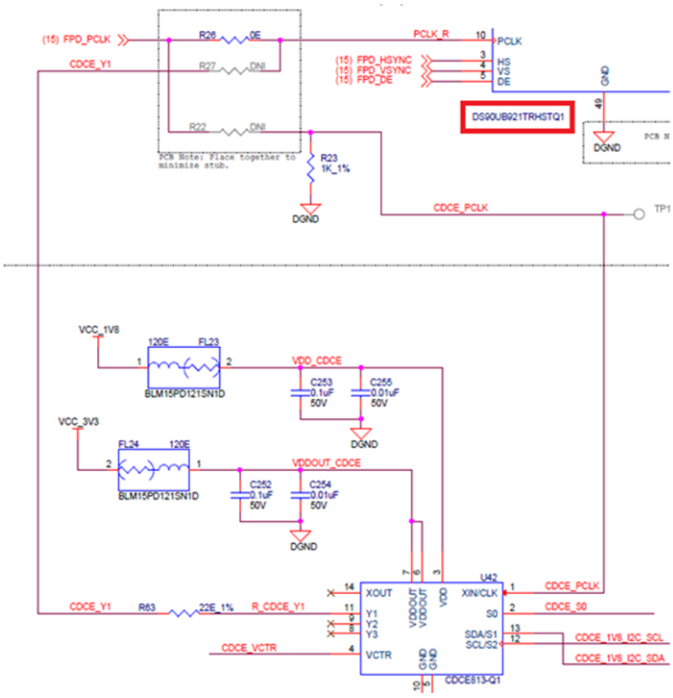


Figure 19. Optional Clock Cleaner to FPD Link Serializer

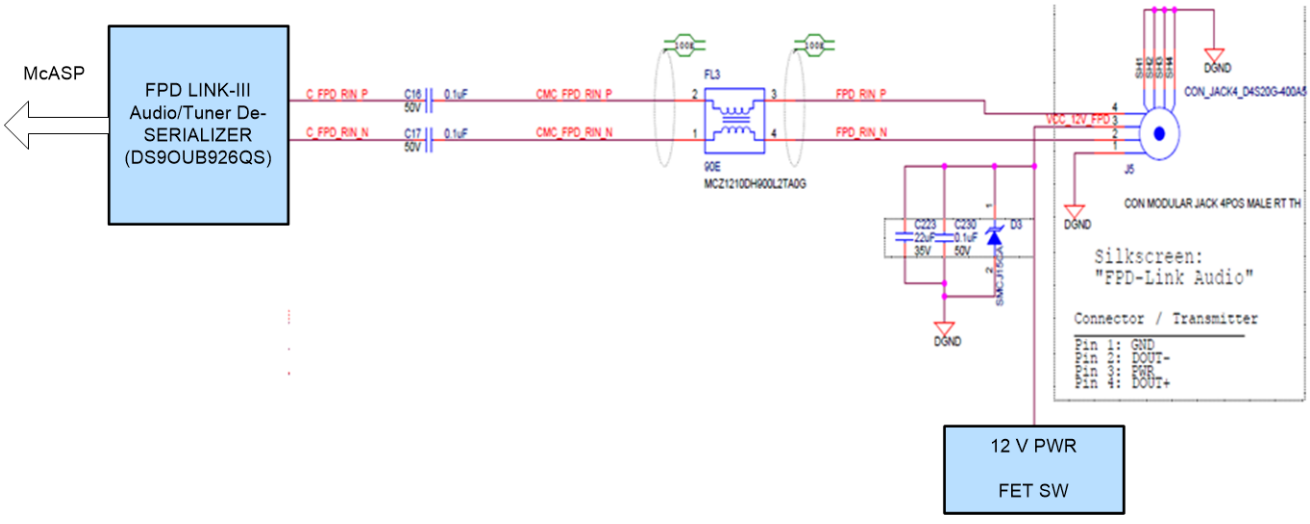


Figure 20. FPD Link Display Serializer Interface

4.12 Parallel Camera Interface

There are two camera module connectors present on infotainment expansion board to support parallel camera interface:

- 32 pin Omni Vision camera module connector
- 36 Pin Leopard imaging camera module connector

Parallel camera data & SYNC signals from both connectors are connected to a 2x 2:1 Camera selection MUX IC Part#: SN74AVCB164245VR. GPIO signal CAM_SEL_OV# is used to select between OV-camera and LI-Camera modules. By default, OV camera signal path is enabled. For GPO mapping, see Section A.2.

The output of camera selection mux is connected to VIN/VOUT selection mux. To route the parallel camera signals to VPFE port of SoC, see Table 10 and Section A.2.

SPI, Reset, PCLK and Power down signals are terminated with Camera connector through 3x level translation circuit IC Part# SN74AVC4T245DGVR (U3, U4 and U5). Camera I2C signals are level translated using IC part# PCA9306DCT.

NOTE: Camera modules will not be the part of delivery kit.

4.12.1 Camera Clock

An optional 24 MHz oscillator IC U38 output is connected to camera module through a buffer IC U35 Mfr. Part# SN74LVC2G125DCUR.

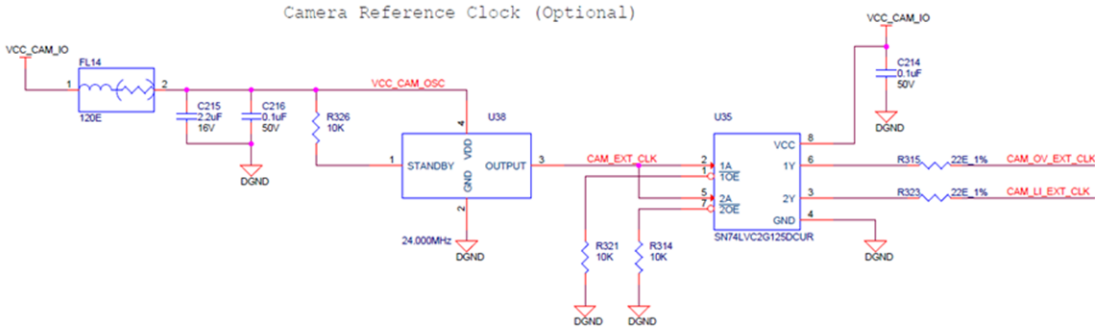


Figure 21. Camera Clock

4.12.2 LI Camera Module Connector

There is one camera-LI module connectors J6 (Part # 52559-3652) on the board.

Table 11 contains the pin out of the LI-camera module connectors.

Table 11. LI-Camera Module Connector Pin Out

J6 connector Pin Out	
Pin No.	**Net Name**
1	VCC_CAM_3V3
2	VCC_CAM_3V3
3	VCC_CAM_3V3
4	VCC_CAM_5V0
5	VCC_CAM_5V0
6	DGND
7	CAM_LI_EXT_CLK
8	DGND
9	R_LI_VIN_PCLK
10	DGND
11	LI_VIN_VD
12	LI_VIN_HD
13	LI_VIN_DATA13
14	LI_VIN_DATA12
15	LI_VIN_DATA11
16	LI_VIN_DATA10
17	LI_VIN_DATA9
18	LI_VIN_DATA8
19	LI_VIN_DATA7
20	LI_VIN_DATA6
21	LI_VIN_DATA5
22	LI_VIN_DATA4
23	LI_VIN_DATA3
24	LI_VIN_DATA2
25	DGND
26	DGND
27	LI_VIN_DATA1
28	LI_VIN_DATA0
29	CAM_I2C_SCL
30	CAM_I2C_SDA
31	LI_SPI3_MISO
32	LI_SPI3_CLK
33	LI_CAM_RST#
34	LI_SPI3_CS0
35	LI_CAM_TRIGGER
36	LI_SPI3_MOSI

4.12.3 OV Camera Module Connector

There is one camera-OV module connector J3 (Part # SSQ-116-02-L-D-RA) on the board.

Table 12 contains the pin out of the OV camera module connectors.

Table 12. OV-Camera Module Connector Pin Out

J3 connector Pin Out			
Pin No.	**Net Name**	**Pin No.**	**Net Name**
1	OV_VIN_DATA5	17	OV_VIN_PCLK_R
2	OV_VIN_DATA4	18	DGND
3	OV_VIN_DATA7	19	VCC_CAM_5V0
4	OV_VIN_DATA6	20	CAM_OV_EXT_CLK
5	OV_VIN_DATA9	21	VCC_CAM_5V0
6	OV_VIN_DATA8	22	DGND
7	OV_VIN_DATA11	23	OV_VIN_DATA3
8	OV_VIN_DATA10	24	OV_VIN_DATA2
9	NC	25	OV_VIN_DATA1
10	R_OV_CAM_PWDN	26	OV_VIN_DATA0
11	NC	27	NC
12	CAM_I2C_SDA	28	NC
13	OV_VIN_HD	29	NC
14	CAM_I2C_SCL	30	NC
15	OV_VIN_VD	31	DGND
16	DGND	32	DGND

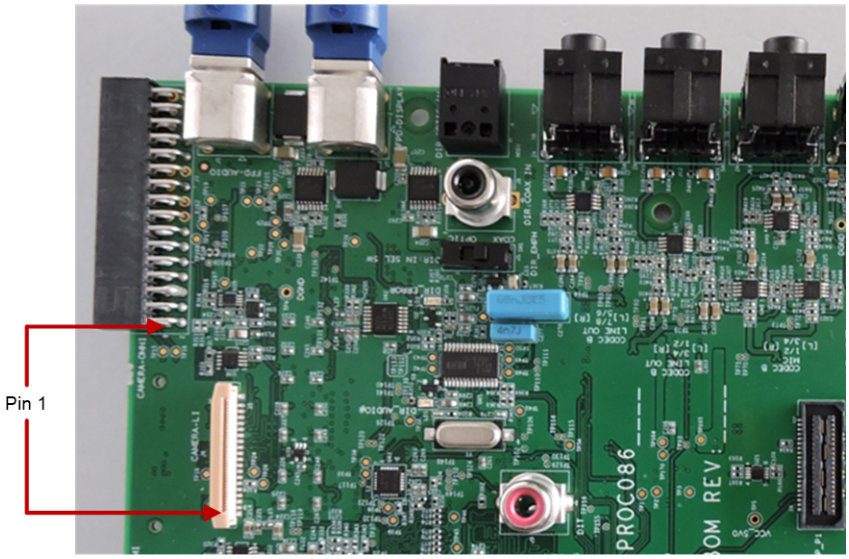


Figure 22. OV and LI-Camera Module Connector Pin1 Marking

Jacinto7 EVM Interface/IO Mapping

A.1 Interface Mapping

J721E EVM interface mapping on infotainment expansion is provided in Table 13.

Table 13. Interface Mapping

INFO Peripheral	INFO Interface	J721E Connectivity
Audio Codec – A (U32)	McASP0 Port (Net name MCASP0_AXR[6:0]*)	McASP0
Audio Codec – B (U19)	McASP0 Port (Net name MCASP0_AXR[13:7]*)	McASP0
FPD Link III Serializer (Display) (U8)	VOUT0 Port (Net name VOUT0_DATA_*)	VOUT0
FPD Link III De-Serializer (Audio) (U2)	McASP1 (Net name MCASP1_AXR_*, UB926_I2S_*)	McASP1 McASP6
Digital Audio Interface Receiver (U45,J8,MOD1)	McASP6 (Net name MCASP6_AXR_*)	McASP6
Digital Audio Interface Transmit (J9)	McASP2 (Net name MCASP2_AXR0)	McASP2
Parallel Camera (OV/LI) (J3 & J6)	VPFE0 (Net name VPFE0_DATA_*)	(see mux selection) VPFE0 or UB921_DIN or HDMI1_DATA
HDMI Transmitter (U41)	VOUT0 (Net name HDMI1_DATA_*)	(see mux selection) VPFE0 or UB921_DIN or HDMI1_DATA
Config EEPROM(U30)	I2C0 (Net name WKUP_I2C0_*)	WKUP_I2C0
Legacy Audio/JAMR3 Interface (J14 , J17 & J20)	McASP11 (Net name MCASP11_AXR_*)	McASP11

A.2 Infotainment Board GPIO Mapping

GPIO expander signal mapping is as shown in Table 14.

Table 14. GPIO Expander Signal Mapping

Jacinto7 EVM -INFO GPIO Expander						
I2C Bus/Address	**GPIO Port**	**Net Name in INFO Board**	**Direction WRT CTRL**	**Default State**	**Active State**	**Remarks**
INFO GPIO Expander - 1 Part# TCA6416ARTWR (AUDIO IO EXPANSION)						
I2C3/0x21	P00	CODEC_RESETn	Output	PD	Active Low	Used as a Reset signal for Audio Codecs A & B
	P01	JAMR3_RESETn	Output	PD	Active Low	Used as a Reset signal for JAMR3 Interface
	P02	JAMR3_PWR_CTRL	Output	NA	Active High	Power EN for JAMR3 Interface
	P03	UB926_RESETn	Output	PD	Active Low	Used as a Reset signal for FPD Audio De-Serializer
	P04	PWR_SW_UB926	Output	PD	Active High	Used as a Power Enable signal for Audio/FPD connector
	P05	UB926_TUNER_RESET	Output	PD	Active Low	Used as a Reset signal for FPD
	P06	UB926_GPIO_SPARE	Output	NA	NA	SPARE GPIO for FPDLink
	P07	UB926_LOCK	Input	NA	NA	Lock Input from FPDLink
	P10	DIR_RESETn	Output	PD	Active Low	Used as a Reset signal for DIR interface
	P11	DIR_CKSEL	Output	PU	NA	Used for DIR System clock source selection Low: PLL (VCO) clock, High: XTI clock
	P12	DIR_FMT0	Output	PU	NA	DOUT Audio Data output format - 24-bit, MSB-first, I2S (Default)
	P13	DIR_FMT1	Output	PU	NA	
	P14	DIR_PSCK0	Output	PD	NA	System clock of PLL selection
	P15	DIR_PSCK1	Output	PD	NA	
	P16	AUDEXP_P16	NA	NA	NA	Reserved GPIO
	P17	McASP6_MUX_SEL	Output	PD	NA	User for Mux selection b/w DIR or FPDLink
INFO GPIO Expander – 2 Part# TCA6416ARTWR (VIDEO IN/OUT IO EXPANSION)						
I2C1/0x21	P00	NC	NA	NA	NA	Not used
	P01	NC	NA	NA	NA	Not used
	P02	NC	NA	NA	NA	Not used
	P03	NC	NA	NA	NA	Not used
	P04	NC	NA	NA	NA	Not used
	P05	VOUTEXP_P04	NA	NA	NA	Terminated with Test point
	P06	VOUTEXP_P05	NA	NA	NA	Terminated with Test point
	P07	NC	NA	NA	NA	Not used
	P10	HDMI_PDn	Output	PD	Active Low	Used as a Power Down signal for HDMI Transmitter
	P11	HDMI_DDC_OE	Output	PD	Active High	Used for HDMI I2C Translator Enable logic
	P12	HDMI_HPD	Input	NA	NA	Used for detection of HDMI cable Hot plug
	P13	UB921_RESETn	Output	PD	Active Low	Used as a Reset signal for FPD III Display Serializer
	P14	PWR_SW_UB921	Output	PD	Active High	Used as a Power Enable signal for Audio/FPD connector
	P15	UB921_INTB	Input	NA	Active High	FPD III Display Serializer INTB = H, normal INTB = L, Interrupt request
	P16	VOUTEXP_P16	NA	NA	NA	Terminated with Test point
	P17	VOUTEXP_P17	NA	NA	NA	Terminated with Test point

Table 15. SoC GPIO Mapping

Info Peripheral	Peripheral IO	Direction (for SoC)	Default	Active State	J721E Connectivity
FPD LINK III Display	Interrupt	Input	PU	Active Low	GPIO0_79
Camera Mux Selection	Enable	Output	NA	'0'-OV '1'-LI	GPIO0_78
LI/OV Camera	Trigger	I/O	PD	Active High	GPIO0_31
	Reset	Output	PU	Active Low	GPIO0_32
JAMR3 Interface	JAMR3_GPIO0	I/O	NA	NA	GPIO0_65
	JAMR3_GPIO1	I/O	NA	NA	GPIO0_66
	JAMR3_GPIO2	I/O	NA	NA	GPIO0_67
FPD Link III De-serializer	UB926_GPIO1	I/O	NA	NA	GPIO0_11
	UB926_GPIO2	I/O	NA	NA	GPIO0_45
	UB926_GPIO3	I/O	NA	NA	GPIO0_46
Audio IO Expander	Interrupt	Input	PU	Active Low	GPIO1_23
Video IO Expander	Interrupt	Input	PU	Active Low	GPIO1_24
VIN/VOUT MUX SELECTION	Select0	Output	PD	SEL [1:0] '10'-HDMI '11'-CAM '01'-FPD	I2C0 (0x20), P14
	Select1	Output	PU		I2C0 (0x20), P15

A.3 I2C Address Mapping

Table 16 provides the complete I2C address mapping details on infotainment expansion.

Table 16. INFO Expansion I2C Table

J7ES EVM –Infotainment Expansion I2C Table			
I2C Port	**Device/Function**	**Part#**	**I2C Address**
WKUP_I2C0	Board ID EEPROM	CAT24C256W	0x52
WKUP_I2C0	JAMR3 EEPROM	CAT24C256WI	0x51
SoC_I2C0	Reserved	TP55, TP56	NA
SoC_I2C1	VOUT DDC link	<connector interface>	TBD
SoC_I2C1	I2C GPIO Expander (Video)	TCA6416ARTWR	0x21
SoC_I2C1	FPD Link-III Serializer (VOUT to FPD)	DS90UB921-Q1	0x1A
SoC_I2C1	CDCI (clock generator)	CDCE813-Q1	0x65
SoC_I2C2	Reserved	TP52, TP53	NA
SoC_I2C3	Audio Codec - A	PCM3168A-Q1	0x47
SoC_I2C3	Audio Codec - B	PCM3168A-Q1	0x46
SoC_I2C3	JAMR3 GPIO Expander	PCF8575	0x22 Requires modification on JAMR3
SoC_I2C3	Legacy Auio/JAMR3 Interface	AFE8310	0x048, 0x049, 0x04A &0x04B
SoC_I2C3	FPD Link-III De-Serializer (FPD to McASP)	DS90UB926Q-Q1	0x3B
SoC_I2C3	I2C GPIO Expander (Audio)	TCA6416ARTWR	0x21
SoC_I2C6	Camera Sensor, Parallel	<connector interface>	TBD

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2019) to A Revision **Page**

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