High-Performance, Two-Channel, 24-Bit, 216kHz Sampling Multi-Bit Delta-Sigma Analog-to-Digital Converter

FEATURES

- Supports Linear PCM Output Data
  - Output Sampling Rates from 8kHz to 216kHz
- Differential Voltage Inputs
- On-Chip Voltage Reference Improves Power-Supply Noise Rejection
- Dynamic Performance (24-bit word length)
  - Dynamic Range (–60dB input, A-weighted): 123dB typical
  - Dynamic Range (–60dB input, 20kHz bandwidth): 121dB typical
  - Total Harmonic Distortion + Noise (–1dB input, 20kHz bandwidth): –108dB typical
  - Channel Separation: 135dB
- Low Power Dissipation:
  - 305mW typical for 48kHz sampling rate
  - 330mW typical for 96kHz sampling rate
  - 340mW typical for 192kHz sampling rate
- Linear Phase Digital Decimation Filtering
  - Select from Classic or Low Group Delay Filter Responses
  - Low Passband Ripple
    Classic: ±0.00015dB
    Low Group Delay: ±0.001dB
- Digital High-Pass Filtering Removes DC Offset
  - Left and Right Channel Filters May Be Disabled Independently
- Audio Serial Port Interface
  - Master or Slave Mode Operation
  - Supports Left-Justified, I^{2}S™, and TDM Data Formats
- Output Word Length Reduction
- Overflow Indicators for the Left and Right Channels
- Analog Power Supply:
  +4.0V nominal
- Digital Power Supply:
  +3.3V nominal
- Power-Down Mode: 4mW typical
- Package: TQFP-48, RoHS compliant

APPLICATIONS

- Digital Audio Recorders and Mixing Desks
- Digital Live Sound Consoles
- Digital Audio Effects Processors
- Surround Sound Encoders
- Broadcast Studio Equipment
- Data Acquisition and Measurement Systems
- Audio Test Systems
- Sonar

DESCRIPTION

The PCM4220 is a high-performance, two-channel analog-to-digital (A/D) converter designed for use in professional audio applications. Offering outstanding dynamic performance, the PCM4220 provides 24-bit linear PCM output data, with support for output word length reduction to 20-, 18-, or 16-bits. The PCM4220 includes three sampling modes, supporting output sampling rates from 8kHz to 216kHz. The PCM4220 is ideal for a variety of digital audio recording and processing applications.

A linear phase digital decimation filtering engine supports Classic and Low Group Delay filter responses, allowing optimization for either studio or live sound applications. In addition, digital high-pass filtering is provided for DC offset removal. The The PCM4220 is configured using dedicated control pins for selection of sampling modes, audio data formats and word length, decimation filter response, high-pass filter disable, and reset/power-down functions.

While providing uncompromising performance, the PCM4220 addresses power concerns with just over 300mW typical total power dissipation, making the device suitable for multi-channel audio systems. The PCM4220 is typically powered from a +4.0V analog supply and a +3.3V digital supply. The digital I/O is logic-level compatible with common digital signal processors, digital interface transmitters, and programmable logic devices. The PCM4220 is available in a TQFP-48 package, which is RoHS-compliant.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	VALUE
Power supplies	
VCC1, VCC2	–0.3V to +6.0V
VDD	–0.3V to +4.0V
Digital input voltage	
All digital input and I/O pins	–0.3V < (VDD + 0.3V) < +4.0V
Analog input voltage	
VINL+, VINL–, VINR+, VINR–	–0.3V < (VCC + 0.3V) < +6.0V
Input current (all pins except power and ground)	±10mA
Ambient operating temperature	–40°C to +85°C
Storage temperature	–65°C to +150°C

(1) These limits are stress ratings only. Stresses beyond these limits may result in permanent damage. Extended exposure to absolute maximum ratings may degrade device reliability. Normal operation or performance at or beyond these limits is not specified or ensured.

ELECTRICAL CHARACTERISTICS: DIGITAL AND DYNAMIC PERFORMANCE

All specifications are at T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

PARAMETER	CONDITIONS	PCM4220			UNIT
		MIN	TYP	MAX	
DIGITAL I/O CHARACTERISTICS (Applies to all digital pins)					
High-level input voltage, V_{IH}		0.7 × VDD		VDD	V
Low-level input voltage, V_{IL}		0		0.3 × VDD	V
High-level input current, I_{IH}			1	10	µA
Low-level input current, I_{IL}			1	10	µA
High-level output voltage, V_{OH}	I_O = –2mA	0.8 × VDD		VDD	V
Low-level output voltage, V_{OL}	I_O = +2mA	0		0.2 × VDD	V
Input capacitance, C_{IN}			3		pF
PCM OUTPUT SAMPLING RATE, f_S					
	Normal mode	8		54	kHz
	Double Speed mode	54		108	kHz
	Quad Speed mode	108		216	kHz
MASTER CLOCK INPUT					
Normal mode, MCKI = 256f_S		2.048		13.824	MHz
Double Speed mode, MCKI = 128f_S		6.912		13.824	MHz
Quad Speed mode, MCKI = 64f_S		6.912		13.824	MHz
DYNAMIC PERFORMANCE(1)					
PCM Output, Normal Mode, f_S = 48kHz	**BW = 22Hz to 20kHz**				
Total harmonic distortion + noise (THD+N)	f = 997Hz, –1dB input		–108	–100	dB
	f = 997Hz, –20dB input		–100		dB
	f = 997Hz, –60dB input		–61		dB
Dynamic range, no weighting	f = 997Hz, –60dB input		121		dB
Dynamic range, A-weighted	f = 997Hz, –60dB input	118	123		dB
Channel separation	f = 10kHz, –1dB input	115	135		dB
PCM Output, Double Speed Mode, f_S = 96kHz	**BW = 22Hz to 40kHz**				
Total harmonic distortion + noise (THD+N)	f = 997Hz, –1dB input		–108		dB
	f = 997Hz, –20dB input		–98		dB
	f = 997Hz, –60dB input		–58		dB
Dynamic range, no weighting	f = 997Hz, –60dB input		118		dB
Dynamic range, A-weighted	f = 997Hz, –60dB input		123		dB
Channel separation	f = 10kHz, –1dB input		135		dB
PCM Output, Quad Speed Mode, f_S = 192kHz	**BW = 22Hz to 40kHz**				
Total harmonic distortion + noise (THD+N)	f = 997Hz, –1dB input		–107		dB
	f = 997Hz, –20dB input		–98		dB
	f = 997Hz, –60dB input		–58		dB
Dynamic range, no weighting	f = 997Hz, –60dB input		118		dB
Dynamic range, A-weighted	f = 997Hz, –60dB input		123		dB
Channel separation	f = 10kHz, –1dB input		135		dB
PCM Output, Quad Speed Mode, f_S = 192kHz	**BW = 22Hz to 80kHz**				
Total harmonic distortion + noise (THD+N)	f = 997Hz, –1dB input		–106		dB
	f = 997Hz, –20dB input		–91		dB
	f = 997Hz, –60dB input		–52		dB
Dynamic range, no weighting	f = 997Hz, –60dB input		112		dB
Dynamic range, A-weighted	f = 997Hz, –60dB input		123		dB
Channel separation	f = 10kHz, –1dB input		135		dB

(1) Typical PCM output performance is measured and characterized with an Audio Precision SYS-2722 192kHz test system and a PCM4222EVM evaluation module modified for use with the PCM4220. Measurement bandwidth and weighting settings are noted in the *Parameter* and *Conditions* columns. THD+N is measured without the use of weighting filters. Master mode operation is utilized for all typical performance parameters, with the master clock input frequency (MCKI) set to 12.288MHz.

ELECTRICAL CHARACTERISTICS: DIGITAL AND DYNAMIC PERFORMANCE (continued)

All specifications are at T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

PARAMETER	CONDITIONS	PCM4220			UNIT
		MIN	TYP	MAX	
Digital Decimation Filter Characteristics: Classic Response					
Passband				0.4535 × f_S	Hz
Passband ripple				±0.00015	dB
Stop band		0.5465 × f_S			Hz
Stop band attenuation		–100			dB
Group delay			39/f_S		Seconds
Digital Decimation Filter Characteristics: Low Group Delay Response					
Passband				0.4167 × f_S	Hz
Passband ripple				±0.001	dB
Stop band		0.5833 × f_S			Hz
Stop band attenuation		–90			dB
Group delay			21/f_S		Seconds
Digital High-Pass Filter Characteristics					
–3dB corner frequency	High-pass filter enabled			f_S/48000	Hz

ELECTRICAL CHARACTERISTICS: ANALOG INPUTS, OUTPUTS, AND DC ERROR

All specifications are at T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

PARAMETER	CONDITIONS	PCM4220			UNIT
		MIN	TYP	MAX	
ANALOG INPUTS					
Full-scale input range					
Differential input	Referenced from VINL+ to VINL–, or VINR+ to VINR–		5.6		V_{PP}
Per input pin	Applies to VINL+, VINL–, VINR+, or VINR–		2.8		V_{PP}
Input impedance	Applies to VINL+, VINL–, VINR+, or VINR–		2.8		kΩ
Common-mode rejection			100		dB
ANALOG OUTPUTS					
Common-mode output voltage					
Left channel, VCOML	Measured from VCOML to AGND		0.4875 × VCC2		V
Right channel, VCOMR	Measured from VCOMR to AGND		0.4875 × VCC1		V
Common-mode output current	Applies to VCOML or VCOMR			200	µA
DC ERROR					
Output offset error	Digital high-pass filter disabled		3		mV
Offset drift	Digital high-pass filter disabled		3.5		µV/°C

ELECTRICAL CHARACTERISTICS: POWER SUPPLIES

All specifications are at T_A = +25°C, VCC1 = VCC2 = +4.0V, VDD = +3.3V, and MCKI = 12.288MHz, unless otherwise noted.

PARAMETER	CONDITIONS	PCM4220			UNIT
		MIN	TYP	MAX	
POWER SUPPLIES					
Recommended supply voltage range					
VCC1, VCC2	0°C <T_A ≤ +85°C	+3.8	+4.0	+4.2	V
VCC1, VCC2	–40°C ≤ T_A ≤ 0°C	+3.9	+4.0	+4.2	V
VDD	–40°C ≤ T_A ≤ +85°C	+2.4	+3.3	+3.6	V
Supply current: power-down	$\overline{RST}$ (pin 36) held low with no clocks applied				
ICC1 + ICC2	VCC1 = VCC2 = +4.0V		600		µA
IDD	VDD = +3.3V		325		µA
Supply current: f_S = 48kHz					
ICC1 + ICC2	VCC1 = VCC2 = +4.0V		65	75	mA
IDD	VDD = +3.3V		14	18	mA
Supply current: f_S = 96kHz					
ICC1 + ICC2	VCC1 = VCC2 = +4.0V		65		mA
IDD	VDD = +3.3V		21		mA
Supply current: f_S = 192kHz					
ICC1 + ICC2	VCC1 = VCC2 = +4.0V		65		mA
IDD	VDD = +3.3V		24		mA
Total power dissipation: power-down			3.5		mW
Total power dissipation: f_S = 48kHz			305	360	mW
Total power dissipation: f_S = 96kHz			330		mW
Total power dissipation: f_S = 192kHz			340		mW

ELECTRICAL CHARACTERISTICS: AUDIO INTERFACE TIMING

All specifications are at T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

PARAMETER	CONDITIONS	PCM4220			UNIT
		MIN	TYP	MAX	
AUDIO SERIAL PORT					
LRCK period, t_{LRCKP}	All data formats	4.62		125	µs
LRCK high/low time, t_{LRCKHL}					
Left-Justified, I^2S, and TDM Master mode formats		0.45 × t_{LRCKP}		0.55 × t_{LRCKP}	µs
TDM slave mode formats		t_{BCKP}		0.55 × t_{LRCKP}	µs
BCK period, t_{BCKP}	Left-Justified and I^2S data formats				
Normal sampling mode		t_{LRCKP}/128			ns
Double Speed sampling mode		t_{LRCKP}/64			ns
Quad Speed sampling mode		t_{LRCKP}/64			ns
BCK period, t_{BCKP}	TDM data formats				
Normal sampling mode		t_{LRCKP}/256			ns
Double Speed sampling mode		t_{LRCKP}/128			ns
Quad Speed sampling mode		t_{LRCKP}/64			ns
BCK high/low time, t_{BCKHL}	All data formats	0.45 × t_{BCKP}		0.55 × t_{BCKP}	ns
Data output delay, t_{DO}	All data formats			10	ns

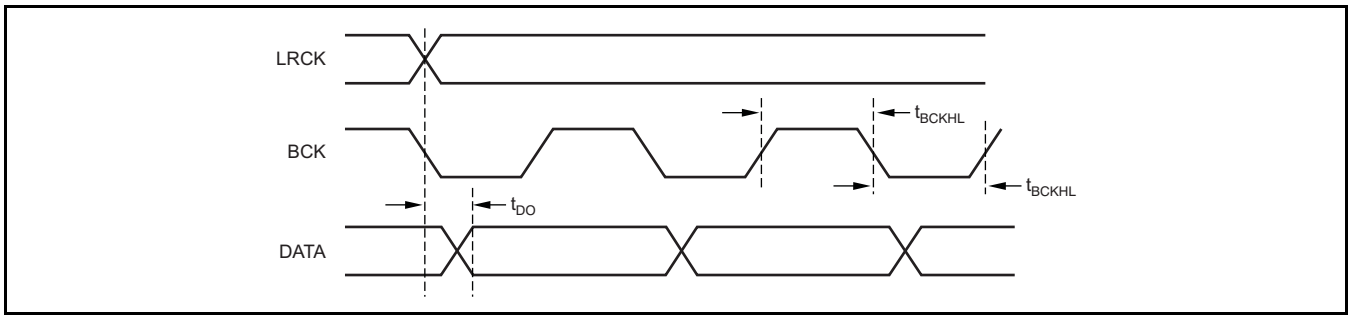


Figure 1. Audio Serial Port Timing: Left-Justified and I²S Data Formats

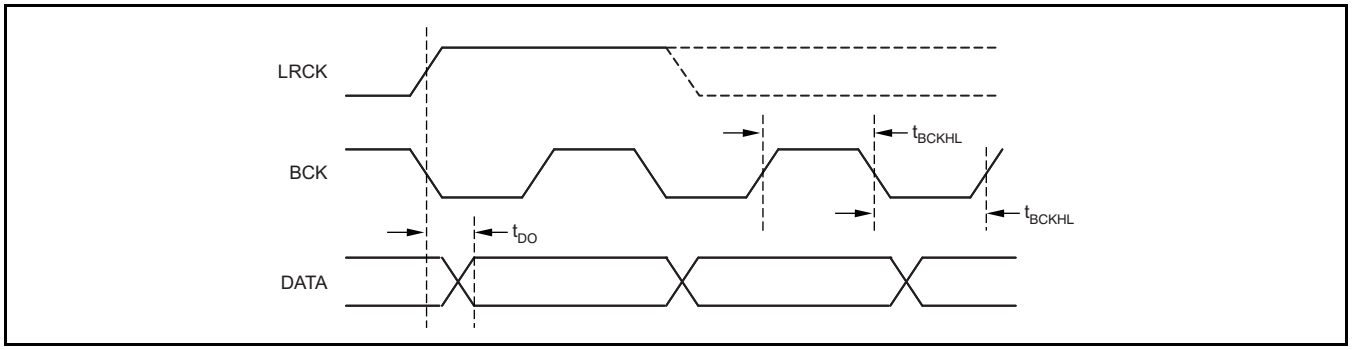
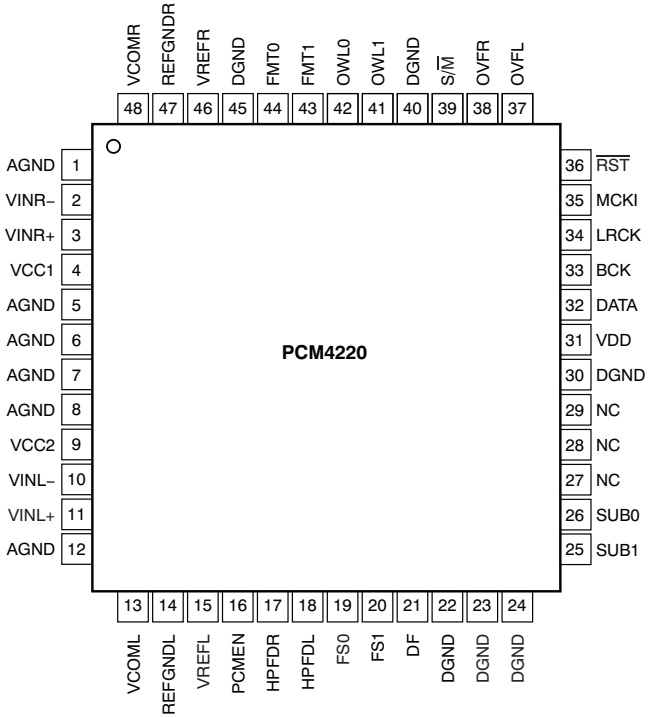


Figure 2. Audio Serial Port Timing: TDM Data Formats

PIN CONFIGURATION

PFB PACKAGE
TQFP-48
(TOP VIEW)



TERMINAL FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	1	Ground	Analog ground
VINR–	2	Input	Right channel inverting, 2.8V_{PP} nominal full-scale
VINR+	3	Input	Right channel noninverting, 2.8V_{PP} nominal full-scale
VCC1	4	Power	Analog supply, +4.0V nominal
AGND	5	Ground	Analog ground
AGND	6	Ground	Analog ground
AGND	7	Ground	Analog ground
AGND	8	Ground	Analog ground
VCC2	9	Power	Analog supply, +4.0V nominal
VINL–	10	Input	Left channel inverting, 2.8V_{PP} nominal full-scale
VINL+	11	Input	Left channel noninverting, 2.8V_{PP} nominal full-scale
AGND	12	Ground	Analog ground
VCOML	13	Output	Left channel common-mode voltage, (0.4875 × VCC2) nominal
REFGNDL	14	Ground	Left channel reference ground, connect to analog ground
VREFL	15	Output	Left channel reference output for decoupling purposes only
PCMEN	16	Input	PCM output enable (active high)
HPFDR	17	Input	Right channel high-pass filter disable (active high)
HPFDL	18	Input	Left channel high-pass filter disable (active high)

TERMINAL FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
FS0 FS1	19 20	Input	Sampling modes: FS0 = 0 and FS1 = 0: Normal mode FS0 = 1 and FS1 = 0: Double Speed mode FS0 = 0 and FS1 = 1: Quad Speed mode FS0 = 1 and FS1 = 1: Reserved Sampling mode
DF	21	Input	Digital decimation filter response: DF = 0: Classic filter response DF = 1: Low Group Delay response
DGND	22	Ground	Digital ground
DGND	23	Ground	Digital ground
DGND	24	Ground	Digital ground
SUB1 SUB0	25 26	Input	TDM active sub-frame: SUB0 = 0 and SUB1 = 0: Sub-frame 0 SUB0 = 1 and SUB1 = 0: Sub-frame 1 SUB0 = 0 and SUB1 = 1: Sub-frame 2 SUB0 = 1 and SUB1 = 1: Sub-frame 3
NC	27	—	No external connection, internally bonded to ESD pad
NC	28	—	No external connection, internally bonded to ESD pad
NC	29	—	No external connection, internally bonded to ESD pad
DGND	30	Ground	Digital ground
VDD	31	Power	Digital supply, +3.3V nominal
DATA	32	Output	Audio serial port data
BCK	33	I/O	Audio serial port bit clock
LRCK	34	I/O	Audio serial port left/right word clock
MCKI	35	Input	Master clock
$\overline{\text{RST}}$	36	Input	Reset and power-down (active low)
OVFL	37	Output	Left channel overflow flag (active high)
OVFR	38	Output	Right channel overflow flag (active high)
S/$\overline{\text{M}}$	39	Input	Audio serial port Slave/Master mode: S/$\overline{\text{M}}$ = 0: Master mode S/$\overline{\text{M}}$ = 1: Slave mode
DGND	40	Output	Digital ground
OWL1 OWL0	41 42	Input	Output word length: OWL0 = 0 and OWL1 = 0: 24-bits OWL0 = 1 and OWL1 = 0: 18-bits OWL0 = 0 and OWL1 = 1: 20-bits OWL0 = 1 and OWL1 = 1: 16-bits
FMT1 FMT0	43 44	Input	Audio data format: FMT0 = 0 and FMT1 = 0: Left-justified FMT0 = 1 and FMT1 = 0: I^2S FMT0 = 0 and FMT1 = 1: TDM FMT0 = 1 and FMT1 = 1: TDM with one BCK delay
DGND	45	Ground	Digital ground
VREFR	46	Output	Right channel reference output for decoupling purposes only
REFGNDR	47	Ground	Right channel reference ground, connect to analog ground
VCOMR	48	Output	Right channel common-mode voltage (0.4875 × VCC1 nominal)

TYPICAL CHARACTERISTICS

At T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

FFT PLOT

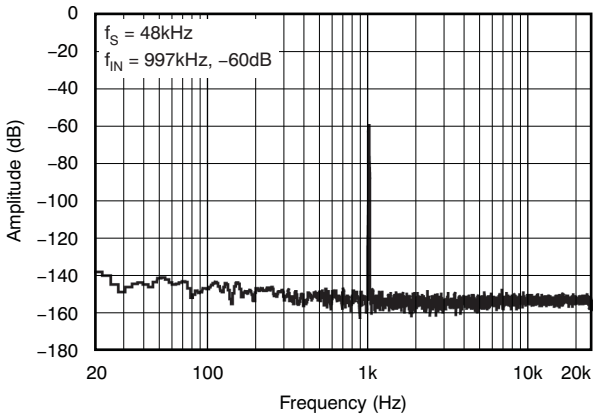


Figure 3.

FFT PLOT

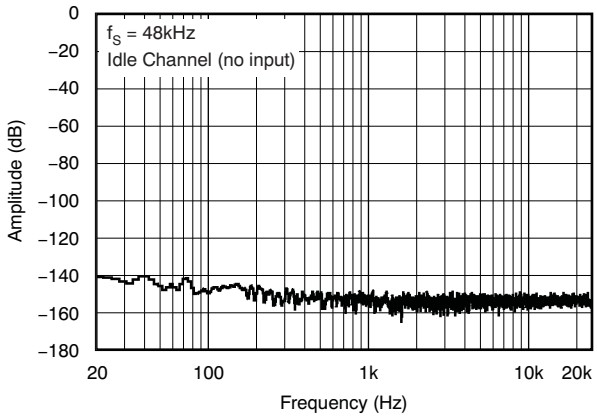


Figure 4.

THD+N vs INPUT FREQUENCY

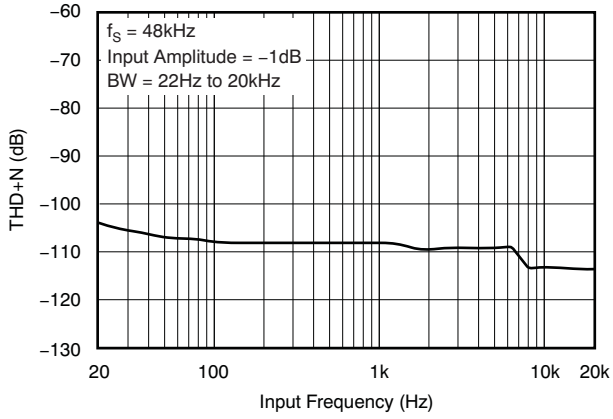


Figure 5.

THD+N vs INPUT AMPLITUDE

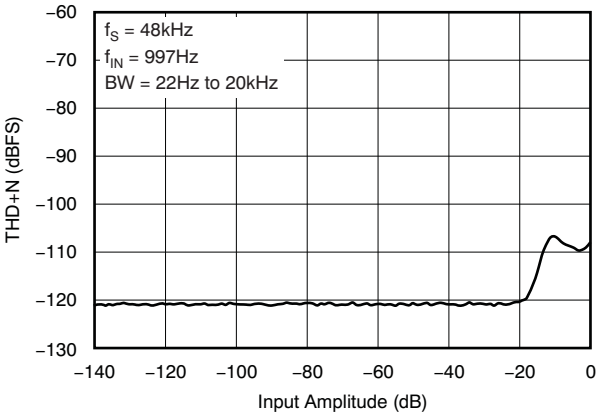


Figure 6.

CHANNEL SEPARATION vs INPUT FREQUENCY

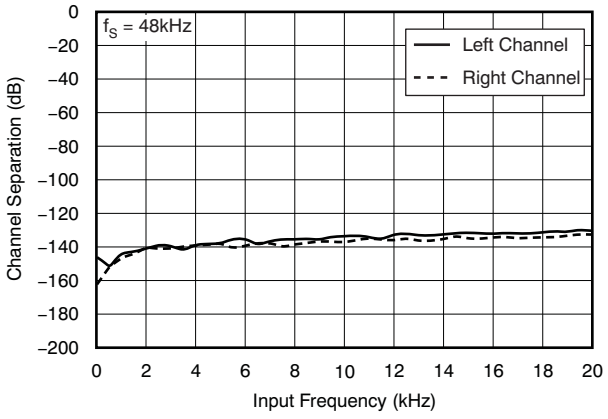


Figure 7.

LINEARITY

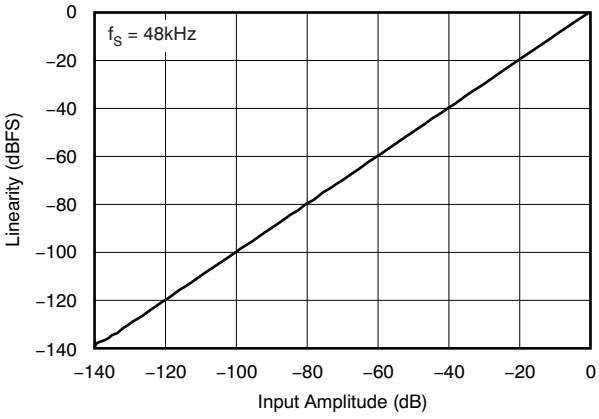


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

FFT PLOT

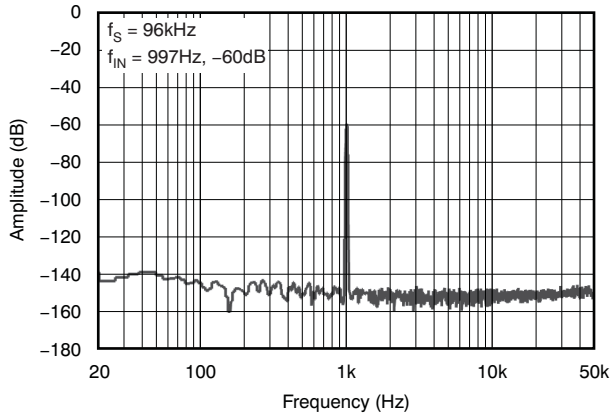


Figure 9.

FFT PLOT

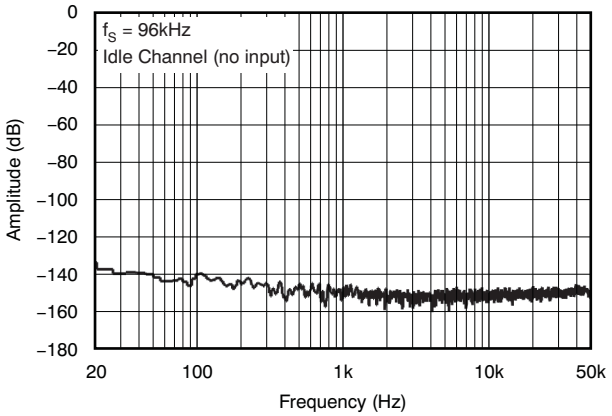


Figure 10.

THD+N vs INPUT FREQUENCY

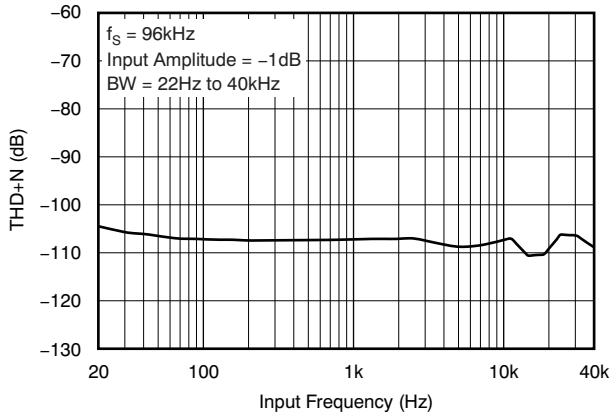


Figure 11.

THD+N vs INPUT AMPLITUDE

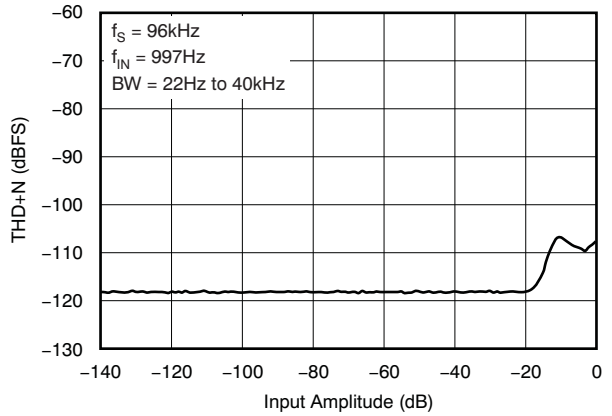


Figure 12.

CHANNEL SEPARATION vs INPUT FREQUENCY

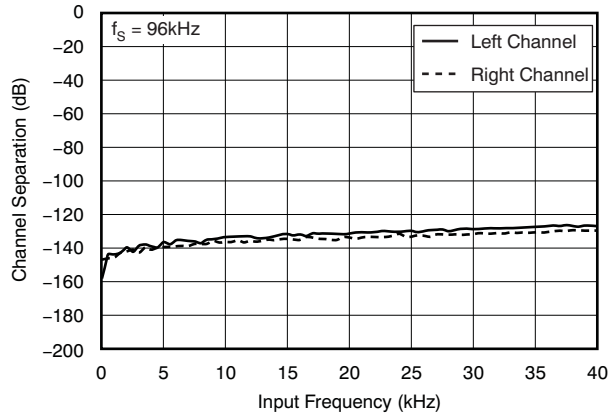


Figure 13.

LINEARITY

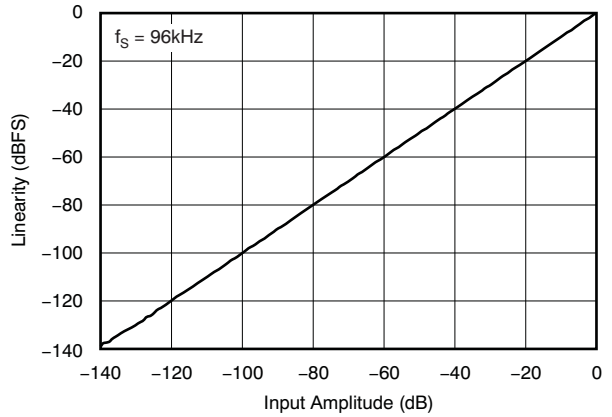


Figure 14.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

FFT PLOT

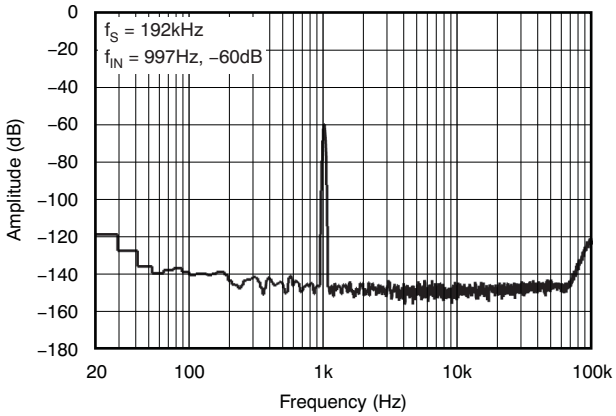


Figure 15.

FFT PLOT

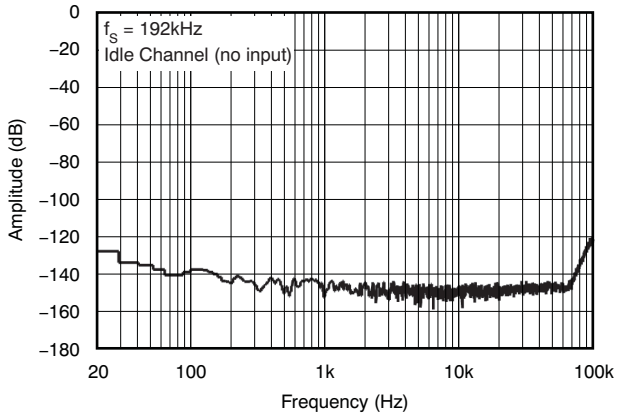


Figure 16.

THD+N vs INPUT FREQUENCY

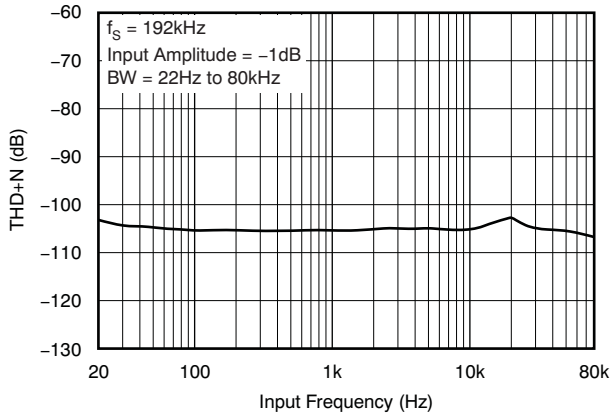


Figure 17.

THD+N vs INPUT AMPLITUDE

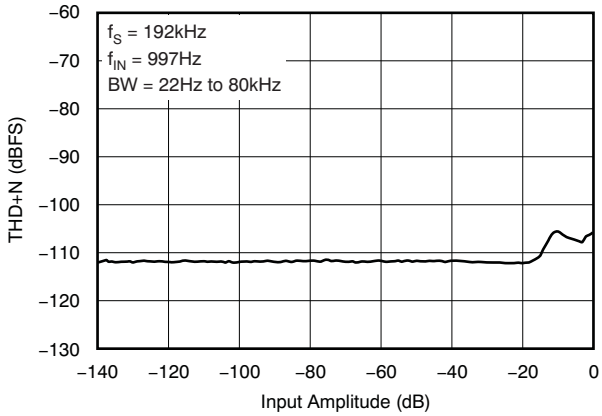


Figure 18.

CHANNEL SEPARATION vs INPUT FREQUENCY

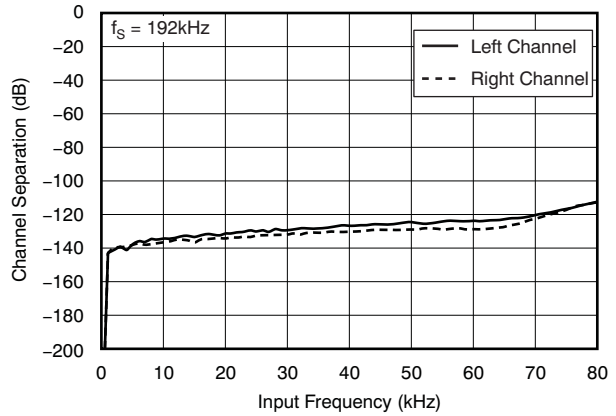


Figure 19.

LINEARITY

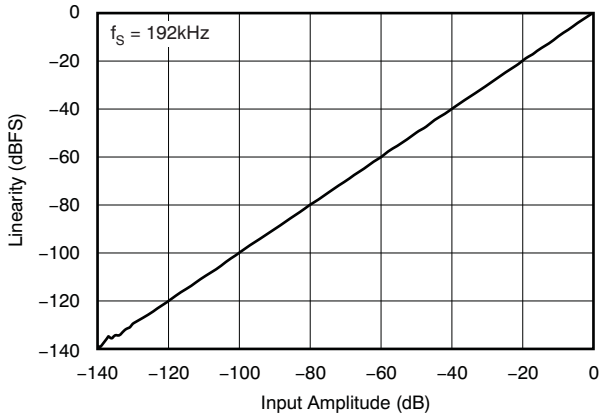


Figure 20.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

FREQUENCY RESPONSE (Up to 20kHz)

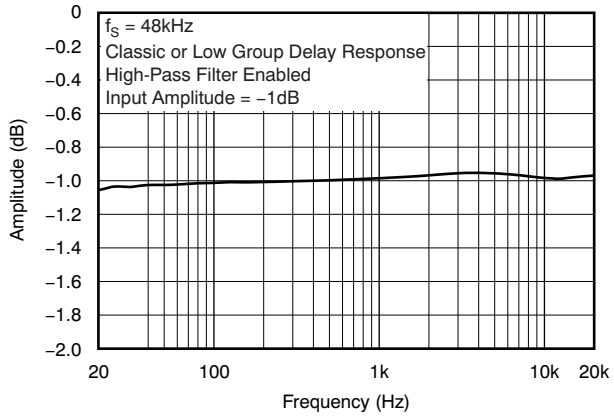


Figure 21.

FREQUENCY RESPONSE (Up to 40kHz)

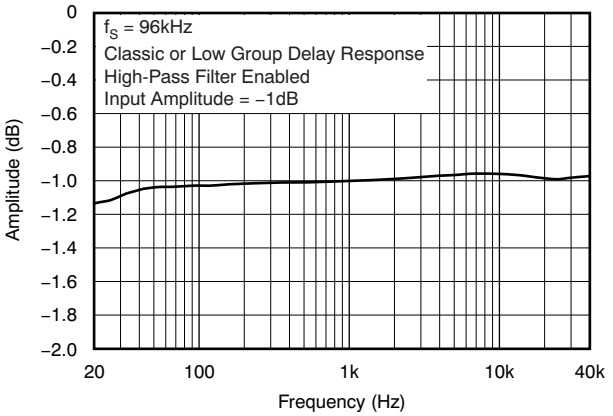


Figure 22.

FREQUENCY RESPONSE (Up to 80kHz)

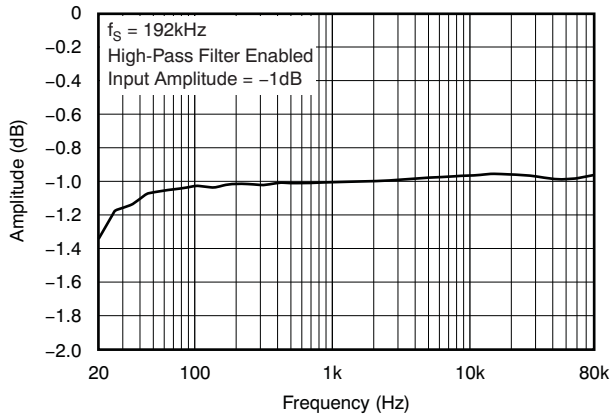


Figure 23.

DIGITAL DECIMATION FILTER, CLASSIC RESPONSE Overall Frequency Response

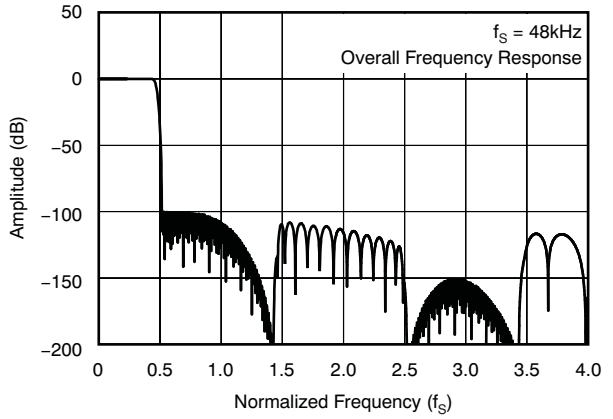


Figure 24.

DIGITAL DECIMATION FILTER, CLASSIC RESPONSE Stop Band Detail

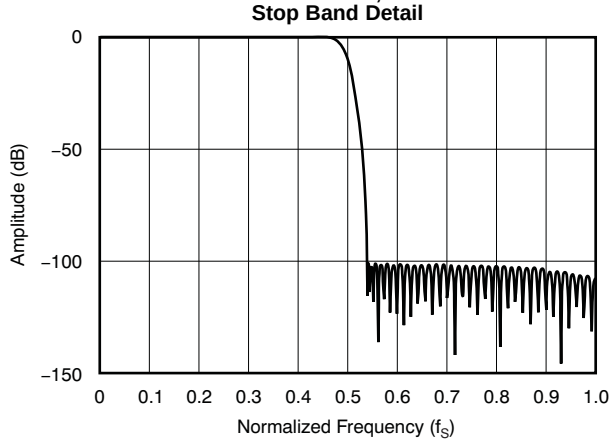


Figure 25.

DIGITAL DECIMATION FILTER, CLASSIC RESPONSE Passband Ripple Detail

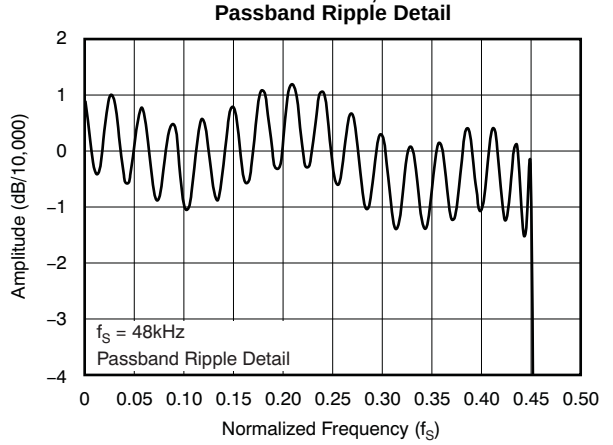


Figure 26.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

DIGITAL DECIMATION FILTER, CLASSIC RESPONSE
Transition Band Detail

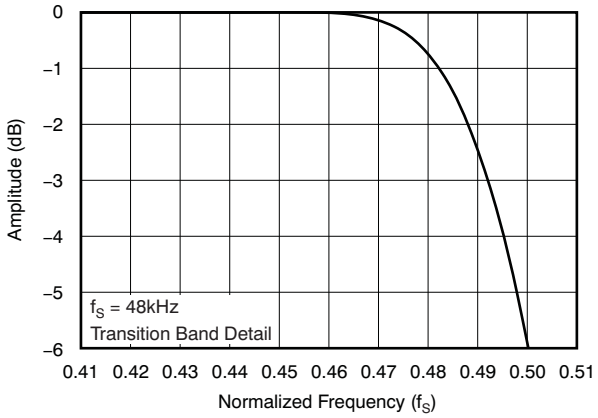


Figure 27.

DIGITAL DECIMATION FILTER, LOW GROUP DELAY RESPONSE
Overall Frequency Response

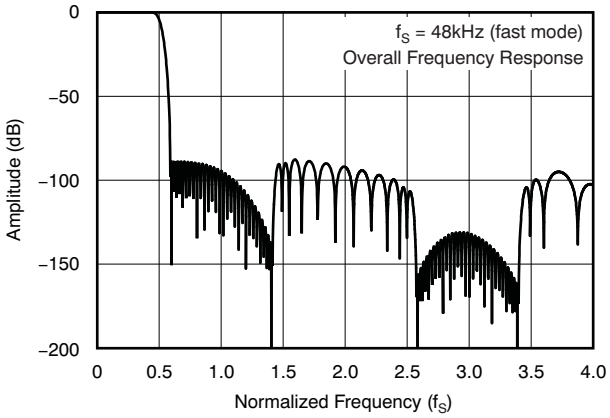


Figure 28.

DIGITAL DECIMATION FILTER, LOW GROUP DELAY RESPONSE
Stop Band Detail

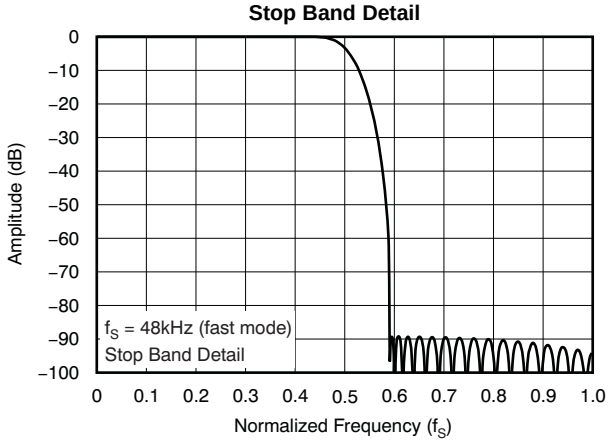


Figure 29.

DIGITAL DECIMATION FILTER, LOW GROUP DELAY RESPONSE
Passband Ripple Detail

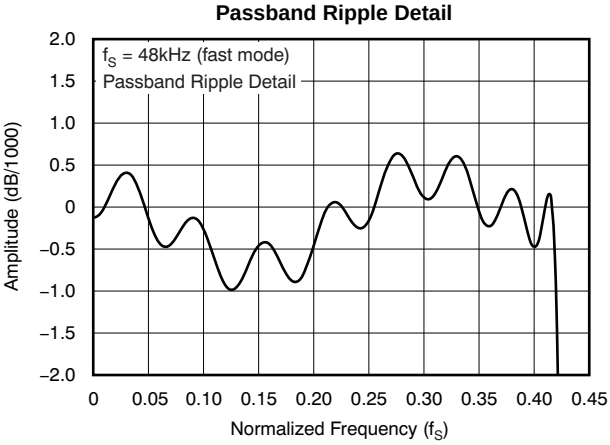


Figure 30.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

DIGITAL DECIMATION FILTER, LOW GROUP DELAY RESPONSE
Transition Band Detail

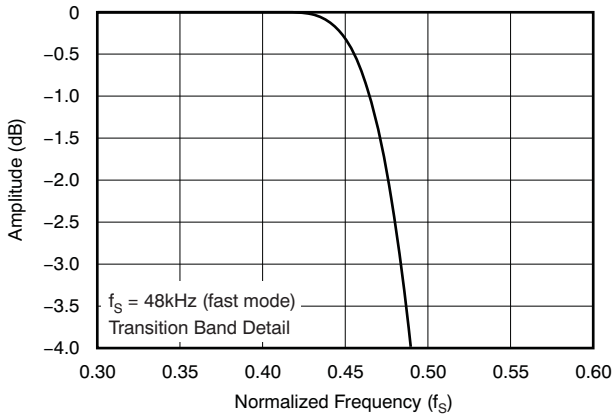


Figure 31.

DIGITAL HIGH-PASS FILTER
Passband Response

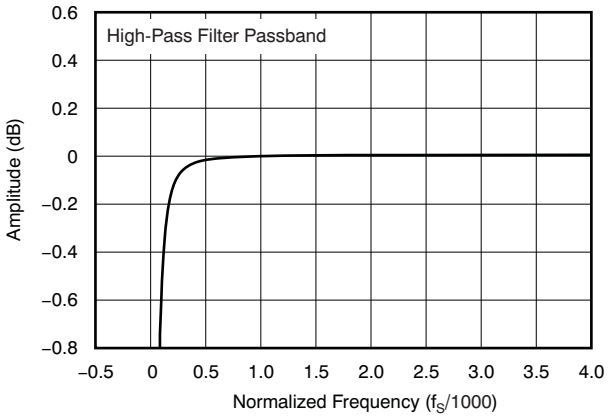


Figure 32.

DIGITAL HIGH-PASS FILTER
Stop Band Response

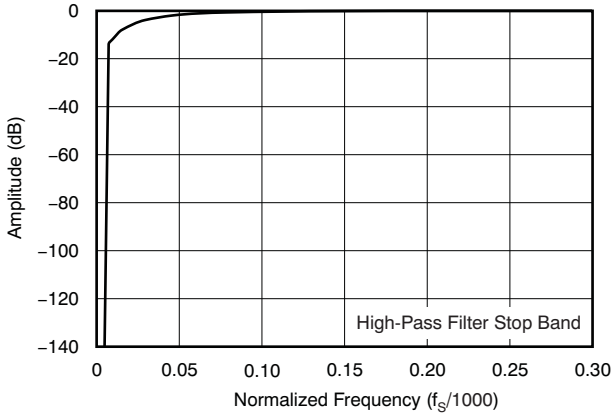


Figure 33.

PRODUCT OVERVIEW

The PCM4220 is a two-channel, multi-bit delta-sigma (ΔΣ) A/D converter. The 6-bit output from the delta-sigma modulators is routed to the digital decimation filter, where the output of the filter provides linear PCM data. The linear PCM data are output at the audio serial port interface for connection to external processing and logic circuitry.

Figure 34 shows a simplified functional block diagram for the PCM4220, highlighting the interconnections between the various functional blocks.

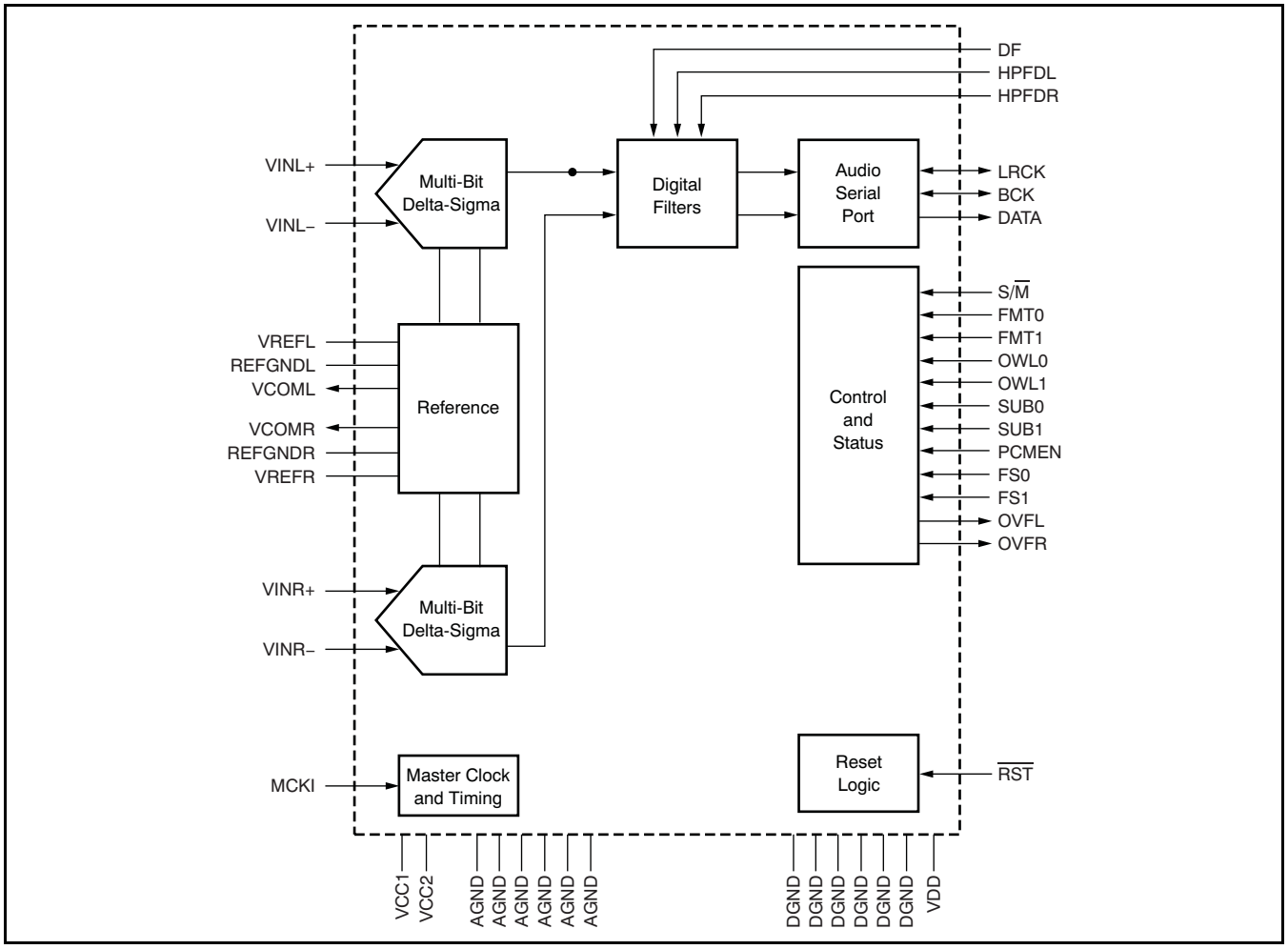


Figure 34. Functional Block Diagram

ANALOG INPUTS

The PCM4220 includes two analog inputs, referred to as the *left* and *right* channels. Each channel includes a pair of differential voltage input pins. The left channel inputs are named VINL– (pin 10) and VINL+ (pin 11), respectively. The right channel inputs are named VINR– (pin 2) and VINR+ (pin 3), respectively. Each pin of an input pair has a nominal full-scale input of $2.8V_{PP}$. The full-scale input for a given pair is specified as $5.6V_{PP}$ differential in the Electrical Characteristics table. Figure 35 shows the full-scale input range of the PCM4220, with the input signals centered on the nominal common-mode voltage of +1.95V.

In a typical application, the front end is driven by a buffer amplifier or microphone/line level preamplifier. Examples are given in the *Input Buffer Circuits* section of this datasheet. The analog inputs of the PCM4220 may be driven up to the absolute maximum input rating without instability. If the analog input voltage is expected to exceed the absolute maximum input ratings in a given application, it is recommended that input clamping or limiting be added to the analog input circuitry prior to the PCM4220 in order to provide protection against damaging the device. Specifications for the analog inputs are given in the Electrical Characteristics and Absolute Maximum Ratings tables of this data sheet.

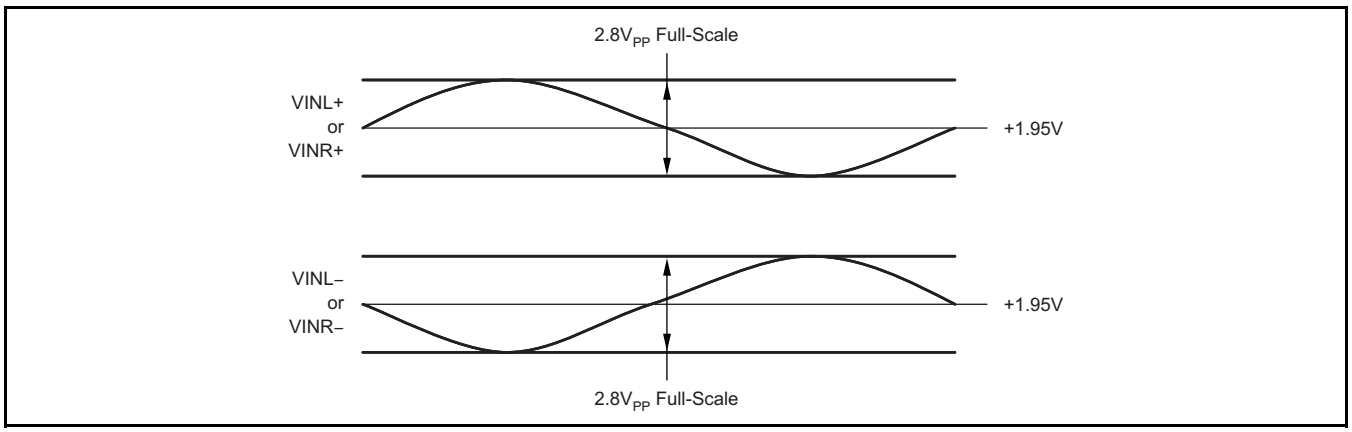


Figure 35. Full-Scale Analog Input Range

VOLTAGE REFERENCE

The PCM4220 includes an on-chip, band-gap voltage reference. The band-gap output voltage is buffered and then routed to the two delta-sigma modulators. The inclusion of an on-chip reference circuit enhances the power-supply noise rejection of the PCM4220. The buffered reference voltage for each channel is filtered using external capacitors. The capacitors are connected between VREFL (pin 15) and REFGNDL (pin 14) for the left channel, and VREFR (pin 46) and REFGNDR (pin 47) for the right channel. Figure 36 illustrates the recommend reference decoupling capacitor values and connection scheme.

The 10nF to 100nF capacitors in Figure 36 may be metal film or X7R/C0G ceramic chip capacitors. The 100µF capacitors may be polymer tantalum chip (Kemet T520 series or equivalent) or aluminum electrolytic.

The VREFL and VREFR pins are not designed for biasing external input circuitry. Two common-mode voltage outputs are provided for this purpose, and are discussed in the following section.

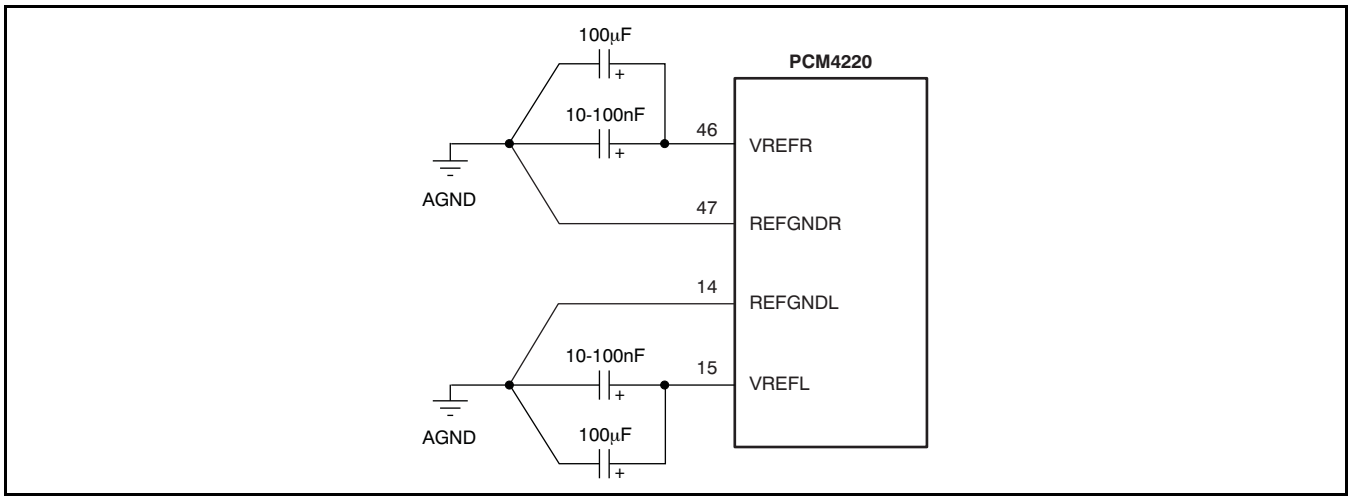


Figure 36. Recommended Reference Capacitor Connections and Values

COMMON-MODE VOLTAGE OUTPUTS

The PCM4220 includes two dc common-mode voltage outputs, VCOML (pin 13) and VCOMR (pin 48), which correspond to the left and right input channels, respectively. The common-mode voltage is utilized to bias internal op amps within the modulator section of the PCM4220, and may be used to bias external input circuitry when proper design guidelines are followed. The common-mode voltages are derived from the VCC1 and VCC2 analog power supplies using internal voltage dividers. The voltage divider outputs are buffered and then routed to internal circuitry and the VCOML and VCOMR outputs.

The common-mode output voltage is nominally equal to (0.4875 × VCC1) for VCOMR and (0.4875 × VCC2) for VCOML. Given an analog supply voltage of +4.0V connected to both VCC1 and VCC2, the resulting common-mode voltages are +1.95V.

The common-mode voltage outputs have limited drive capability. If multiple bias points are to be driven, or the external bias nodes are not sufficiently high impedance, an external output buffer is recommended. Figure 37 shows a typical buffer configuration using the OPA227. The op amp utilized in the buffer circuit should exhibit low dc offset and drift characteristics, as well as low output noise.

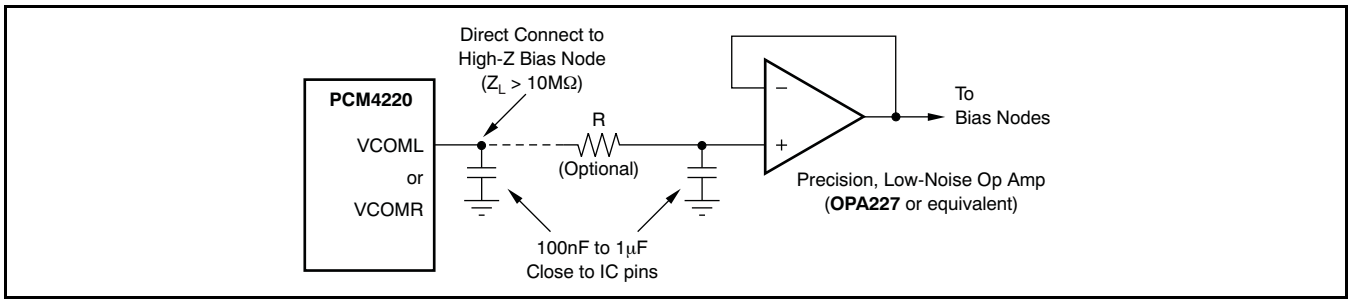


Figure 37. Common-Mode Output Connections

MASTER CLOCK INPUT

The PCM4220 requires a master clock for operating the internal logic and modulator circuitry. The master clock is supplied from an external source, connected at the MCKI input (pin 35). Table 1 summarizes the requirements for various operating modes of the PCM4220. Referring to Table 1, the term f_S refers to the PCM4220 PCM output sampling rate (that is, 48kHz, 96kHz, 192kHz, etc.). Refer to the Electrical Characteristics table for timing specifications related to the master clock input.

For best performance, the master clock jitter should be maintained below 40ps peak amplitude.

Table 1. Master Clock Requirements

OPERATING MODE	REQUIRED MASTER CLOCK (MCKI) RATE
PCM Normal	$256f_S$
PCM Double Speed	$128f_S$
PCM Quad Speed	$64f_S$

RESET AND POWER-DOWN OPERATION

The PCM4220 includes an external reset input, $\overline{RST}$ (pin 36), which may be utilized to force an internal reset initialization or power-down sequence. The reset input is active low. Figure 38 shows the required timing for an external forced reset.

A power-down state for the PCM422 may be initiated by forcing and holding the reset input low for the duration of the desired power-down condition. Minimum power is consumed during this state when all clock inputs for the PCM4220 are forced low. Before releasing the reset input by forcing a high state, the master clock should be enabled so that the PCM4220 can execute a reset initialization sequence.

While the $\overline{RST}$ pin is forced low, or during reset initialization, the audio serial port data and clock outputs are driven low.

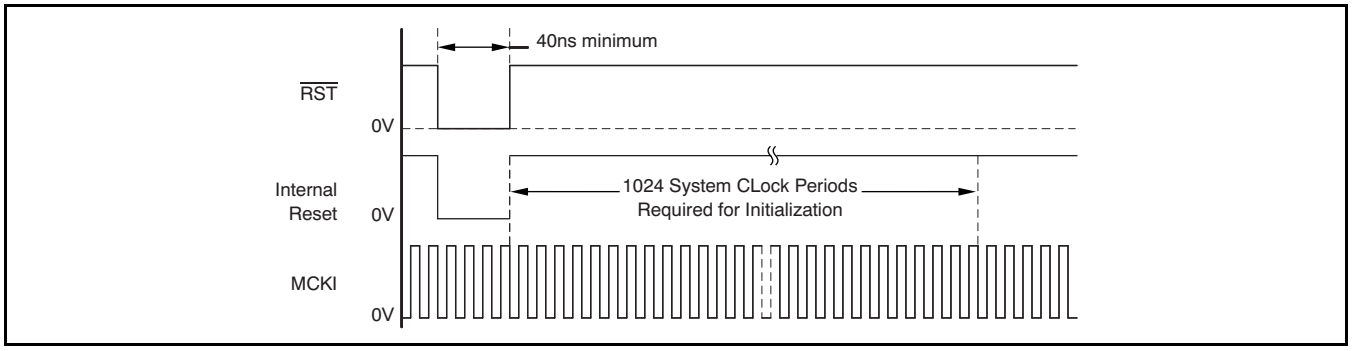


Figure 38. External Reset Sequence

DISABLED STATES FOR THE PCM4220 AUDIO SERIAL PORT

When PCMEN (pin 16) is driven low, the PCM output is disabled. The audio serial port data and clocks are driven low.

PCM OUTPUT AND SAMPLING MODES

The PCM4220 supports 24-bit linear PCM output data when the PCMEN input (pin 16) is forced high. The PCM output is disabled when PCMEN is forced low. The 24-bit output data may be dithered to 20-, 18-, or 16-bits using internal word length reduction circuitry. Refer to the *Output Word Length Reduction* section of this data sheet for additional information.

The PCM4220 supports three PCM sampling modes, referred to as Normal, Double Speed, and Quad Speed. The sampling mode is determined by the state of the FS0 and FS1 inputs (pins 19 and 20, respectively). Table 2 summarizes the sampling modes available for the PCM4220.

Normal sampling mode supports output sampling rates from 8kHz to 54kHz. The ΔΣ modulator operates with 128x oversampling in this mode. Both the Classic and Low Group Delay decimation filter responses are available in Normal mode. The master clock (MCKI) rate must be 256x the desired output sampling rate for Normal operation.

The Double Speed sampling mode supports output sampling rates from 54kHz to 108kHz. The delta-sigma modulator operates with 64x oversampling in this mode. Both the Classic and Low Group Delay decimation filter responses are available in Double Speed mode. The master clock (MCKI) rate must be 128x the desired output sampling rate for Double Speed operation.

Quad Speed sampling mode supports output sampling rates from 108kHz to 216kHz. The delta-sigma modulator operates with 32x oversampling in this mode. Only the Low Group Delay decimation filter response is available in Quad Speed mode. The master clock (MCKI) rate must be 64x the desired output sampling rate for Quad Speed operation.

Table 2. PCM Sampling Mode Configuration

FS1 (pin 20)	FS0 (pin 19)	SAMPLING MODE
LO	LO	Normal, 8kHz ≤ f_S ≤ 54kHz
LO	HI	Double Speed, 54kHz < f_S ≤ 108kHz
HI	LO	Quad Speed, 108kHz < f_S ≤ 216kHz
HI	HI	Reserved

AUDIO SERIAL PORT INTERFACE

The PCM output mode supports a three-wire synchronous serial interface. This interface includes a serial data output (DATA, pin 32), a serial bit or data clock (BCK, pin 33), and a left/right word clock (LRCK, pin 34). The BCK and LRCK clock pins may be inputs or outputs, depending on the Slave or Master mode configuration. Figure 39 illustrates Slave and Master mode serial port connections to an external audio signal processor or host device.

The audio serial port supports four data formats that are illustrated in Figure 40, Figure 42, and Figure 43. The I^2S and Left-Justified formats support two channels of audio output data. The TDM data formats can support up to eight channels of audio output data on a single data line. The audio data format is selected using the FMT0 and FMT1 inputs (pins 44 and 43, respectively). Table 3 summarizes the audio data format options. For all formats, audio data are represented as two's complement binary data, with the MSB transmitted first. Regardless of the format selection, audio data are always clocked out of the port on the falling edge of the BCK clock.

Table 3. PCM Audio Data Format Selection

FMT1 (pin 43)	FMT0 (pin 44)	AUDIO DATA FORMAT
LO	LO	Left-Justified
LO	HI	I^2S
HI	LO	TDM
HI	HI	TDM with data delayed one BCK cycle from LRCK rising edge

The LRCK clock rate should always be operated at the desired output sampling rate, or f_S. In Slave mode, the LRCK clock is an input, with the rate set by an external audio bus master (that is, a clock generator, digital signal processor, etc.). In Master mode, the LRCK clock is an output, derived from the master clock input using on-chip clock dividers (as is the BCK clock). The clock divider is configured using the FS0 and FS1 pins, which are discussed in the *PCM Output and Sampling Modes* section of this datasheet.

For the I^2S and Left-Justified data formats, the BCK clock output rate is fixed in Master mode, with the Normal mode being $128f_S$ and the Double and Quad Speed modes being $64f_S$. In Slave Mode, a BCK clock input rate of $64f_S$ or $128f_S$ is recommended for Normal mode, while $64f_S$ is recommended for Double and Quad Rate modes.

For the TDM data formats, the BCK rate depends upon the sampling mode for either Slave or Master operation. For Normal sampling, the BCK must be $256f_S$. Double Speed mode requires $128f_S$, while Quad Speed mode requires $64f_S$. This requirement limits the maximum number of channels carried by the TDM formats to eight for Normal mode, four for Double Rate mode, and two for Quad Rate mode.

When using the TDM formats, the sub-frame assignment for the device must be selected using the SUB0 and SUB1 inputs (pins 26 and 25, respectively). Table 4 summarizes the sub-frame selection options. A sub-frame contains two 32-bit time slots, with each time slot carrying 24 bits of audio data corresponding to either the left or right channel of the PCM4220. Refer to Figure 41 through Figure 43 for TDM interfacing connections and sub-frame formatting details. For the TDM format with one BCK delay, the serial data output is delayed by one BCK period after the rising edge of the LRCK clock.

Table 4. TDM Sub-frame Assignment

SUB1 (pin 25)	SUB0 (pin 26)	SUB-FRAME ASSIGNMENT
LO	LO	Sub-frame 0
LO	HI	Sub-frame 1
HI	LO	Sub-frame 2
HI	HI	Sub-frame 3

When using TDM formats with Double Speed sampling, it is recommended that the SUB1 pin be forced low. When using TDM formats with Quad Speed sampling, it is recommended that both the SUB0 and SUB1 pins be forced low.

For all serial port modes and data formats, when driving capacitive loads greater than 30pF with the data and clock outputs, it is recommended that external buffers be utilized to ensure data and clock integrity at the receiving device(s).

For specifications regarding audio serial port operation, the reader is referred to the Electrical Characteristics: Audio Interface Timing table, as well as Figure 1 and Figure 2 in this data sheet.

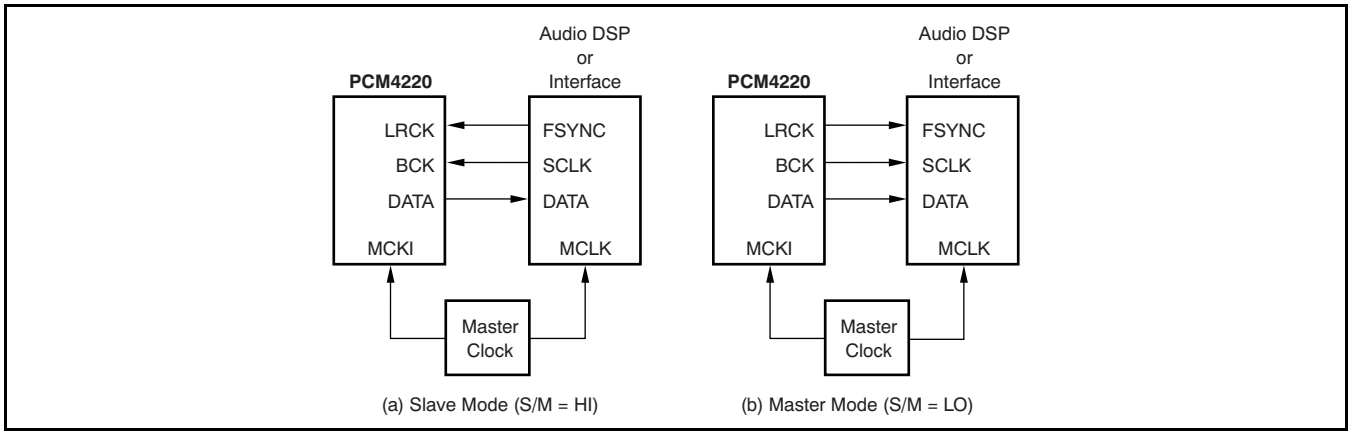


Figure 39. Slave and Master Mode Operation

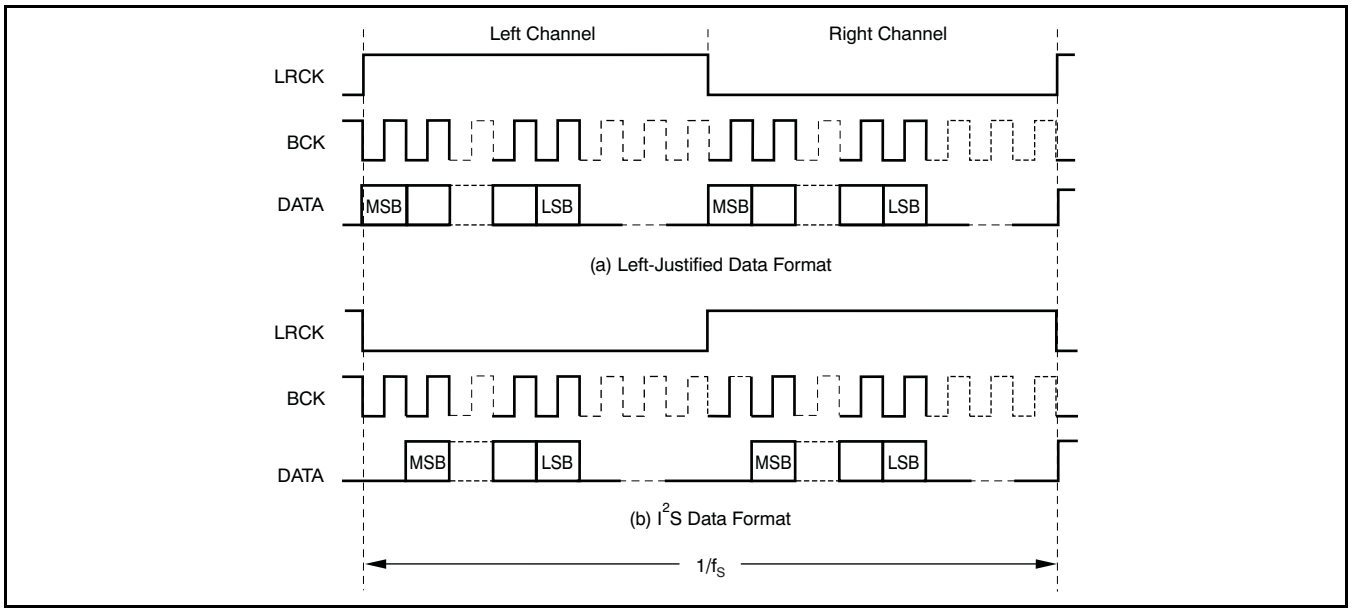


Figure 40. Left-Justified and I²S Data Formats

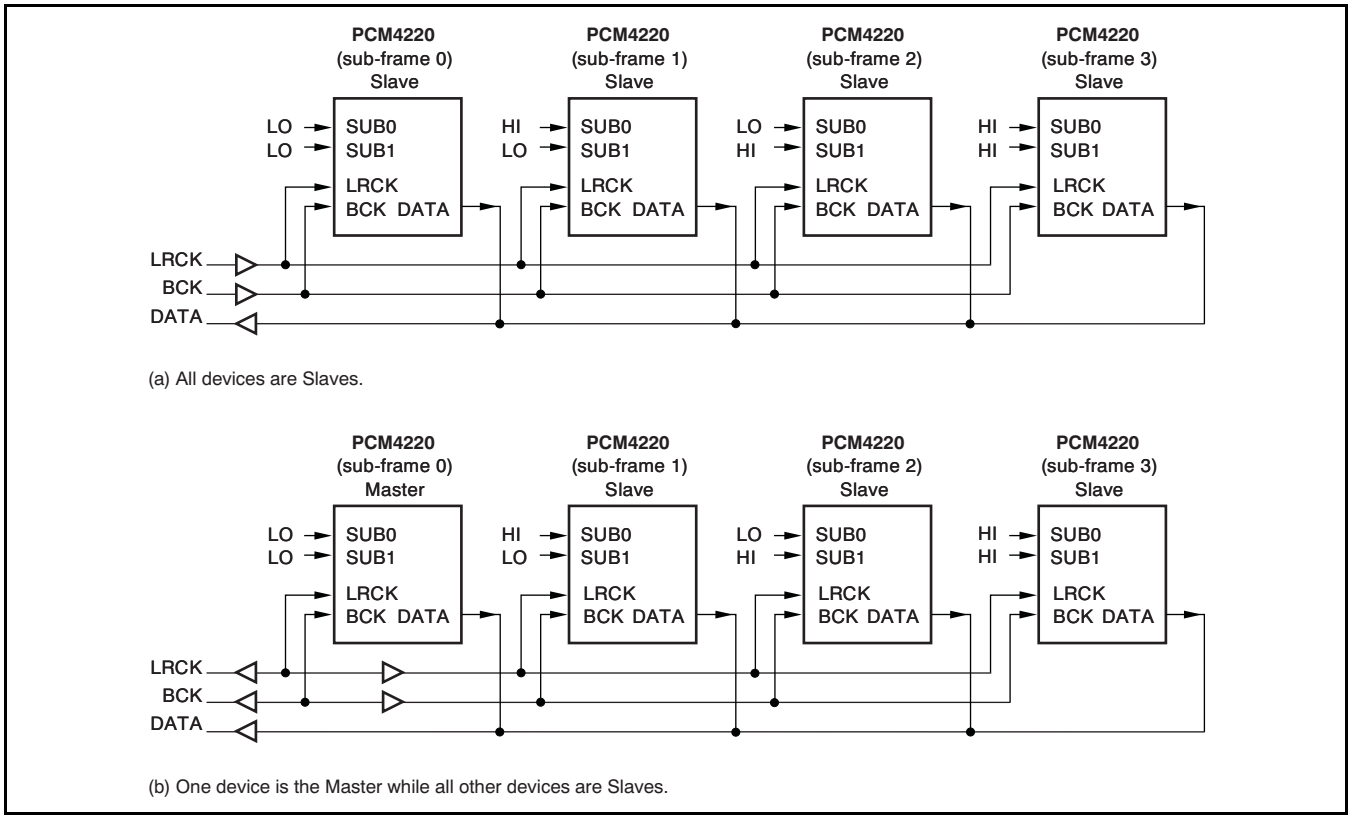
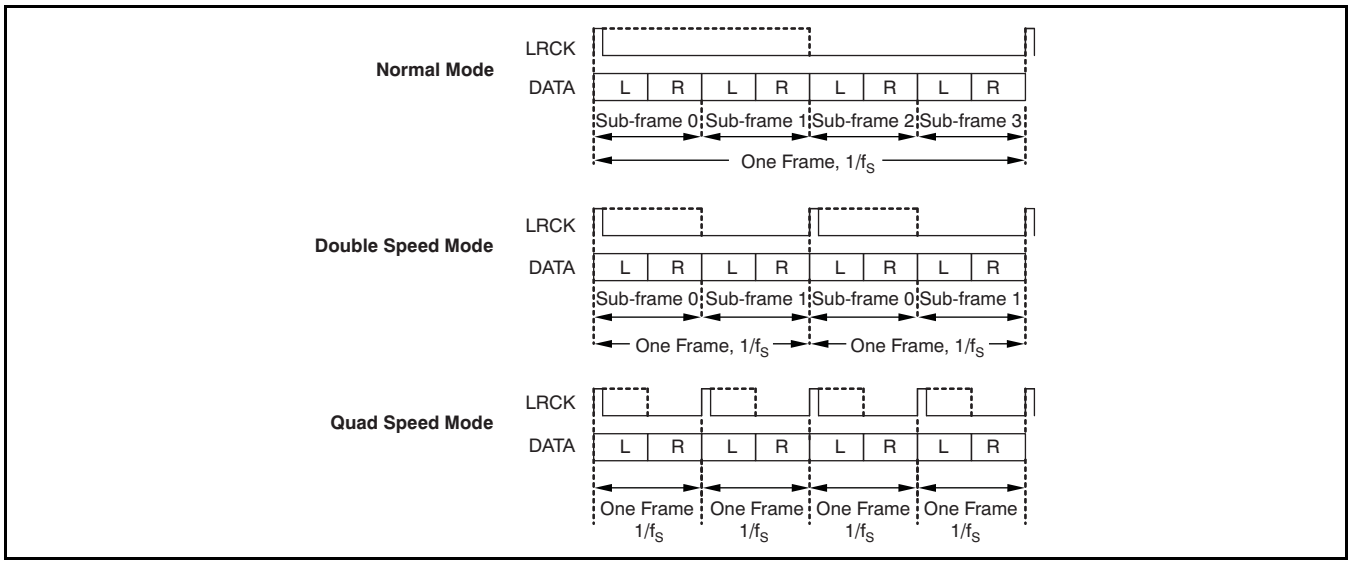
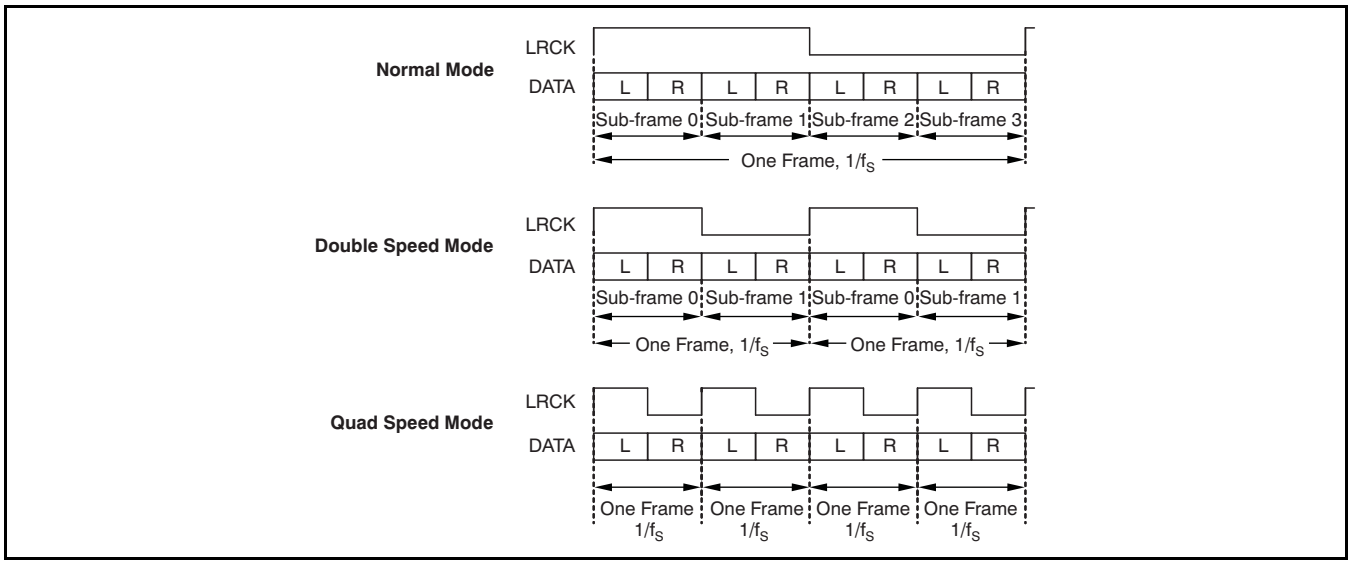


Figure 41. TDM Mode Interface Connections (PCM Normal Mode Shown)



NOTE: Each L or R channel time slot is 32 bits long, with 24-bit data Left-Justified in the time slot. Audio data is MSB first. Sub-frame assignments for each PCM4220 device are selected by the corresponding SUB0 and SUB1 pin settings.

Figure 42. TDM Data Formats: Slave Mode



NOTE: Each L or R channel time slot is 32 bits long, with 24-bit data Left-Justified in the time slot. Audio data is MSB first. Sub-frame assignments for each PCM4220 device are selected by the corresponding SUB0 and SUB1 pin settings.

Figure 43. TDM Data Formats: Master Mode

DIGITAL DECIMATION FILTER

The PCM4220 digital decimation filter is a linear phase, multistage finite impulse response (FIR) design with two user-selectable filter responses. The decimation filter provides the digital downsampling and low-pass anti-alias filter functions for the PCM4220.

The Classic filter response is typical of traditional audio data converters, with Figure 24 through Figure 27 detailing the frequency response, and the related specifications given in the Electrical Characteristics table. The group delay for the Classic filter is $39/f_S$, or 812.5µs for f_S = 48kHz and 406.25µs for f_S = 96kHz. The Classic filter response is not available for the Quad Speed sampling mode.

The Low Group Delay response provides a lower latency option for the decimation filter, and is detailed in Figure 28 through Figure 31, with the relevant specifications given in the Electrical Characteristics table. The Low Group Delay filter response is available for all sampling modes. The group delay for this filter is $21/f_S$, or 437.5µs for f_S = 48kHz, 218.75µs for f_S = 96kHz, and 109.375µs for f_S = 192kHz.

The decimation filter response is selected using the DF input (pin 21), with the settings summarized in Table 5. For Quad Speed sampling mode operation, the Low Group Delay filter is always selected, regardless of the DF pin setting.

Table 5. Decimation Filter Response Selection

DF (pin 21)	DECIMATION FILTER RESPONSE
LO	Classic response, with group delay = $39/f_S$
HI	Low Group Delay response, with group delay = $21/f_S$

DIGITAL HIGH-PASS FILTER

The PCM4220 incorporates digital high-pass filters for both the left and right audio channels, with the purpose of removing the ΔΣ modulator dc offset from the audio output data. Figure 32 and Figure 33 detail the frequency response for the digital high-pass filter. The f_{-3dB} frequency is approximately $f_S/48000$, where f_S is the PCM output sampling rate.

Two inputs, HPFDR (pin 17) and HPFDL (pin 18), allow the digital high-pass filter to be enabled or disabled individually for the right and left channels, respectively. Table 6 summarizes the operation of the high-pass filter disable pins.

Table 6. Digital High-Pass Filter Configuration

HPFDR (pin 17) or HPFDL (pin 18)	HIGH-PASS FILTER STATE
LO	Enabled for the corresponding channel
HI	Disabled for the corresponding channel

PCM OUTPUT WORD LENGTH REDUCTION

The PCM4220 is typically configured to output 24-bit linear PCM audio data. However, internal word length reduction circuitry may be utilized to reduce the 24-bit data to 20-, 18-, or 16-bit data. This reduction is accomplished by using a Triangular PDF dithering function. The OWL0 (pin 42) and OWL1 (pin 41) inputs are utilized to select the output data word length. Table 7 summarizes the output word length configuration options.

Table 7. PCM Audio Data Word Length Selection

OWL1 (pin 41)	OWL0 (pin 42)	OUTPUT WORD LENGTH
LO	LO	24 bits
LO	HI	18 bits
HI	LO	20 bits
HI	HI	16 bits

OVERFLOW INDICATORS

The PCM4220 includes two active-high digital overflow outputs, OVFL (pin 37) and OVFR (pin 38), corresponding to the left and right channels, respectively. These outputs are functional when the PCM output mode is enabled, as the overflow detection circuitry is incorporated into the digital filter engine. The overflow indicators are forced high whenever a digital overflow is detected for a given channel. The overflow indicators may be utilized as clipping flags, and monitored using a host processor or light-emitting diode (LED) indicators. When driving a LED, the overflow output may be buffered to ensure adequate drive for the LED. A recommended buffer is Texas Instruments' SN74LVC1G125. Equivalent buffers may be substituted

TYPICAL CONNECTIONS

Figure 44 provides a typical connection diagram for the PCM4220. Recommended power-supply bypass and reference filter capacitors are shown. These components should be located as close to the corresponding PCM4220 package pins as physically possible. Larger power-supply bypass capacitors may be placed on the bottom side of the printed circuit board (PCB). However, reference decoupling capacitors should be located on the top side of the PCB to avoid issues with added via inductance.

As Figure 44 illustrates, the audio host device may be a digital signal processor (DSP), digital audio interface transmitter (DIT), or a programmable logic device.

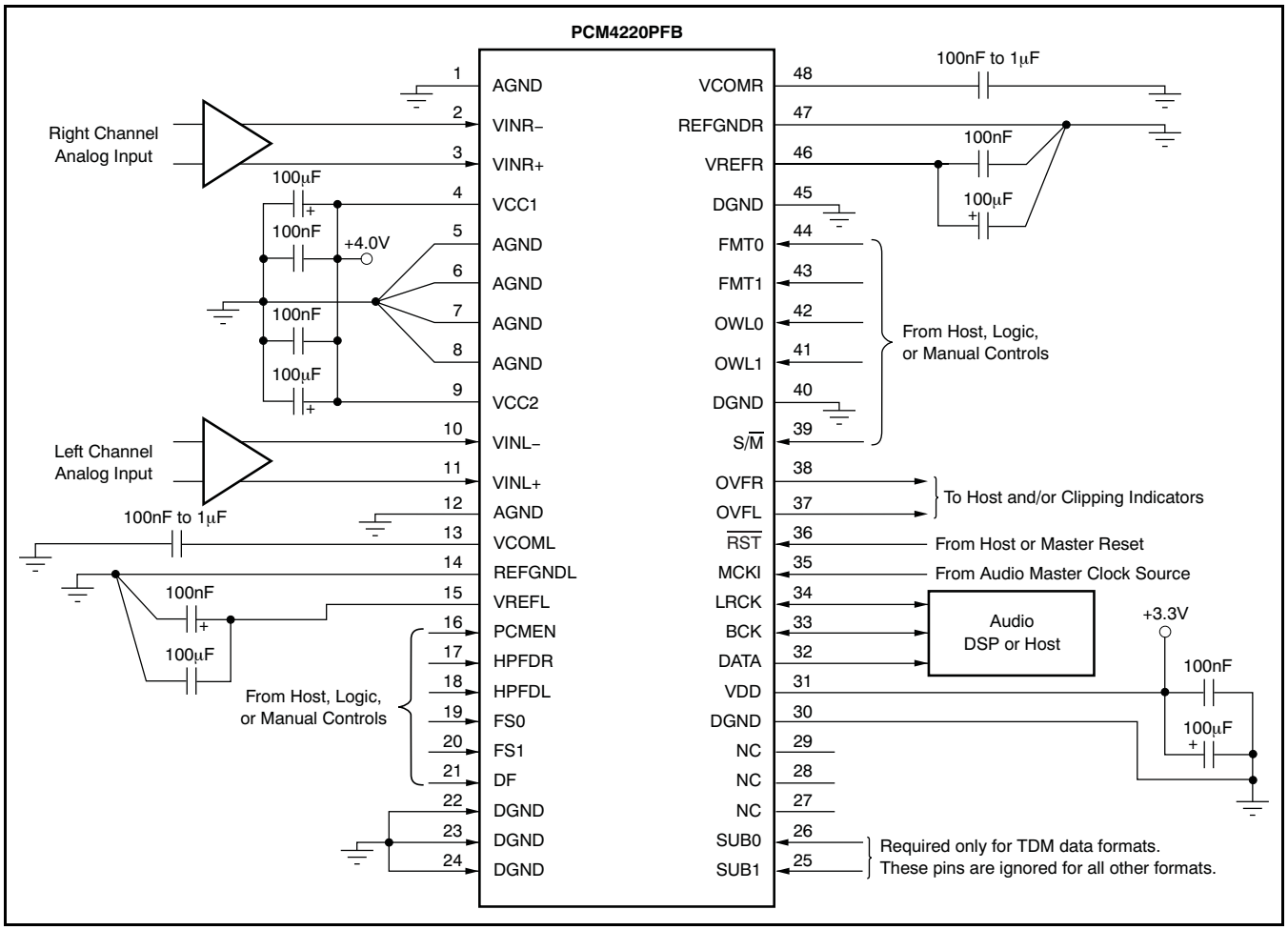


Figure 44. Typical Connections for PCM and DSD Output Modes

INPUT BUFFER CIRCUITS

The PCM4220 is typically preceded in an application by an input buffer or preamplifier circuit. The input circuit is required to perform anti-aliasing filtering, in addition to application-specific analog gain scaling, limiting, or processing that may be needed. At a minimum, first-order, low-pass anti-aliasing filtering is necessary. The input buffer must be able to perform the input filtering requirement, in addition to driving the switched-capacitor inputs of the PCM4220 device. The buffer must have adequate bandwidth, slew rate, settling time, and output drive capability to perform these tasks.

Figure 45 illustrates the input buffer/filter circuit utilized on the PCM4222EVM evaluation module, where the PCM4222 analog input section is identical to the PCM4220. This circuit has been optimized for measurement purposes, so that it does not degrade the dynamic characteristics of the PCM4220. The resistors are primarily 0.1% metal film. The 40.2Ω resistor is 1% tolerance thick film. The 1nF and 2.7nF capacitors may be either PPS

film or C0G ceramic capacitors; both types perform with equivalent results in this application. Surface-mount devices are utilized throughout because they provide superior performance when combined with a wideband amplifier such as the OPA1632. The DGN package version of the OPA1632 is utilized; this package includes a thermal pad on the bottom side. The thermal pad must be soldered to the PCB ground plane for heat sink and mechanical support purposes.

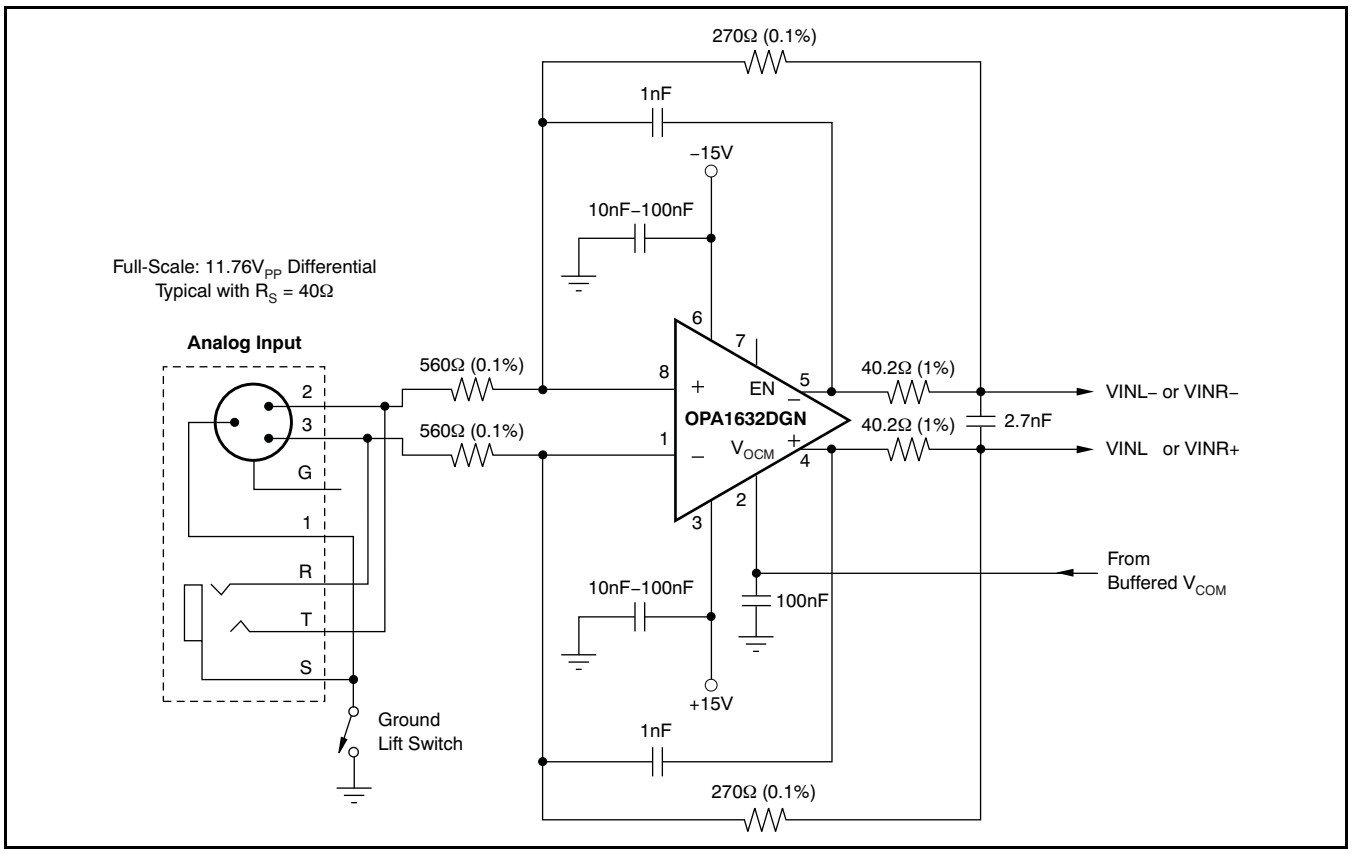
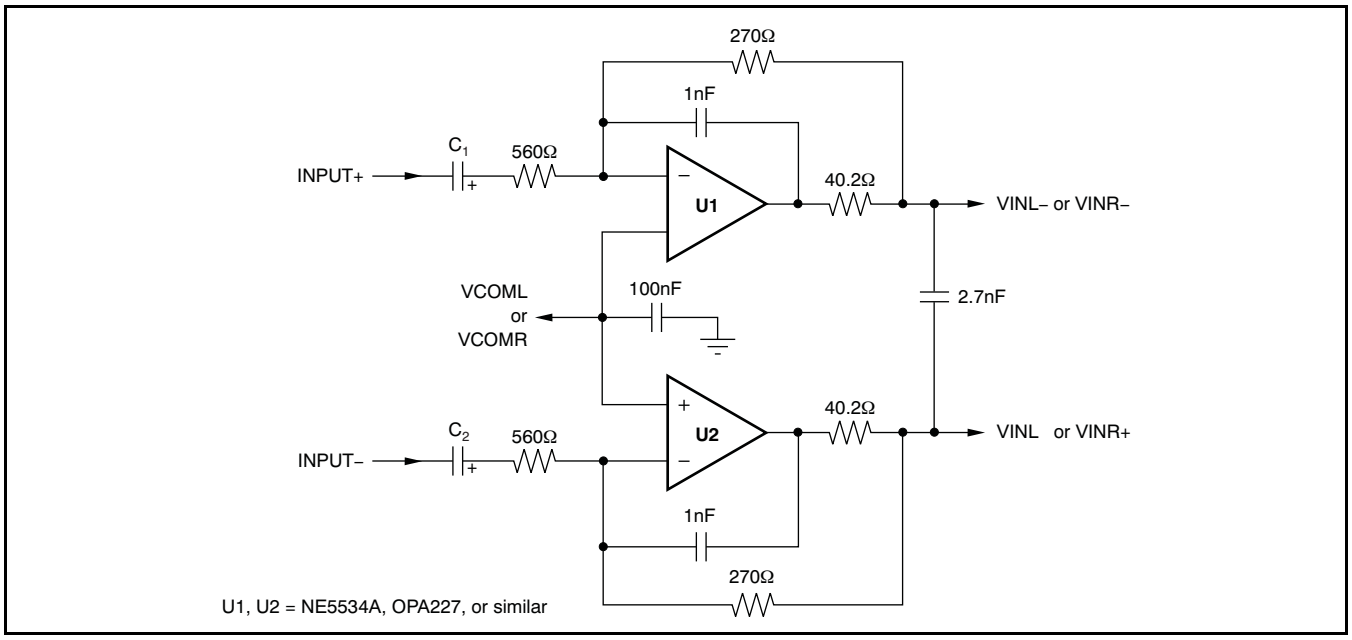


Figure 45. Differential Input Buffer Circuit Utilizing the OPA1632

Figure 46 demonstrates the same circuit topology of Figure 45, while using standard single or dual op amps. The noise level of this circuit is adequate for obtaining the typical A-weighted dynamic range performance for the PCM4220. However, unweighted performance may suffer, depending upon the op amp noise specifications. Near-typical THD+N can be achieved with this configuration, although this performance also depends on the op amps used for the application. The NE5534A and OPA227 (the lower cost 'A' version) are good candidates from a noise and distortion perspective, and are reasonably priced. More expensive lower-noise models, such as the OPA211, should also work well for this configuration. Feedback and input resistor values may be changed to alter circuit gain. However, it is recommended that all circuit changes be simulated and then tested on the bench using a working prototype to verify performance.

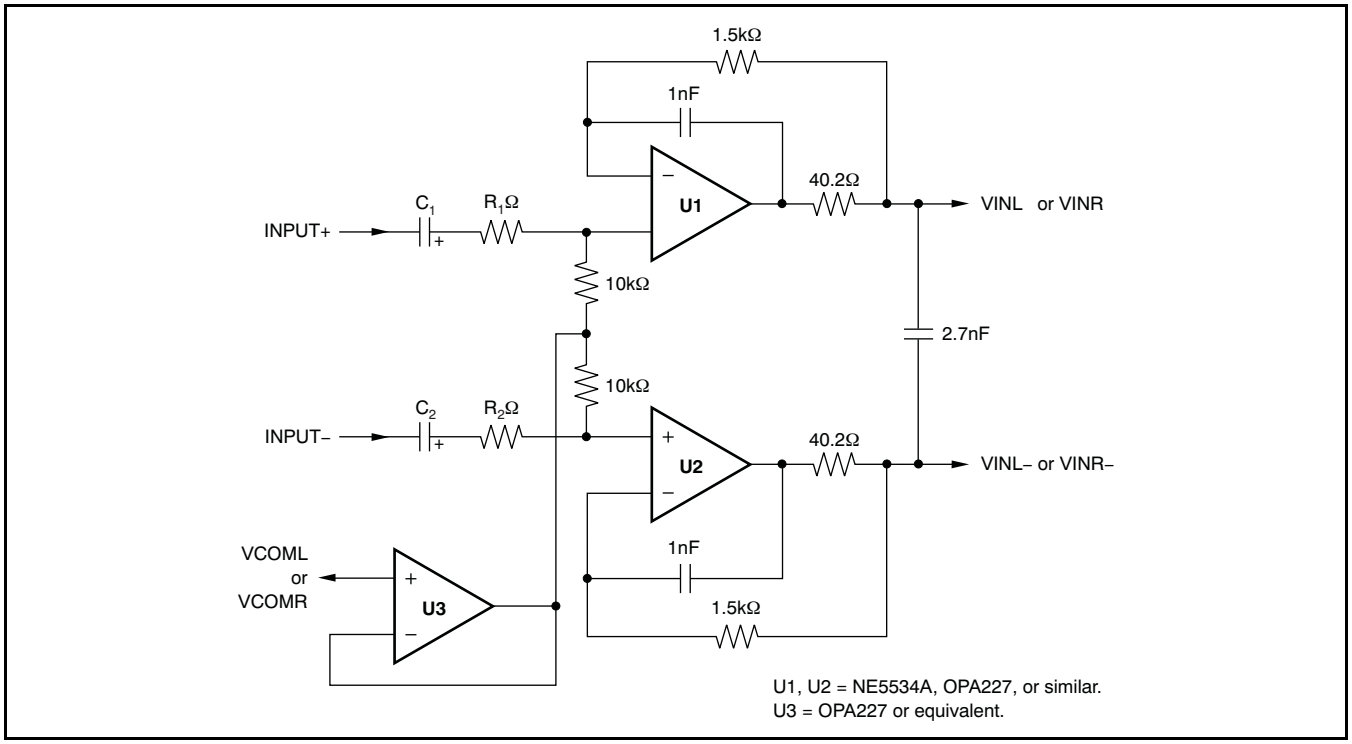
Figure 47 illustrates a differential input circuit that employs a noninverting architecture. The total noise and distortion is expected to be higher than that measured for Figure 45 and Figure 46. As with Figure 46, the NE5534A and OPA227 are good candidates for this circuit, although similar op amps should yield equivalent results.

A useful tool for simulating the circuits shown here is TINA-TI, a free schematic capture and SPICE-based simulator program available from the Texas Instruments web site. This tool includes macro models for many TI and Burr-Brown branded amplifiers and analog integrated circuits. TINA-TI runs on personal computers using Microsoft Windows® operating systems (Windows 2000 or newer).



NOTE: C_1 and C_2 provide ac coupling. They may be removed if the dc offset from the circuit is negligible.

Figure 46. Alternative Buffer Circuit Using Standard Op Amps



NOTE: R_1 and R_2 are optional. When used, values may be selected for the desired attenuation.

NOTE: C_1 and C_2 provide ac coupling. They may be removed if the dc offset from the circuit is negligible.

Figure 47. Noninverting Differential Input Buffer Utilizing Standard Op Amps

INTERFACING TO DIGITAL AUDIO TRANSMITTERS (AES3, IEC60958-3, and S/PDIF)

The serial output of audio analog-to-digital converters is oftentimes interfaced to transmitter devices that encode the serial output data to either the AES3 or IEC60958-3 (or S/PDIF) interface formats. Texas Instruments manufactures several devices that perform this encoding, including the DIT4192, DIX4192, SRC4382, and SRC4392. This section describes and illustrates the audio serial port interface connections required for communications between the PCM4220 and these devices. Register programming details for the DIX4192 and SRC4382/4392 are also provided.

Figure 48 shows the interface between a PCM4220 and a DIT4192 transmitter. This configuration supports sampling frequencies and encoded frame rates from 8kHz to 216kHz. For this example, the audio data format must be either Left-Justified or I^2S; TDM formats are not supported by the DIT4192. In addition, the PCM4220 VDD supply and DIT4192 VIO supply must be the same voltage, to ensure logic level compatibility.

Figure 49 illustrates the audio serial port interface between the PCM4220 and either a DIX4192 transceiver or SRC4382/SRC4392 combo sample rate converter/transceiver device. Port A of the DIX4192 or SRC4382/SRC4392 is utilized for this example. Data acquired by Port A are sent on to the DIT function block within the interface device for AES3 encoding and transmission.

The DIX4192 and SRC4382/SRC4392 are software-configurable, with control register and data buffer settings that determine the operation of internal function blocks. Table 8 and Table 9 summarize the control register settings for the Port A and the DIT function blocks for both A/D Converter Master and Slave modes, respectively. Input sampling and encoded frame rates from 8kHz to 216kHz are supported with the appropriate register settings.

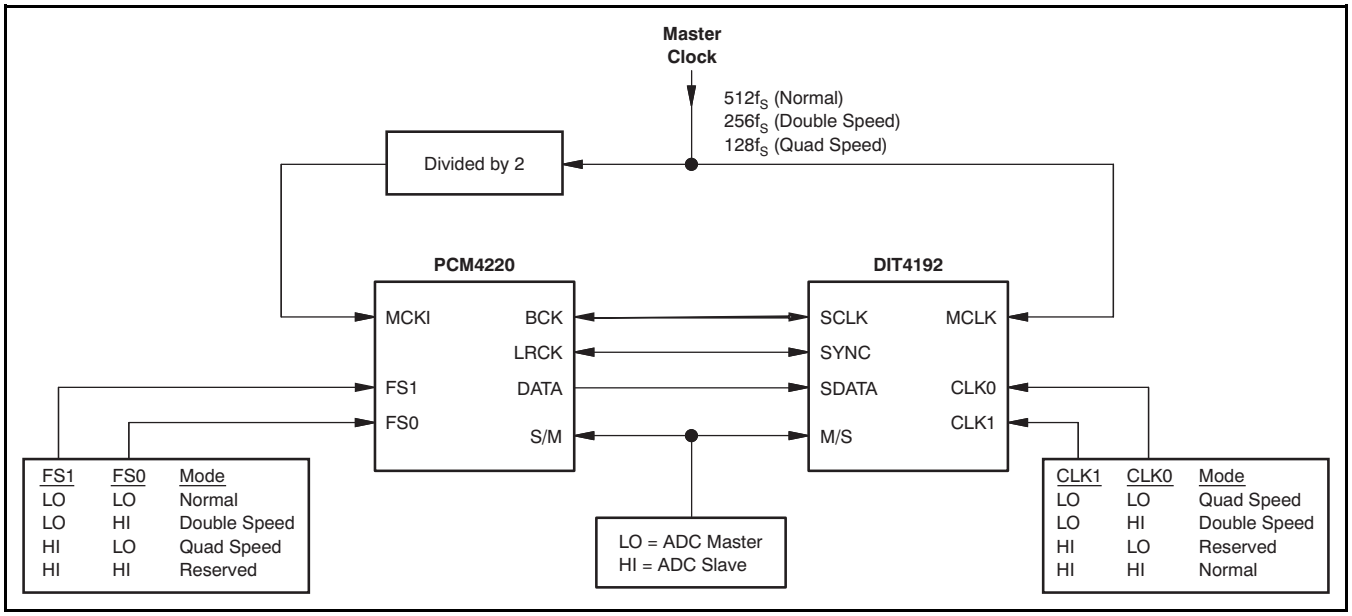
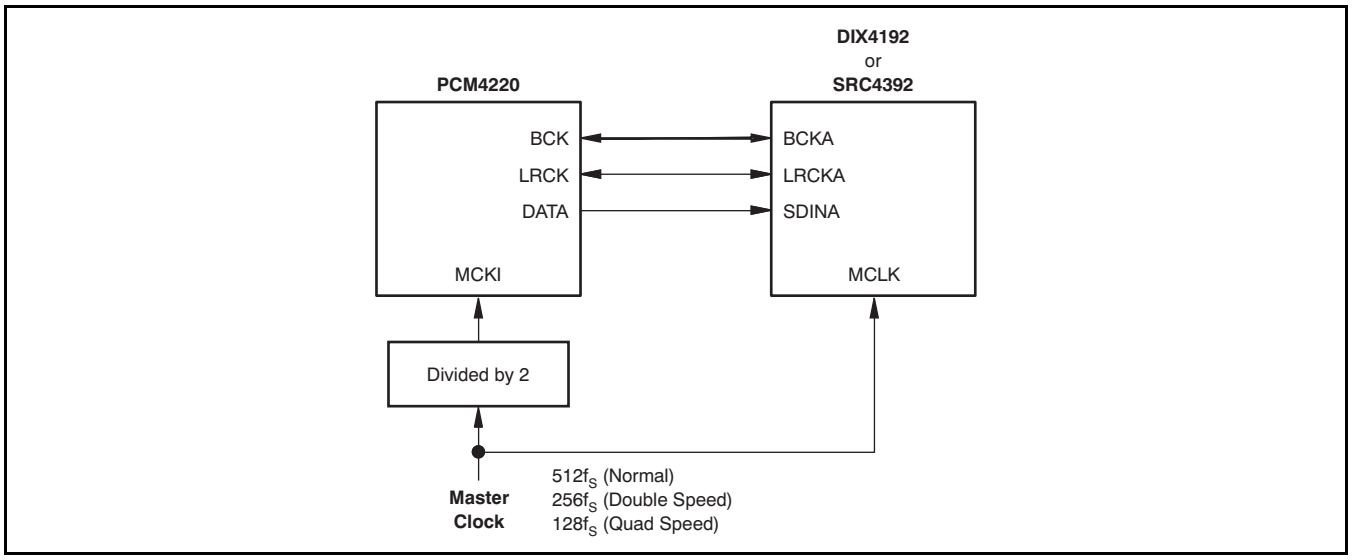


Figure 48. Interfacing the PCM4220 to a DIT4192



NOTE: VDDPCM4220 = VIODIX4192 or SRC4392.

Audio data format if I^2S or Left Justified.

Interface supports ADC Slave or Master configurations, depending on DIX4192, SRC4382, or SRC4392 register setup.

Figure 49. Interfacing the PCM4220 to a DIX4192, SRC4382, or SRC4392

Table 8. Register Configuration Sequence for an ADC Master Mode Interface

REGISTER ADDRESS (hex)	REGISTER DATA (hex)	COMMENTS
7F	00	Select Register Page 0
03	00 01	Port A is Slave mode with Left-Justified audio data format, or Port A is Slave mode with I^2S Data format
04	00	Default for Port A Slave mode operation
07	64 24 04	Divide MCLK by 512 for Normal sampling, or Divide MCLK by 256 for Double Speed Sampling, or Divide MCLK by 128 for Quad Speed sampling
08	00	Line Driver and AESOUT buffer enabled
09	01	Data buffers on Register Page 2 are the source for the DIT channel status (C) and user (U) data
01	34	Power up Port A and the DIT

Table 9. Register Configuration Sequence for an ADC Slave Mode Interface

REGISTER ADDRESS (hex)	REGISTER DATA (hex)	COMMENTS
7F	00	Select Register Page 0
03	08 09	Port A is Master mode with Left-Justified audio data format, or Port A is Master mode with I^2S Data format
04	03 01 00	Divide MCLK by 512 for Normal sampling, or Divide MCLK by 256 for Double Speed sampling, or Divide MCLK by 128 for Quad Speed sampling
07	64 24 04	Divide MCLK by 512 for Normal sampling, or Divide MCLK by 256 for Double Speed Sampling, or Divide MCLK by 128 for Quad Speed sampling
08	00	Line Driver and AESOUT buffer enabled
09	01	Data buffers on Register Page 2 are the source for the DIT channel status (C) and user (U) data
01	34	Power up Port A and the DIT

The DIT channel status (C) and user (U) data bits in register page 2 may be programmed after the DIT block has powered up. To program these bits, disable buffer transfers by setting the BTD bit in control register 0x08 to '1'. Then, select register page 2 using register address 0x7F. You can now load the necessary C and U data registers for the intended application by writing the corresponding data buffer addresses. When you have finished writing the C and U data, select register page 0 using register address 0x7F. Re-enable buffer transfers by setting the BTD bit in control register 0x08 to '0'.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2007) to Revision C **Page**

- Corrected statement concerning direction to drive PCMEN (pin 16) to disable PCM output 18

Changes from Revision A (May 2007) to Revision B **Page**

- Changed Figure 26 y-axis value from (dB) to (db/10,000) 12
- Changed Figure 30 y-axis value from (dB) to (db/1000) 13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM4220PFB	ACTIVE	TQFP	PFB	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	PCM4220	Samples
PCM4220PFBR	ACTIVE	TQFP	PFB	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	PCM4220	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

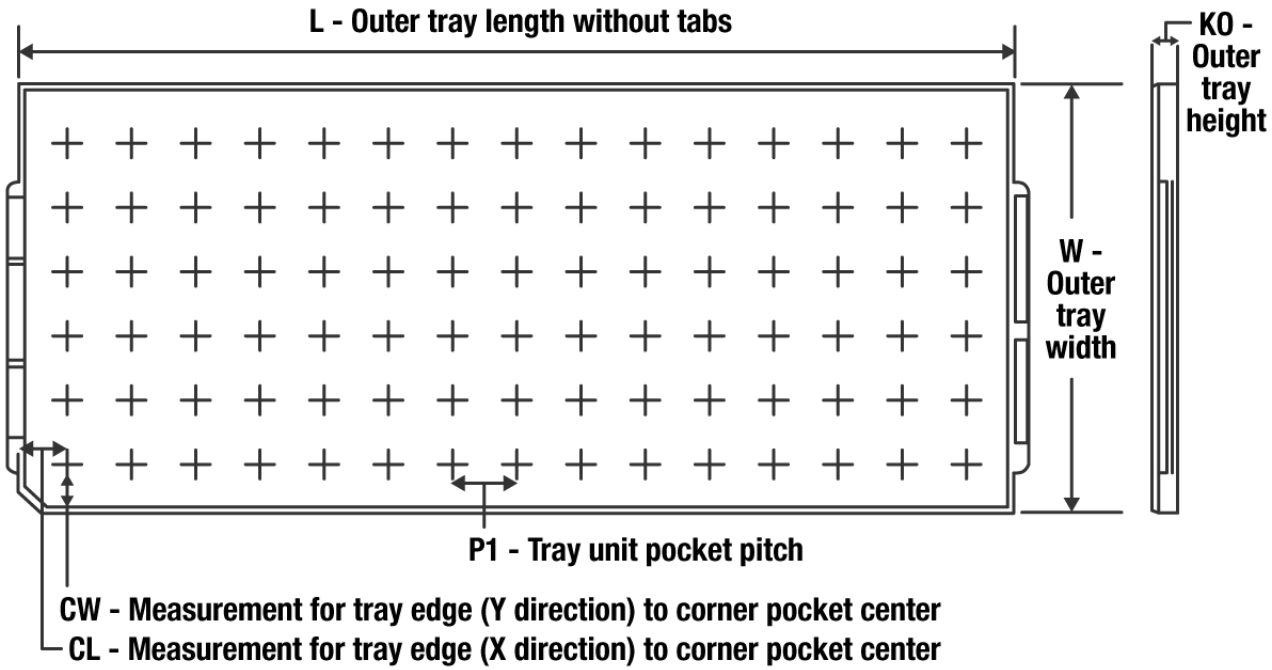
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY



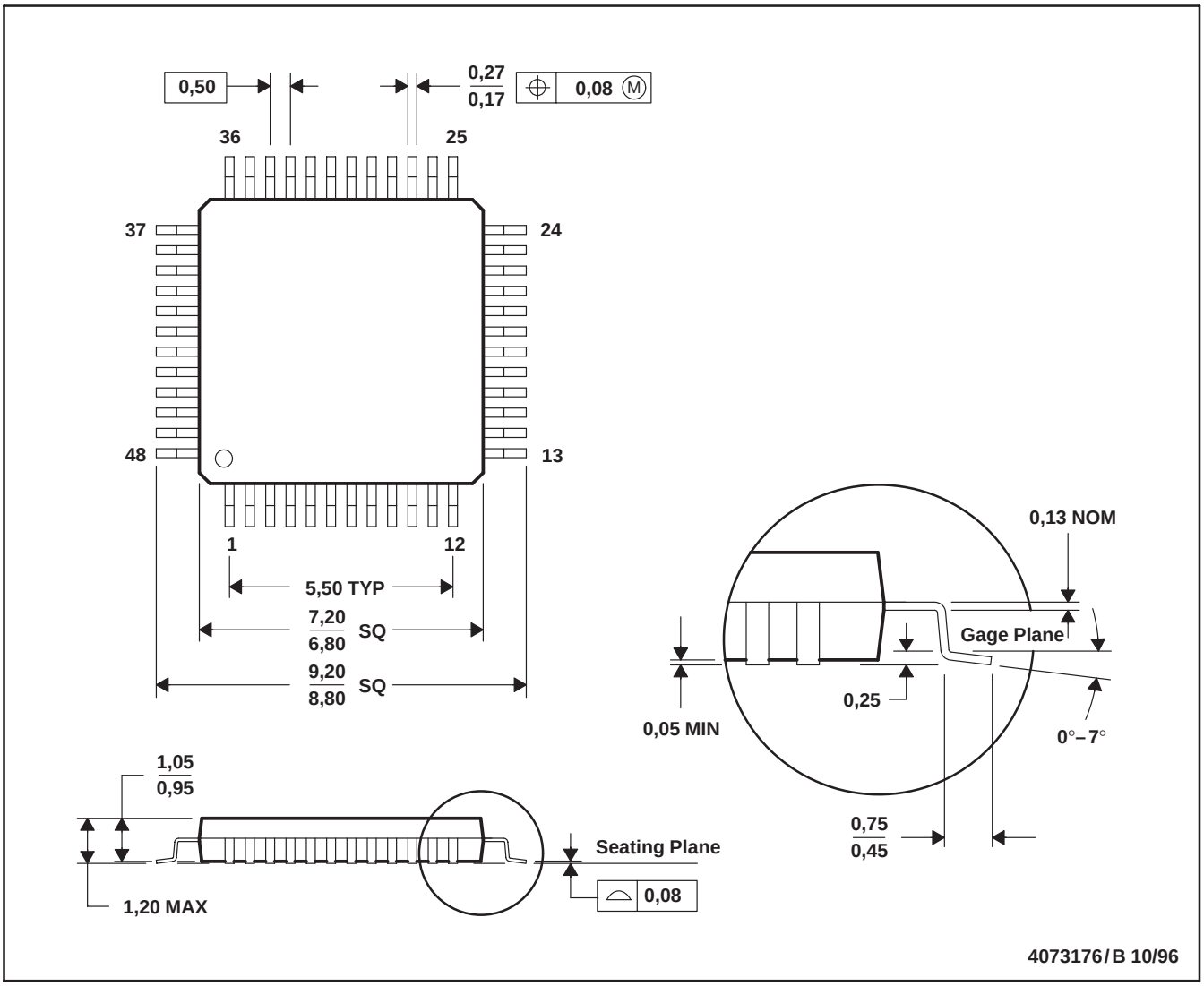
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
PCM4220PFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

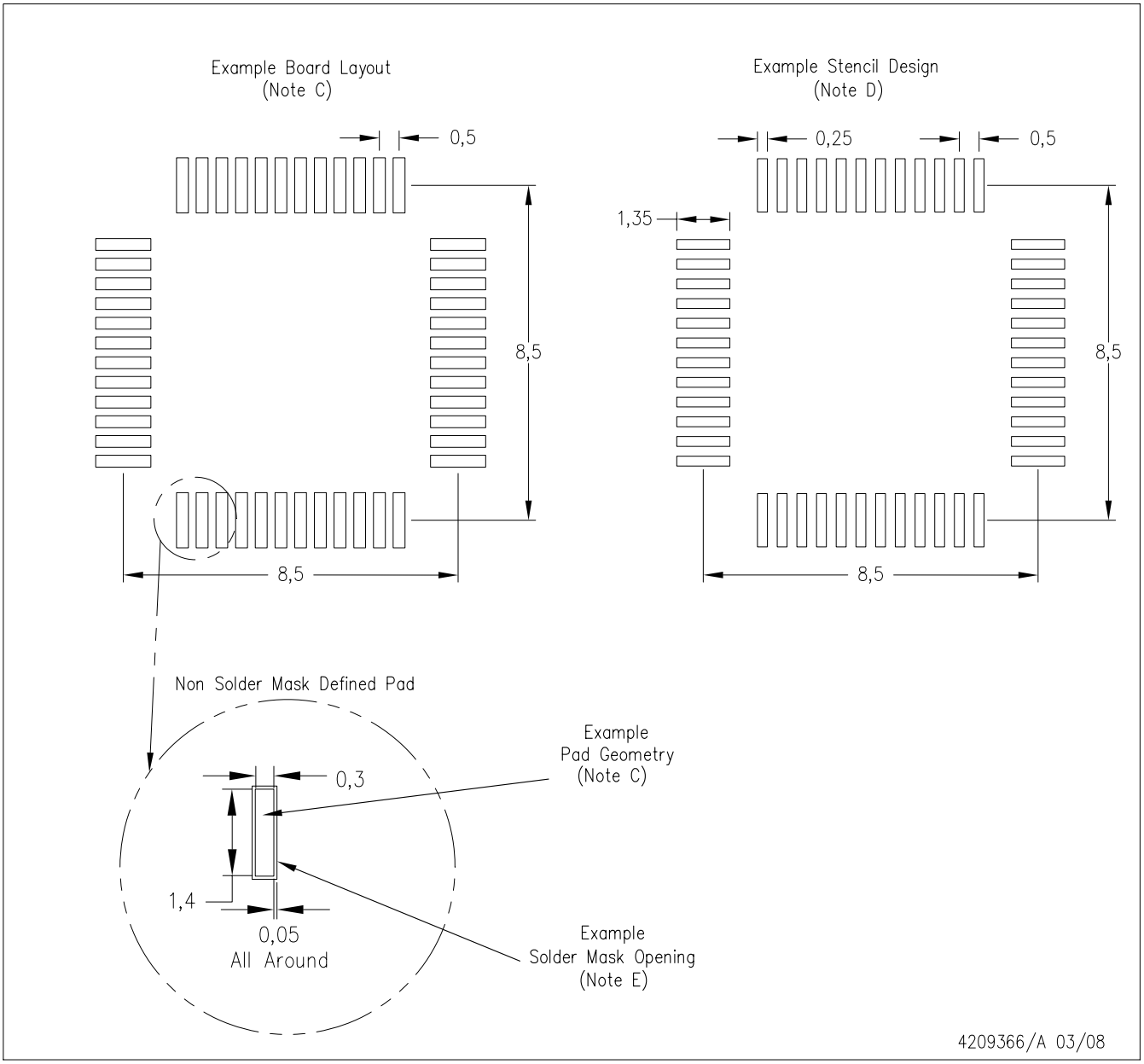
MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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