

U_B12	BI2.SchDoc
U_B13	BI3.SchDoc
U_B14	BI4.SchDoc
U_B15	BI5.SchDoc
U_B16	BI6.SchDoc
U_B34	B34.SchDoc

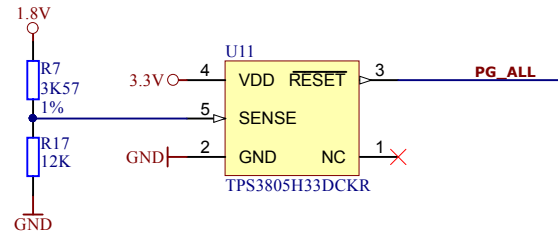
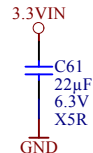
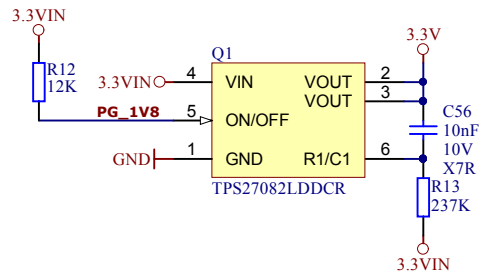
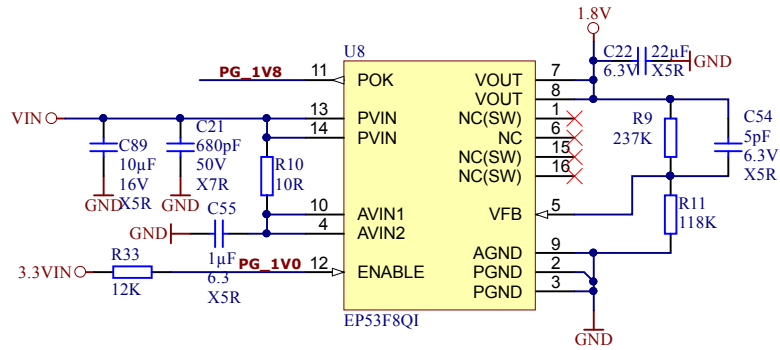
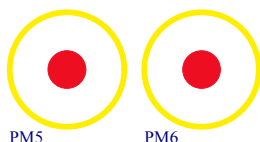
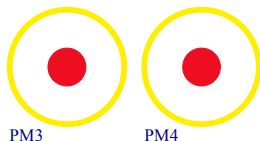
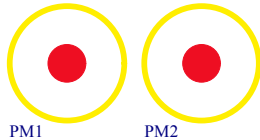
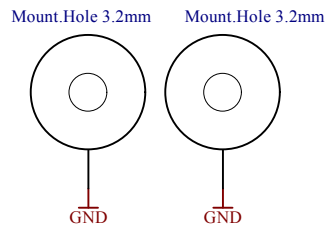
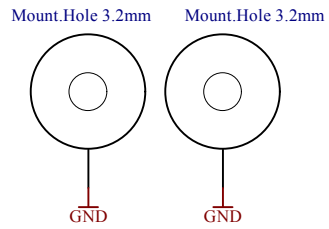
U_FPGA-MGT	FPGA-MGT.SchDoc
U_FPGA-CFG	FPGA-CFG.SchDoc
U_FPGA-MISC	FPGA-MISC.SchDoc
U_FPGA-PWR	FPGA-PWR.SchDoc

U_PWR1	PWR1.SchDoc
U_PWR2	PWR2.SchDoc

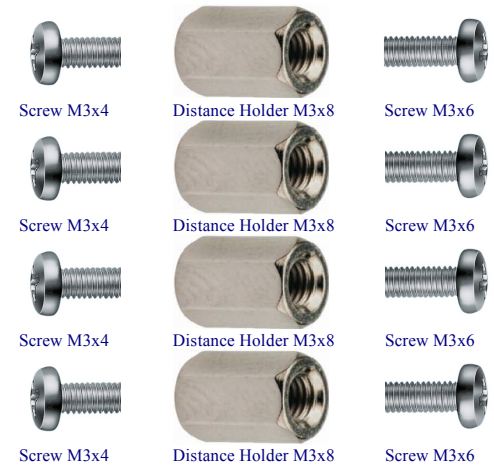
U_Clock	Clock.SchDoc
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U_B2B-Connectors	B2B-Connectors.SchDoc
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U_B33	B33.SchDoc
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Top of Board

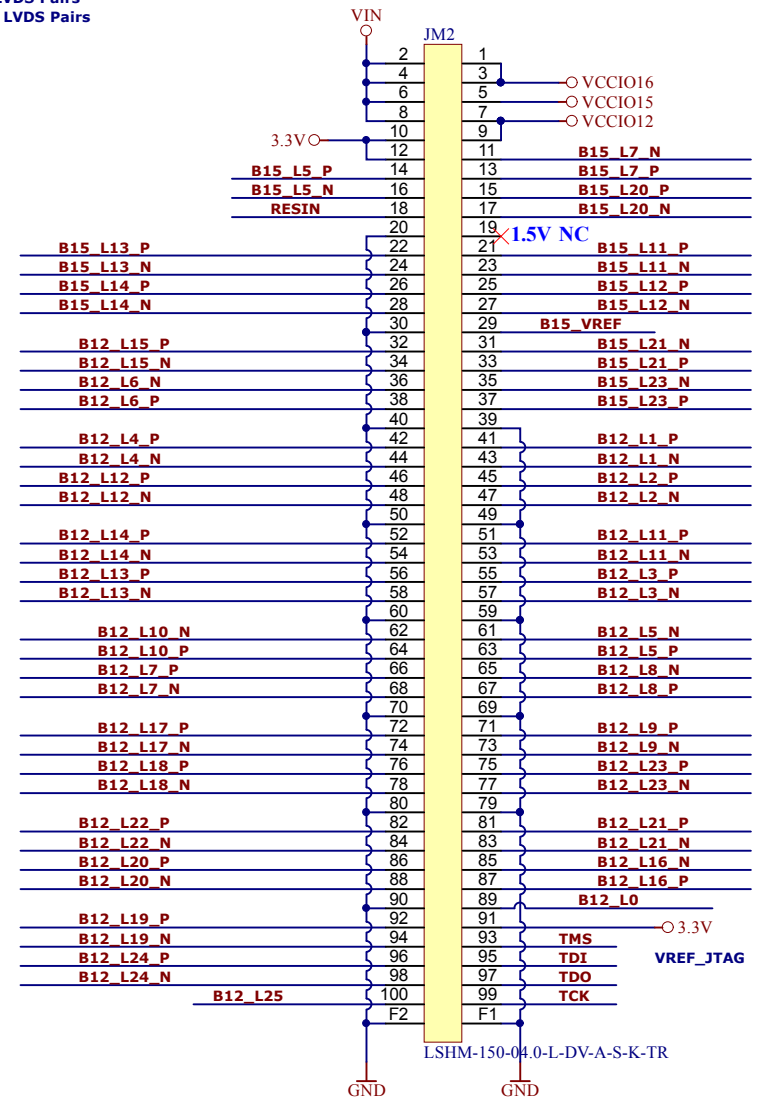
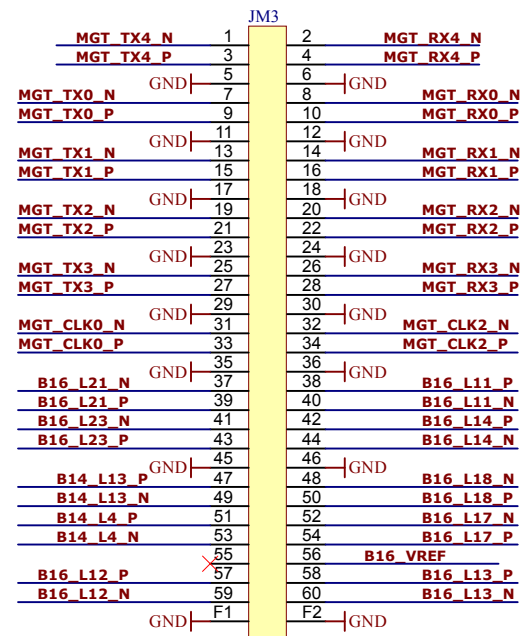
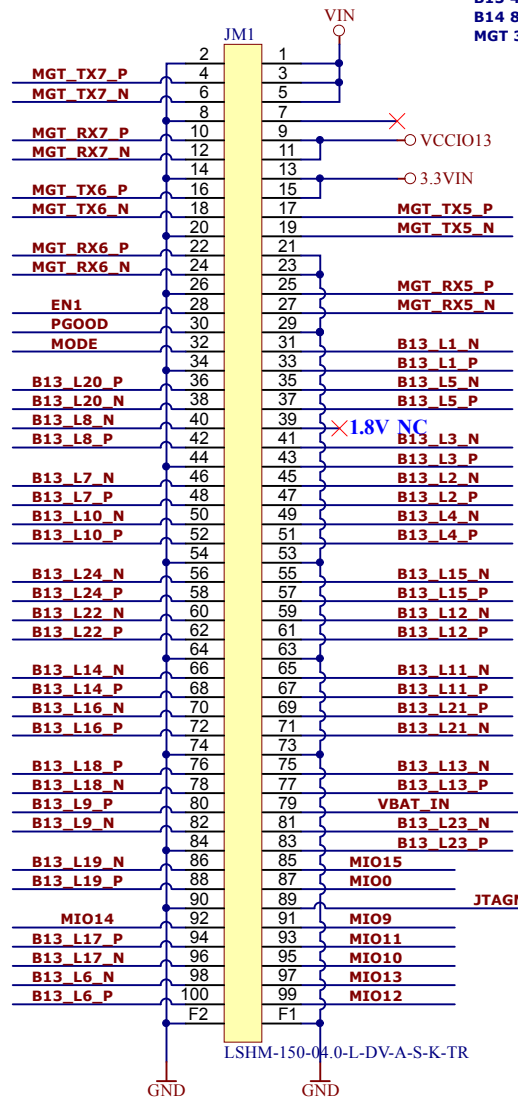


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B13 48 IO, 24 LVDS Pairs
B14 8 IO, 3.3V
MGT 3 Lanes

B16 16 IO, 8 LVDS Pairs
MGT 4 + 1 Lanes
B14 4 IO, 3.3V

B15 18 IO, 9 LVDS Pairs
B12 48 IO, 24 LVDS Pairs
B12 2 IO



TE0720 Compatibility
MIO0 8 pins => 8 IO B14
USB D+,D-, vbusen,otg_id => 4 IO B14
SGMII => MGT
MIO1(SDCARD) => MGT
ETH MD1 => MGT
B34 => B16, MGT
B35 => B13
B13 => B12
B33 => B15

Clock Capable I/O
All pins named
Bxx_H_X
Bxx_I_X
Bxx_O_X
Bxx_T_X
Bxx_C_X
Bxx_D_X
Bxx_E_X
Bxx_F_X
Bxx_G_X
Bxx_H_X
Bxx_I_X
Bxx_J_X
Bxx_K_X
Bxx_L_X
Bxx_M_X
Bxx_N_X
Bxx_O_X
Bxx_P_X
Bxx_Q_X
Bxx_R_X
Bxx_S_X
Bxx_T_X
Bxx_U_X
Bxx_V_X
Bxx_W_X
Bxx_X_X
Bxx_Y_X
Bxx_Z_X
Are Clock Capable I/O's

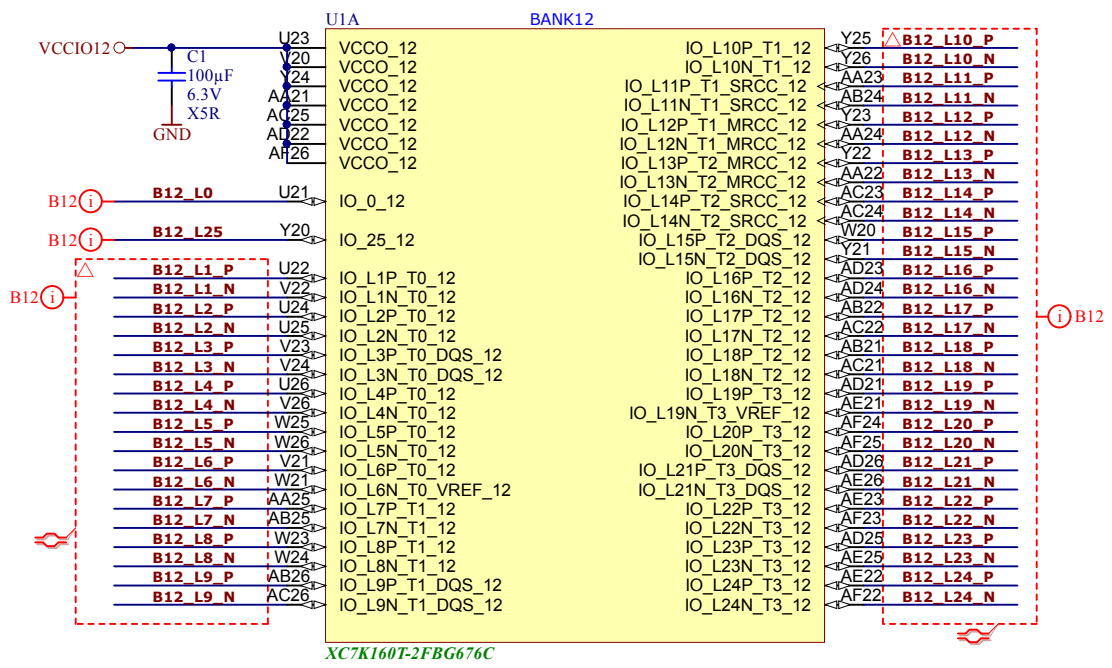


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Filename: B2B-Connectors.SchDoc		

B12_FIXED (i) △

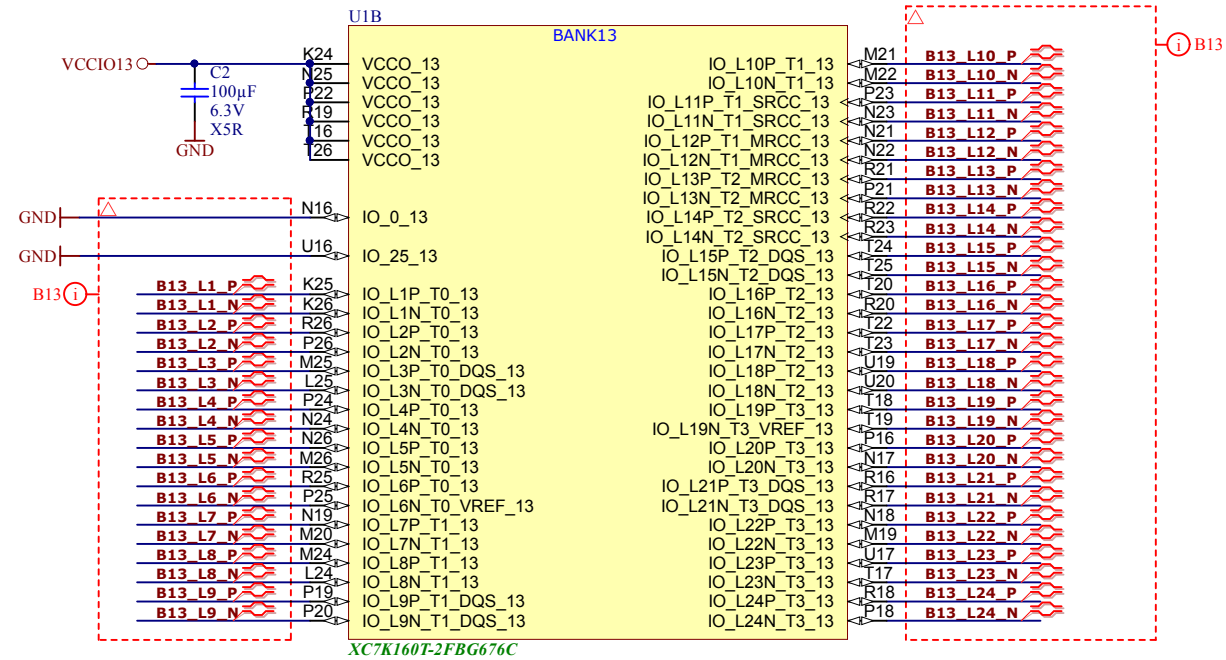
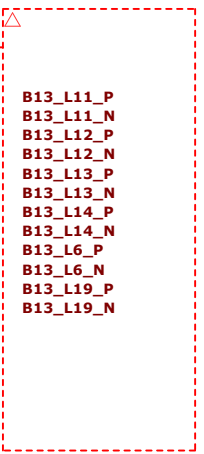
B12 L11 P
B12 L11 N
B12 L12 P
B12 L12 N
B12 L13 P
B12 L13 N
B12 L14 P
B12 L14 N
B12 L19 P
B12 L19 N
B12 L6 P
B12 L6 N

K70T version does not have this bank!



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B13_FIXED



XC7K160T-2FBG676C



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A4	Number: TE0741 TE0741-160-2CF	Rev. 02
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Filename: B13.SchDoc		

1

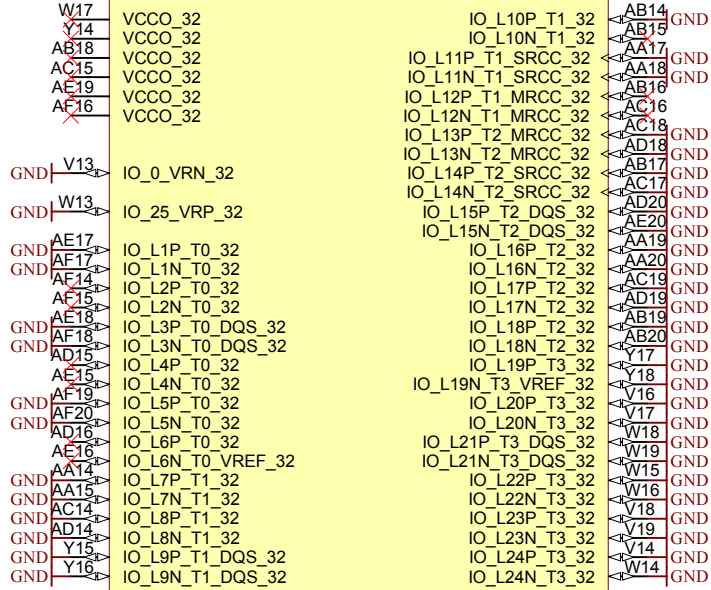
2

3

4

UIF

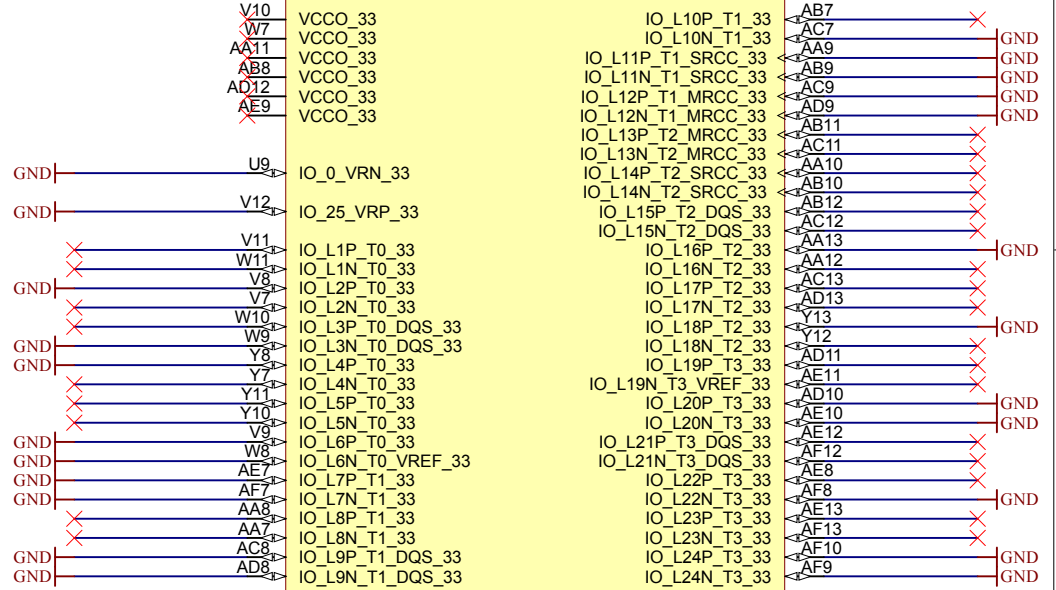
BANK32



XC7K160T-2FBG676C

UIG

BANK33



XC7K160T-2FBG676C



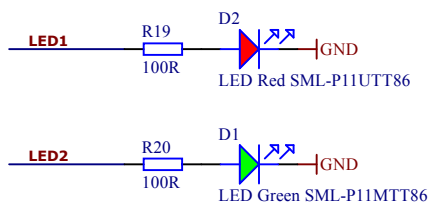
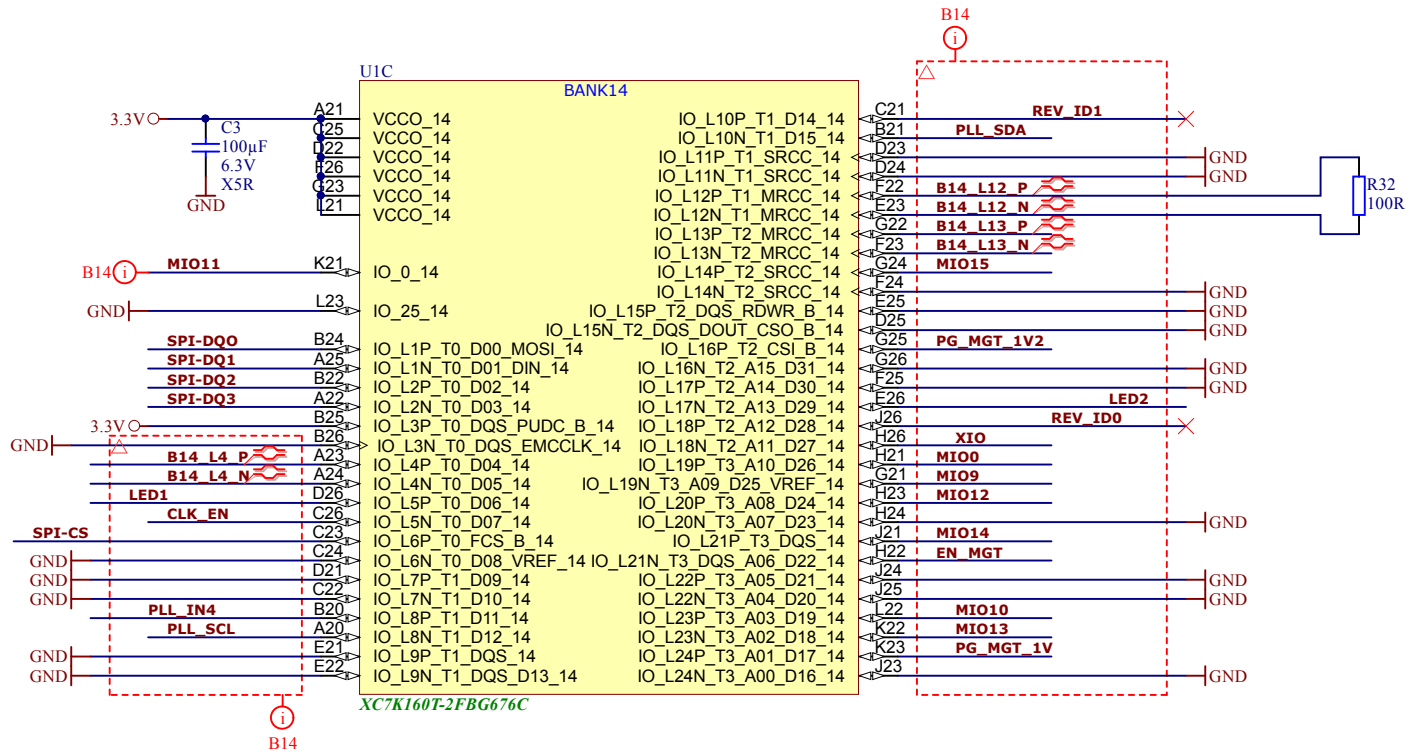
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Date: 2013-11-06	Copyright: 2013 Trenz Electronic GmbH	Page5 of 15
Filename: B33.SchDoc		

1

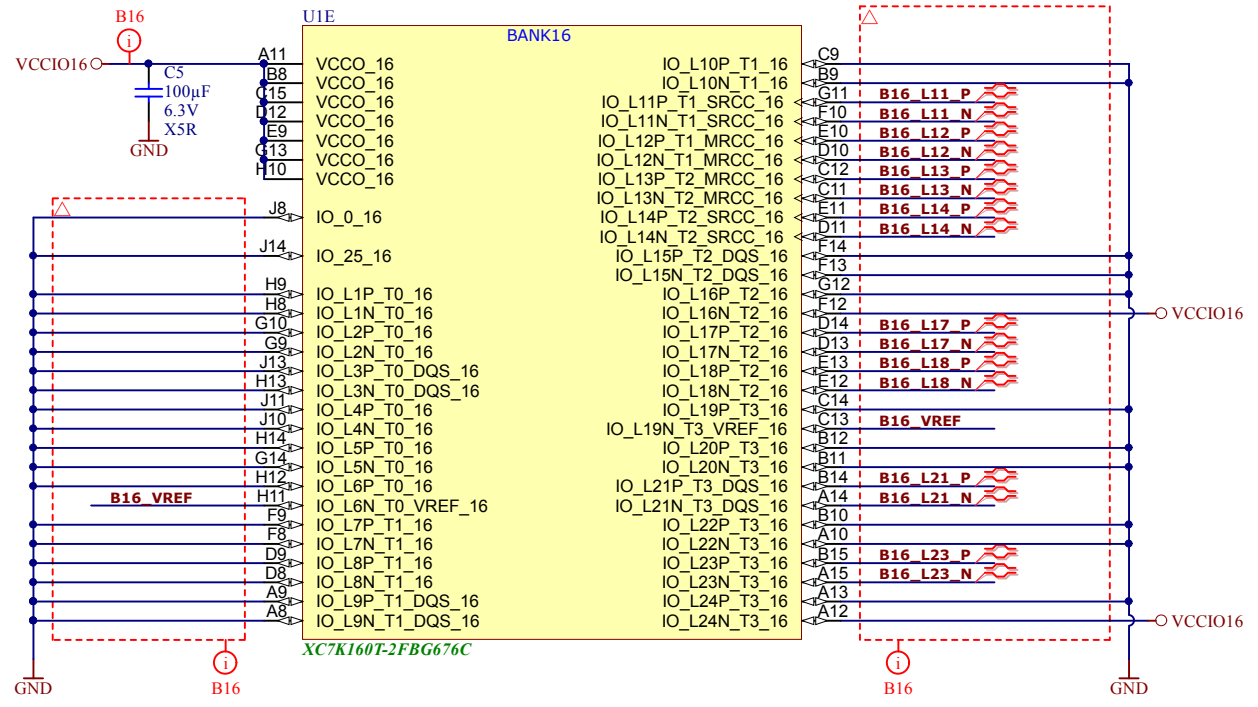
2


3

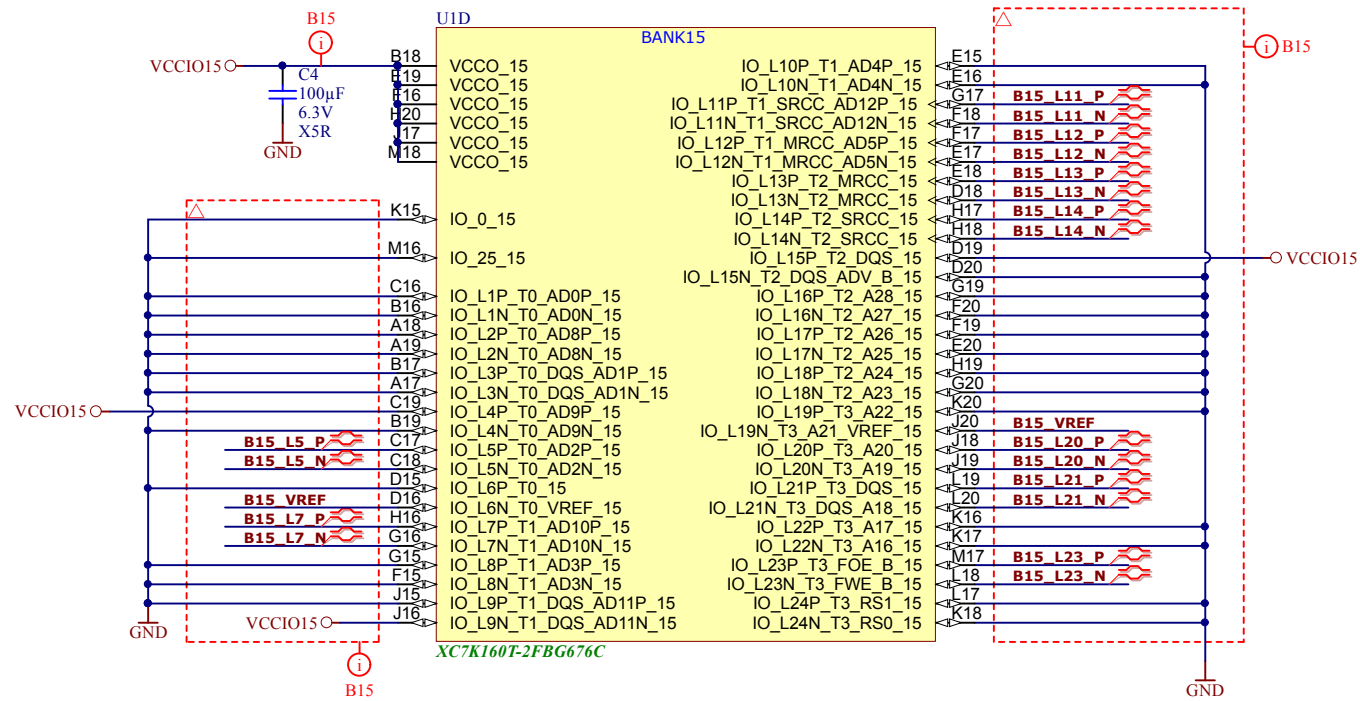
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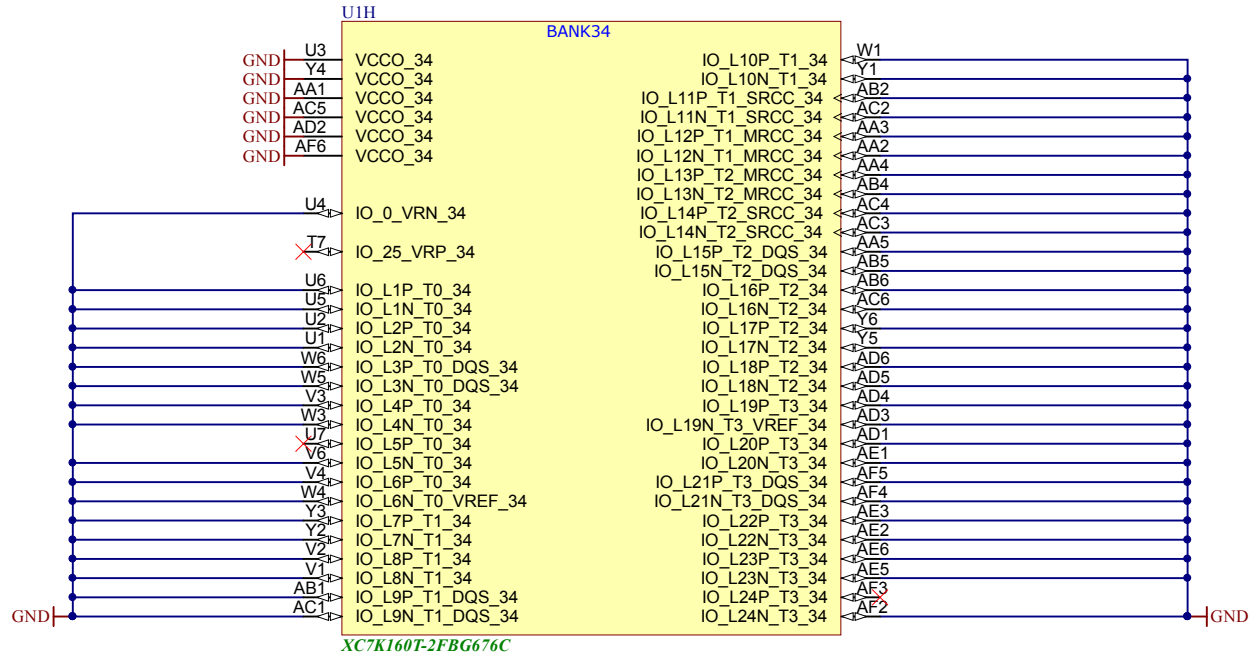
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Date: 2013-11-06		Copyright: 2013 Trenz Electronic GmbH	
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Filename: B14.SchDoc			




		Title: TE0741	
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Date: 2013-11-06		Copyright: 2013 Trenz Electronic GmbH	
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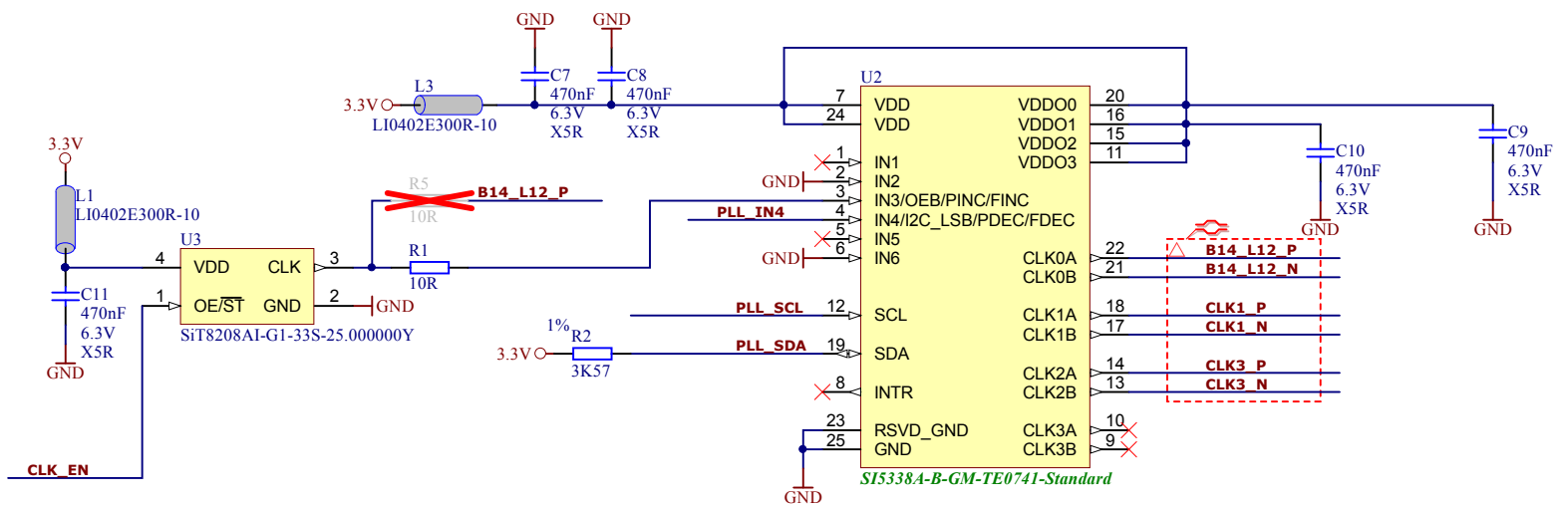
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A4	Number: TE0741 TE0741-160-2CF	Rev. 02
Date: 2013-11-06	Copyright: 2013 Trenz Electronic GmbH	Page 7 of 15
Filename: B15.SchDoc		




XC7K160T-2FBG676C

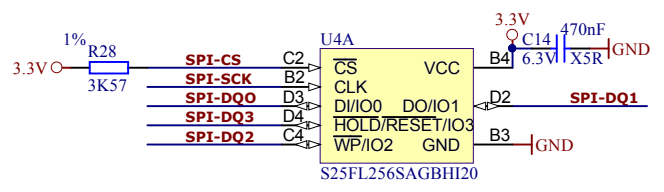
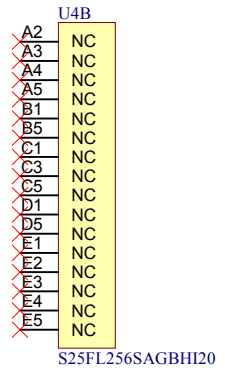
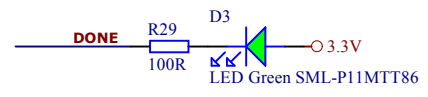
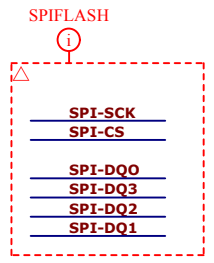
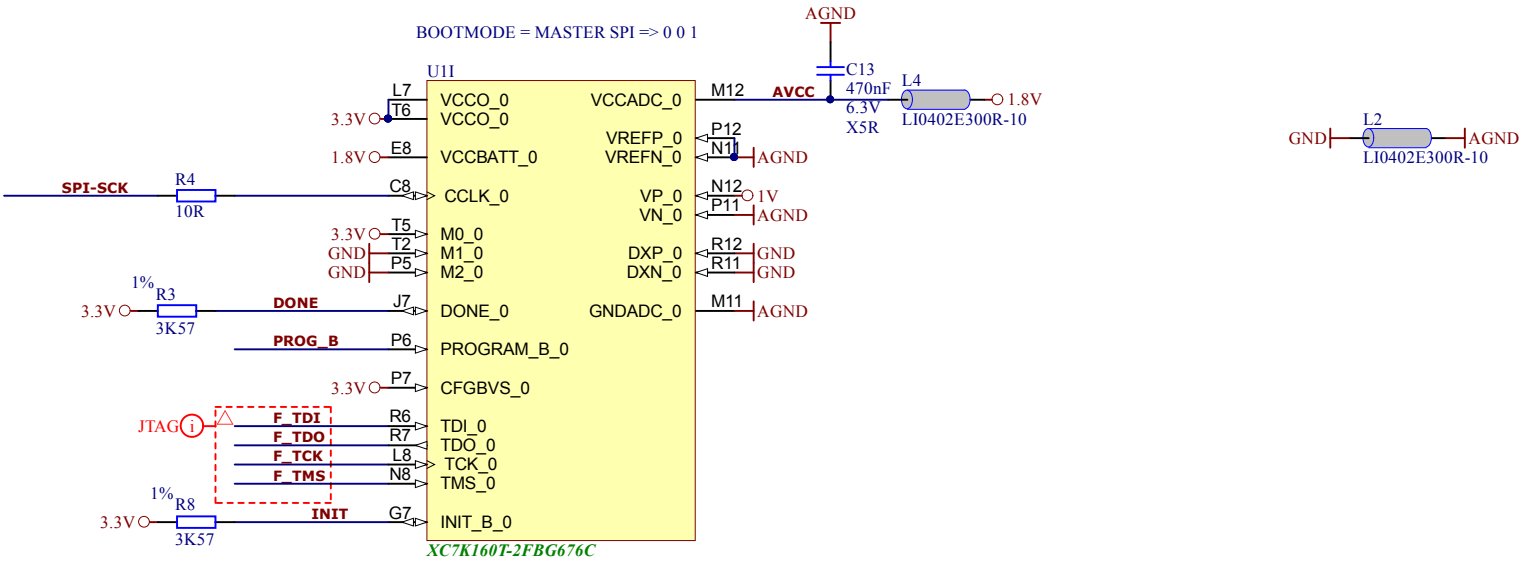


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Date: 2013-11-06	Copyright: 2013 Trenz Electronic GmbH	Page 8 of 15
Filename: B34.SchDoc		

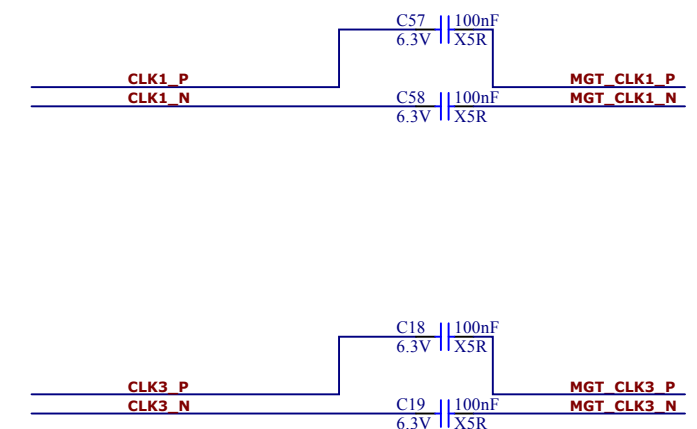
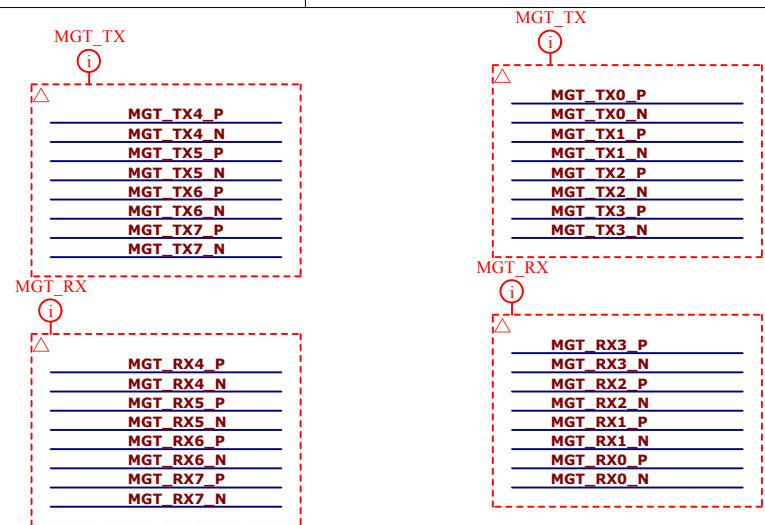
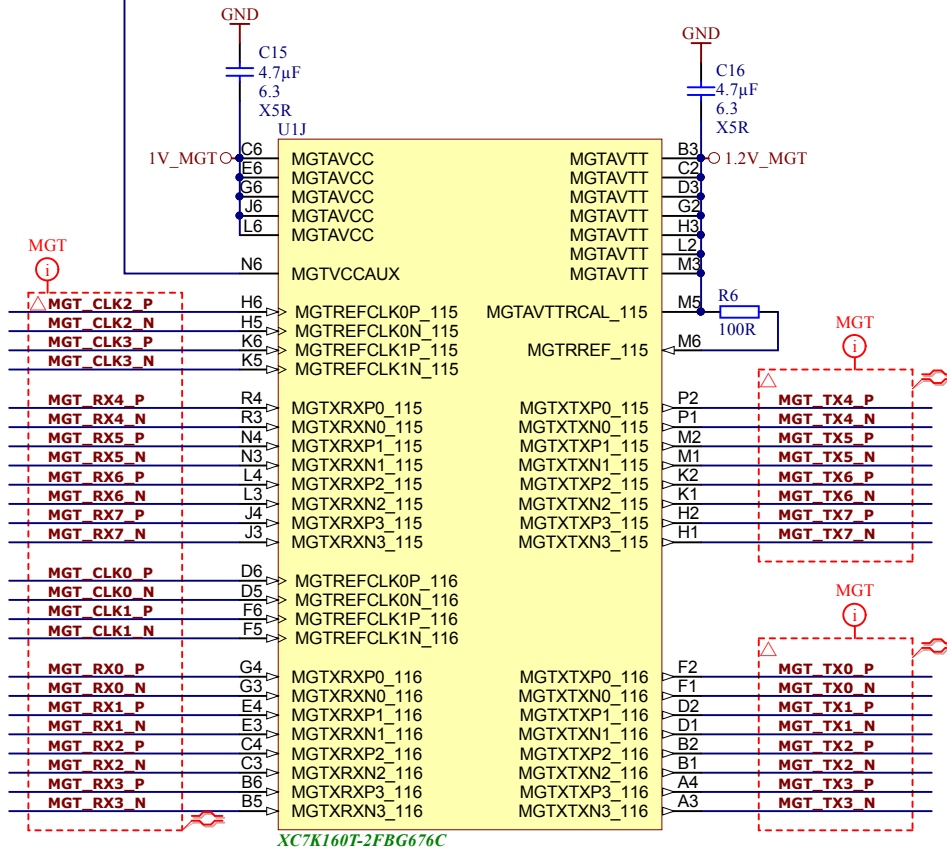
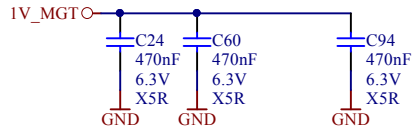
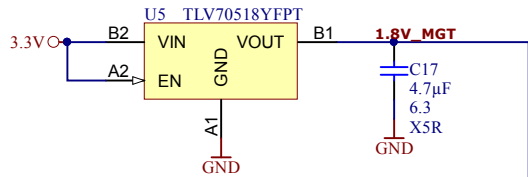


		Title: TE0741	
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Date: 2013-11-06		Copyright: 2013 Trenz Electronic GmbH	
Page 9		of 15	
Filename: Clock.SchDoc			

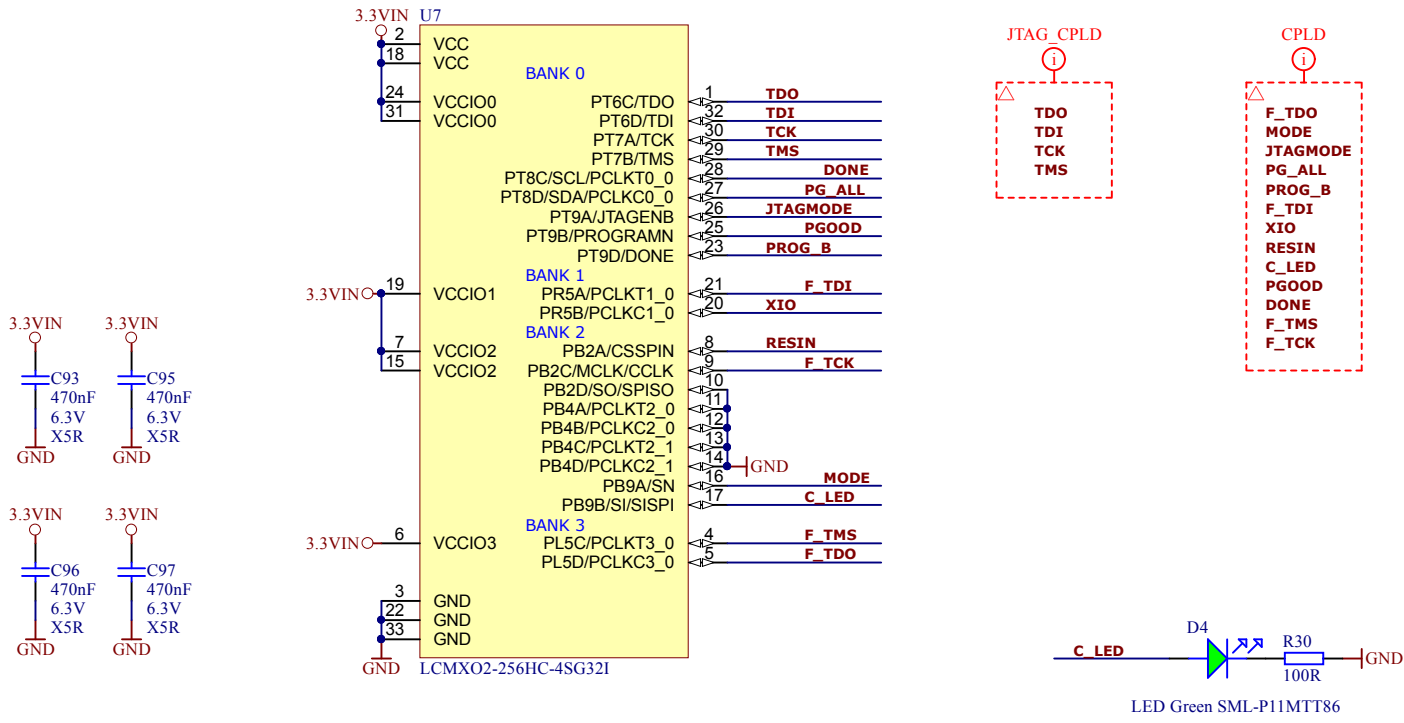
BOOTMODE = MASTER SPI => 0 0 1



Title: TE0741		
A4	Number: TE0741 TE0741-160-2CF	Rev. 02
Date: 2013-11-06	Copyright: 2013 Trenz Electronic GmbH	Page 10 of 15
Filename: FPGA-CFG.SchDoc		



Title: TE0741		
A4	Number: TE0741 TE0741-160-2CF	Rev. 02
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Filename: FPGA-MGT.SchDoc		



	Title: TE0741	
	A4	Number: TE0741 TE0741-160-2CF
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	Page 12 of 15	Rev. 02
Filename: FPGA-MISC.SchDoc		

1

2

3

4

A

A

B

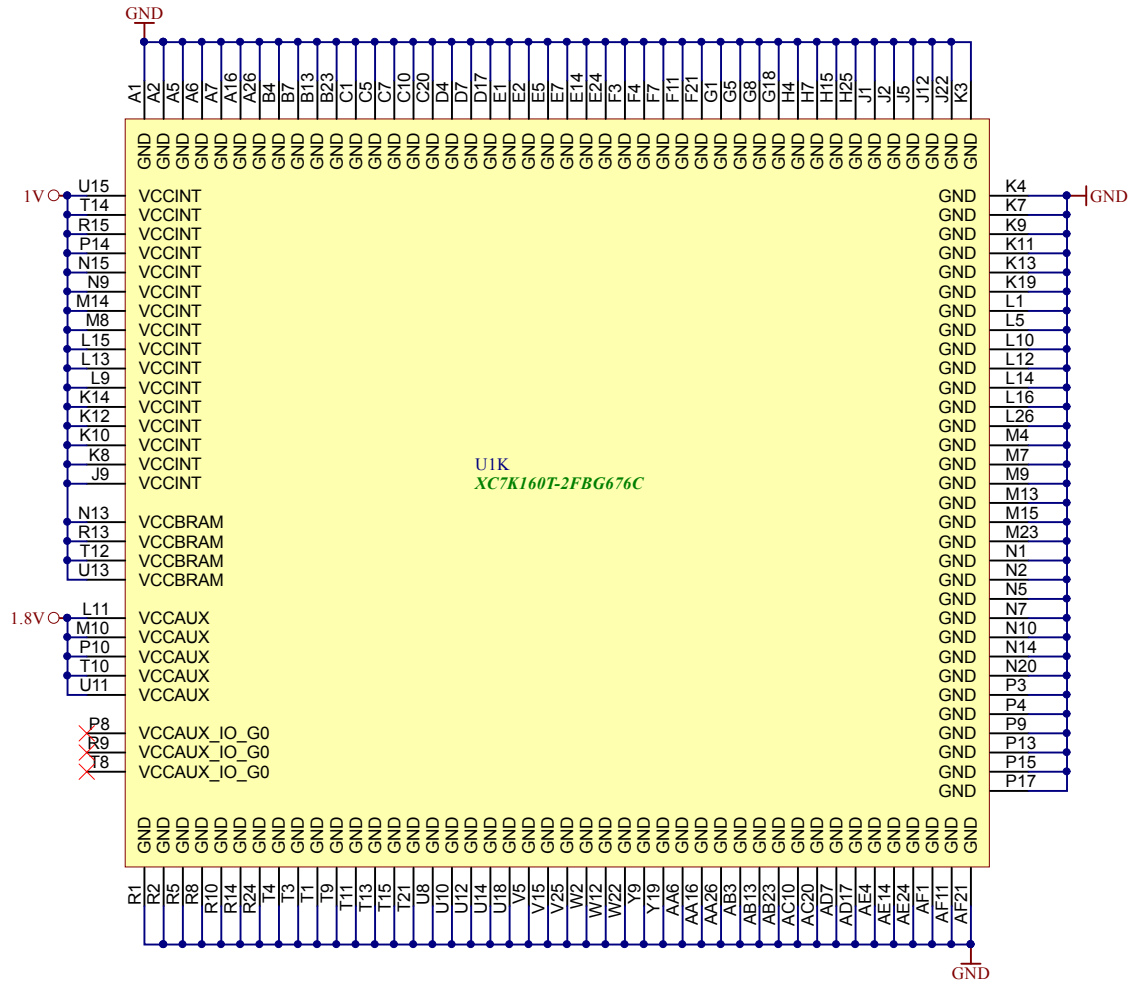
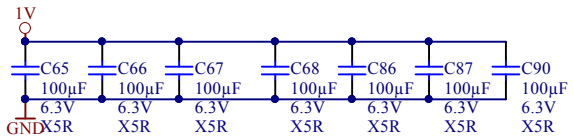
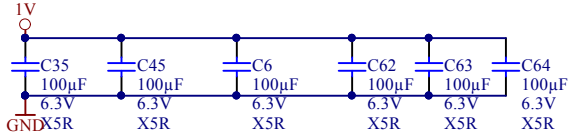
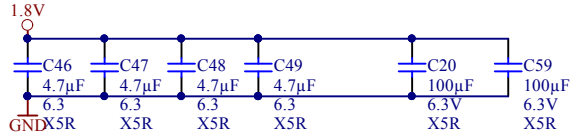
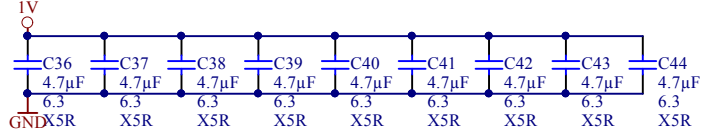
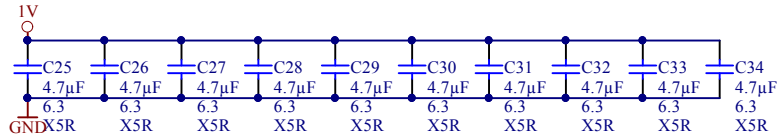
B

C

C

D

D



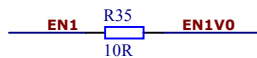
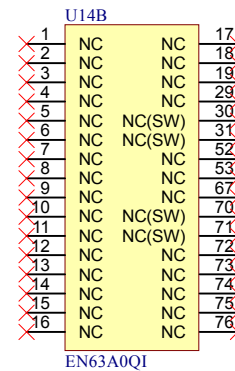
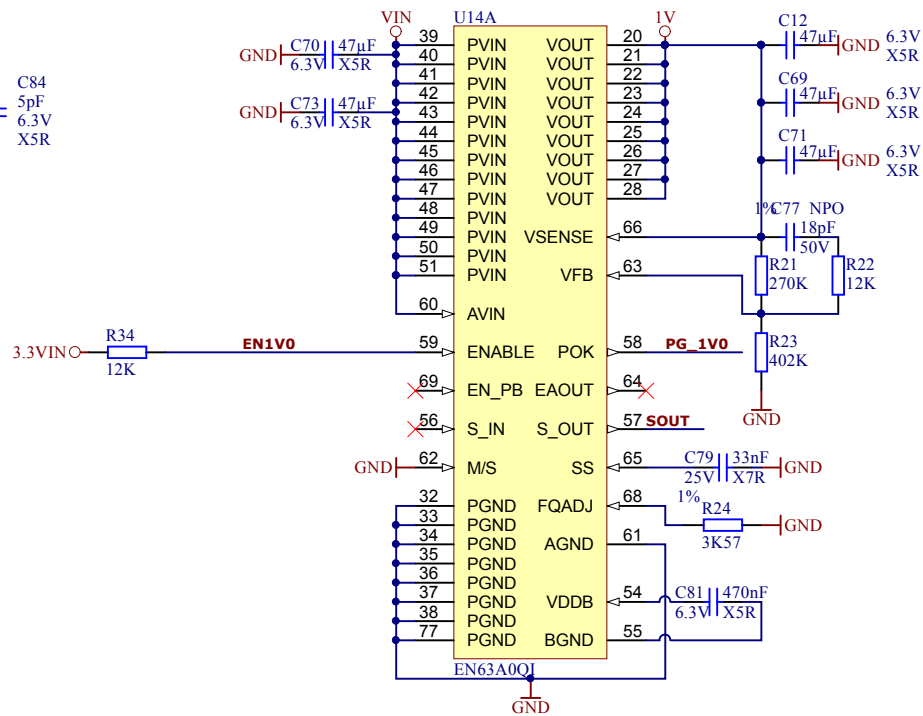
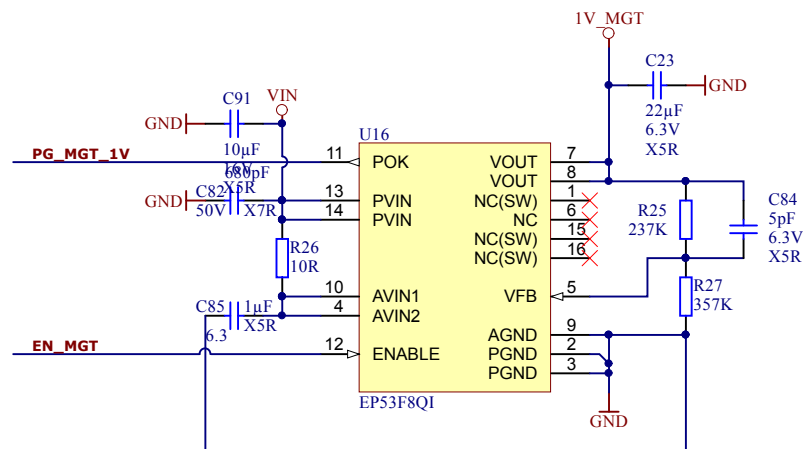
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Filename: FPGA-PWR.SchDoc		

1

2

3

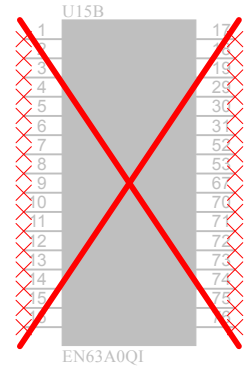
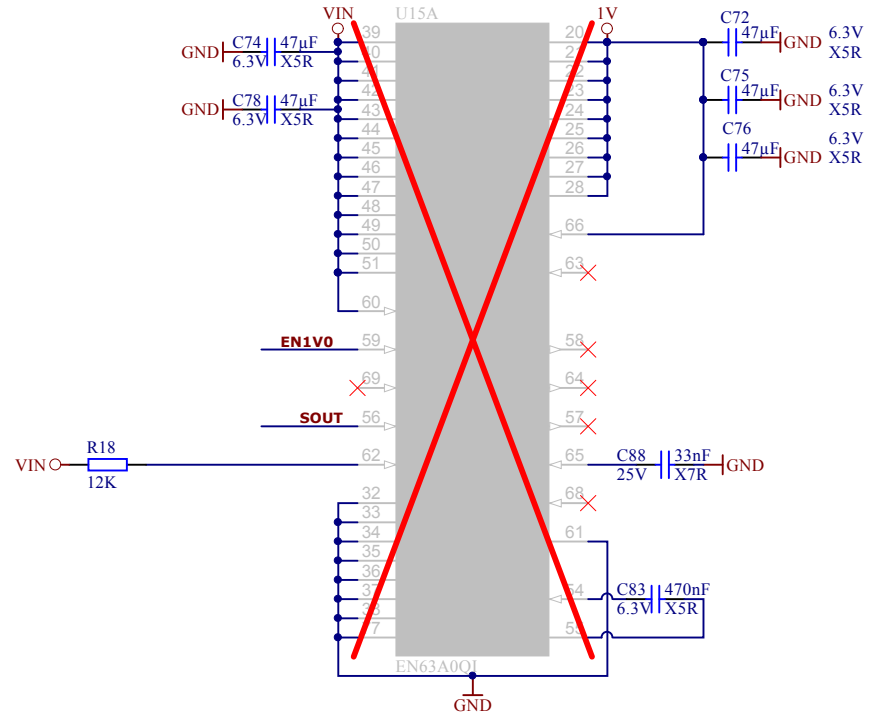
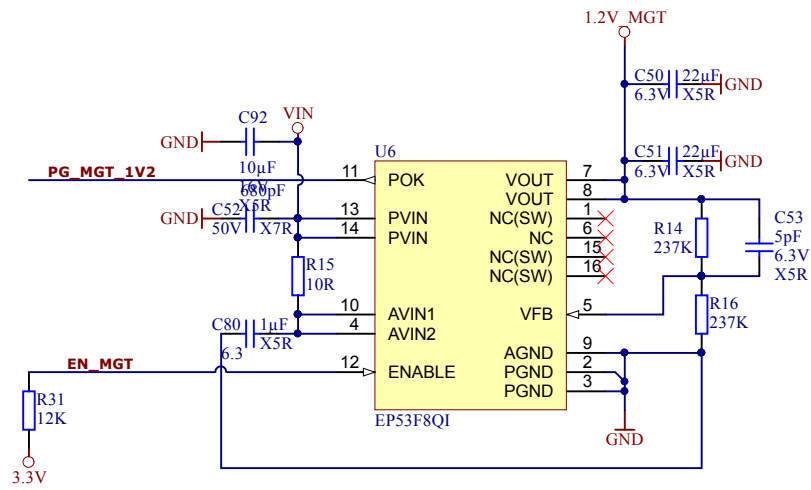
4




Not mount if baseboard EN1 circuit cause problems



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A4	Number: TE0741 TE0741-160-2CF	Rev. 02
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		Title: TE0741	
		A4	Number: TE0741 TE0741-160-2CF
Date: 2013-11-06		Copyright: 2013 Trenz Electronic GmbH	
Date: 2013-11-06		Page 15 of 15	
Filename: PWR2.SchDoc			