*Click **here** to ask an associate for production status of specific part numbers.*

MAX20474

3.0V to 5.5V Input, 6V to 18V Output, Synchronous Boost Converter

General Description

The MAX20474 is a high-efficiency DC-DC converter that boosts 3.0V to 5.5V input supply from 6V to 18V at up to 1A load. The boost converter achieves ±1.5% output error over load, line, and temperature range.

The device features a 2.2MHz fixed-frequency PWM mode for better noise immunity and load-transient response, as well as a pulse-frequency modulation mode (skip) for increased efficiency during light-load operation. The 2.2MHz frequency operation allows for the use of all ceramic capacitors and minimizes external components. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. Integrated low R_{DSON} switches improve efficiency at heavy loads and make planning the layout a much simpler task with respect to discrete solutions.

Other features include True Shutdown™, soft-start, overcurrent, and overtemperature protections.

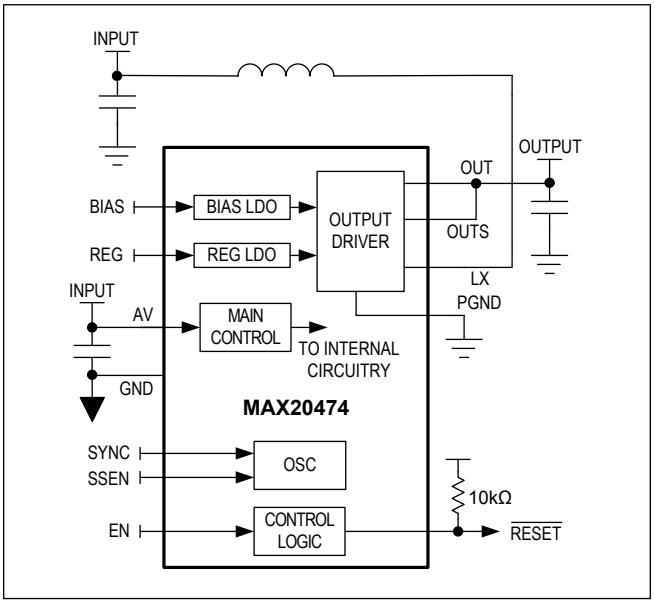
Applications

- Automotive Point of Load

Benefits and Features

- Synchronous Boost Converter for Small Solution Size
  - 4.0A Peak Input Current
  - Resistor-Adjustable Output Voltage from 6V to 18V
  - 6V to 18V Fixed Output Selection in 0.25V Steps
  - 3.0V to 5.5V Operating Supply Voltage
  - 2.2MHz Operation
  - $\overline{\text{RESET}}$ Output
  - Spread Spectrum
- High Precision
  - ±1.5% Output Voltage Accuracy, Fixed
  - ±2.2% Output Voltage Accuracy, Adj
  - 81 ± 3% UV Monitoring
  - 121 ± 3% OV Monitoring
  - Good Load-Transient Performance
- Robust for the Automotive Environment
  - Current-Mode, Forced-PWM, and SKIP Operation
  - Overtemperature and Short-Circuit Protection
  - 3mm x 3.5mm, 14-Pin TDFN
  - -40°C to +125°C Automotive Temperature Range

Simplified Block Diagram



True Shutdown is a trademark of Maxim Integrated Products, Inc.

***Ordering Information** appears at end of data sheet.*

19-101170; Rev 1; 2/22

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LIST OF TABLES

Absolute Maximum Ratings

EN, SYNC, SSEN, BIAS, AV, RESET to GND ..... -0.3V to +6V
OUTS, OUT to PGND ..... -0.3V to +22V
REG to OUT ..... -6V to OUT + 0.3V
LX to PGND (*Note 1*) ..... -0.3V to OUT + 0.3V
GND to PGND ..... -0.3V to +0.3V
LX Continous RMS Current 4A
Output Short-Circuit Duration ..... Continuous

Continuous Power Dissipation (*Note 2*) (T_A = +70°C, derate 22.15mW/°C above +70°C) 1771.87mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (Reflow) ..... +260°C

Note 1: Self-protected from transient voltages exceeding these limits in circuit under normal operation.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TDFN

Package Code	T143A3+1C
Outline Number	**21-100420**
Land Pattern Number	**90-100149**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	45.15°C/W
Junction to Case (θ_{JC})	7.54°C/W

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_{AV} = 5V, EN = 5V, T_A = T_J = -40°C to +125°C, V_{OUT} = 12V, Typical values are at T_A = +25°C under normal conditions unless otherwise noted. (*Note 3*)
Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	VIN		3		5.5	V
AV_UVLO Rising	AV_UVLOR	AV rising			2.5	V
AV_UVLO Falling	AV_UVLOF	AV falling		2.2		V
Shutdown Supply Current	I_{SHDN}	EN = LOW, SYNC = LOW, T_A = +25°C		1		µA
Supply Current	I_{IN}	EN = HIGH, I_{OUT} = 0mA, SYNC = LOW		400		µA
PWM Switching Frequency	f_{SW}	Internally generated	2	2.2	2.4	MHz
Spread Spectrum	SS	SSEN enabled		±3		%
OUT						
Output Voltage Accuracy	V_{OUT}	PWM mode, I_{LOAD} = 0A to I_{MAX}, internal feedback	-1.5		+1.5	%
		PWM mode, I_{LOAD} = 0A to I_{MAX}, external feedback	-2.2		+2.2	

Electrical Characteristics (continued)

(V_{AV} = 5V, EN = 5V, T_A = T_J = -40°C to +125°C, V_{OUT} = 12V, Typical values are at T_A = +25°C under normal conditions unless otherwise noted. (*Note 3*)
Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

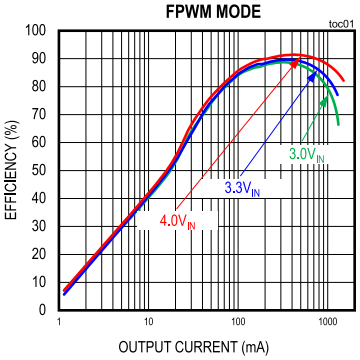
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Feedback Voltage Accuracy	V_{OUT}	PWM mode, I_{LOAD} = 0A to I_{MAX}	794	812	830	mV
pMOS On-Resistance	R_{HS}	V_{AV} = 3.3V, I_{LX} = 1.0A		150		mΩ
nMOS On-Resistance	R_{LS}	V_{AV} = 3.3V, I_{LX} = 1.0A		100		mΩ
nMOS Current-Limit Threshold	I_{LIM2}		3.0	4.0	5.0	A
LX Leakage Current	I_{LXLKG}	LX = PGND or OUT, T_A = 25°C		0.1		µA
Maximum Duty Cycle	DC_{MAX}		88			%
OUT Discharge Resistance	R_{DISCH}	V_{EN} = 0V (connected to OUT) power dissipation		300		Ω
SKIP Threshold	THSKIP	Percentage of nMOS current-limit threshold		25		%
Soft-Start Time	t_{SS}			1.9		ms
THERMAL OVERLOAD						
Thermal Shutdown Temperature	T_{SHDN}	T_J rising		165		°C
Hysteresis	T_{HYST}			15		°C
RESET						
OV Threshold	OVACC	Rising, % of nominal output	118	121	124	%
UV Threshold	UVACC	Falling, % of nominal output	78	81	84	%
Active Hold Period	t_{HOLD}	Option 1 (default)		0.5		ms
OV/UV Delay Filter	$t_{OVUVDEL}$	10% below/above threshold		10		µs
Output-High Leakage Current	I_{RLKG}	T_A = +25°C		0.1		µA
Output Low Level	V_{ROL}	Sinking -2mA			0.2	V
EN, SSEN, AND SYNC INPUTS						
Input High Level	V_{IH}		1.5			V
Input Low Level	V_{IL}				0.5	V
Input Hysteresis	V_{HYST}			0.1		V
SYNC Input Pulldown	R_{SYNCPD}	EN high		100		kΩ
SYNC Input Frequency Range	f_{SYNC}		1.7		2.6	MHz
EN Pulldown Current				1		µA

Note 3: All units are 100% production tested at +25˚C. All temperature limits are guaranteed by design.

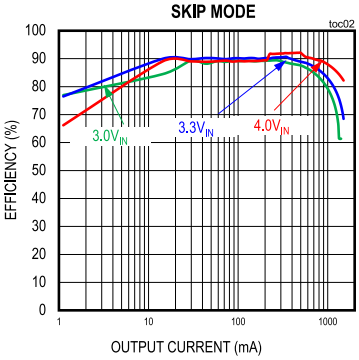
Typical Operating Characteristics

(T_A = +25°C)

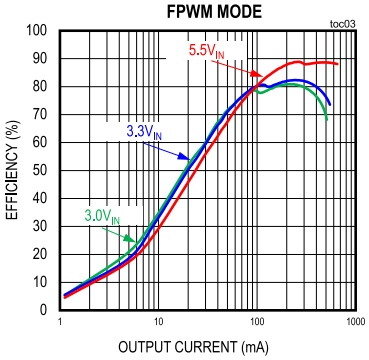
EFFICIENCY vs. INPUT VOLTAGE
6V OUTPUT
FPWM MODE



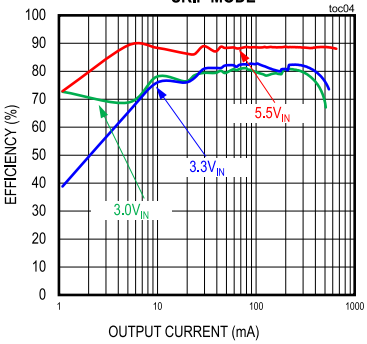
EFFICIENCY vs. INPUT VOLTAGE
6V OUTPUT
SKIP MODE



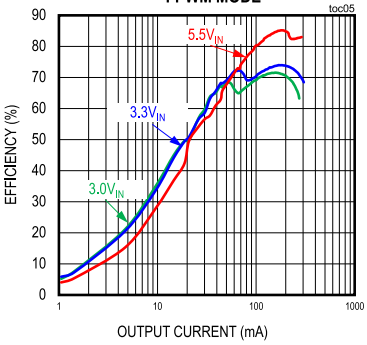
EFFICIENCY vs. INPUT VOLTAGE
12V OUTPUT
FPWM MODE



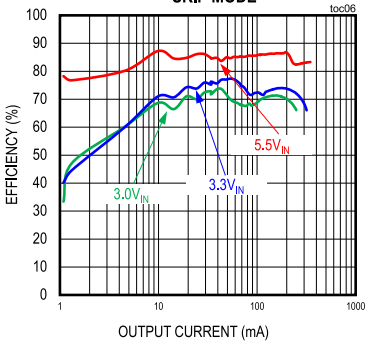
EFFICIENCY vs. INPUT VOLTAGE
12V OUTPUT
SKIP MODE



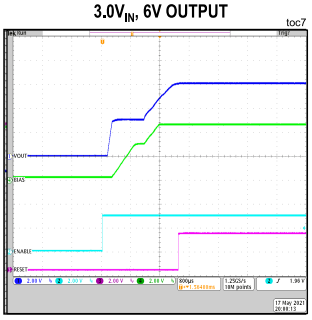
EFFICIENCY vs. INPUT VOLTAGE
18V OUTPUT
FPWM MODE



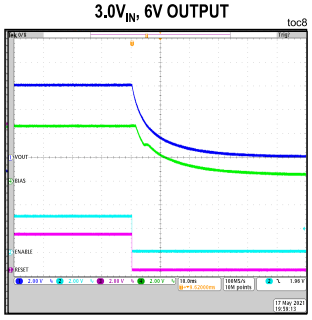
EFFICIENCY vs. INPUT VOLTAGE
18V OUTPUT
SKIP MODE



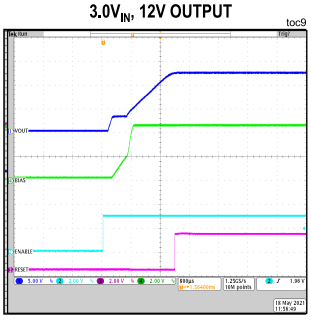
STARTUP WAVEFORM
3.0V$_{IN}$, 6V OUTPUT



SHUTDOWN WAVEFORM
3.0V$_{IN}$, 6V OUTPUT



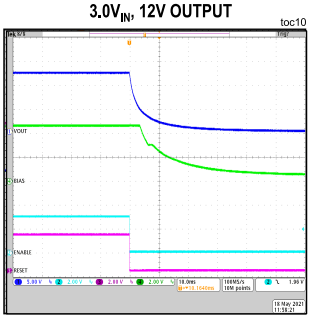
STARTUP WAVEFORM
3.0V$_{IN}$, 12V OUTPUT



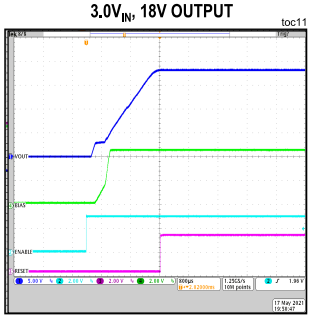
Typical Operating Characteristics (continued)

(T_A = +25°C)

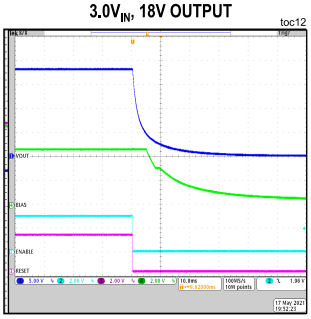
SHUTDOWN WAVEFORM
$3.0V_{IN}$, 12V OUTPUT



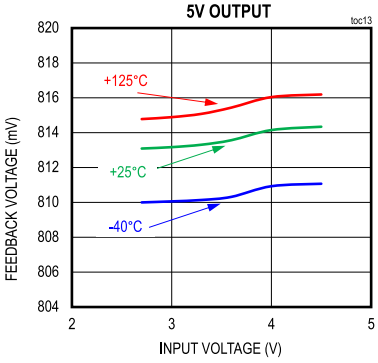
STARTUP WAVEFORM
$3.0V_{IN}$, 18V OUTPUT



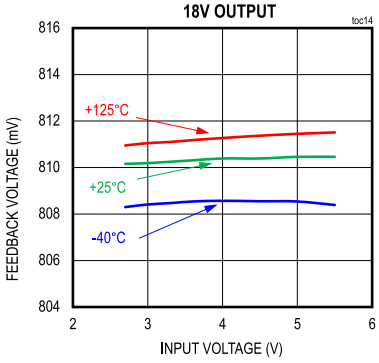
SHUTDOWN WAVEFORM
$3.0V_{IN}$, 18V OUTPUT



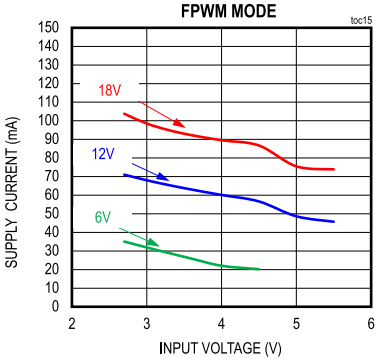
FEEDBACK VOLTAGE
vs. INPUT VOLTAGE
5V OUTPUT



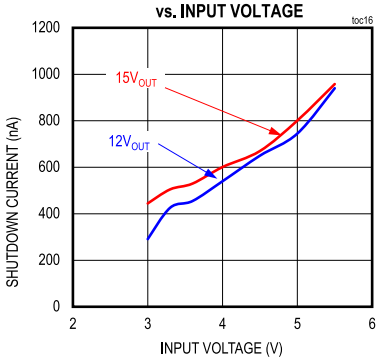
FEEDBACK VOLTAGE
vs. INPUT VOLTAGE
18V OUTPUT



SUPPLY CURRENT
vs. INPUT VOLTAGE
FPWM MODE



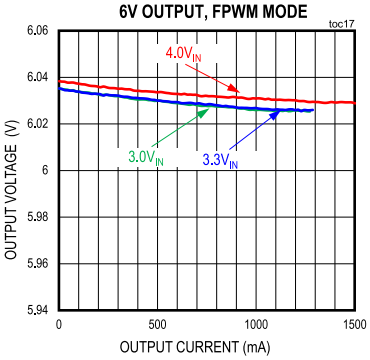
SHUTDOWN CURRENT
vs. INPUT VOLTAGE



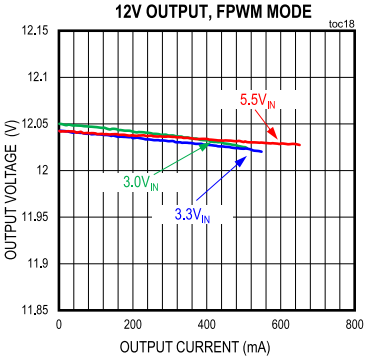
Typical Operating Characteristics (continued)

(T_A = +25°C)

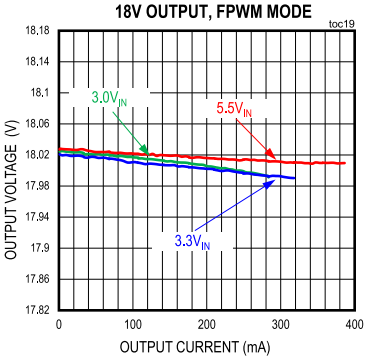
LOAD REGULATION vs. INPUT VOLTAGE 6V OUTPUT, FPWM MODE



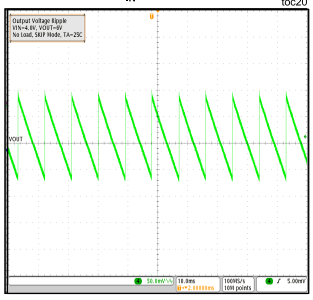
LOAD REGULATION vs. INPUT VOLTAGE 12V OUTPUT, FPWM MODE



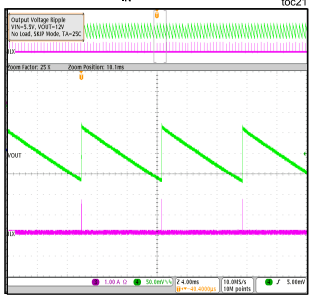
LOAD REGULATION vs. INPUT VOLTAGE 18V OUTPUT, FPWM MODE



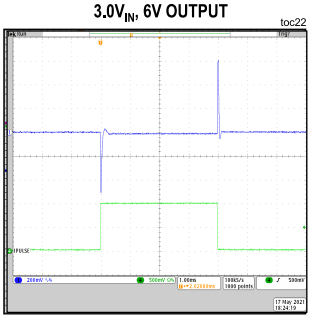
OUTPUT VOLTAGE RIPPLE $4.0V_{IN}$, 6V OUTPUT



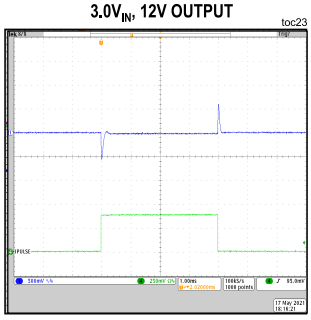
OUTPUT VOLTAGE RIPPLE $5.5V_{IN}$, 12V OUTPUT



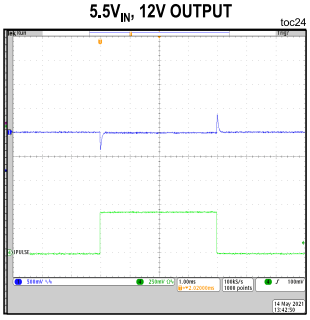
OUTPUT VOLTAGE TRANSIENT $3.0V_{IN}$, 6V OUTPUT



OUTPUT VOLTAGE TRANSIENT $3.0V_{IN}$, 12V OUTPUT



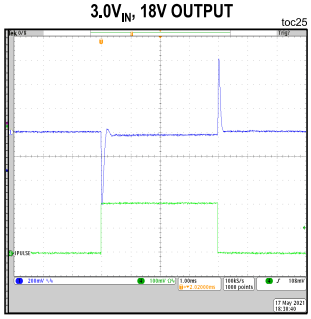
OUTPUT VOLTAGE TRANSIENT $5.5V_{IN}$, 12V OUTPUT



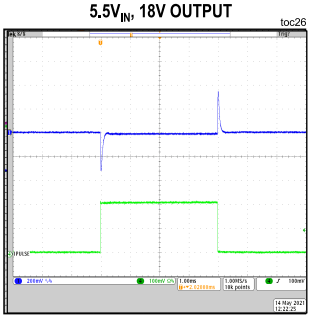
Typical Operating Characteristics (continued)

(T_A = +25°C)

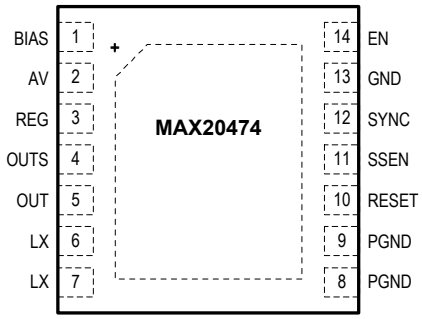
OUTPUT VOLTAGE TRANSIENT
$3.0V_{IN}$, 18V OUTPUT



OUTPUT VOLTAGE TRANSIENT
$5.5V_{IN}$, 18V OUTPUT



Pin Configuration



14 TDFN
3mm x 3.5mm

Pin Description

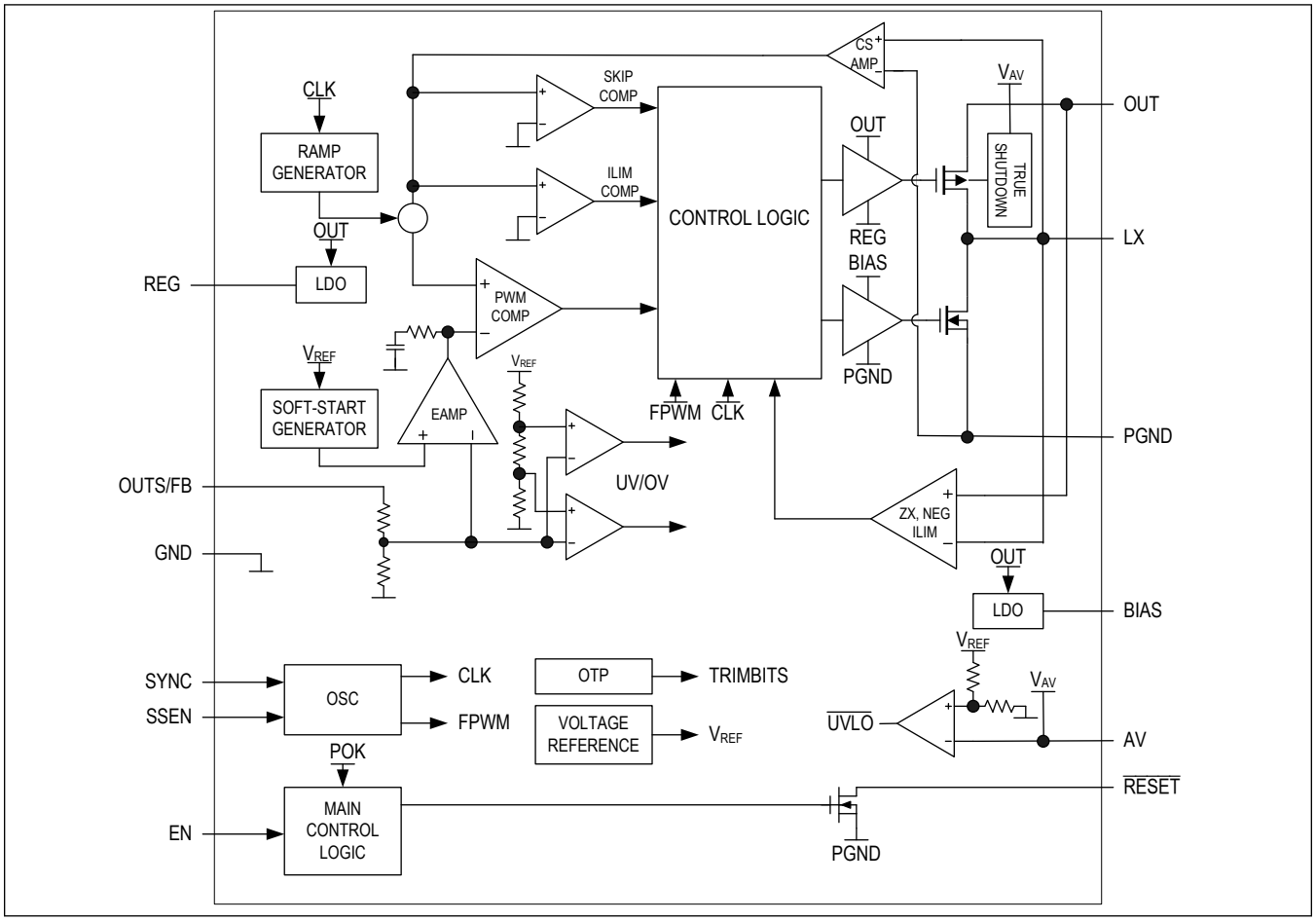
PIN	NAME	FUNCTION
1	BIAS	BIAS LDO Output. Connect a 2.2µF ceramic capacitor to from BIAS to GND.
2	AV	Analog Power Input Supply. Connect a 0.1µF ceramic capacitor from AV to GND.
3	REG	LDO Output. Connect a capacitor from REG to OUT. See *REG Pin Considerations* for required value.
4	OUTS	Output Voltage Feedback Pin. Connect this pin to the output capacitor for part numbers with fixed output voltage or through a resistor-divider for the adjustable output version.
5	OUT	Output Voltage.
6,7	LX	Inductor Connection. Connect LX to the switched side of the inductor.
8,9	PGND	Power Ground.
10	$\overline{\text{RESET}}$	Open-Drain RESET Output. To obtain a logic signal, pull up $\overline{\text{RESET}}$ with an external resistor.

Pin Description (continued)

PIN	NAME	FUNCTION
11	SSEN	Spread-Spectrum Enable. Connect to input supply to enable spread spectrum or to ground to disable.
12	SYNC	SYNC Input. Connect SYNC to GND or leave unconnected to enable SKIP-mode operation under light loads. Connect SYNC to AV or an external clock to enable fixed-frequency forced-PWM-mode operation.
13	GND	Ground. Connect all ground pins to the EP.
14	EN	Active-High Enable. Drive EN HIGH for normal operation.
—	EP	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PGND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Functional Diagrams

Internal Block Diagram



Detailed Description

The MAX20474 is a high-efficiency, 6V to 18V output synchronous DC-DC boost converter that boosts the input supply of 3.0V to 5.5V to an output voltage of 6V to 18V. The boost converter has True Shutdown so the output voltage is 0V when off. The boost converter achieves ±1.5% output error over load, line, and temperature ranges for the fixed output voltage options.

The device features a 2.2MHz fixed-frequency PWM mode for better noise immunity and load-transient response, and a pulse-frequency modulation (SKIP) mode for increased efficiency during light-load operation. The 2.2MHz frequency operation allows for the use of all ceramic capacitors and minimizes external components. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. The spread modulation can be factory-set to pseudorandom. Integrated low-R_{DSON} switches improve efficiency at heavy loads and make the layout a much simpler task with respect to discrete solutions.

For each output, the MAX20474 contains high-accuracy, factory-set OV/UV thresholds that are mapped to the $\overline{\text{RESET}}$ pin. Diagnostics on the $\overline{\text{RESET}}$ and OUT pins guarantee high reliability and fail-safe operation.

In light-load applications, a logic input (SYNC) allows the devices to operate either in SKIP mode for reduced current consumption or fixed-frequency, forced-PWM (FPWM) mode to eliminate frequency variation and help minimize EMI. Protection features include cycle-by-cycle current limit and thermal shutdown with automatic recovery.

Enable Input (EN)

The enable control inputs (EN) activate the device channel from their low-power shutdown state. EN has an input threshold of 1V (typ) with a hysteresis of 80mV (typ). When an enable input goes high, the associated output voltage ramps up with the programmed soft-start time.

$\overline{\text{RESET}}$ Output

The device features an open-drain $\overline{\text{RESET}}$ output that asserts low when the corresponding output voltage is outside of the UV/OV window. $\overline{\text{RESET}}$ remains asserted for a fixed timeout period after the output rises up to its regulated voltage. The fixed timeout period is factory-programmable between 0.5ms, 3.7ms, 7.4ms, or 14.9ms. Contact the factory for a preprogrammed timeout period. To obtain a logic signal, place a pullup resistor between the $\overline{\text{RESET}}$ pin and the system I/O voltage.

Internal Oscillator

The device has a spread-spectrum oscillator that varies the internal operating frequency up by ±3% relative to the internally generated operating frequency of 2.2MHz (typ). This function does not apply to externally applied oscillation frequency. The spread frequency generated is pseudorandom with a repeat rate well below the audio band.

Synchronization (SYNC)

The device has an on-chip oscillator that provides a fixed switching frequency of 2.2MHz. Depending on the condition of SYNC, two operation modes exist.

Operation Mode 1, SKIP: If SYNC is unconnected or at GND, the device will operate in the highly efficient pulse-skipping mode if the load current is below the SKIP mode current threshold.

Operation Mode 2, FPWM: If SYNC is at AV or has an applied frequency from an external source, then the device is in forced-PWM mode.

SYNC may be switched to SKIP or FPWM at any time during operation. An external clock may also be applied or disabled at any time during operation as well. However, to minimize overshoots and undershoots affecting downstream circuits during on-the-fly mode transitions with SYNC, it is recommended to disable the MAX20474 first then transition SYNC to SKIP or FPWM, or enable or disable an external clock.

Charge Mode

When the MAX20474 is enabled through the EN pin or AV crossing the UVLO_rising threshold, the high-side pMOS is configured as a constant current source. While not switching, the high-side pMOS delivers a 2A (typ) constant charging

current to the output until the V_{OUT} voltage rises to the equivalent of the BIAS voltage (4.5V, typ). Once V_{OUT} rises to the BIAS voltage, the MAX20474 enters boost mode where the high-side pMOS begins to switch.

The MAX20474 enters hiccup mode under the following conditions: 1) startup into hard short, and 2) hard short after regulation. During startup into hard short conditions, the high-side pMOS will be unable to charge up the output voltage to the BIAS voltage, so the MAX20474 enters hiccup mode and automatically retries after 120ms. If the MAX20474 is shorted to ground after the soft-start period, the boost again enters hiccup mode and automatically retries after 120ms.

Soft-Start

The MAX20474 includes a fixed soft-start of 1.9ms. Soft-start time limits start-up inrush current by forcing the output voltage to ramp up towards its regulation point.

Current Limit/Short-Circuit Protection

The device features a current limit that protects the device against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the low-side MOSFET remains on until the inductor current reaches the low-side MOSFET's current-limit threshold. The converter then turns on the high-side MOSFET to allow the inductor current to ramp down. Once the inductor current crosses below the high-side MOSFET current-limit threshold, the converter turns on the low-side MOSFET again. This cycle repeats until the short or overload condition is removed.

When a short-circuit condition is expected in the system, it is vital that an additional capacitor is implemented on the REG pin of the MAX20474. See the *REG Pin Considerations* section to determine what value of capacitor is required for short-circuit conditions.

PWM/SKIP Modes

The device features an input (SYNC) that puts the converter either in SKIP mode or forced PWM mode of operation. See the *Pin Description* section for more details. In PWM mode, the converter switches at a constant frequency with variable on-time. In SKIP mode, the converter's switching frequency is load dependent until the output load reaches a certain threshold. At higher load current, the switching frequency does not change and the operating mode is similar to the PWM mode. SKIP mode helps improve efficiency in light load applications by allowing the converter to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converter does not switch MOSFETs on and off as often as is the case in the PWM mode. Consequently, the gate charge and switching losses are much lower in SKIP mode.

Overtemperature Protection

Thermal overload protection limits the total power dissipation in the MAX20474. When the junction temperature exceeds +165°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C.

OUTS Pin Considerations

The OUTS pin of the MAX20474 does not protect against open-circuit conditions. If the OUTS pin is open, the high-side MOSFET of the output stage will attempt to regulate the output voltage leading to damage. Careful consideration should be taken for adjustable output voltage options where open circuits can occur due to poor connections of the feedback resistors (e.g., cold solder joints). For fixed output voltage options, the OUTS pin is shorted to the OUT pin, therefore only PCB pad or trace damage can be considered for an open condition.

BIAS Pin Considerations

The BIAS pin provides a external connection to a bypass capacitor for the internal BIAS LDO. It is not recommended for any other external circuitry to connect to the BIAS pin as the BIAS LDO does not source current.

REG Pin Considerations

The MAX20474 does not implement self-protection when the REG pin is shorted to ground; irreparable damage can occur. The REG pin also requires additional protection when the OUT pin is shorted to ground to cause a short-circuit condition. When the application use case requires short-circuit protection, a capacitor from the REG pin to ground is required. Table 1 outlines the conditions and capacitance values necessary for REG pin protection during OUT pin shorts

to ground for either variant (e.g., fixed output voltage or adjustable output voltage).

Table 1. REG Pin Capacitance Recommendations for Short-Circuit Protection

OUTPUT VOLTAGE	CAPACITANCE FROM OUT TO REG	CAPACITANCE FROM REG TO GND	NOTES
<8V	220nF	330nF	X7R, 50V, ±10% CGA3E3X7R1H334K080AB
≥8V	220nF	220nF	X7R, 50V, ±10% CGA3E3X7R1H224K080AB
6V to 18V	330nF	Open	When short protection is not required

Applications Information

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. A 2.2µF X7R ceramic capacitor is recommended for the AV pin.

Inductor Selection

The MAX20474 fixed voltage option has an optimally designed slope compensation for a 1µH inductor ±20% for the entire range of input (3.3V to 5.5V) and output voltages (6V to 18V). The MAX20474 adjustable voltage option implements a fixed slope compensation for the entire range of input and output voltages. Therefore, in the case of an adjustable output option, greater care of selecting an inductor value is required if the system design implements a value other than a 1µH inductor ±20%. General guidance on inductor calculations is discussed below; however, contact the Analog Devices factory applications engineer for guidance verifying a different inductor value that is implemented in the end system.

Generally, choosing an inductor value for the MAX20474 is a tradeoff between inductor size and type, inductor ripple requirements, and input current limit.

The inductor type may be a ferrite core or a soft-saturation core. For a ferrite core, the saturation current should be greater than the maximum current limit. For a soft-saturation core, the saturation current can be less than the maximum current limit as long as the inductance at the maximum current limit is greater than 50% of the nominal inductance.

Equation 1 is the ideal, canonical equation used to calculate the peak-to-peak ripple in a boost converter.

Equation 1:

$$2\,\Delta i_L = \left(\frac{V_{IN}}{L \cdot f_{SW}}\right) \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

where $2\Delta i_L$ is the peak-to-peak inductor ripple chosen to meet system requirements.

Equation 1 is rearranged to calculate the required inductor value to meet the desired ripple amplitude:

Equation 2:

$$L = \left(\frac{V_{IN}}{2\,\Delta i_L \cdot f_{SW}}\right) \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

where $2\Delta i_L$ is typically limited to 30% of the maximum load current.

Equation 2 illustrates that a smaller inductance value will yield higher ripple current. Care must be taken regarding the ripple amplitude as the MAX20474 implements peak current limit on the input. Therefore, the sum of the peak current and maximum load current should not exceed the input current limit. Equation 3 is used to calculate the peak current in the inductor.

Equation 3:

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

The ripple requirements, core saturation, and value determine the inductor package sizing. See the *Layout Considerations*, as inductor sizing affects component orientation and layout.

Boost Output Capacitor

The MAX20474 is designed to be stable with low-ESR ceramic capacitors. Other capacitor types are not recommended, as the ESR zero can affect stability of the device. The following output capacitor calculations are guidelines based on nominal conditions. The phase margin must be measured on the final circuit to verify that proper stability is achieved.

$$COUT_{MIN} = \frac{110\mu s \cdot A}{V_{OUT}}$$

$$COUT_{NOM} = \frac{220\mu s \cdot A}{V_{OUT}}$$

$$COUT_{MAX} = 2.5 \cdot C_{NOM}$$

External Feedback Resistors

The MAX20474 is available in a fixed voltage output through factory trim and an adjustable voltage output version. The output voltage range for both versions is 6V to 18V. For a desirable output voltage for the adjustable option, the following equation is necessary to calculate the external feedback resistors:

$$R_{HIGH} = R_{LOW}\left[\frac{V_{OUT}}{V_{REF}} - 1\right]$$

where V_{REF} = 812mV (typ) per the *Electrical Characteristics* table.

The parallel combination of R_{HIGH} and R_{LOW} should be ≤30kΩ to help reduce errors due to PCB contamination. It is important for the fixed output variant of the MAX20474 that VOUTS is shorted to V_{OUT} for proper operation or damage can occur to the device.

Layout Considerations

Similar to buck converters, boost converters like the MAX20474 should follow similar guidelines for proper PCB layout. With the MAX20474 IC as the focal point in the PCB layout, use the following guidelines to ensure excellent device performance, including thermals and efficiency.

1. The exposed pad of the MAX20474 must be connected to a copper plane for excellent thermal conductivity. Thermal design is dictated by the copper weight, thermal area, and number of vias implemented to achieve thermal performance. As a rule of thumb, it is best to use 2oz solid copper planes on the top board layer with vias from the exposed pad to a second solid copper plane. Real world designs often use 1oz copper for cost considerations; therefore, it is imperative to via connect (4 to 6, depending on hole size) to as many board layers together for a larger thermal plane.

2. The routing and placement of the output capacitors are critical for a boost. Similar to a buck converter's input capacitors, a boost's output capacitors experience high dI/dt as the current waveforms are high-RMS, discontinuous currents. The required output ceramic capacitors should be placed very close to the OUT pin (≤10mils or ≤0.254mm) and oriented where the return path back to the PGND pins are as short as possible; this is typically done on the top layer. The greater the length of the power ground return loop in the path of the output capacitor bank will add undesired parasitic resistance and inductance. This can lead to greater ringing on the LX node that reduces efficiency and higher EMI.

3. The routing and placement of the input capacitors are not as critical as the output capacitors since the input current to a boost is a low-RMS continuous current. It is still recommended that the input capacitors are placed close to the IC and oriented to minimize the return path back to the MAX20474's PGND pins again on the top layer. This specific distance will be influenced by the package size of the inductor, as the input capacitor is placed before the boost inductor.

4. The AV and BIAS capacitors provide external bypassing to their respective analog blocks. Place these capacitors (≤40mils, ≤1mm) away from their respective pins.

5. The REG capacitor placement should minimize parasitic resistance in the path of the capacitor to the REG pin. See *REG Pin Considerations* for additional information regarding short-circuit protection system requirements.

Figure 1 is one example of a suggested layout for the MAX20474. For additional guidance or questions regarding layout, contact the Analog Devices factory applications engineer.

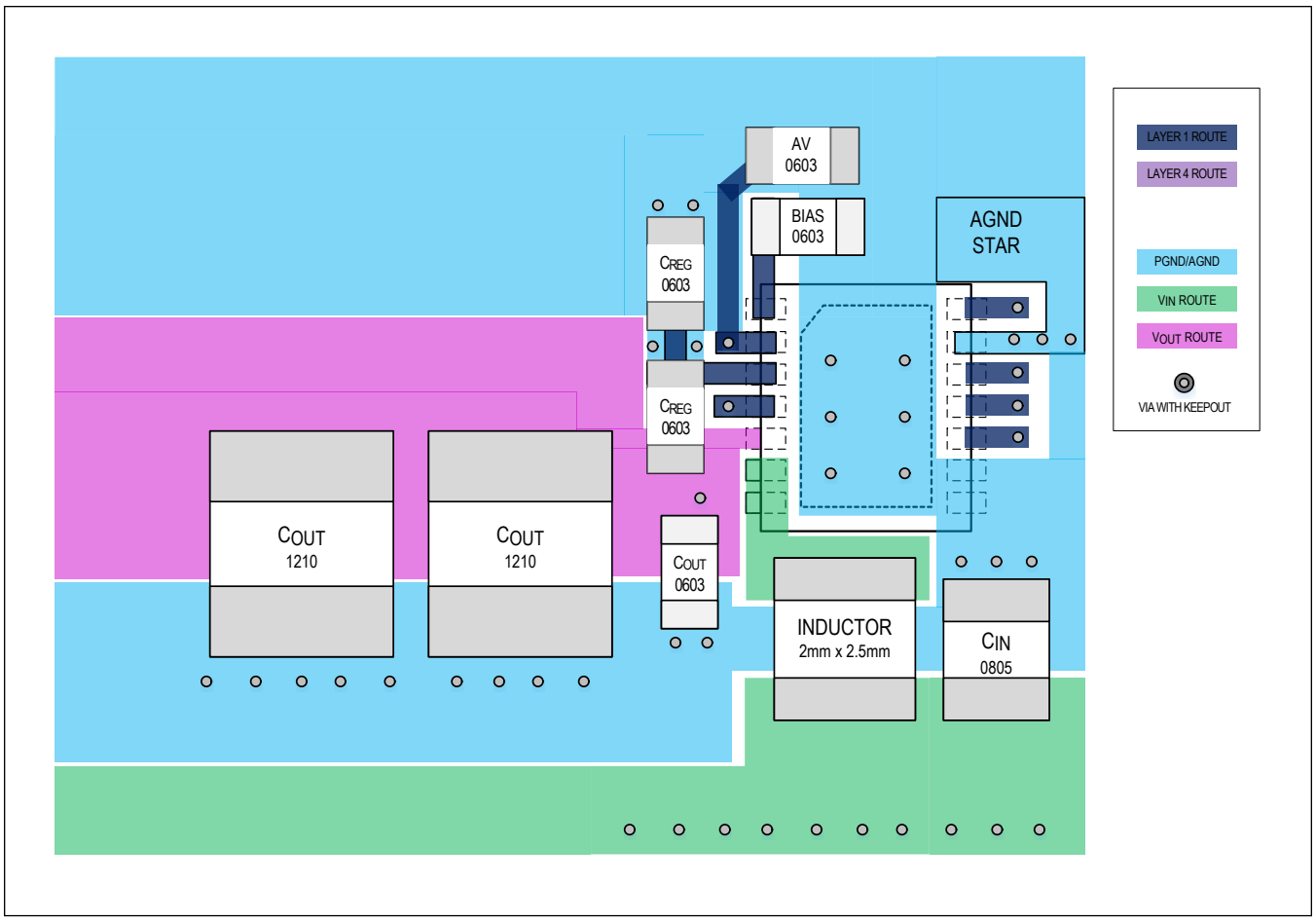
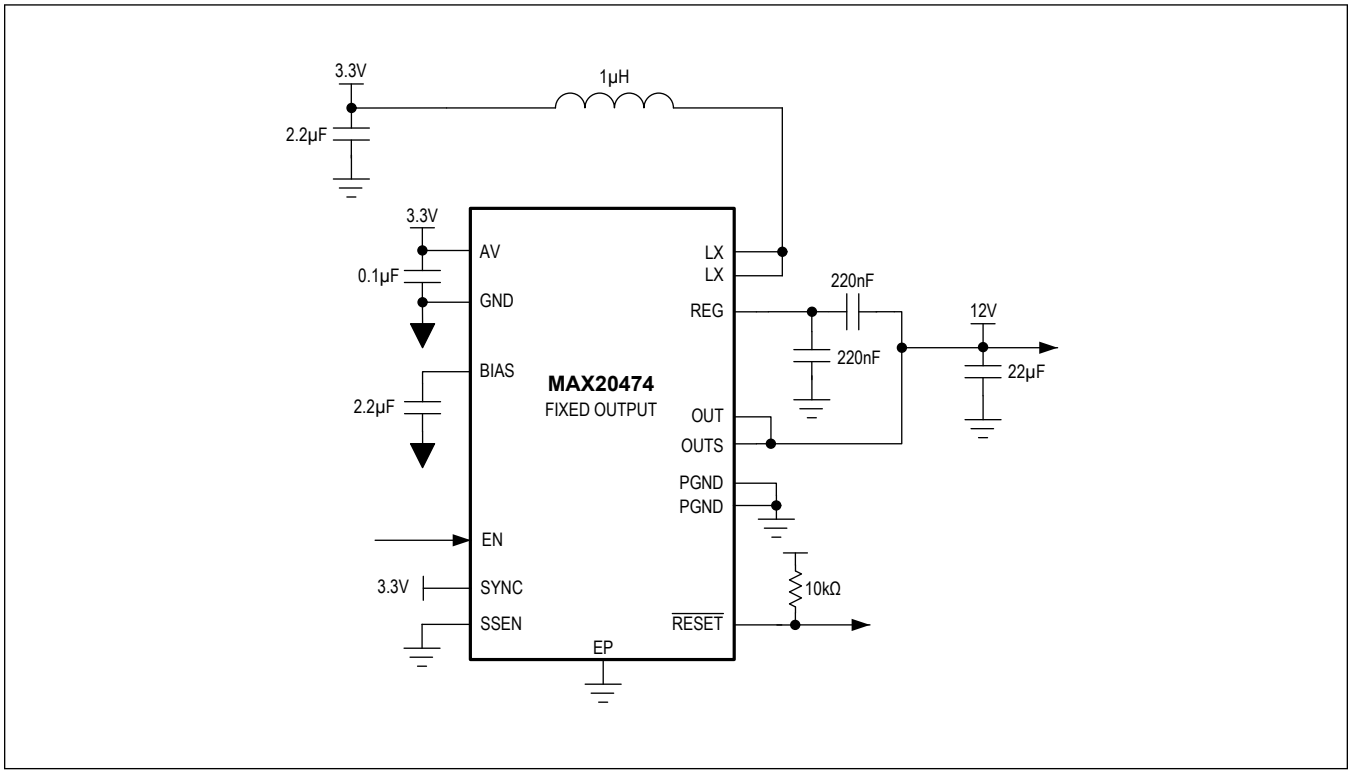


Figure 1. MAX20474 Layout Suggestion

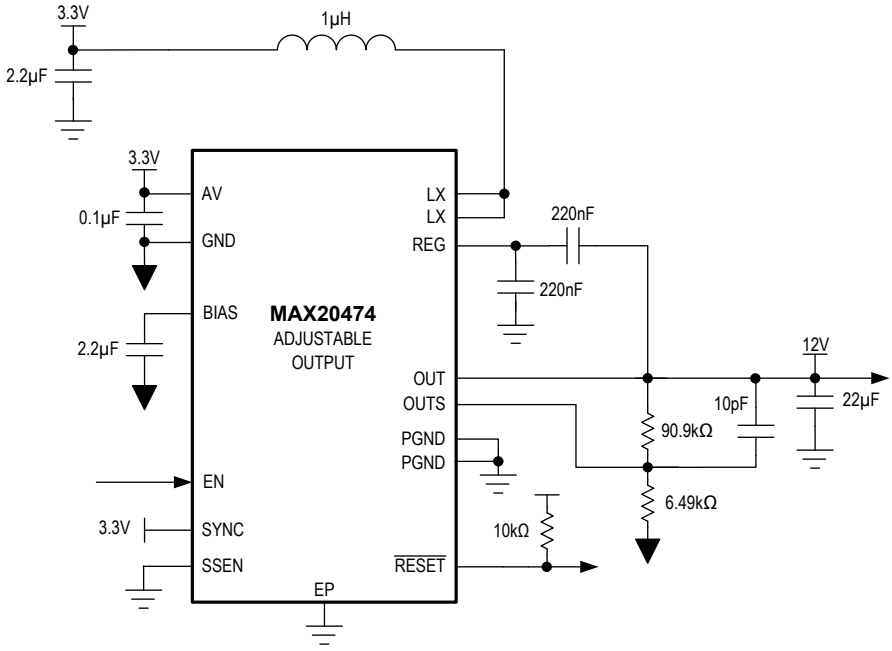
Typical Application Circuits

Fixed Output



Typical Application Circuits (continued)

Adjustable 12V Output



Ordering Information

PART	OUTPUT VOLTAGE	INPUT CURRENT LIMIT	TEMP RANGE
MAX20474ATDA/V+	Adjustable	4A	-40°C to +125°C
MAX20474ATDB/V+*	12V	4A	-40°C to +125°C

**Future product—contact factory for availability.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

/V Denotes an automotive-qualified part.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/21	Release for Market Intro	—
1	2/22	Updated *Pin Description*, *Detailed Description*, and *Applications Information*	10–12, 14–16