Dual Voltage Detector With Adjustable Hysteresis

Check for Samples: TPS3806I33-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C4B**
- **Dual Voltage Detector With Adjustable Hysteresis, 3.3-V Adjustable and 2-V Adjustable**
- **Assured Reset at V_{DD} = 0.8 V**
- **Supply Current: 3 µA Typical at V_{DD} = 3.3 V**
- **Independent Open-Drain Reset Outputs**
- **6-Pin SOT-23 Package**

APPLICATIONS

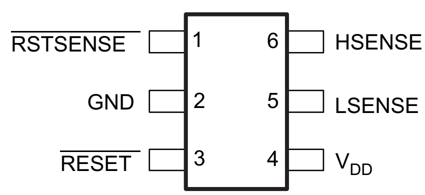
- **Voltage Supervisor**
- **Voltage Detector**
- **Battery Monitor**

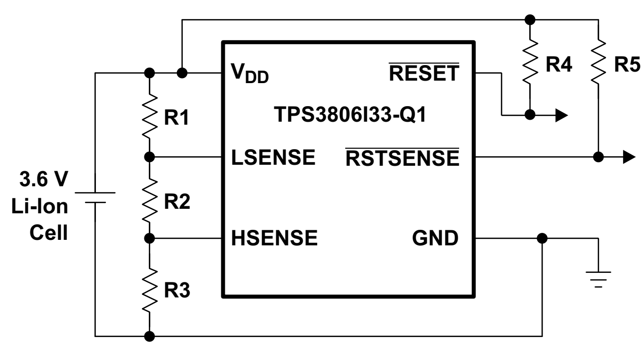
DESCRIPTION

The TPS3806I33-Q1 integrates two independent voltage detectors for battery voltage monitoring. During power on, the device asserts $\overline{RESET}$ and $\overline{RSTSENSE}$ when supply voltage V_{DD} or the voltage at the LSENSE input becomes higher than 0.8 V. Thereafter, the supervisory circuit monitors V_{DD} and LSENSE, keeping $\overline{RESET}$ and $\overline{RSTSENSE}$ active as long as V_{DD} and LSENSE remain below the threshold voltage, V_{IT}. As soon as V_{DD} or LSENSE rises above the threshold voltage V_{IT}, the device deasserts $\overline{RESET}$ or $\overline{RSTSENSE}$, respectively. The TPS3806I33-Q1 device has a fixed-sense threshold voltage V_{IT} set by an internal voltage divider at V_{DD} and an adjustable second-LSENSE input. In addition, one can set an upper voltage threshold at HSENSE to allow a wide adjustable hysteresis window.

The devices are available in a 6-pin SOT-23 package. Characterization of the TPS3806I33-Q1 device is for operation over a temperature range of –40°C to 125°C.

TPS3806I33-Q1
DBV PACKAGE
(TOP VIEW)





Typical Operating Circuit

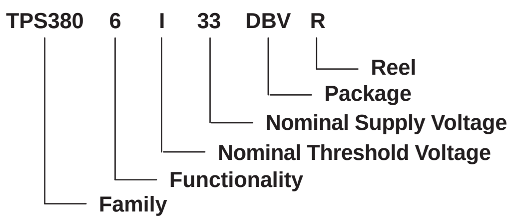
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION(1)

T_A	PACKAGE	QUANTITY	PART NUMBER	TOP-SIDE SYMBOL	STATUS
–40°C to 125°C	DBV (SOT-23)	Reel of 3000	TPS3806I33QDBVRQ1	PZHQ	Active

(1) For the most-current package and ordering information, see the Package Option Addendum located at the end of this data sheet or refer to the TI Web site at www.ti.com.



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		TPS3806I33-Q1	UNIT
Supply voltage, V_{DD} (2)		7	V
All other pins(2)		–0.3 to 7	V
Maximum low-output current, I_{OL}		5	mA
Maximum high-output current, I_{OH}		–5	mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)		±10	mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)		±10	mA
Operating free-air temperature range, T_A		–40 to 125	°C
Storage temperature range, T_{stg}		–65 to 150	°C
Electrostatic discharge rating, ESD	Human-body model (HBM) AEC-Q100 Classification Level H2	2	kV
	Charged-device model (CDM) AEC-Q100 Classification Level C4B	750	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation, the device must not be continuously operated at 7 V for more than t = 1000 h.

THERMAL INFORMATION

THERMAL METRIC[1]		TPS3806I33-Q1 DBV 6 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance[2]	188.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	130.9	°C/W
θ_{JB}	Junction-to-board thermal resistance[4]	34.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter[5]	25.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter[6]	33.8	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.3	6	V
Input voltage, V_I	0	V_{DD} + 0.3	V
Operating free-air temperature range, T_A	–40	125	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage		V_{DD} = 1.5 V, I_{OL} = 1 mA			0.3	V
			V_{DD} = 3.3 V, I_{OL} = 2 mA				
			V_{DD} = 6 V, I_{OL} = 3 mA				
	Power-up reset voltage(1)		V_{DD} ≥ 0.8 V, I_{OL} = 50 µA			0.2	V
V_{IT}	Negative-going input threshold voltage(2)	LSENSE	T_A = 25°C	1.198	1.207	1.216	V
		TPS3806I33-Q1		2.978	3	3.022	
		LSENSE	T_A = 0°C to 70°C	1.188	1.207	1.226	
		TPS3806I33-Q1		2.952	3	3.048	
		LSENSE	T_A = –40°C to 125°C	1.183	1.207	1.231	
		TPS3806I33-Q1		2.94	3	3.06	
V_{hys}	Hysteresis		1.2 V < V_{IT} < 2.5 V		60		mV
			2.5 V < V_{IT} < 3.5 V		90		
I_I	Input current	LSENSE, HSENSE		–25		25	nA
I_{OH}	High-level output current		V_{DD} = V_{IT} + 0.2 V, V_{OH} = V_{DD}			300	nA
I_{DD}	Supply current		V_{DD} = 3.3 V, output unconnected		3	5	µA
			V_{DD} = 6 V, output unconnected		4	6	
C_i	Input capacitance		V_I = 0 V to V_{DD}		1		pF

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active. $t_{r,VDD}$ ≥ 15 µs/V
(2) To ensure best stability of the threshold voltage, place a bypass capacitor (ceramic, 0.1 µF) near the supply terminals.

SWITCHING CHARACTERISTICS

at R_L = 1 MΩ, C_L = 50 pF, T_A = –40°C to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{RESET}$ delay	V_{IH} = 1.05 x V_{IT}, V_{IL} = 0.95 x V_{IT}		5	100	µs
		LSENSE to $\overline{RSTSENSE}$ delay					
t_{PLH}	Propagation (delay) time, low-to-high-level output	V_{DD} to $\overline{RESET}$ delay			5	100	µs
		HSENSE to $\overline{RSTSENSE}$ delay					

TIMING REQUIREMENTS

at R_L = 1 MΩ, C_L = 50 pF, T_A = –40°C to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse duration	At V_{DD}	V_{IH} = 1.05 x V_{IT}, V_{IL} = 0.95 x V_{IT}	5.5			µs
		At SENSE					

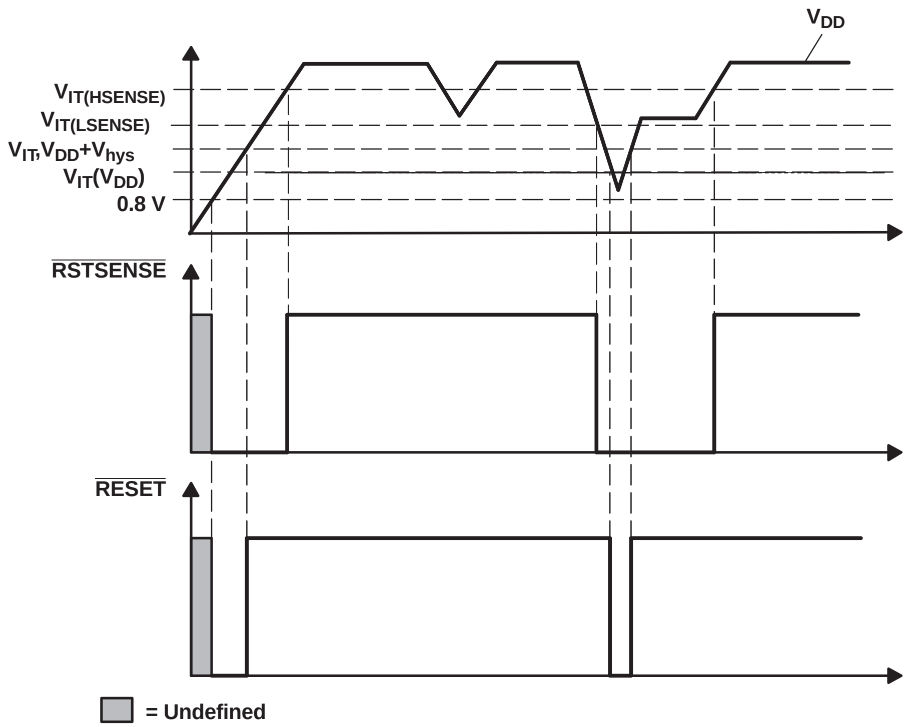


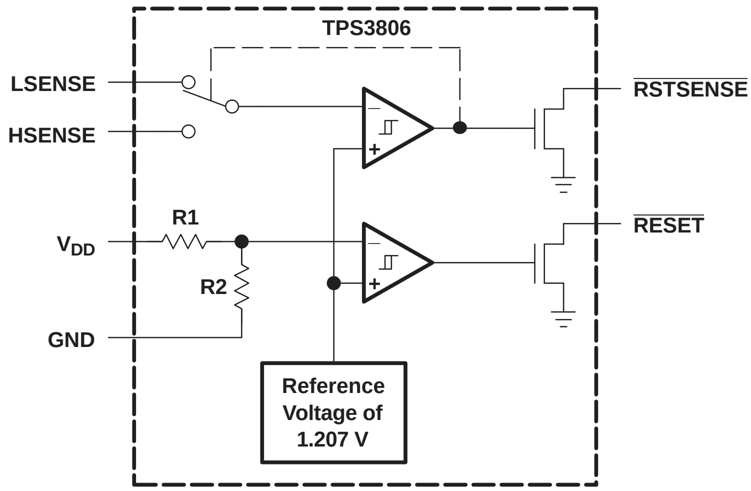
Table 2. TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GND	2	I	Ground
HSENSE	6	I	Adjustable hysteresis input
LSENSE	5	I	Adjustable sense input
$\overline{\text{RESET}}$	3	O	Active-low open-drain reset output (from V_{DD})
$\overline{\text{RSTSENSE}}$	1	O	Active-low open-drain reset output (from LSENSE)
V_{DD}	4	I	Input supply voltage and fixed sense input

FUNCTION AND TRUTH TABLE

TPS3806I33-Q1			
$V_{DD} > V_{IT}$	$\overline{\text{RESET}}$	LSENSE > V_{IT}	$\overline{\text{RSTSENSE}}$
0	L	0	L
1	H	1	H

FUNCTIONAL BLOCK DIAGRAM



Detailed Description

Operation

The TPS3806I33-Q1 monitors battery voltage and asserts $\overline{\text{RESET}}$ when a battery becomes discharged below a certain threshold voltage. A comparator monitors the battery voltage via an external resistor divider. When the voltage at the LSENSE input drops below the internal reference voltage, the $\overline{\text{RSTSENSE}}$ output pulls low. The output remains low until the battery is replaced, or recharged above a second higher trip-point, set at HSENSE. One can monitor a second voltage at V_{DD}. The independent $\overline{\text{RESET}}$ output pulls low when the voltage at V_{DD} drops below the fixed threshold voltage. Because the TPS3806I33-Q1 outputs are open-drain MOSFETs, most applications may require a pullup resistor.

Programming the Threshold Voltage Levels

Calculate the low-voltage threshold at LSENSE according to Equation 1:

$$V_{(LSENSE)} = V_{ref}\left(\frac{R1 + R2 + R3}{R2 + R3}\right) \tag{1}$$

where V_{ref} = 1.207 V

Calculate the high-voltage threshold at HSENSE as shown in Equation 2:

$$V_{(HSENSE)} = V_{ref}\left(\frac{R1 + R2 + R3}{R3}\right) \tag{2}$$

where V_{ref} = 1.207 V

To minimize battery current draw, TI recommends using 1 MΩ as the total resistor value $R_{(tot)}$, with $R_{(tot)}$ = R1 + R2 + R3.

TYPICAL CHARACTERISTICS

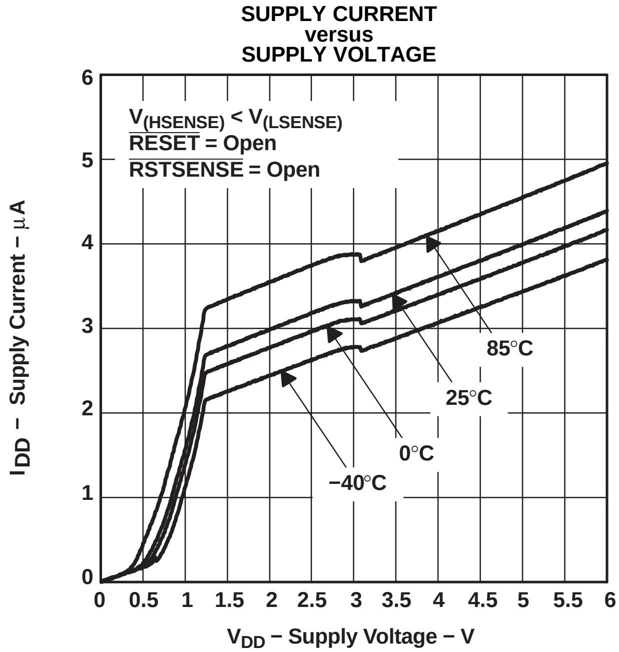


Figure 1.

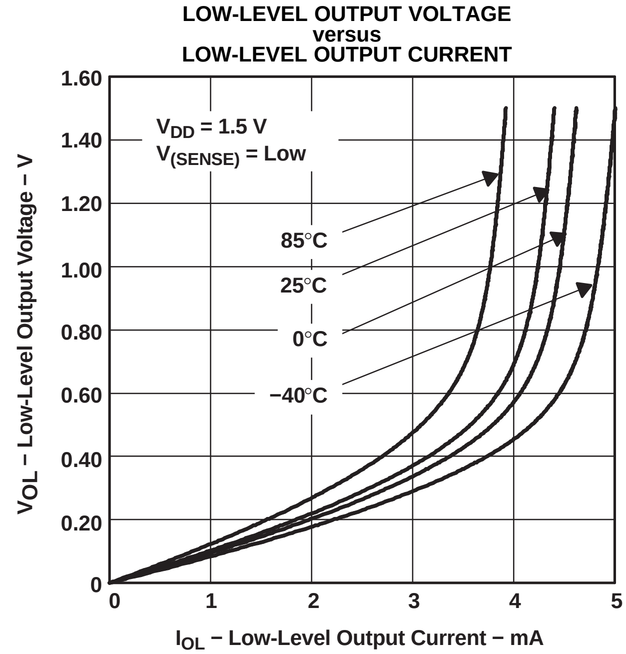


Figure 2.

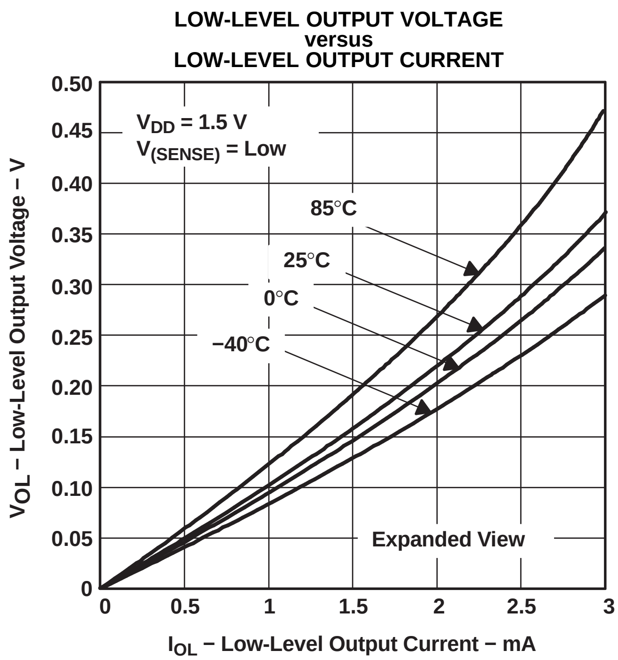


Figure 3.

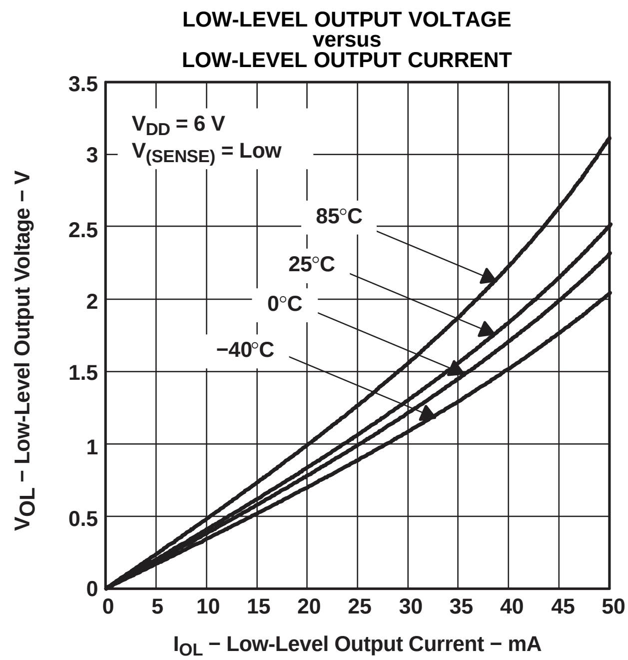


Figure 4.

TYPICAL CHARACTERISTICS (continued)

LOW-LEVEL OUTPUT VOLTAGE versus LOW-LEVEL OUTPUT CURRENT

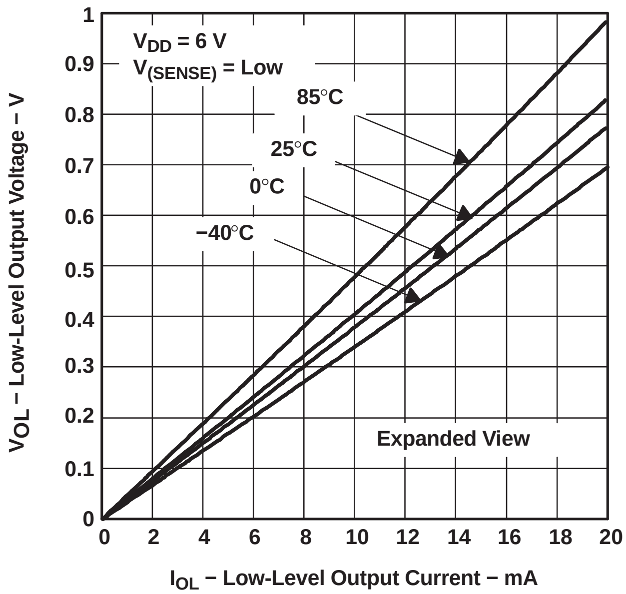


Figure 5.

NORMALIZED INPUT THRESHOLD VOLTAGE versus FREE-AIR TEMPERATURE AT V_{DD}

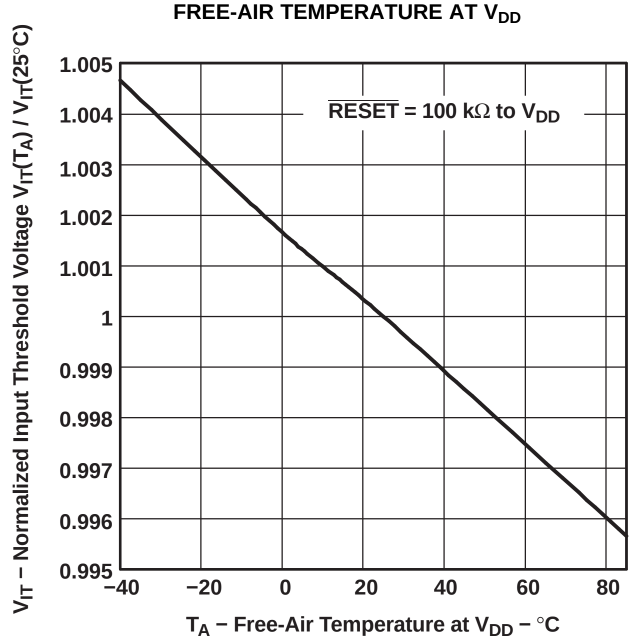


Figure 6.

MINIMUM PULSE DURATION AT V_{DD} versus V_{DD} THRESHOLD OVERDRIVE VOLTAGE

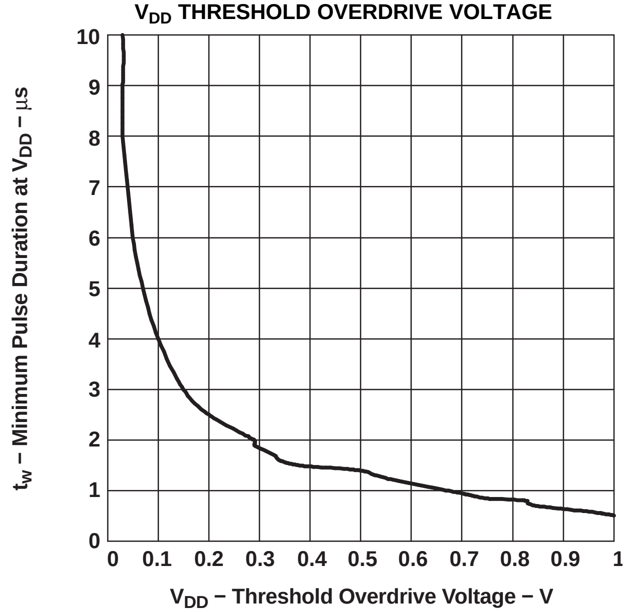


Figure 7.

MINIMUM PULSE DURATION AT LSENSE versus LSENSE THRESHOLD OVERDRIVE VOLTAGE

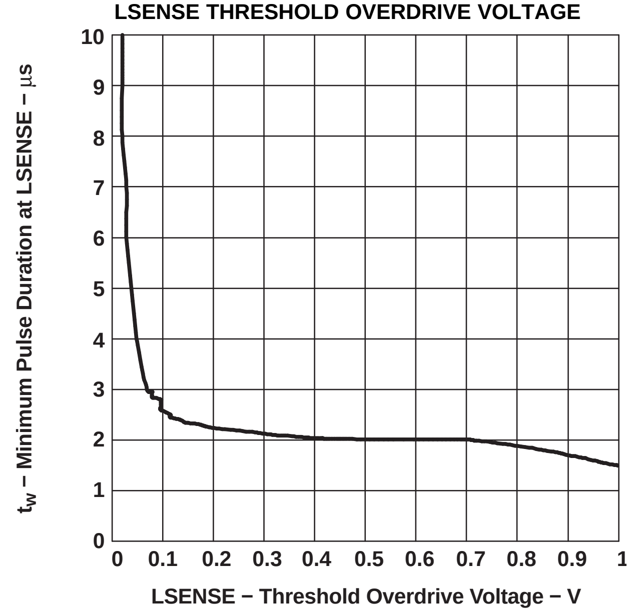


Figure 8.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3806I33QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PZHQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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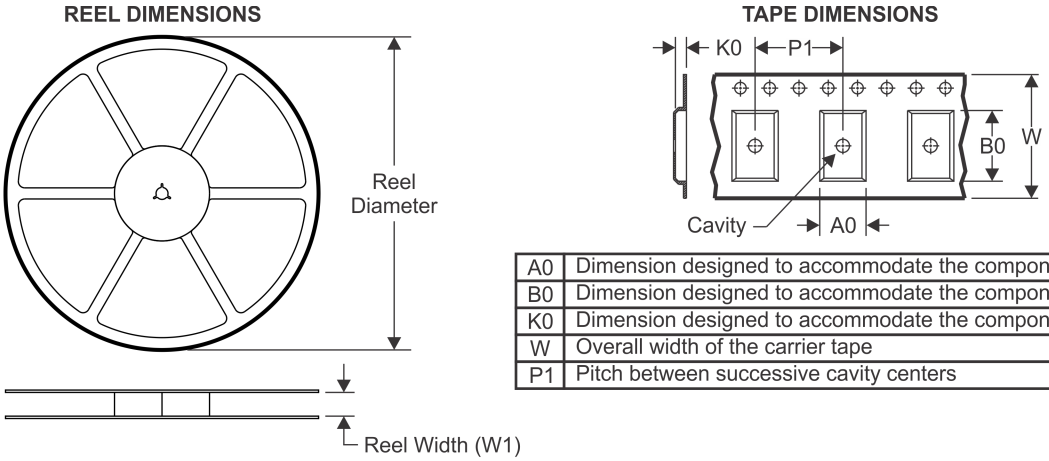
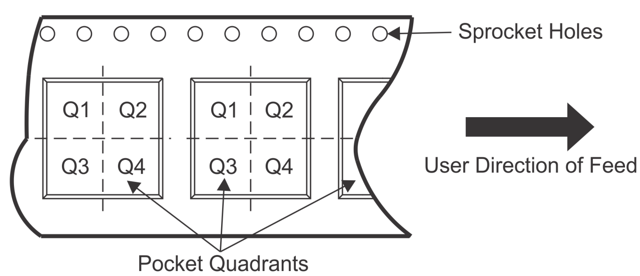
TAPE AND REEL INFORMATION



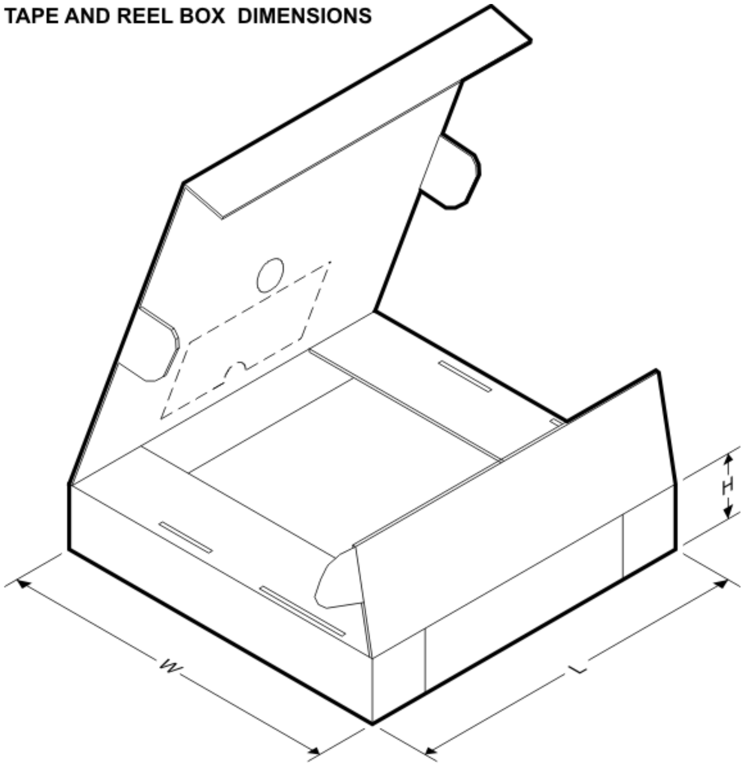
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

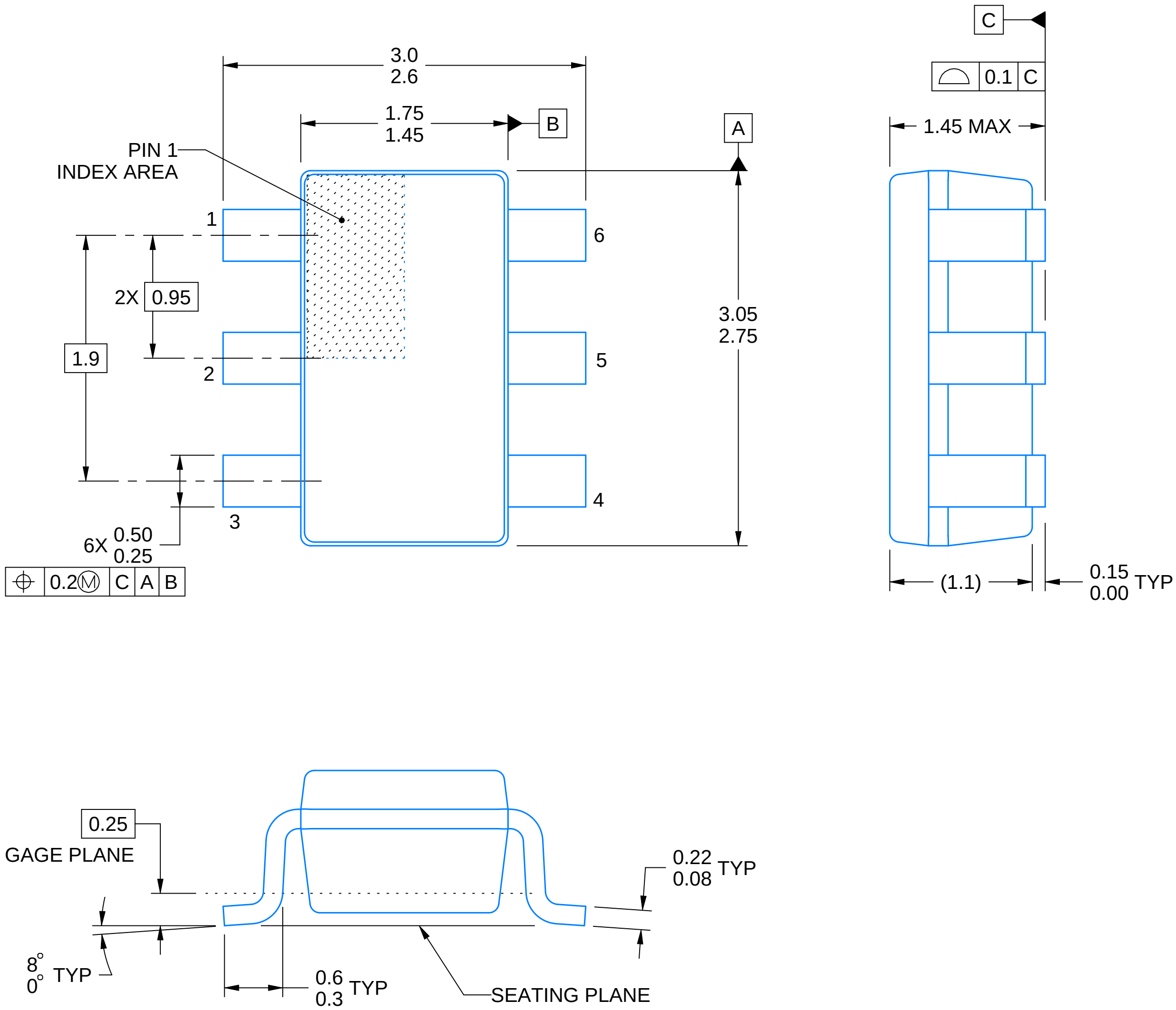
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3806I33QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3806I33QDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0



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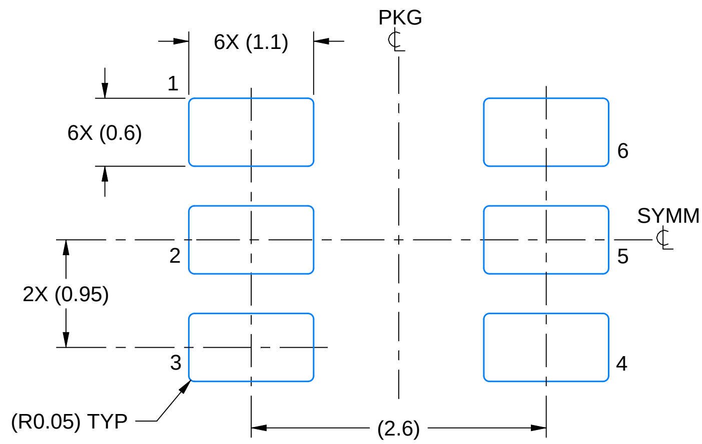
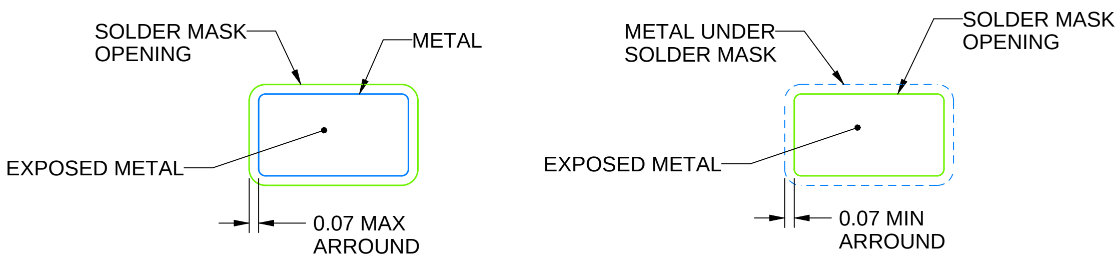
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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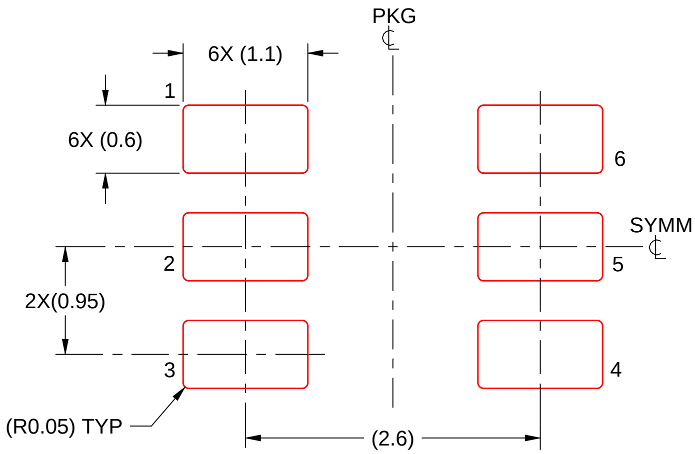
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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