Click here to ask about the production status of specific part numbers.

MAX22700D–MAX22702D
MAX22700E–MAX22702E

Ultra-High CMTI Isolated Gate Drivers

General Description

The MAX22700–MAX22702 are a family of single-channel isolated gate drivers with ultra-high common-mode transient immunity (CMTI) of 300kV/µs (typ). The devices are designed to drive silicon-carbide (SiC) or gallium-nitride (GaN) transistors in various inverter or motor control applications with different output gate-drive circuitry and B-side supply voltages. The devices feature variants with output options for gate driver common pin GNDB (MAX22700), Miller Clamp (MAX22701), and adjustable undervoltage-lockout UVLO (MAX22702). In addition, variants are offered as differential (D versions) or single-ended (E versions) inputs. All devices have integrated digital galvanic isolation using Maxim's proprietary process technology. The MAX22700–MAX22702 feature isolation for a withstand voltage rating of $3kV_{RMS}$ (narrow SOIC package) or $5kV_{RMS}$ (wide SOIC package) for 60 seconds.

All devices support a minimum pulse width of 20ns with a maximum pulse width distortion of 2ns. The part-to-part propagation delay is matched within 2ns (max) at +25°C ambient temperature, and 5ns (max) over the -40°C to +125°C operating temperature range. This feature reduces the power transistor's dead time, thus improving overall efficiency.

The MAX22700 and the MAX22702 have a maximum R_{DSON} of 1.25Ω for the low-side driver, and the MAX22701 has an R_{DSON} of 2.5Ω for the low-side driver. All devices have a maximum R_{DSON} of 4.5Ω for the high-side driver. See the *Ordering Information* for suffixes associated with each option.

The MAX22700–MAX22702 are available either in an 8-pin wide-body SOIC package with 8mm creepage and clearance, or in a smaller 8-pin narrow-body SOIC package with 4mm of creepage and clearance. The narrow SOIC package material has a minimum comparative tracking index (CTI) of 600, which gives it a group I rating in creepage tables, while the wide SOIC package material has a minimum CTI of 400, which gives it a group II rating in creepage tables. All devices are rated for operation at ambient temperatures of -40°C to +125°C.

Applications

- Isolated Gate Driver for Inverters
- Motor Drives
- UPS and PV Inverters

Benefits and Features

- Matching Propagation Delay
  - 20ns Minimum Pulse Width
  - 35ns Propagation Delay at Room Temperature
  - 2ns Part-to-Part Propagation Delay Matching at Room Temperature
  - 5ns Part-to-Part Propagation Delay Matching over -40°C to +125°C Temperature Range
- High CMTI (300kV/µs, typ)
- Robust Galvanic Isolation
  - Withstands $3kV_{RMS}$ (Narrow SOIC) or $5kV_{RMS}$ (Wide SOIC) for 60s (V_{ISO})
  - Continuously Withstands $600V_{RMS}$ (Narrow SOIC) or $848V_{RMS}$ (Wide SOIC) (V_{IOWM})
  - Withstands ±5kV Surge Between GNDA and V_{SSB} with 1.2/50µs Waveform
- Precision UVLO
- Options to Support a Broad Range of Applications
  - 3 Output Options: GNDB, Miller Clamp, or Adjustable UVLO
  - 2 Input Configurations: Single-Ended with Enable (E versions) or Differential (D versions)

Safety Regulatory Approvals

- UL According to UL1577
- cUL According to CSA Bulletin 5A
- VDE 0884-11 Basic Insulation (Wide SOIC) (Pending)

***Ordering Information* appears at end of data sheet.**

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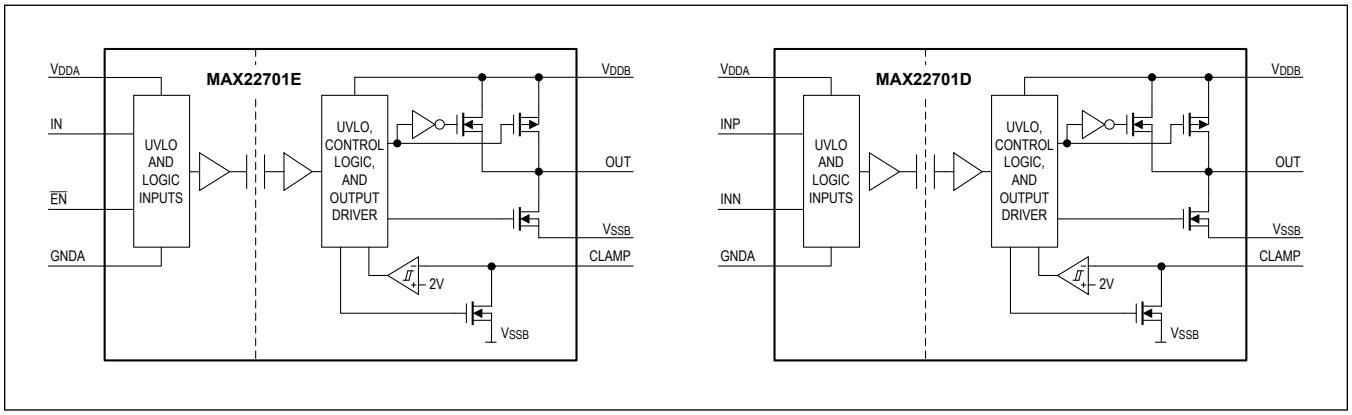
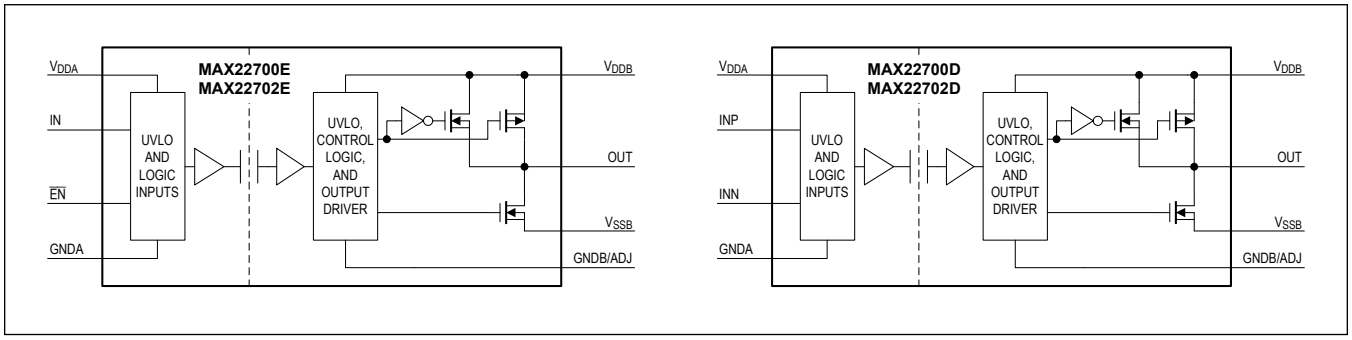
Functional Diagrams

MAX22701



MAX22700 and MAX22702



Absolute Maximum Ratings

V_{DDA} to GNDA ..... -0.3V to +6V
V_{DDB} to GNDB ..... -0.3V to +40V
GNDB to V_{SSB} ..... -0.3V to +40V
V_{DDB} to V_{SSB} ..... -0.3V to +40V
INP, INN, IN, $\overline{EN}$ to GNDA ..... -0.3V to +6V
V_{DDB} to ADJ ..... -0.3V to +6V
CLAMP to V_{SSB} ..... -0.3V to (V_{DDB} + 0.3V)
OUT to V_{SSB} ..... -0.3V to (V_{DDB} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
Narrow SOIC (derate 9.39mW/°C above +70°C) 750.89mW
Wide SOIC (derate 8.51mW/°C above +70°C) 681.14mW
Operating Temperature Range ..... -40ºC to +125ºC
Maximum Junction Temperature ..... +150ºC
Storage Temperature Range ..... -60ºC to +150ºC
Soldering Temperature (reflow) ..... +260ºC

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

8 Narrow SOIC

Package Code	S8MS+23
Outline Number	21-0041
Land Pattern Number	90-0096
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	106.54°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	44.91°C/W

8 Wide SOIC

Package Code	W8MS+6
Outline Number	21-100415
Land Pattern Number	90-100146
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	117.45°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	58.48°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

DC Electrical Characteristics

(V_{DDA} - V_{GNDA} = 5V, V_{DDB} - V_{SSB} = 20V, V_{GNDA} = V_{SSB} = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage	V_{DDA}	Relative to GNDA	3		5.5	V
	V_{DDB}	Relative to GNDB, MAX22700	13		28	
		Relative to V_{SSB}, MAX22701	13		28	
		Relative to V_{SSB}, MAX22702	6		28	
	V_{SSB}	Relative to GNDB, MAX22700	-16		0	
Differential Supply	V_{DIFF}	V_{DDB} - V_{SSB}, MAX22700	13		28	V
Undervoltage-Lockout Threshold	V_{UVLOAP}	V_{DDA} rising	2.69	2.82	2.95	V
	V_{UVLOAN}	V_{DDA} falling	2.59	2.72	2.85	
Undervoltage-Lockout Threshold Hysteresis	V_{UVLOA_HYST}			100		mV
Undervoltage-Lockout Threshold	V_{UVLOBP}	V_{DDB} rising, relative to GNDB, MAX22700		13	13.3	V
	V_{UVLOBN}	V_{DDB} falling, relative to GNDB, MAX22700	11.6	12		
	V_{UVLOBP}	V_{DDB} rising, relative to V_{SSB}, MAX22701		13	13.3	
	V_{UVLOBN}	V_{DDB} falling, relative to V_{SSB}, MAX22701	11.6	12		
	V_{UVLOBP}	V_{DDB} rising, relative to ADJ, MAX22702		2	2.05	
	V_{UVLOBN}	V_{DDB} falling, relative to ADJ, MAX22702	1.79	1.84		
Undervoltage-Lockout Threshold Hysteresis	V_{UVLOB_HYST}	MAX22700, MAX22701		1		V
		MAX22702		0.16		
SUPPLY CURRENT						
A-Side Quiescent Supply Current	I_{DDA}	V_{DDA} = 5V, INN/$\overline{EN}$ = V_{DDA}		5	6.5	mA
		V_{DDA} = 3.3V, INN/$\overline{EN}$ = V_{DDA}		3	4	
A-Side Active Supply Current	I_{DDA}	V_{DDA} = 5V, f_{PWM} = 1MHz		5	6.5	mA
		V_{DDA} = 3.3V, f_{PWM} = 1MHz		3	4	
B-Side Quiescent Positive Supply Current	I_{DDB}	INN/$\overline{EN}$ = V_{DDA}		3.5	6	mA
B-Side Active Positive Supply Current	I_{DDB}	f_{PWM} = 1MHz (*Note 2*)		6	10	mA
B-Side Ground Current	I_{GNDB}	MAX22700	-25			µA
LOGIC INTERFACE (INP, INN, IN, $\overline{EN}$)						
Input High Voltage	V_{IH}		0.7 x V_{DDA}			V
Input Low Voltage	V_{IL}				0.3 x V_{DDA}	V
Input Hysteresis	V_{HYS}			0.1 x V_{DDA}		mV
Input Pullup Current	I_{PU}	INN, $\overline{EN}$ (*Note 3*)	-10	-5	-1.5	µA
Input Pulldown Current	I_{PD}	INP, IN (*Note 3*)	1.5	5	10	µA
Input Capacitance	C_{IN}	f_{PWM} = 1MHz		2		pF

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = 5V, V_{DDB} - V_{SSB} = 20V, V_{GNDA} = V_{SSB} = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADJ (MAX22702 ONLY)							
Input Leakage Current	I_{ADJ}	V_{DDB} - V_{ADJ} = 3V		-100		100	nA
GATE DRIVER							
High-Side Transistor On-Resistance	R_{DSON_H}	I_{OUT} = -100mA (*Note 3*)				4.7	Ω
Low-Side Transistor On-Resistance	R_{DSON_L}	I_{OUT} = 100mA (*Note 3*)	MAX22700/ MAX22702			1.25	Ω
			MAX22701			2.5	
Output-Voltage High	V_{OH}	I_{OUT} = -10mA (*Note 3*)			19.95		V
Output-Voltage Low	V_{OL}	I_{OUT} = 10mA (*Note 3*)	MAX22700/ MAX22702		0.01		V
			MAX22701		0.02		
High-Side Transistor Peak Output Current	I_{OH}	C_L = 10nF, f_{PWM} = 1kHz (*Note 2*)		2.35	4		A
Low-Side Transistor Peak Output Current	I_{OL}	C_L = 10nF, f_{PWM} = 1kHz (*Note 2*)	MAX22700/ MAX22702	3.7	5.7		A
			MAX22701	1.9	2.85		
Active Pulldown Voltage	V_{OUTSD}	I_{OUT} = 150mA (*Note 3*)				2.2	V
MILLER CLAMP (MAX22701 ONLY)							
Miller Clamp Transistor On-Resistance	R_{DSON_CLMP}	I_{CLAMP} = 100mA (*Note 3*)				2.5	Ω
Miller Clamp Threshold	V_{TH_CLMP}			1.7	2	2.3	V
Miller Clamp Turn-On Time	t_{ON}	See Figure 2			20		ns
THERMAL SHUTDOWN							
Thermal-Shutdown Threshold	T_{SHDN}				160		°C
Thermal-Shutdown Hysteresis	T_{SHDN_HYS}				25		°C

Dynamic Characteristics

(V_{DDA} - V_{GNDA} = 5V, V_{DDB} - V_{SSB} = 20V, V_{GNDA} = V_{SSB} = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	(*Note 4*)			300		kV/µs
Minimum Pulse Width	PW_{MIN}	C_L = 200pF				20	ns
Maximum PWM Frequency	f_{PWM}			1			MHz
Propagation Delay (Figure 1)	t_{PLH}	C_L = 200pF, output is not connected to CLAMP pin (MAX22701) (*Note 5*)	T_A = +25°C to +125°C	34		39	ns
			T_A = +25°C	34	35	36	
			T_A = -40°C to +25°C	31		36	
	t_{PHL}		T_A = +25°C to +125°C	34		39	
			T_A = +25°C	34	35	36	
			T_A = -40°C to +25°C	31		36	
Part-to-Part Propagation Delay Matching (Figure 1)	t_{PM}	C_L = 200pF (*Note 5*)	T_A = +25°C			2	ns
			T_A = -40°C to +125°C, parts at the same temperature			5	
Pulse Width Distortion	PWD	C_L = 200pF, $\lvert t_{PLH} - t_{PHL} \rvert$				2	ns
Peak Eye Diagram Jitter	$T_{JIT(PK)}$	1MHz square wave, C_L = 200pF			60		ps
Rise Time (Figure 1)	t_R	C_L = 200pF, 20% to 80% (*Note 2*)				3.6	ns
Fall Time (Figure 1)	t_F	C_L = 200pF, 80% to 20% (*Note 2*)	MAX22700/ MAX22702			1.8	ns
			MAX22701			2.5	

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design and characterization.

Note 2: Not production tested. Guaranteed by design and characterization.

Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDA or V_{SSB}), unless otherwise noted.

Note 4: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. CMTI is tested with the transient generator connected between GNDA and V_{SSB} (V_{CM} = 1000V).

Note 5: Propagation delay is measured from 50% of the input to 2V at the output.

ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD		Human Body Model, All Pins		±4		kV

Insulation Characteristics - 8 Narrow SOIC

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.5 (t = 1s, partial discharge < 5pC)		1272		V_P
Maximum Repetitive-Peak Isolation Voltage	V_{IORM}	(*Note 6*)		848		V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (*Note 6*)		600		V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s (*Note 6*)		4242		V_P
Maximum Withstand Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (*Note 6*, *Note 7*)		3000		V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Basic insulation, 1.2/50µs pulse per IEC 61000-4-5 (*Note 6*, *Note 9*)		5		kV
Insulation Resistance	RIO	V_{IO} = 500V, T_A = 25°C		> 10^{12}		Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C		> 10^{11}		
		V_{IO} = 500V at T_S = 150°C		> 10^9		
Barrier Capacitance Side A-to-Side B	CIO	f_{SW} = 1MHz (*Note 8*)		1		pF
Minimum Creepage Distance	CPG	Narrow SOIC		4		mm
Minimum Clearance Distance	CLR	Narrow SOIC		4		mm
Internal Clearance		Distance through insulation		0.015		mm
Comparative Tracking Index	CTI	Material Group I (IEC 60112)		> 600		
Climate Category				40/125/21		
Pollution Degree (DIN VDE 0110, Table 1)				2		

Insulation Characteristics - 8 Wide SOIC

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.5 (t = 1s, partial discharge < 5pC)		1800		V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(*Note 6*)		1200		V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (*Note 6*)		848		V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s (*Note 6*)		7000		V_P
Maximum Withstand Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (*Note 6*, *Note 7*)		5000		V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Basic insulation, 1.2/50µs pulse per IEC 61000-4-5 (*Note 6*, *Note 9*)		5		kV
Insulation Resistance	RIO	V_{IO} = 500V, T_A = 25°C		> 10^{12}		Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C		> 10^{11}		
		V_{IO} = 500V at T_S = 150°C		> 10^9		
Barrier Capacitance Side A-to-Side B	CIO	f_{SW} = 1MHz (*Note 8*)		1		pF
Minimum Creepage Distance	CPG	Wide SOIC		8		mm
Minimum Clearance Distance	CLR	Wide SOIC		8		mm
Internal Clearance		Distance through insulation		0.015		mm
Comparative Tracking Index	CTI	Material Group II (IEC 60112)		> 400		
Climate Category				40/125/ 21		
Pollution Degree (DIN VDE 0110, Table 1)				2		

Note 6: V_{ISO}, V_{IOTM}, V_{IOSM}, V_{IOWM}, and V_{IORM} are defined by the IEC 60747-5-5 standard.
Note 7: Product is qualified at V_{ISO} for 60s and 100% production tested at 120% of V_{ISO} for 1s.
Note 8: Capacitance is measured with all pins on side A and side B tied together.
Note 9: Devices are immersed in oil during surge characterization.

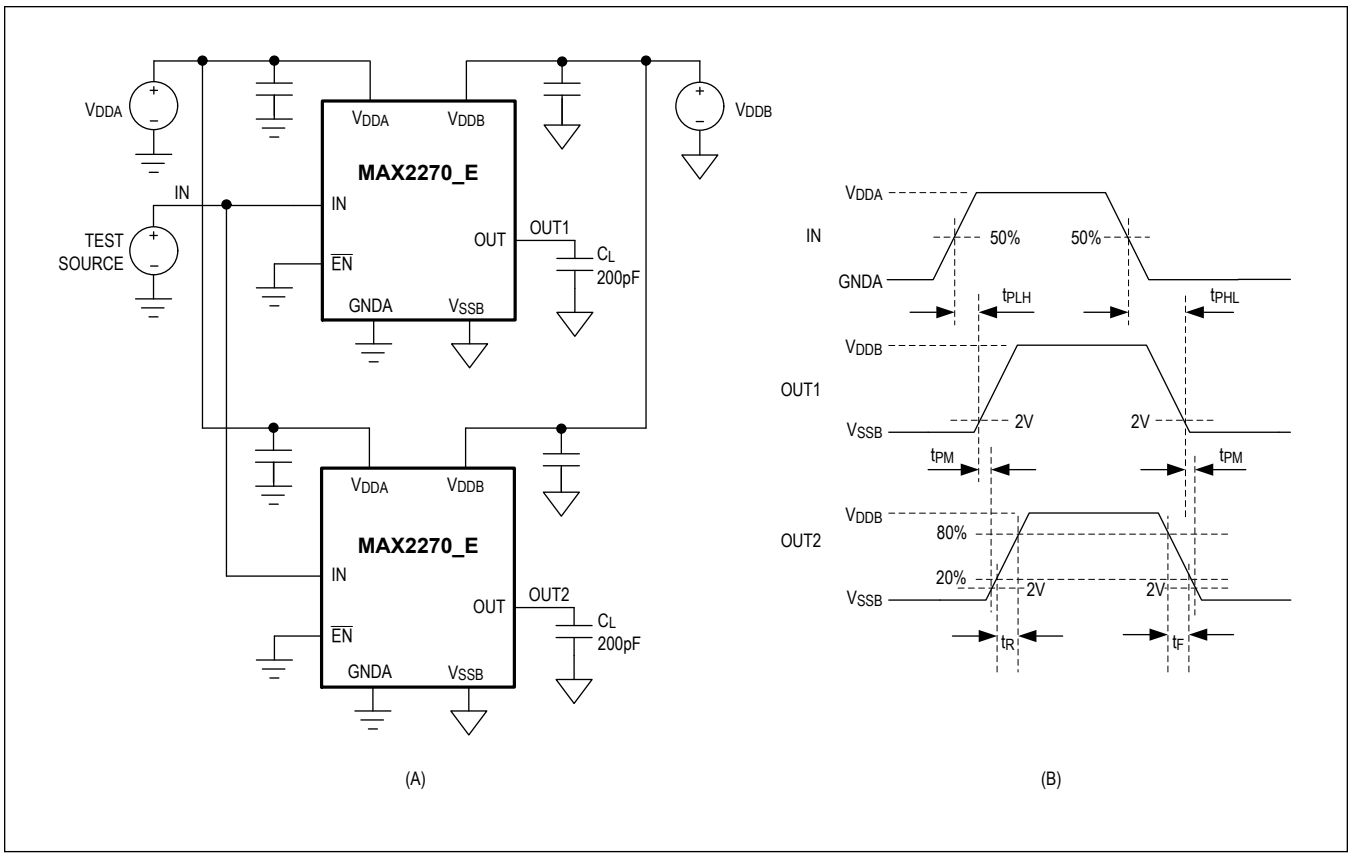


Figure 1. Test Circuit (A) and Timing Diagram (B)

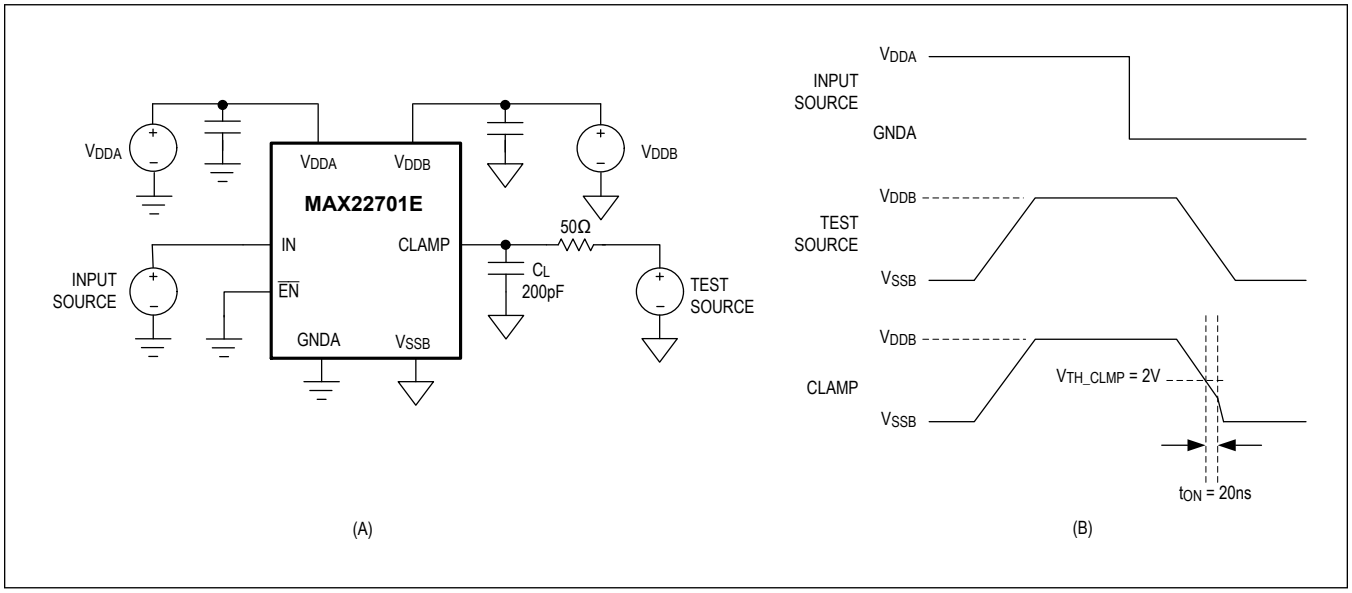
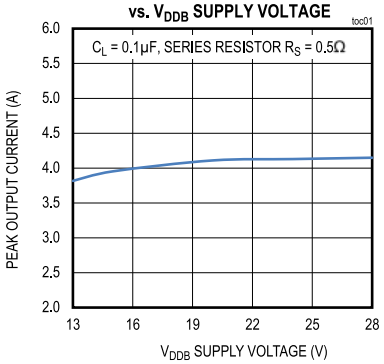


Figure 2. MAX22701 Miller Clamp Test Circuit (A) and Timing Diagram (B)

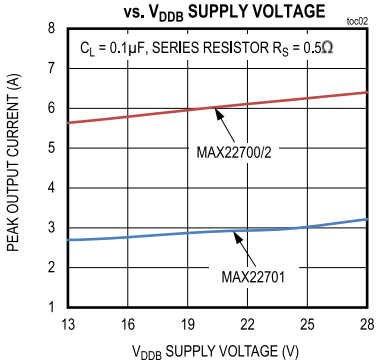
Typical Operating Characteristics

(V_{DDA} - V_{GNDA} = 5V, V_{DDB} - V_{SSB} = 20V, V_{GNDA} = V_{SSB}, T_A = +25°C, unless otherwise noted.)

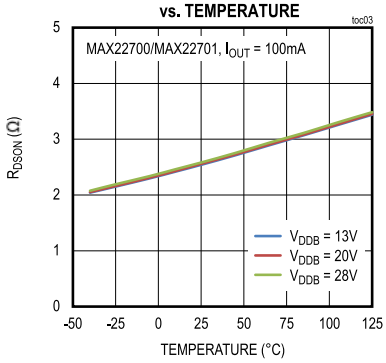
HIGH-SIDE PEAK OUTPUT CURRENT vs. V_{DDB} SUPPLY VOLTAGE



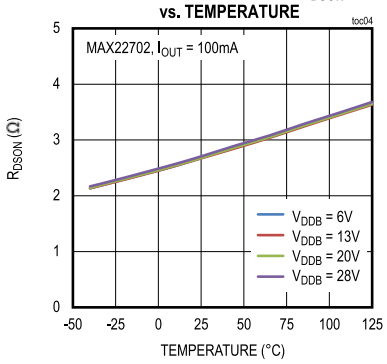
LOW-SIDE PEAK OUTPUT CURRENT vs. V_{DDB} SUPPLY VOLTAGE



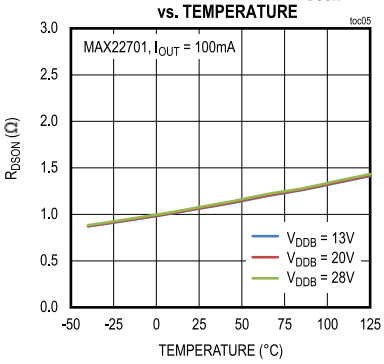
HIGH-SIDE TRANSISTOR R_{DSON} vs. TEMPERATURE



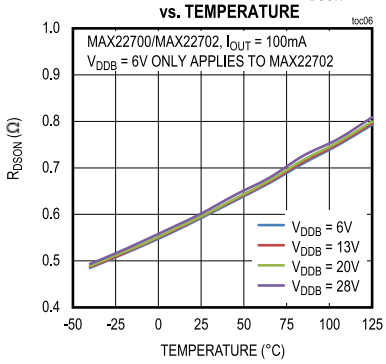
HIGH-SIDE TRANSISTOR R_{DSON} vs. TEMPERATURE



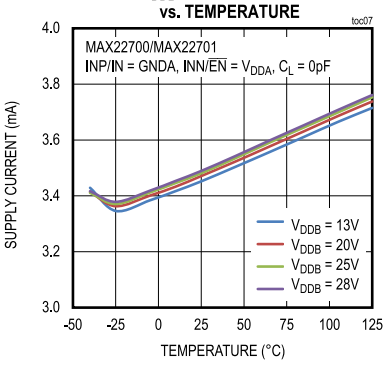
LOW-SIDE TRANSISTOR R_{DSON} vs. TEMPERATURE



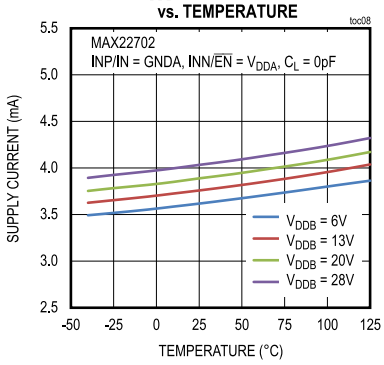
LOW-SIDE TRANSISTOR R_{DSON} vs. TEMPERATURE



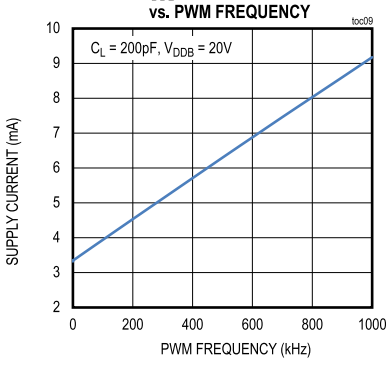
V_{DDB} SUPPLY CURRENT vs. TEMPERATURE



V_{DDB} SUPPLY CURRENT vs. TEMPERATURE



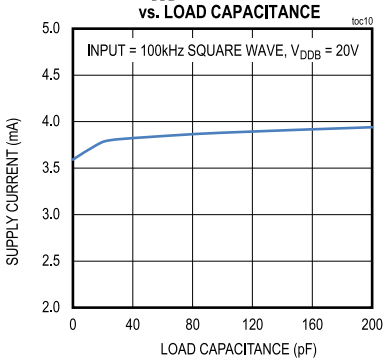
V_{DDB} SUPPLY CURRENT vs. PWM FREQUENCY



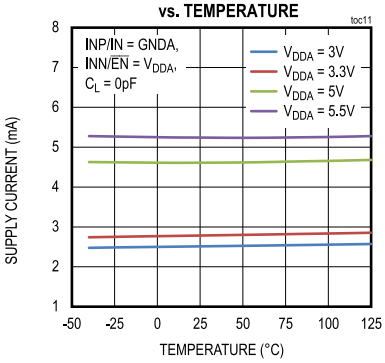
Typical Operating Characteristics (continued)

(V_{DDA} - V_{GNDA} = 5V, V_{DDB} - V_{SSB} = 20V, V_{GNDA} = V_{SSB}, T_A = +25°C, unless otherwise noted.)

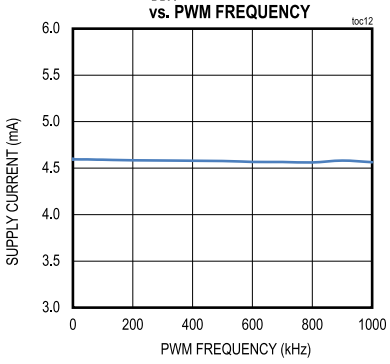
V_{DDB} SUPPLY CURRENT vs. LOAD CAPACITANCE



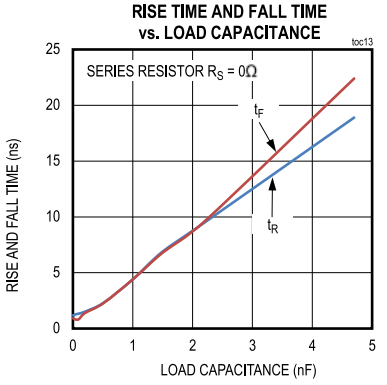
V_{DDA} SUPPLY CURRENT vs. TEMPERATURE



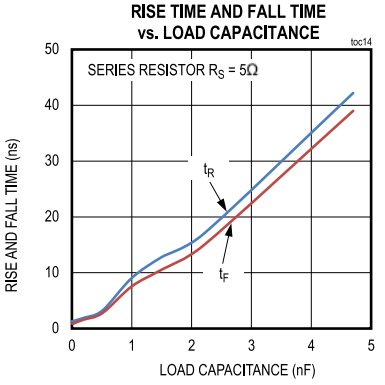
V_{DDA} SUPPLY CURRENT vs. PWM FREQUENCY



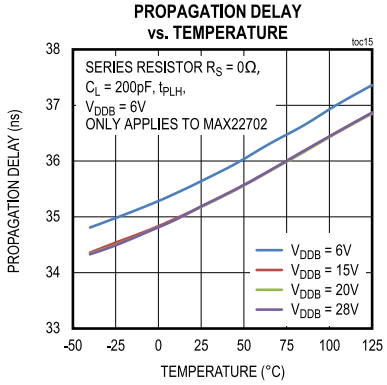
RISE TIME AND FALL TIME vs. LOAD CAPACITANCE



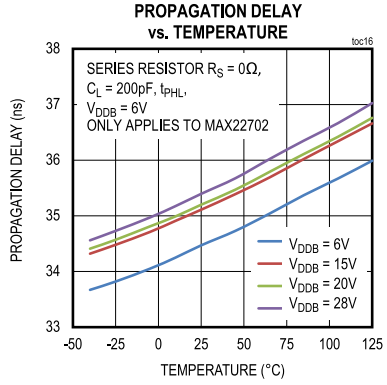
RISE TIME AND FALL TIME vs. LOAD CAPACITANCE



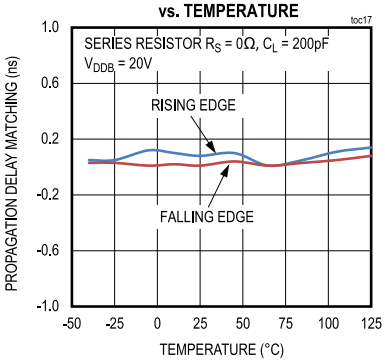
PROPAGATION DELAY vs. TEMPERATURE



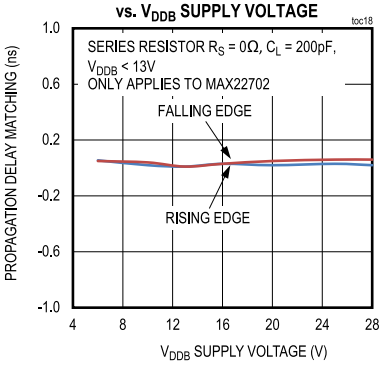
PROPAGATION DELAY vs. TEMPERATURE



PART-TO-PART PROPAGATION DELAY MATCHING vs. TEMPERATURE



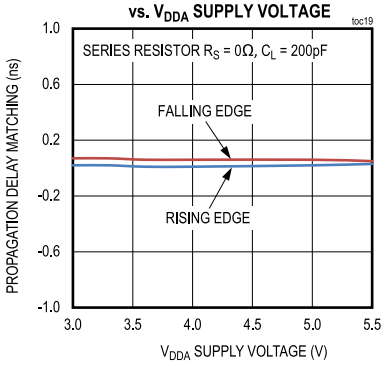
PART-TO-PART PROPAGATION DELAY MATCHING vs. V_{DDB} SUPPLY VOLTAGE



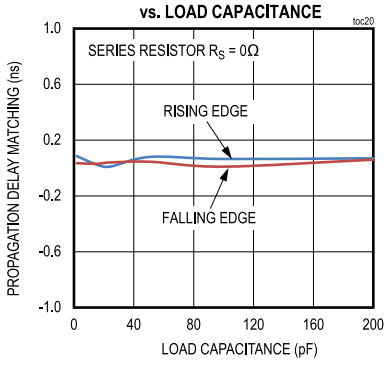
Typical Operating Characteristics (continued)

(V_{DDA} - V_{GNDA} = 5V, V_{DDB} - V_{SSB} = 20V, V_{GNDA} = V_{SSB}, T_A = +25°C, unless otherwise noted.)

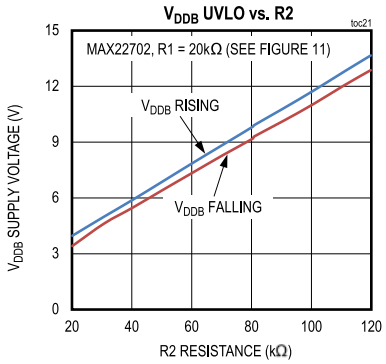
PART-TO-PART PROPAGATION DELAY MATCHING vs. V_{DDA} SUPPLY VOLTAGE



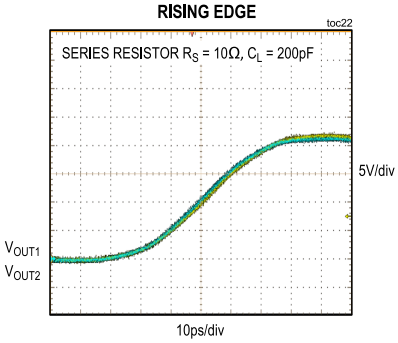
PART-TO-PART PROPAGATION DELAY MATCHING vs. LOAD CAPACITANCE



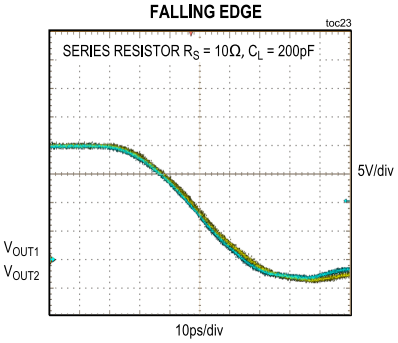
V_{DDB} UVLO vs. R2



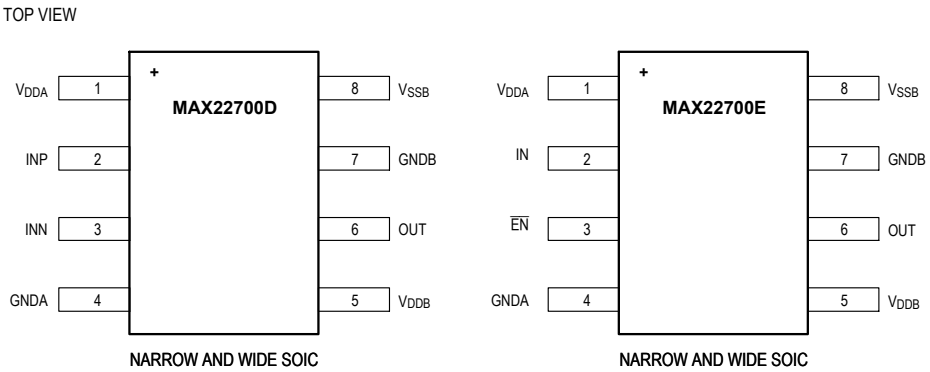
PART-TO-PART PROPAGATION DELAY MATCHING RISING EDGE



PART-TO-PART PROPAGATION DELAY MATCHING FALLING EDGE



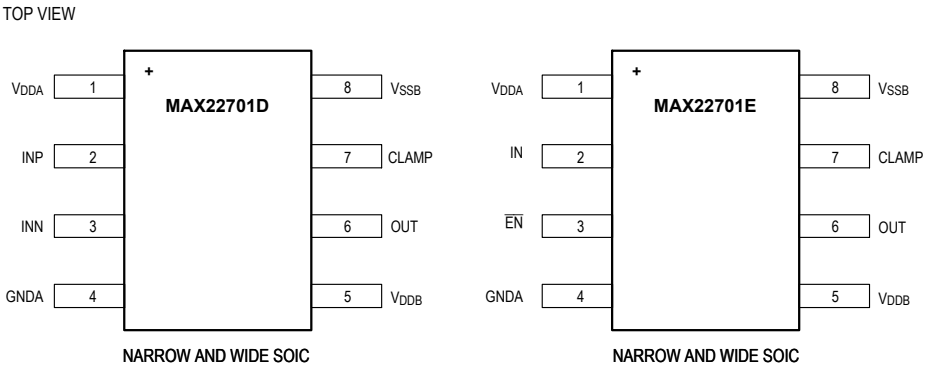
Pin Configurations - MAX22700



Pin Description - MAX22700

PIN		NAME	FUNCTION	REF SUPPLY
MAX22700D	MAX22700E			
POWER				
1	1	V_{DDA}	Power Supply Input for Side A (Transmitter Side). Bypass V_{DDA} to GNDA with 1nF || 0.1µF || 1µF ceramic capacitors as close as possible to the pin.	GNDA
4	4	GNDA	Ground Reference for Side A (Transmitter Side).	GNDA
5	5	V_{DDB}	Positive Power Supply Input for Side B (Driver Side). Bypass V_{DDB} to V_{SSB} with 1nF || 0.1µF || 1µF ceramic capacitors as close as possible to the pin. Place an additional 22µF capacitor between V_{DDB} and V_{SSB}.	GNDB
8	8	V_{SSB}	Negative Power Supply Input for Side B (Driver Side).	GNDB
7	7	GNDB	Gate Driver Common Pin. Connect to the power transistor's source pin. The B-side UVLO is referenced to GNDB in the MAX22700 versions.	GNDB
INPUTS				
2	-	INP	Non-Inverting PWM Input on Side A (D Version). Has a weak internal pulldown. Connect the differential PWM control inputs to INP and INN. Refer to Table 2 for Inputs vs. Output Truth table.	GNDA
3	-	INN	Inverting PWM Input on Side A (D Version). Has a weak internal pullup to V_{DDA}. Connect the differential PWM control inputs to INP and INN. Refer to Table 2 for Inputs vs. Output Truth table.	GNDA
-	2	IN	Single-Ended PWM Input on Side A (E Version). Has a weak internal pulldown. Refer to Table 3 for Inputs vs. Output Truth table.	GNDA
-	3	$\overline{EN}$	Active-Low Enable on Side A (E Version). Has a weak internal pullup to V_{DDA}.	GNDA
OUTPUT				
6	6	OUT	Gate Driver Output on Side B.	GNDB

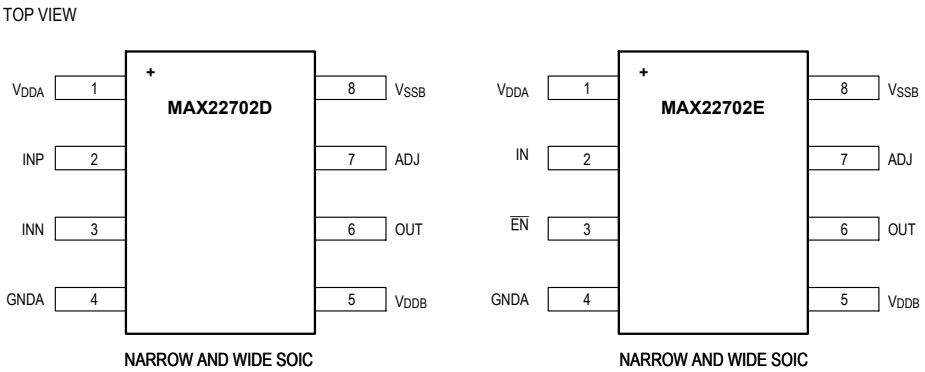
Pin Configurations - MAX22701



Pin Description - MAX22701

PIN		NAME	FUNCTION	REF SUPPLY
MAX22701D	MAX22701E			
POWER				
1	1	V_{DDA}	Power Supply Input for Side A (Transmitter Side). Bypass V_{DDA} to GNDA with 1nF || 0.1µF || 1µF ceramic capacitors as close as possible to the pin.	GNDA
4	4	GNDA	Ground Reference for Side A (Transmitter Side).	GNDA
5	5	V_{DDB}	Positive Power Supply Input for Side B (Driver Side). Bypass V_{DDB} to V_{SSB} with 1nF || 0.1µF || 1µF ceramic capacitors as close as possible to the pin. Place an additional 22µF capacitor between V_{DDB} and V_{SSB}.	V_{SSB}
8	8	V_{SSB}	Negative Power Supply Input for Side B (Driver Side).	V_{SSB}
INPUTS				
2	-	INP	Non-Inverting PWM Input on Side A (D Version). Has a weak internal pulldown. Connect the differential PWM control inputs to INP and INN. Refer to Table 2 for Inputs vs. Output Truth table.	GNDA
3	-	INN	Inverting PWM Input on Side A (D Version). Has a weak internal pullup to V_{DDA}. Connect the differential PWM control inputs to INP and INN. Refer to Table 2 for Inputs vs. Output Truth table.	GNDA
-	2	IN	Single-Ended PWM Input on Side A (E Version). Has a weak internal pulldown. Refer to Table 3 for Inputs vs. Output Truth table.	GNDA
-	3	$\overline{EN}$	Active-Low Enable on Side A (E Version). Has a weak internal pullup to V_{DDA}.	GNDA
INPUT/OUTPUT				
7	7	CLAMP	Active Miller Clamp Input/Output on Side B. Prevents false turn-on of the power transistor.	V_{SSB}
OUTPUT				
6	6	OUT	Gate Driver Output on Side B.	V_{SSB}

Pin Configurations - MAX22702



Pin Description - MAX22702

PIN		NAME	FUNCTION	REF SUPPLY
MAX22702D	MAX22702E			
POWER				
1	1	V_{DDA}	Power Supply Input for Side A (Transmitter Side). Bypass V_{DDA} to GNDA with 1nF || 0.1µF || 1µF ceramic capacitors as close as possible to the pin.	GNDA
4	4	GNDA	Ground Reference for Side A (Transmitter Side).	GNDA
5	5	V_{DDB}	Positive Power Supply Input for Side B (Driver Side). Bypass V_{DDB} to V_{SSB} with 1nF || 0.1µF || 1µF ceramic capacitors as close as possible to the pin. Place an additional 22µF capacitor between V_{DDB} and V_{SSB}.	V_{SSB}
8	8	V_{SSB}	Negative Power Supply Input for Side B (Driver Side).	V_{SSB}
INPUTS				
2	-	INP	Non-Inverting PWM Input on Side A (D Version). Has a weak internal pulldown. Connect the differential PWM control inputs to INP and INN. Refer to Table 2 for Inputs vs. Output Truth table.	GNDA
3	-	INN	Inverting PWM Input on Side A (D Version). Has a weak internal pullup to V_{DDA}. Connect the differential PWM control inputs to INP and INN. Refer to Table 2 for Inputs vs. Output Truth table.	GNDA
-	2	IN	Single-Ended PWM Input on Side A (E Version). Has a weak internal pulldown. Refer to Table 3 for Inputs vs. Output Truth table.	GNDA
-	3	$\overline{EN}$	Active-Low Enable on Side A (E Version). Has a weak internal pullup to V_{DDA}.	GNDA
7	7	ADJ	Adjustable UVLO Input on Side B. Connect external resistors between V_{DDB} and ADJ and between ADJ and the power transistor's source pin to adjust the B-side UVLO.	V_{SSB}
OUTPUT				
6	6	OUT	Gate Driver Output on Side B.	V_{SSB}

Detailed Description

The MAX22700–MAX22702 are a family of single-channel isolated gate drivers with an ultra-high CMTI of 300kV/µs (typ). All devices have integrated digital galvanic isolation with an isolation rating of $3kV_{RMS}$ in an 8-pin narrow-body SOIC package, or $5kV_{RMS}$ in an 8-pin wide-body SOIC package. This family of devices offers high common-mode transient immunity, high electromagnetic interference (EMI) immunity, and stable temperature performance through Maxim's proprietary process technology. The devices feature variants with output options for gate driver common pin GNDB (MAX22700), Miller clamp (MAX22701), and adjustable UVLO (MAX22702). In addition, variants are offered as differential inputs INP and INN (D versions) or single-ended input IN with enable $\overline{EN}$ (E versions). Refer to the *Ordering Information* for details.

The MAX22700 has a gate driver common pin (GNDB) that is a reference ground for V_{DDB} and V_{SSB}. V_{SSB} has a voltage range between -16V and 0V with reference to GNDB. The MAX22701 has an active Miller clamp pin, CLAMP, which prevents false turn-on of the external power transistor caused by the Miller current. The MAX22702 provides an adjustable B-side UVLO, offering design flexibility with different types of external power transistors.

All devices support a minimum pulse width of 20ns with maximum pulse-width distortion of 2ns. The part-to-part propagation delay is matched within 2ns maximum at +25°C ambient temperature, and is guaranteed to be within 5ns maximum over the temperature range of -40°C to +125°C.

All MAX22700–MAX22702 have a default-low output. The default is the state the output assumes when the input is either not powered or is open-circuit. The output is set to logic-low when side A or side B supply is in UVLO, the device is in thermal shutdown, or $\overline{EN}$ is high (E versions).

Output Driver Stage

The output driver stage of the MAX22700–MAX22702 features a pullup structure and a pulldown structure. The pullup structure consists of a pMOS transistor and a nMOS transistor in parallel (see the *Functional Diagrams*). The pMOS transistor has a maximum R_{DSON} of 4.5Ω. The nMOS transistor only turns on for a short period of time during the output low-to-high transition and provides a boost current to enable the fast turn-on of the device. The nMOS transistor has a much lower on-resistance than the pMOS transistor; thus the parallel combination of the nMOS and the pMOS enables a faster turn-on during the output low-to-high transition.

The pulldown structure of the MAX22700–MAX22702 consists of a nMOS transistor. The nMOS transistor in the MAX22700 and the MAX22702 has a maximum R_{DSON} of 1.25Ω, while the nMOS in the MAX22701 has an R_{DSON} of 2.5Ω. For the MAX22701, when both OUT and CLAMP pins are connected to the gate of the external power transistor, an additional nMOS is connected in parallel to the pulldown nMOS transistor to prevent false turn-on of the external power transistor by providing an additional low-impedance path to V_{SSB}. Refer to *Active Miller Clamp (MAX22701 Only)* section and the *Functional Diagrams* for details.

Digital Isolation

The MAX22700–MAX22702 provide basic galvanic isolation for digital signals transmitted between two ground domains, and block high-voltage/high-current transients. The devices in the narrow-body SOIC package withstand differences of up to $3kV_{RMS}$ for up to 60 seconds, and up to $848V_{PEAK}$ of continuous isolation. The devices in the wide-body SOIC package withstand differences of up to $5kV_{RMS}$ for up to 60 seconds and up to $1200V_{PEAK}$ of continuous isolation. Refer to Table 1 for certification information.

The devices have two supply inputs (V_{DDA} and V_{DDB}) that independently set the logic levels on either side of the device. V_{DDA} and V_{DDB} are referenced to GNDA and V_{SSB}, respectively. Logic input and output levels match the supply voltages used in the associated power domain. The difference in ground potential between the two power domains can be as large as V_{IOWM} for extended periods of time and withstand surge voltages up to 5kV. Data transfer integrity is maintained for a differential ground potential change up to 300kV/µs (typ).

Table 1. Safety Regulatory Approvals

UL
The MAX22700–MAX22702 are certified under UL1577. For more details, refer to file E351759.
Devices in narrow SOIC package are rated up to $3000V_{RMS}$ isolation voltage for single protection.
Devices in wide SOIC package are rated up to $5000V_{RMS}$ isolation voltage for single protection.
cUL (Equivalent to CSA notice 5A)
The MAX22700–MAX22702 are certified up to $3000V_{RMS}$ (narrow SOIC package) or $5000V_{RMS}$ (wide SOIC package) for single protection. For more details, refer to file E351759.
VDE (Pending)
The MAX22700–MAX22702 in wide SOIC are certified to DIN VDE V 0884-11: 2017-1. Basic Insulation, Maximum Transient Isolation Voltage $7000V_{PK}$, Maximum Repetitive Peak Isolation Voltage $1200V_{PK}$

Note: *These couplers are suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.*

Unidirectional Channel and Active Pulldown

The MAX22700–MAX22702 have an unidirectional channel that passes data in one direction, as indicated in the *Functional Diagrams*. The two internal transistors in the output driver are configured for push-pull operation and feature an active pulldown function to turn off the external power transistor when either side of the power supply is in UVLO. This prevents the external power transistor from falsely turning on during startup or UVLO.

INN vs. $\overline{EN}$ Function

The MAX2270_D features differential PWM inputs (INP and INN). The differential inputs reject input glitches and prevent false turn-on of the output. The output holds the previous value when a glitch is detected on either input (Figure 3). The MAX2270_E features a single-ended input (IN) and an active-low input enable ($\overline{EN}$). The $\overline{EN}$ pin allows the output (OUT) to be quickly set to logic-low, turning off the external power transistor. The output remains at logic-low until the PWM input (IN) receives a logic-high signal (Figure 4).

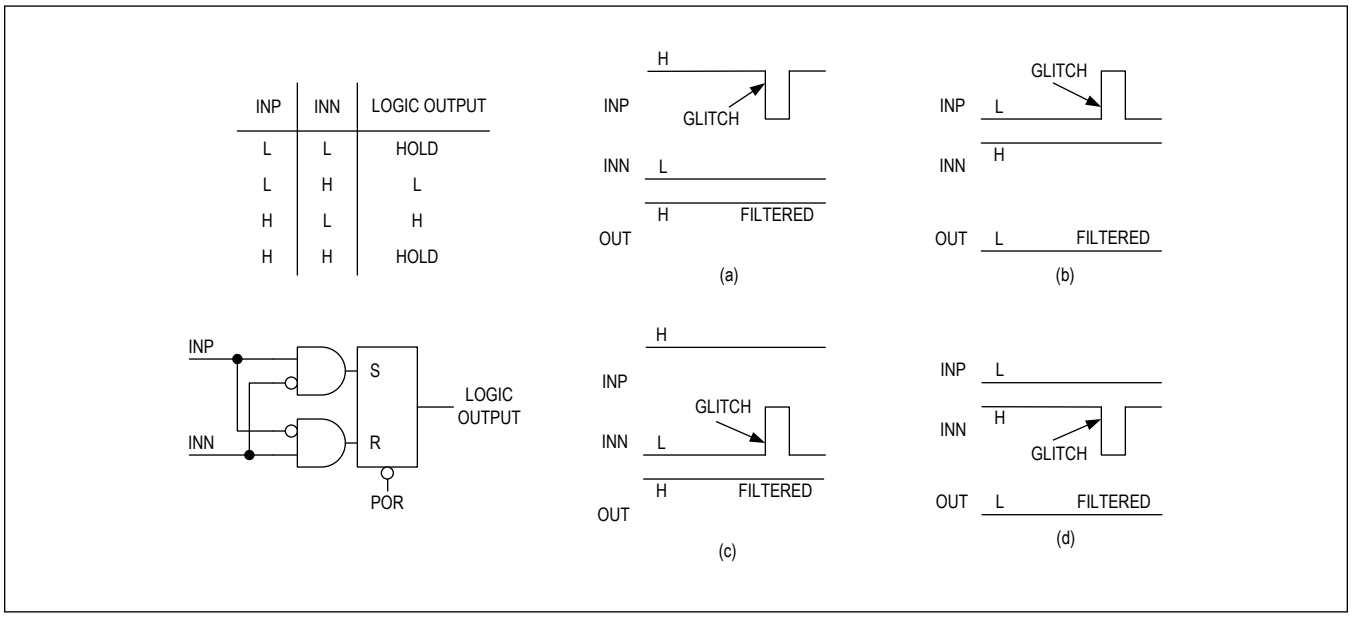


Figure 3. MAX2270_D Differential Inputs

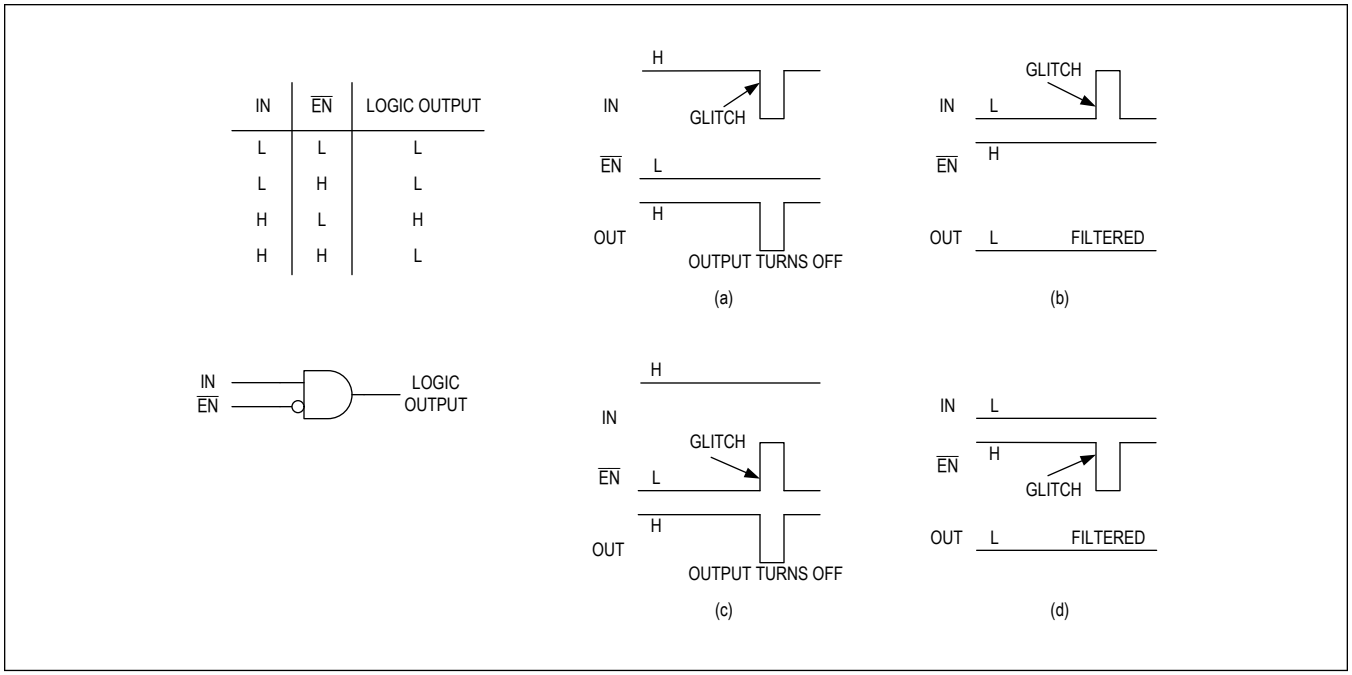


Figure 4. MAX2270_E Single-Ended Input with Enable

Current sources are used at both A-side inputs to prevent the output from falsely turning on by input glitches or noise. The INN pin has a weak pullup and the INP has a weak pulldown in the MAX2270_D devices. The $\overline{EN}$ pin has a weak pullup and the IN pin has a weak pulldown in the MAX2270_E devices. Refer to Table 2 and Table 3 for the Inputs vs. Output Truth Tables.

Table 2. MAX2270_D Inputs vs. Output Truth Table

INP	INN	OUT
Low	Low	Hold
Low	High	Low
High	Low	High
High	High	Hold

Table 3. MAX2270_E Inputs vs. Output Truth Table

IN	$\overline{EN}$	OUT
Low	Low	Low
Low	High	Low (Default)
High	Low	High
High	High	Low (Default)

Undervoltage Lockout (UVLO)

The V_{DDA} and V_{DDB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage condition is detected on either supply, the output is set to logic-low (default state) to turn off the external power transistor, regardless of the state of the MAX22700–MAX22702 inputs. The B-side UVLO has an internal filter to reject any V_{DDB} glitches less than 32µs (typ) (see Figure 9 and Figure 10). Figure 5 through Figure 8 show the behavior of the outputs during power-up and power-down.

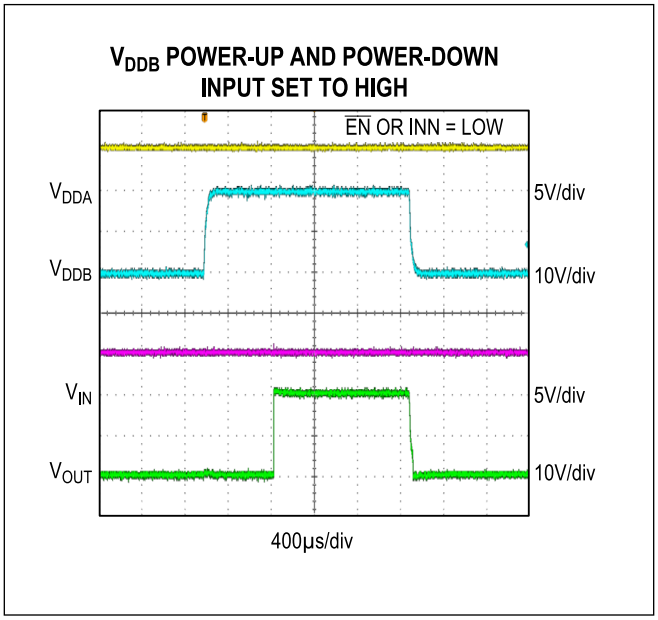


Figure 5. V_{DDB} Undervoltage Lockout Behavior (Input High)

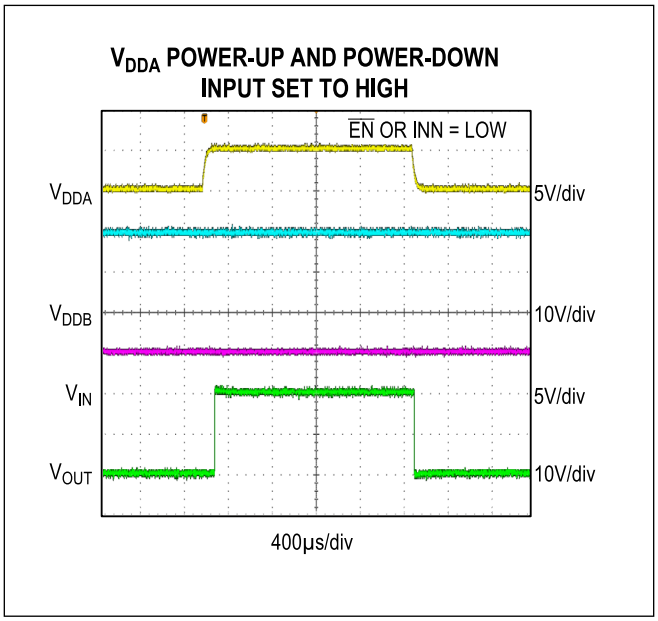


Figure 6. V_{DDA} Undervoltage Lockout Behavior (Input High)

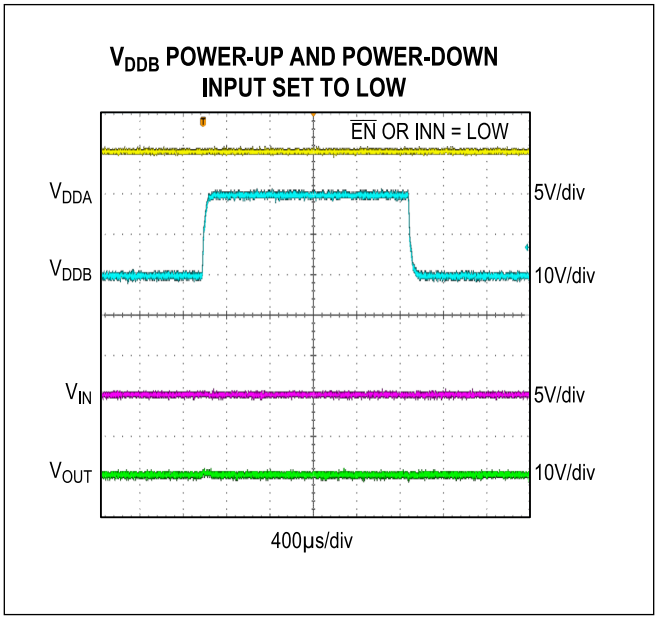


Figure 7. V_{DDB} Undervoltage Lockout Behavior (Input Low)

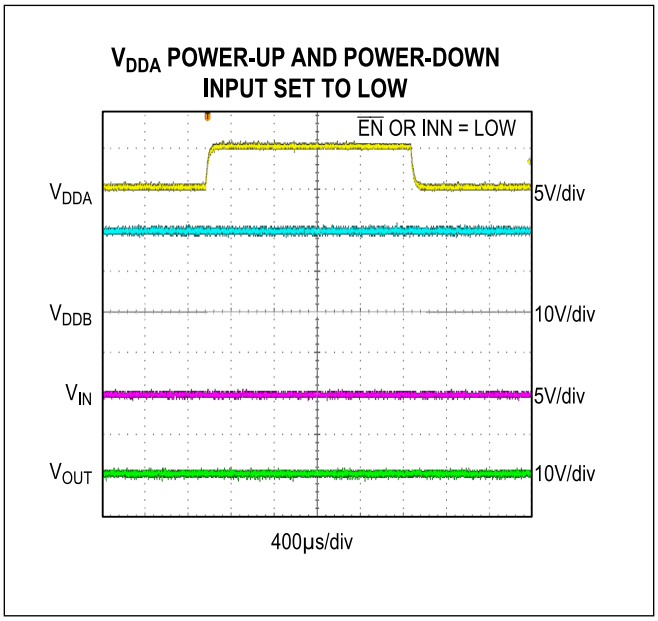


Figure 8. V_{DDA} Undervoltage Lockout Behavior (Input Low)

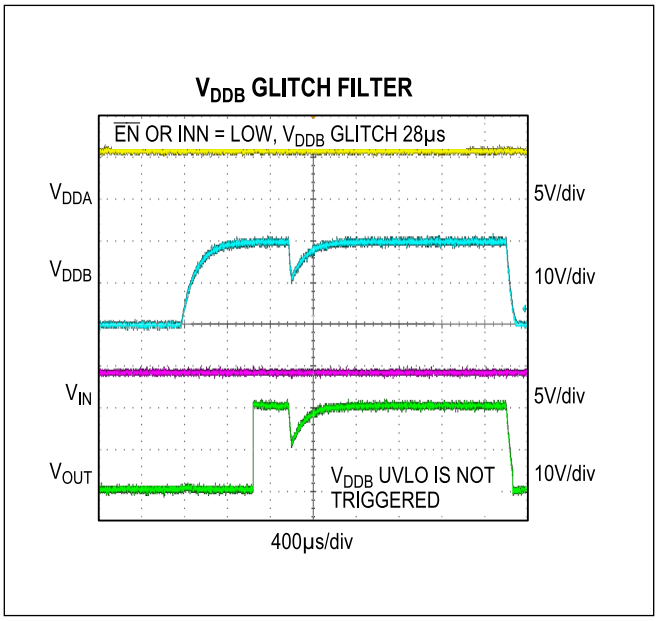


Figure 9. V_{DDB} Undervoltage Lockout Glitch Filter, UVLO Not Triggered

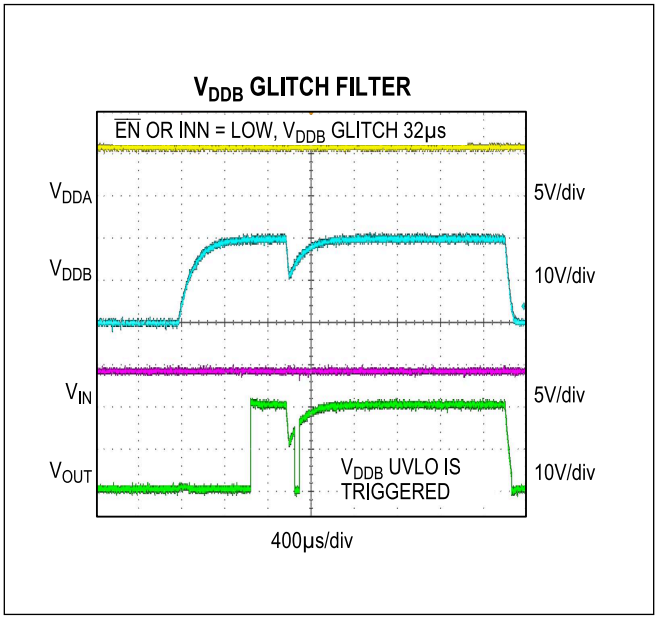


Figure 10. V_{DDB} Undervoltage Lockout Glitch Filter, UVLO Triggered

Thermal Shutdown

The MAX22700–MAX22702 operate at an ambient temperature up to +125°C on a properly designed multilayer PCB. Operating at higher voltages or with heavy output loads increases the junction temperature and power dissipation, and also reduce the maximum allowable operating temperature. See the *Package Information*, *Absolute Maximum Ratings* and *Safety Limits* sections for details.

The MAX22700–MAX22702 is in thermal shutdown when the junction temperature of the device exceeds +160°C (typ). During thermal shutdown, the output is set to logic-low to turn off the external power transistor regardless of the state of the MAX22700–MAX22702 inputs.

Active Miller Clamp (MAX22701 Only)

The MAX22701 features an active Miller clamp to prevent false turn-on of the external power transistor caused by the Miller current. When the external high-side transistor is turned on after the external low-side transistor is turned off, the internal Miller clamp transistor starts to engage when the Miller clamp pin voltage drops below the 2V threshold, and it provides a low-impedance path to direct the Miller current to V_{SSB}. Refer to Figure 2 for a Miller clamp timing diagram.

Adjustable UVLO (MAX22702 Only)

The MAX22702 features an adjustable B-side UVLO to accommodate UVLO requirements of different types of external power transistors. To set a user-defined B-side UVLO, connect external resistors between V_{DDB} and ADJ, and between ADJ and the external power transistor ground so that:

$$V_{ADJ\_UVLO} = 2 \times (1 + R2 \div R1)$$

where R1 is placed between V_{DDB} and ADJ, and R2 is placed between ADJ and the external power transistor ground (see Figure 11).

For example, to set the B-side UVLO to 13V, connect 20kΩ (R1) between V_{DDB} and ADJ. R2 is:

$$(13 \div 2 - 1) \times 20 = 110k\Omega$$

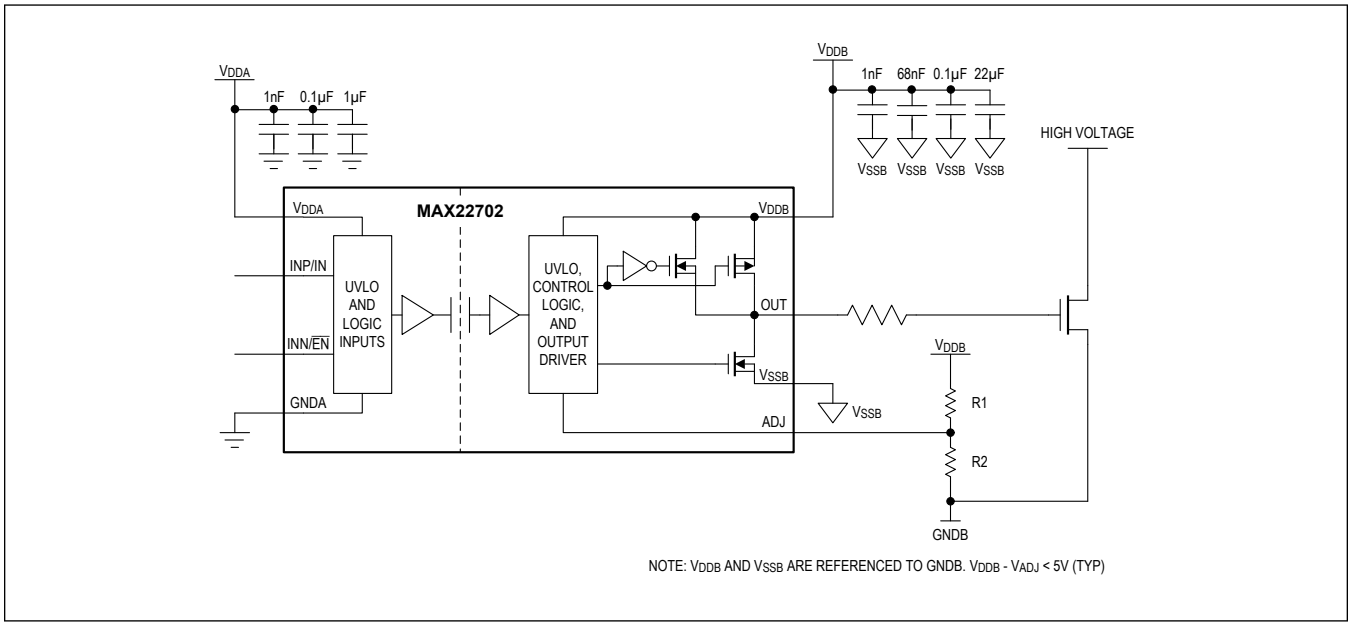


Figure 11. Example Circuit for MAX22702 Adjustable UVLO

Safety Limits

Damage to the IC can result in a low-resistance path to ground or to the supply and, without current limiting, the MAX22700–MAX22702 could dissipate excessive amounts of power. Excessive power dissipation can damage the die and result in damage to the isolation barrier, potentially causing long-term reliability issues. Table 4 shows the safety limits for the MAX22700–MAX22702.

The maximum safety temperature (T_S) for the device is the +150°C maximum junction temperature specified in the *Absolute Maximum Ratings*. The power dissipation (P_D) and junction-to-ambient thermal impedance (θ_{JA}) determine the junction temperature. Thermal impedance values (θ_{JA} and θ_{JC}) are available in the *Package Information* section of the data sheet and power dissipation calculations are discussed in the *Calculating Power Dissipation* section. Calculate the junction temperature (T_J) as:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Figure 12 to Figure 14 show the thermal derating curves for safety limiting the power and the current of the devices. Ensure that the junction temperature does not exceed +150°C.

Table 4. Safety Limiting Values for the MAX22700–MAX22702

PARAMETER	SYMBOL	TEST CONDITIONS		MAX	UNIT
Safety Operating Current on B-Side Pins	I_{OUT}	T_J = 150°C, T_A = 25°C, IN = Low, OUT = V_{DDB}, OUT = Low during thermal shutdown	V_{DDB} = 28V	38	mA
			V_{DDB} = 20V	53	mA
Safety Current on Any Pins (No Damage to Isolation Barrier)	I_S	T_J = 150°C, T_A = 25°C		300	mA
Total Safety Power Dissipation	P_S	T_J = 150°C, T_A = 25°C	8 Narrow SOIC	1173	mW
			8 Wide SOIC	1064	
Maximum Safety Temperature	T_S			150	°C

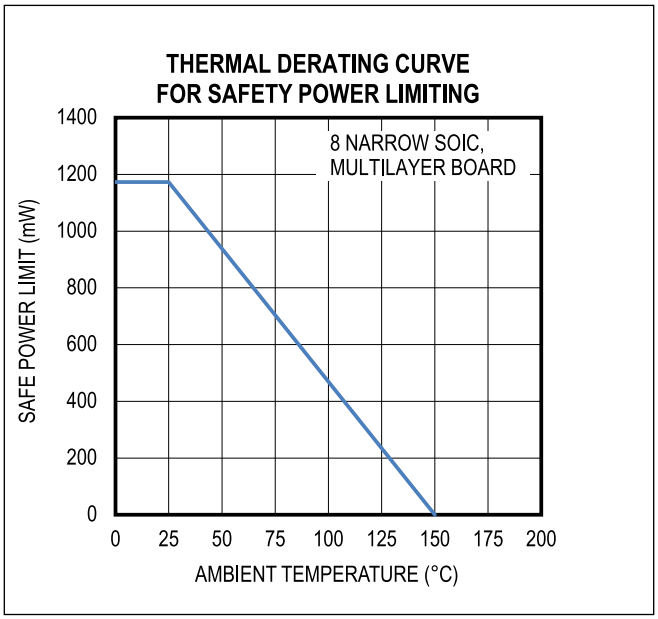


Figure 12. Thermal Derating Curve for Safety Power Limiting (8 Narrow SOIC)

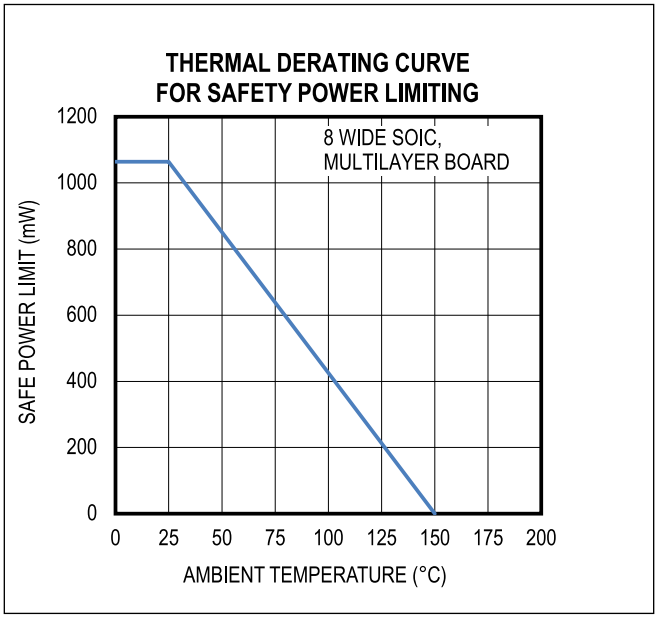


Figure 13. Thermal Derating Curve for Safety Power Limiting (8 Wide SOIC)

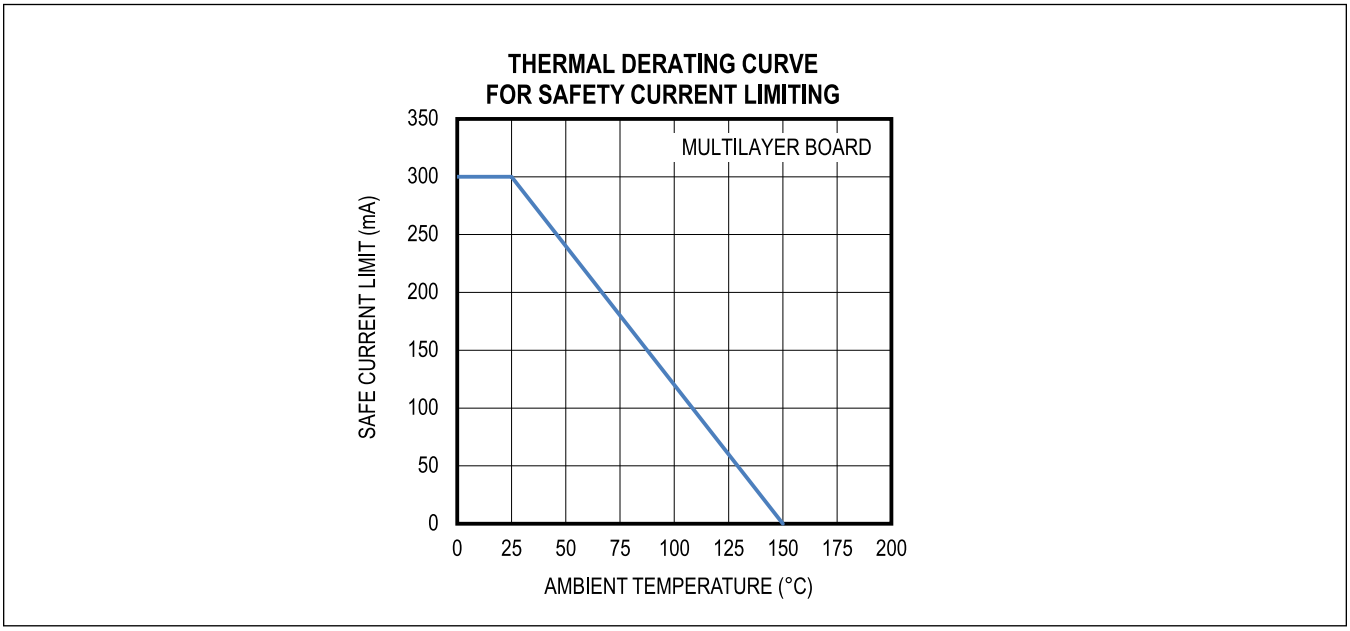


Figure 14. Thermal Derating Curve for Safety Current Limiting

Applications Information

Power-Supply Sequencing

The MAX22700–MAX22702 do not require special power-supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB}. Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with 1nF, 0.1µF, and 1µF low-ESR and low-ESL ceramic capacitors with sufficient voltage rating in parallel to GNDA and V_{SSB}, respectively. To ensure the best performance, place the decoupling capacitors as close to the power-supply pins as possible.

On the B side, it is recommended to place the 1nF and 1µF capacitors close to the V_{SSB} pin, and place the 0.1µF capacitor close to the V_{DDB} pin. To further reduce supply ripple while operating at higher supply voltage and data rates, place a 68nF 1206 C0G/NP0 capacitor across the V_{DDB} pin and V_{SSB} pin as close to the pins as possible. It is also recommended to include a 22µF reservoir capacitor (tantalum or electrolytic type) between V_{DDB} and V_{SSB} in case the V_{DDB} power supply is located far away from the V_{DDB} pin. All bypass capacitors on V_{DDB} are required to have at least a 50V voltage rating.

Layout Considerations

The PCB designer should follow some critical recommendations in order to get the best performance from the design.

- Keep the input/output traces as short as possible. To maintain low signal-path inductance, avoid using vias.
- Place the gate driver as close to the external power transistor as possible to decrease the trace inductance and avoid output ringing.
- Have a solid ground plane underneath the high-speed signal layer.
- Keep the area underneath the MAX22700–MAX22702 free from ground and signal planes. Any galvanic or metallic connection between side A and side B defeats the isolation.
- Have a solid ground plane next to V_{SSB} pin with multiple V_{SSB} vias to reduce the parasitic inductance and minimize the ringing on the output signal.
- Place a 68nF 1206 C0G/NP0 bypass capacitor across pin 5 and pin 8 as close as possible to the pins to mitigate B-side supply ripple.

Calculating Power Dissipation

The required current for the A side of the MAX22700–MAX22702 depends on the V_{DDA} supply voltage and the data rate. The required current for the B side of the MAX22700–MAX22702 depends on the V_{DDB} supply voltage, the data rate, and the load condition. The typical current for different V_{DDA} and V_{DDB} supply voltages at any data rate without external load can be estimated from the graphs in Figure 15 and Figure 16. Please note that the data in Figure 15 and Figure 16 are extrapolated from supply current measurements in a typical operating condition.

The total current for the B side is the sum of the “no load” current (shown in Figure 16) which is a function of the voltage and the data rate, and the “load current”, which depends on the load impedance. Current into a capacitive load is a function of the load capacitance, the switching frequency, and the supply voltage.

$$I_{CL} = C_L \times f_{SW} \times V_{DDB}$$

where:

I_{CL} = Current required to drive the capacitive load.

C_L = Load capacitance on the output pin.

f_{SW} = Switching frequency in Hz.

V_{DDB} = B-side supply voltage.

The total power dissipation (P_D) can be calculated as:

$$P_D = V_{DDA} \times I_{DDA} + V_{DDB} \times I_{DDB}$$

where I_{DDA} is the A-side supply current and I_{DDB} is the B-side supply current.

Example: A MAX22701 is operating with V_{DDA} = 5V, V_{DDB} = 20V. The output is operating at 10kHz with 1nF capacitive load. V_{DDA} must supply about 4.56mA with a 10kHz data rate and a 5V supply voltage according to Figure 15. V_{DDB} must supply the sum of the no load current and the load current. The no load current is about 3.77mA with a 10kHz data rate and a 20V supply voltage according to Figure 16. The load current is equal to 1nF × 10kHz × 20V = 0.2mA. V_{DDB} must therefore supply about 3.97mA. The total power dissipation is 5V × 4.56mA + 20V × 3.97mA = 102.2mW.

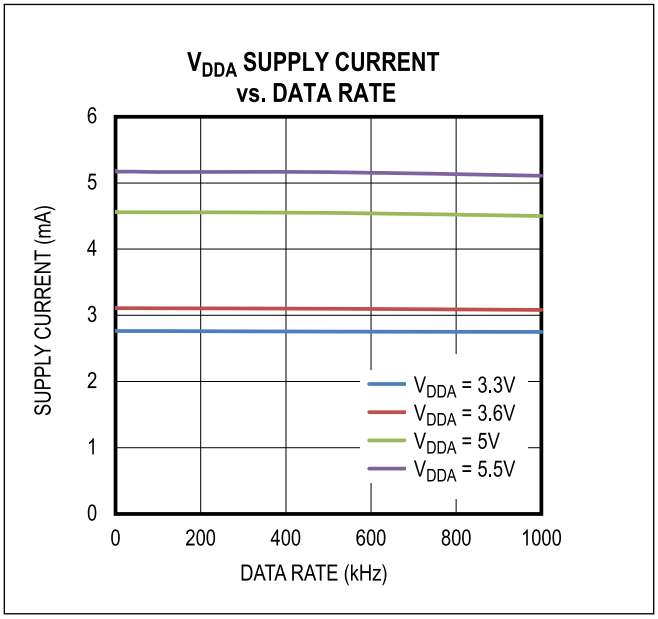


Figure 15. V_{DDA} Supply Current vs. Data Rate (typ)

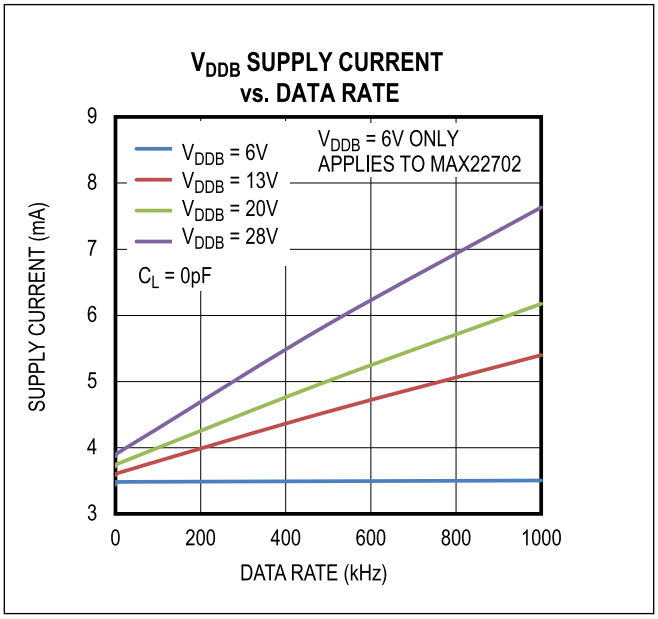


Figure 16. V_{DDB} Supply Current vs. Data Rate (typ)

Gate Driver Output Resistors

External series resistors (R_{ON} and R_{OFF}) between the MAX22700–MAX22702 output and the gate of the power transistor are required in gate driver applications. These resistors control the turn-on and turn-off time of the power transistor to optimize switching efficiency and EMI performance.

The R_{ON} resistance and external FET's gate capacitance determine the turn-on time. The parallel combination of both R_{ON} and R_{OFF} resistance and the external FET's gate capacitance determine the turn-off time. Turn-off time is usually much faster than turn-on time to avoid shoot-through. Figure 17 shows a typical R_{ON} and R_{OFF} network for the MAX22700–MAX22702. R_{ON} and R_{OFF} values should be adjusted based on the required slew rate and the external FET's gate capacitance.

The gate driver output resistors also help limit ringing caused by parasitic inductances and capacitances due to PCB layout and device package leads. Output ringing can happen during high voltage dV/dt and high current di/dt switching. Increasing R_{ON} and R_{OFF} can help reduce the ringing.

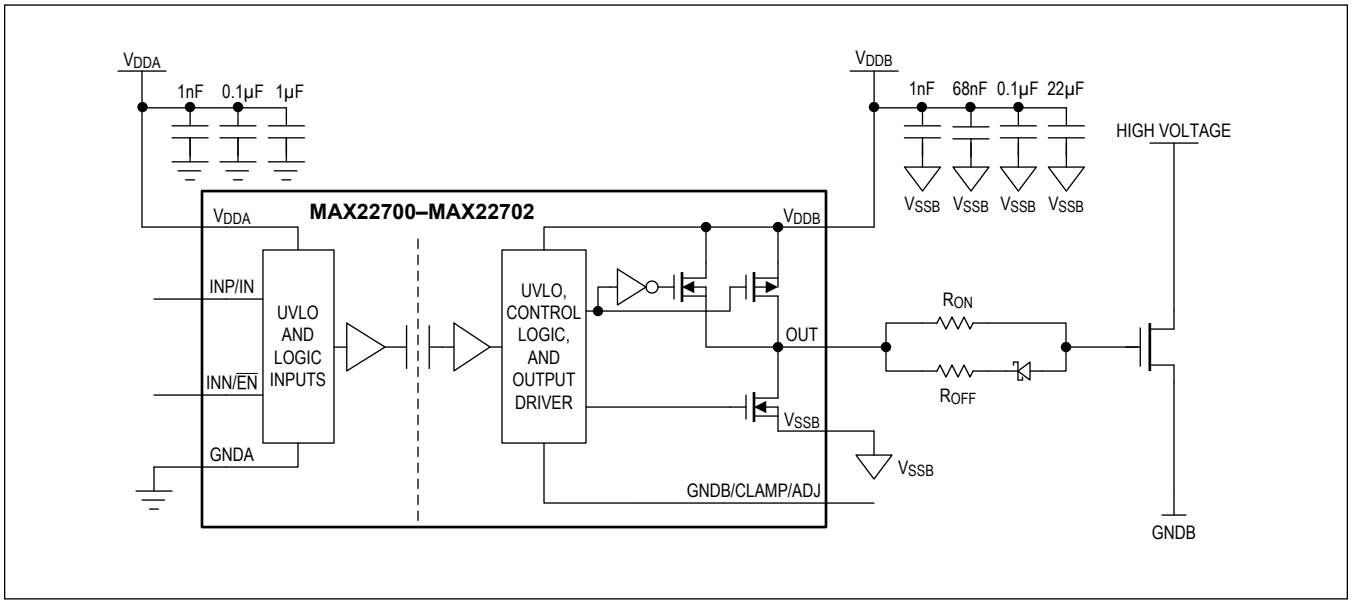


Figure 17. Typical Gate Driver Output Network with R_{ON} and R_{OFF}

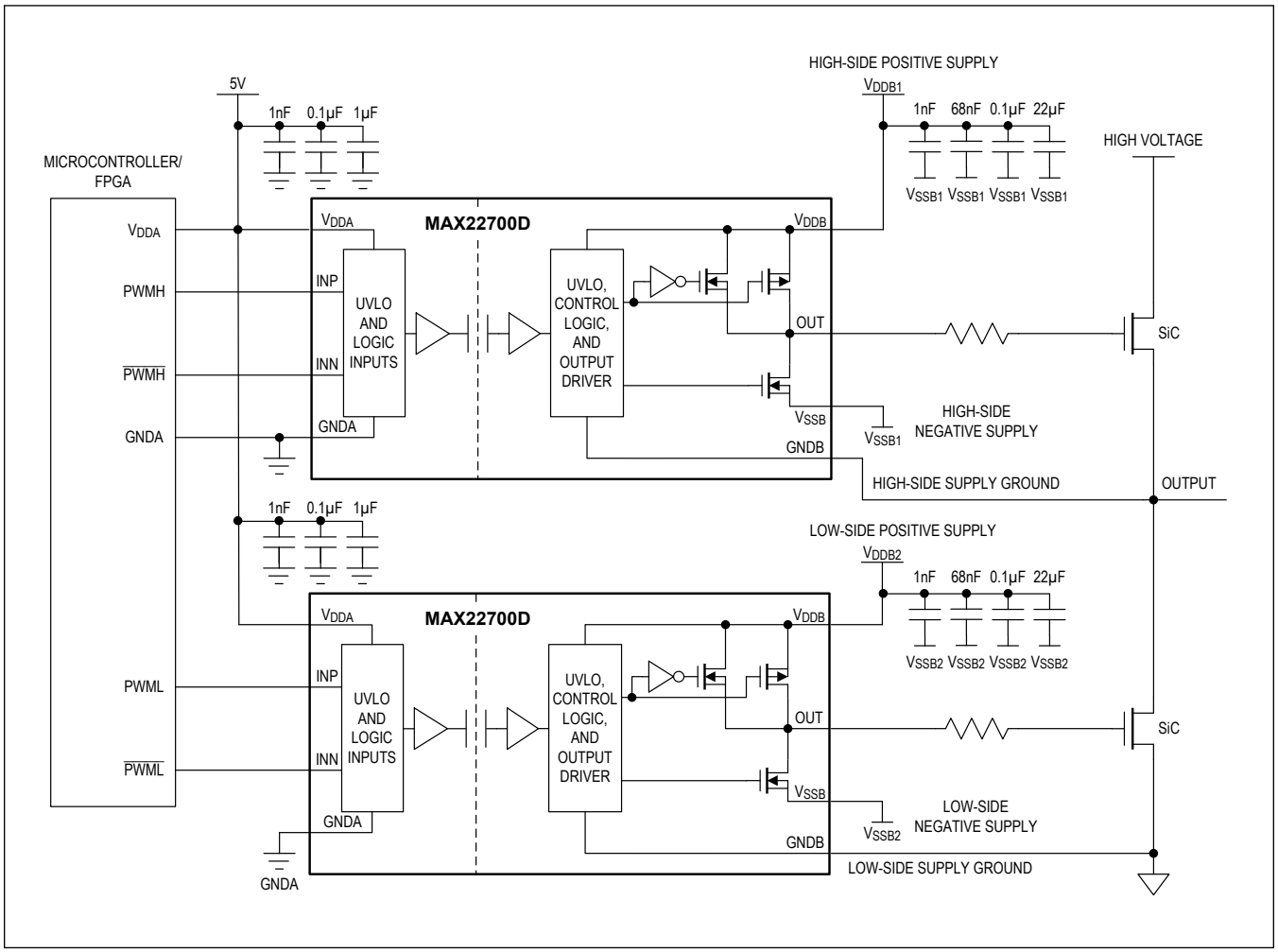
Driving GaN Transistors

The high CMTI rating of 300kV/µs (typ) and the propagation delay matching of 5ns (max) between the high-side and low-side drivers make the MAX22701 and MAX22702 ideal to drive GaN devices. The MAX22702 also features an adjustable B-side UVLO to accommodate the low gate drive voltage of GaN devices.

As shown in the *Typical Application Circuits*, a positive supply (V_{DDB}) and a negative supply (V_{SSB}) with reference to GNDB are required to meet the gate voltage requirement of GaN devices when using the MAX22701 and MAX22702 as GaN gate drivers. A boost current is required during the GaN device's turn-on period; hence a capacitor is placed in series with one of the resistors at the output. This capacitor needs to be discharged during the turn-off period. Therefore, a diode is placed in parallel to the resistor to provide a discharge path. On the layout, it is recommended to place the gate driver very close to the GaN device to minimize series inductance and reduce gate drive loop area. To prevent ringing and support high peak currents when turning on GaN devices, good decoupling is required on the V_{DDB} and V_{SSB} pins.

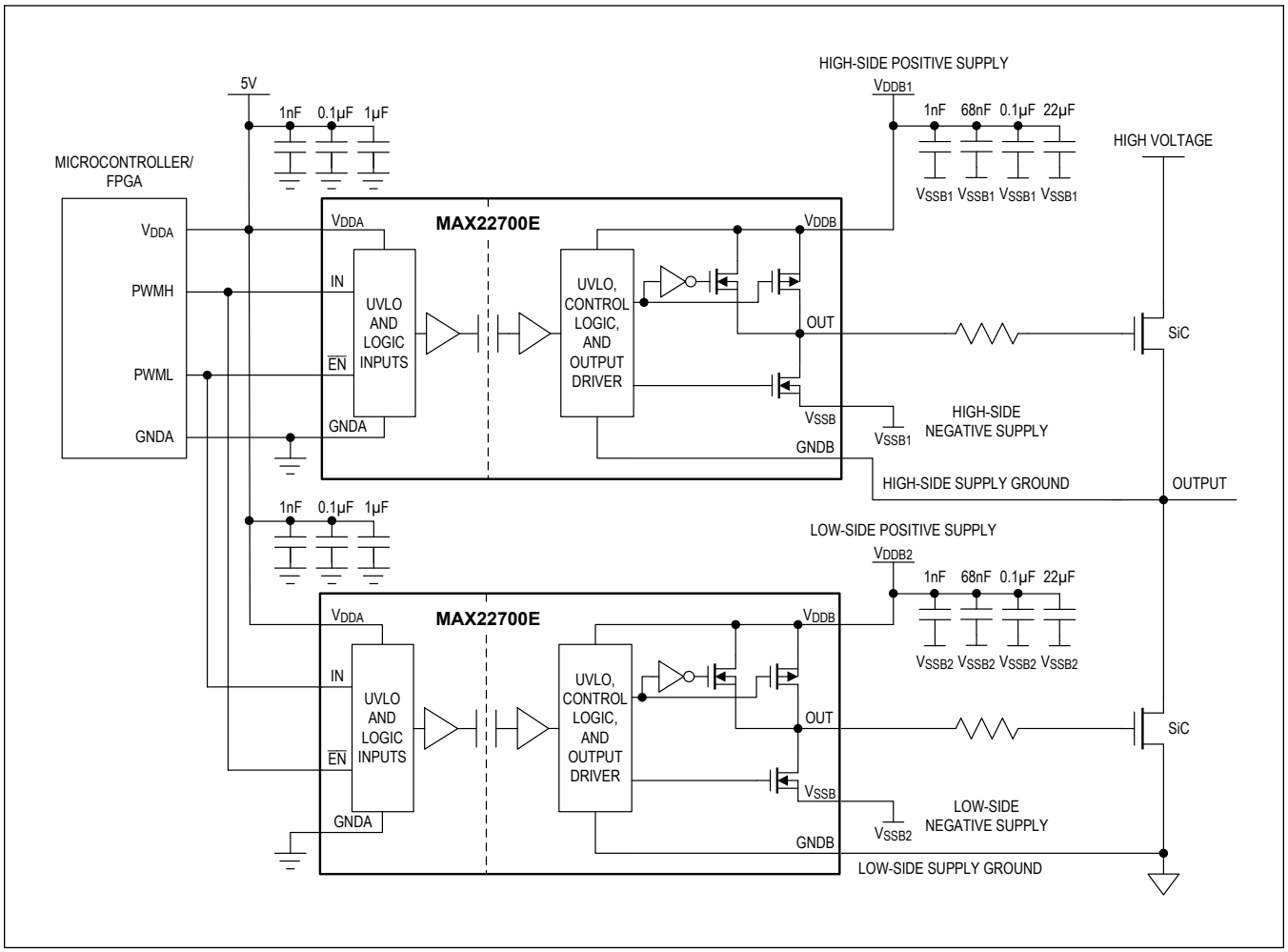
Typical Application Circuits

MAX22700D



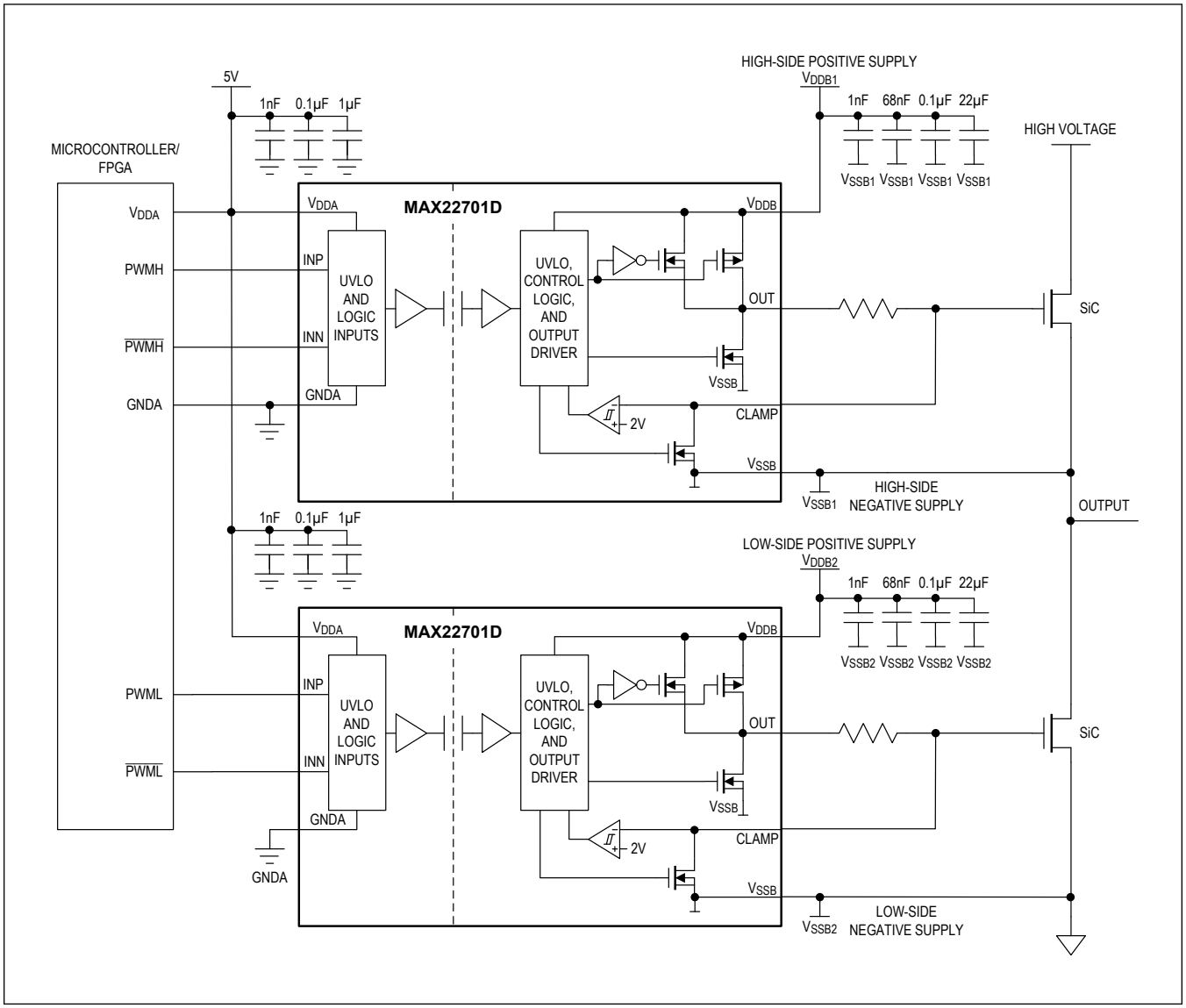
Typical Application Circuits (continued)

MAX22700E



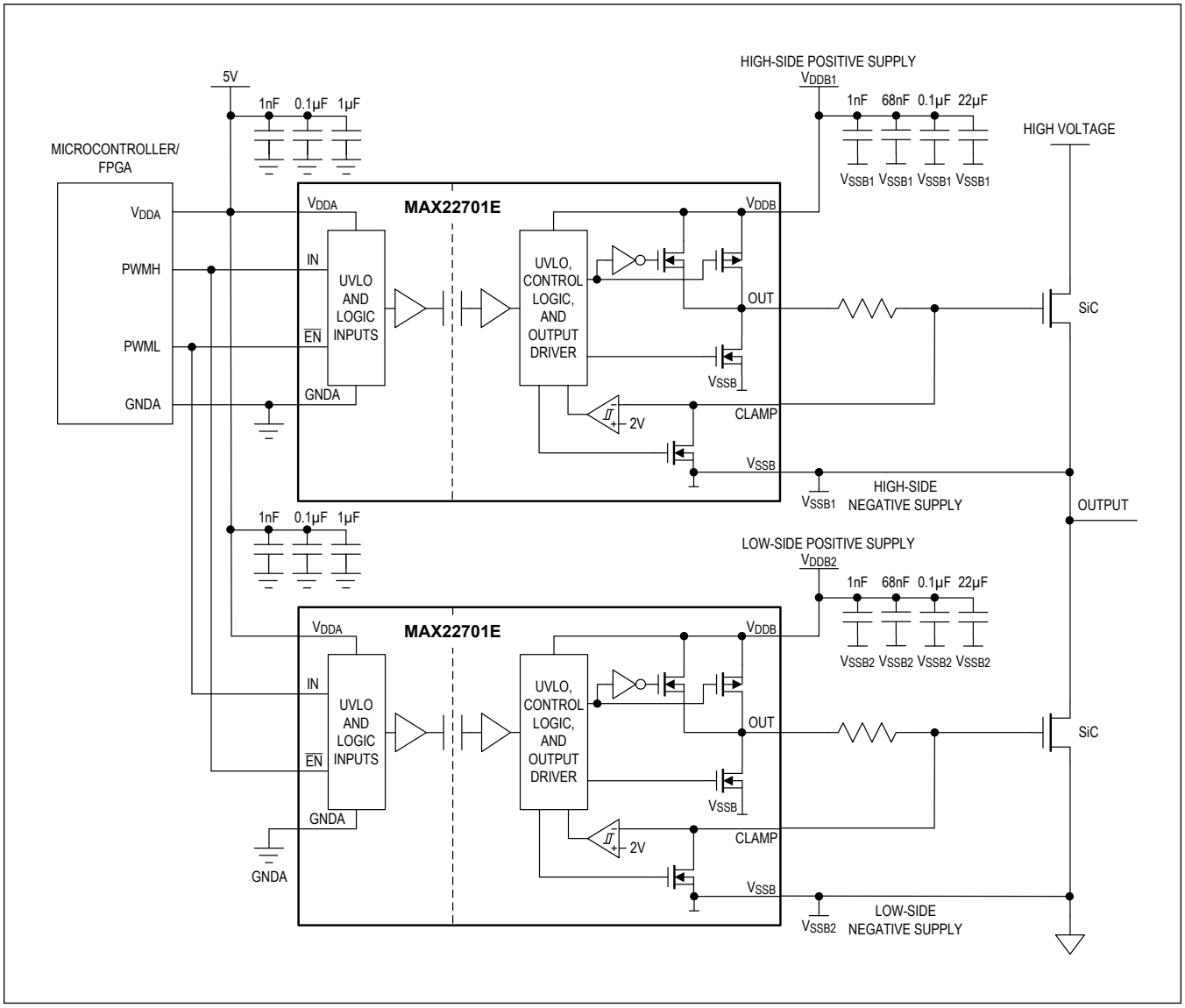
Typical Application Circuits (continued)

MAX22701D



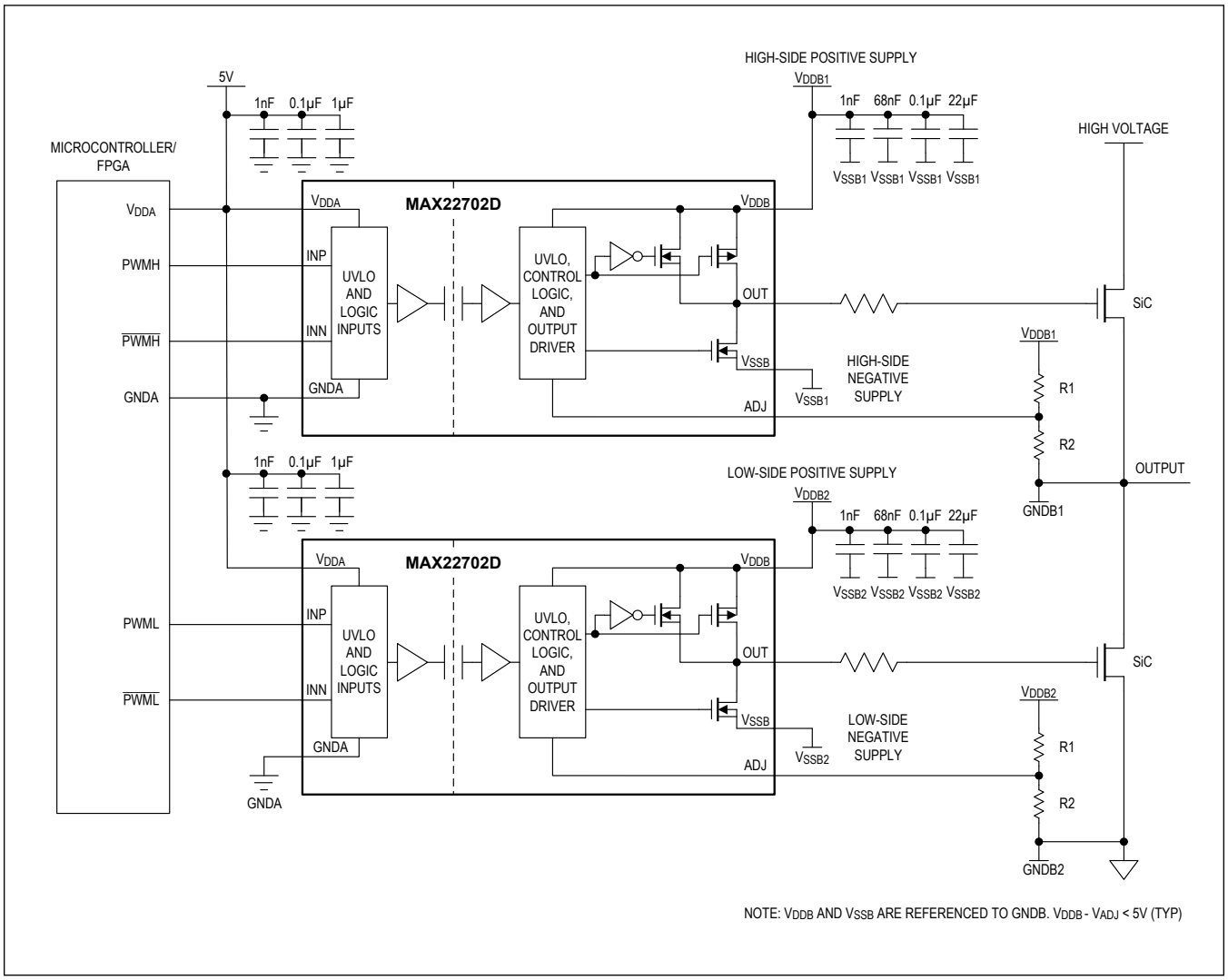
Typical Application Circuits (continued)

MAX22701E



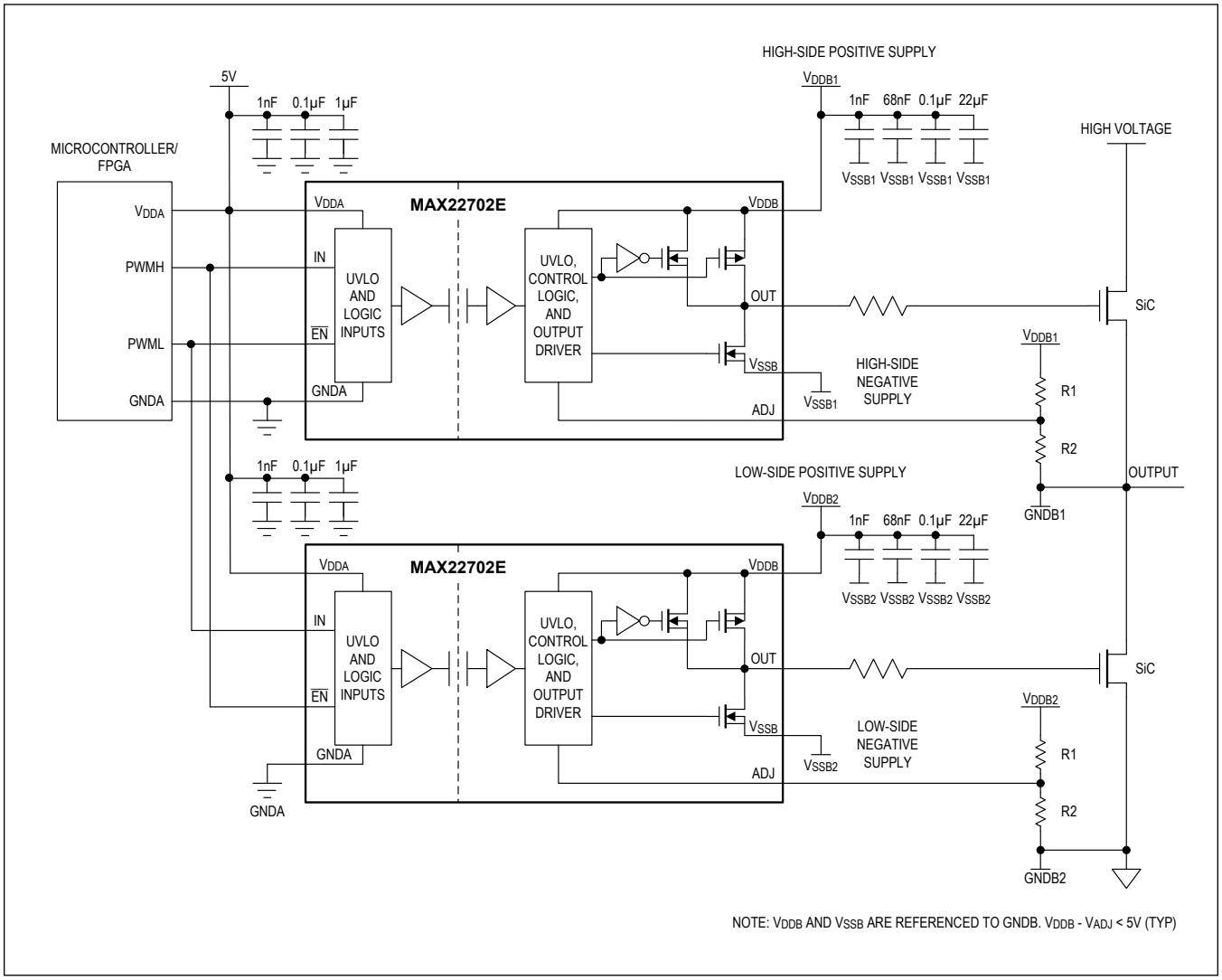
Typical Application Circuits (continued)

MAX22702D



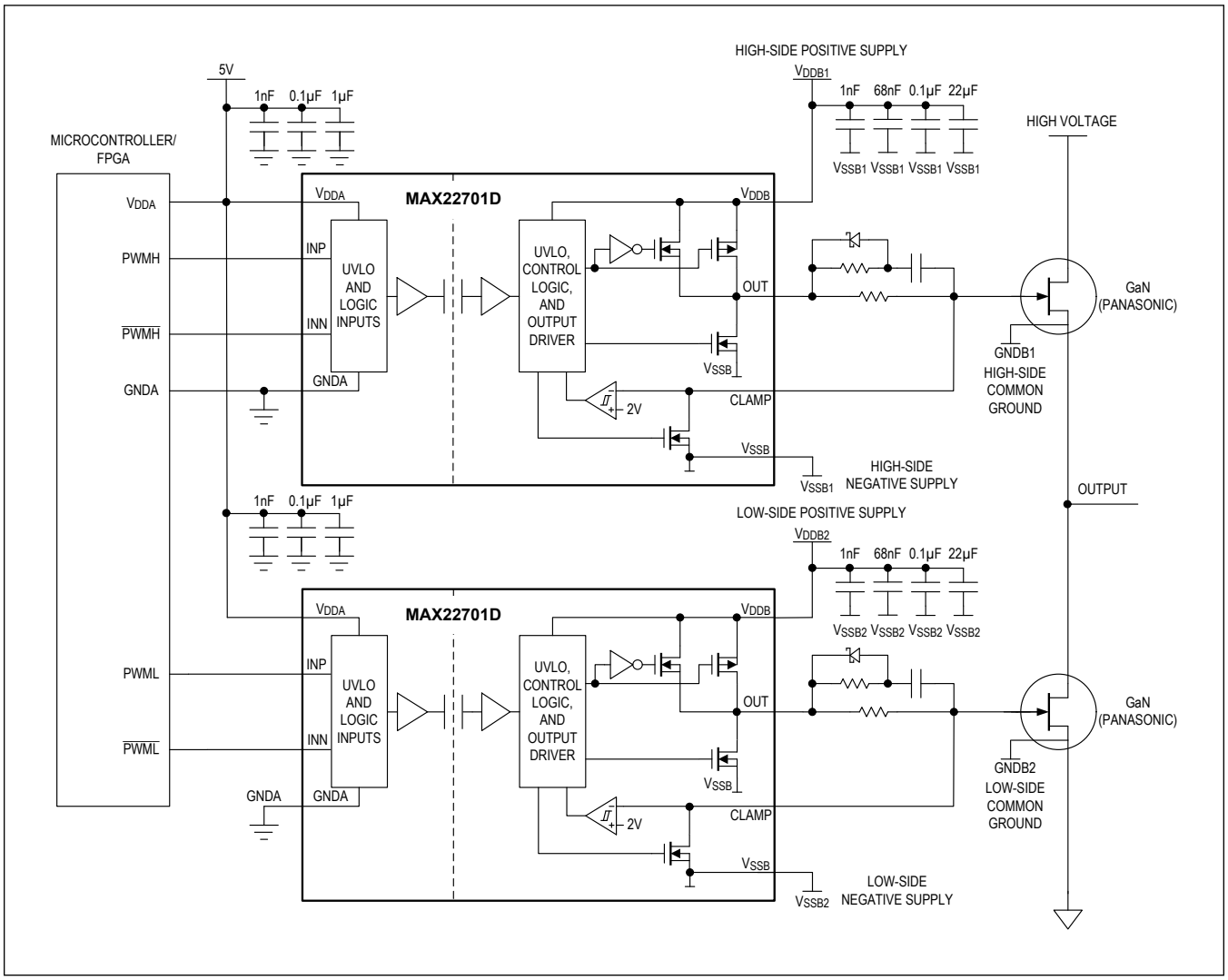
Typical Application Circuits (continued)

MAX22702E



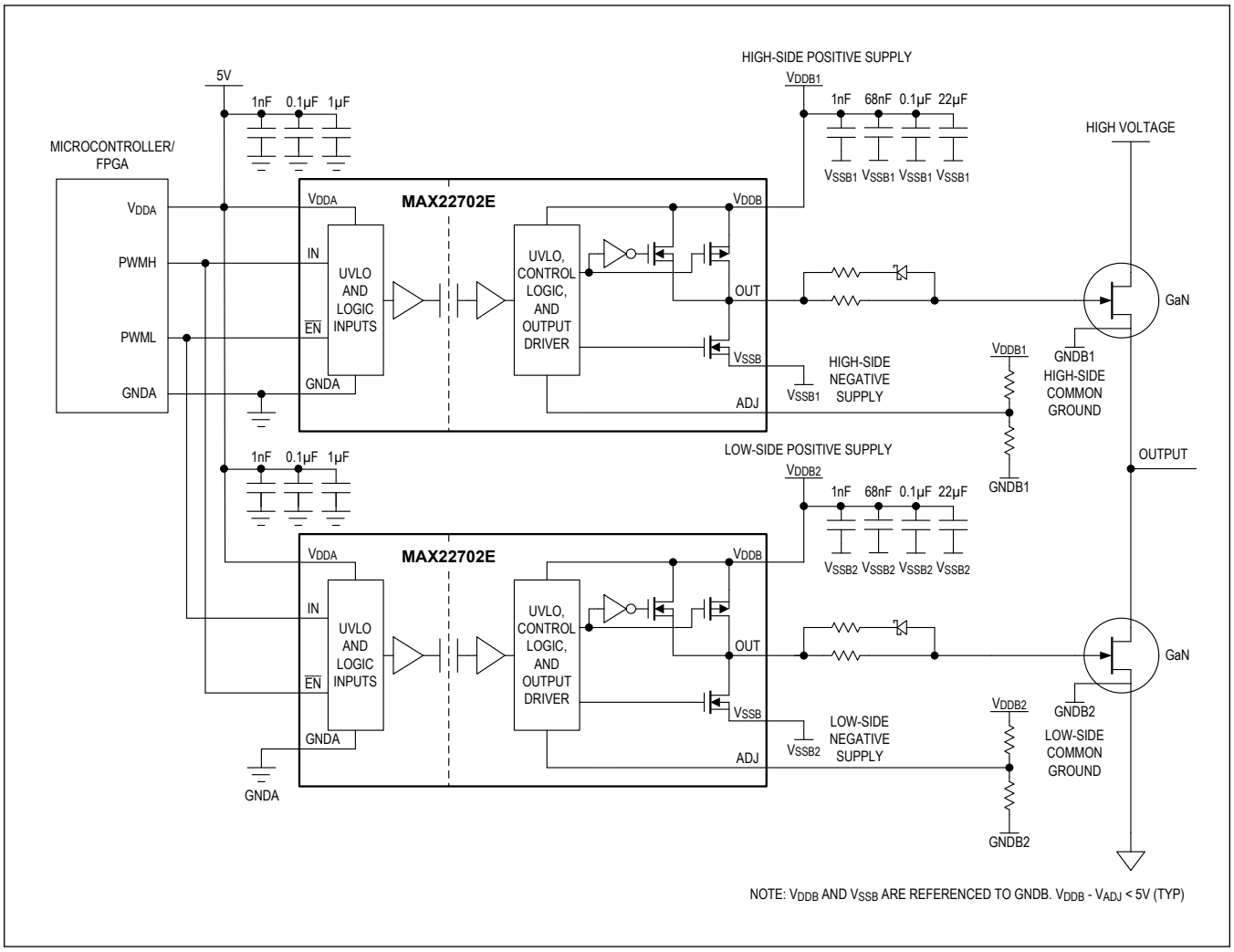
Typical Application Circuits (continued)

MAX22701D as GaN Gate Driver



Typical Application Circuits (continued)

MAX22702E as GaN Gate Driver



Ordering Information

PART NUMBER	INPUTS	PIN 7	UVLO	LOW-SIDE R_{DSON} (Ω)	ISOLATION VOLTAGE (kV_{RMS})	TEMP RANGE (°C)	PIN-PACKAGE
MAX22700DASA+	Differential, INP and INN	GNDB	13V to GNDB	1.25	3	-40 to +125	8 Narrow SOIC
MAX22700DAWA+*	Differential, INP and INN	GNDB	13V to GNDB	1.25	5	-40 to +125	8 Wide SOIC
MAX22700EASA+	Single-Ended, IN and $\overline{EN}$	GNDB	13V to GNDB	1.25	3	-40 to +125	8 Narrow SOIC
MAX22700EAWA+*	Single-Ended, IN and $\overline{EN}$	GNDB	13V to GNDB	1.25	5	-40 to +125	8 Wide SOIC
MAX22701DASA+	Differential, INP and INN	CLAMP	13V to V_{SSB}	2.5	3	-40 to +125	8 Narrow SOIC
MAX22701DAWA+*	Differential, INP and INN	CLAMP	13V to V_{SSB}	2.5	5	-40 to +125	8 Wide SOIC
MAX22701EASA+	Single-Ended, IN and $\overline{EN}$	CLAMP	13V to V_{SSB}	2.5	3	-40 to +125	8 Narrow SOIC
MAX22701EAWA+	Single-Ended, IN and $\overline{EN}$	CLAMP	13V to V_{SSB}	2.5	5	-40 to +125	8 Wide SOIC
MAX22702DASA+	Differential, INP and INN	ADJ	Adjustable	1.25	3	-40 to +125	8 Narrow SOIC
MAX22702DAWA+*	Differential, INP and INN	ADJ	Adjustable	1.25	5	-40 to +125	8 Wide SOIC
MAX22702EASA+	Single-Ended, IN and $\overline{EN}$	ADJ	Adjustable	1.25	3	-40 to +125	8 Narrow SOIC
MAX22702EAWA+*	Single-Ended, IN and $\overline{EN}$	ADJ	Adjustable	1.25	5	-40 to +125	8 Wide SOIC

+Denotes a lead (Pb)-free/RoHS-compliant package.

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/19	Initial release	—
1	8/19	Updated the *Absolute Maximum Ratings* and *Package Information* sections, Table 2, and Figure 1	2, 7
2	9/19	Updated the *General Description*, *Benefits and Features*, *DC Electrical Characteristics*, and *Dynamic Characteristics* sections	1, 4
3	1/20	Removed future product designation from MAX22702EASA+ in the *Ordering Information* section	29
4	5/20	Removed future product designation from MAX22700DASA+ and MAX22701DASA+ in the *Ordering Information* section	29
5	7/20	Updated the *Benefits and Features* and *Digital Isolation* sections; updated Table 1	1, 6, 15
6	10/20	Removed future product designation from MAX22700EASA+ and MAX22702DASA+ in the *Ordering Information* section	29
7	10/20	Updated the *General Description*, *Benefit and Features*, *Safety Regulatory Approvals (Pending), Absolute Maximum Ratings, Package Information, Electrical Characteristics, Pin Configurations, Pin Description, Detailed Description*, *Digital Isolation*, and *Safety Limits* sections; added the *Insulation Characteristics—8 Wide SOIC* table and new Figure 1–2 and renumbered remaining figures; moved the *Functional Diagrams* to the second page; updated Figures 12–13, Table 1, and Table 4; added MAX22700DAWA+, MAX22700EAWA+, MAX22701DAWA+, MAX22701EAWA+, MAX22702DAWA+, and MAX22702EAWA+ as future products to the *Ordering Information* table	1–3, 8–9, 13–16, 17–24, 36
8	4/21	Updated the *General Description, Safety Regulatory Approvals, Electrical Characteristics, Insulation Characteristics—8 Narrow SOIC, Insulation Characteristics—8 Wide SOIC, Typical Operating Characteristics, Power-Supply Decoupling, Layout Considerations,* and *Typical Application Circuit* sections; updated Table 1, Table 4, Figures 5–6, 8, 11, 16–17, and TOC01–TOC08, TOC15–TOC16, and TOC 18	1, 4, 7–8, 10–12, 17, 19, 21, 24–34
9	6/21	Removed future product designation from MAX22701EAWA+ in the *Ordering Information* section	34