Test Procedure for

NCP51820 HB Evaluation Board

Featured ON Products:
NCP51820

ON Semiconductor.com

REVISION HISTORY

Rev.	Date	Description	Edited By
0.01	07/8/2019	Initial	MP

Purpose:

This is a “GO/NO-GO” test methodology for the NCP51820 GaN Driver Evaluation Board (EVB). The included test procedure will catch most abnormally constructed boards. Boards which don’t pass this test procedure will need more extensive testing by an Applications Engineer.

Required Equipment:

- **(1) DC/DC Power supply: Power supply capable of supplying:**

  +12VDC – 1A

  Example: INSTEK GPS4303
- **(1) Dual channel, > 100MHz oscilloscope**

  Example: LeCroy 64MXI
- **(1) passive probe and one differential probe**

  Example (diff probe): LeCroy ADP305
- **(1) Dual-Channel Pulse generator capable of supplying:**

  5V, 20 kHz, 50% duty-cycle square wave.

  Example: Tektronix AFG3102.
- **(1) NCP51820 HB EVB Test Board (see Figure 3)**

Figure 1. NCP51820 HB EVB

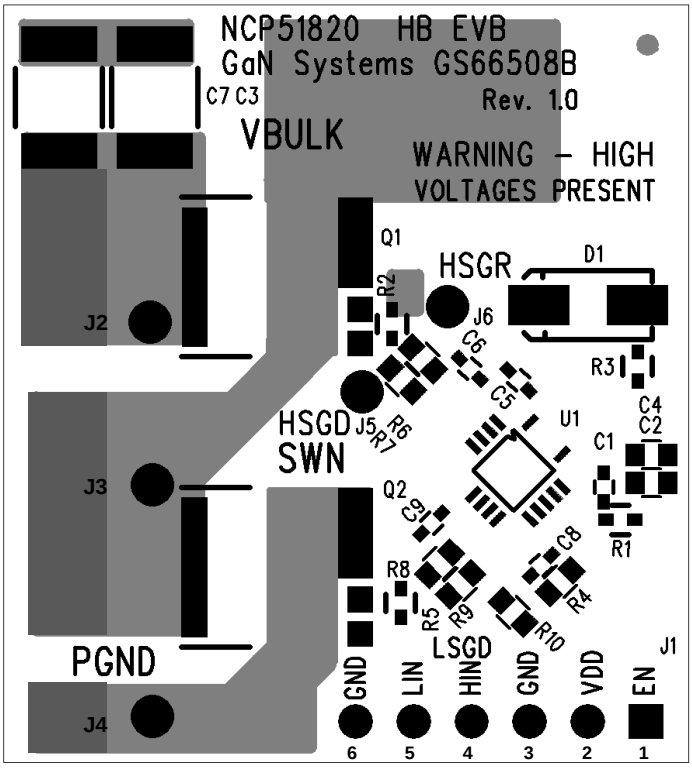

Figure 2. NCP51820 HB EVB Top Assy Drawing

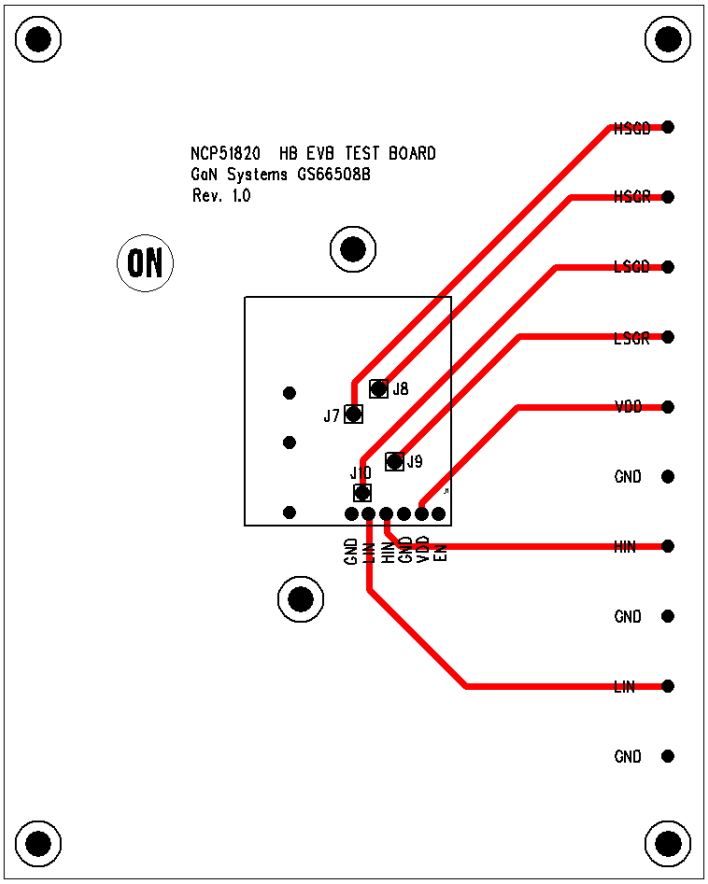

Figure 3. NCP51820 HB EVB Test Board

Test equipment setup:

1) Set DC power supply (VDD) to +12VDC.
2) Set both channels of the pulse generator to 20 kHz, +5V amplitude 50% duty cycle square wave, each channel referenced to 0V. Set channel two 180^0 out of phase with channel one, as shown in Figure 5.
3) Set scope horizontal to 10us/div
4) Set both scope channels to 5V/div.
5) Connect test equipment to Test Board as shown in Figure 4. Connect the passive scope probe to LSGD and LSGR and differential scope probe to HSGD and HSGR as shown in Figure 4.

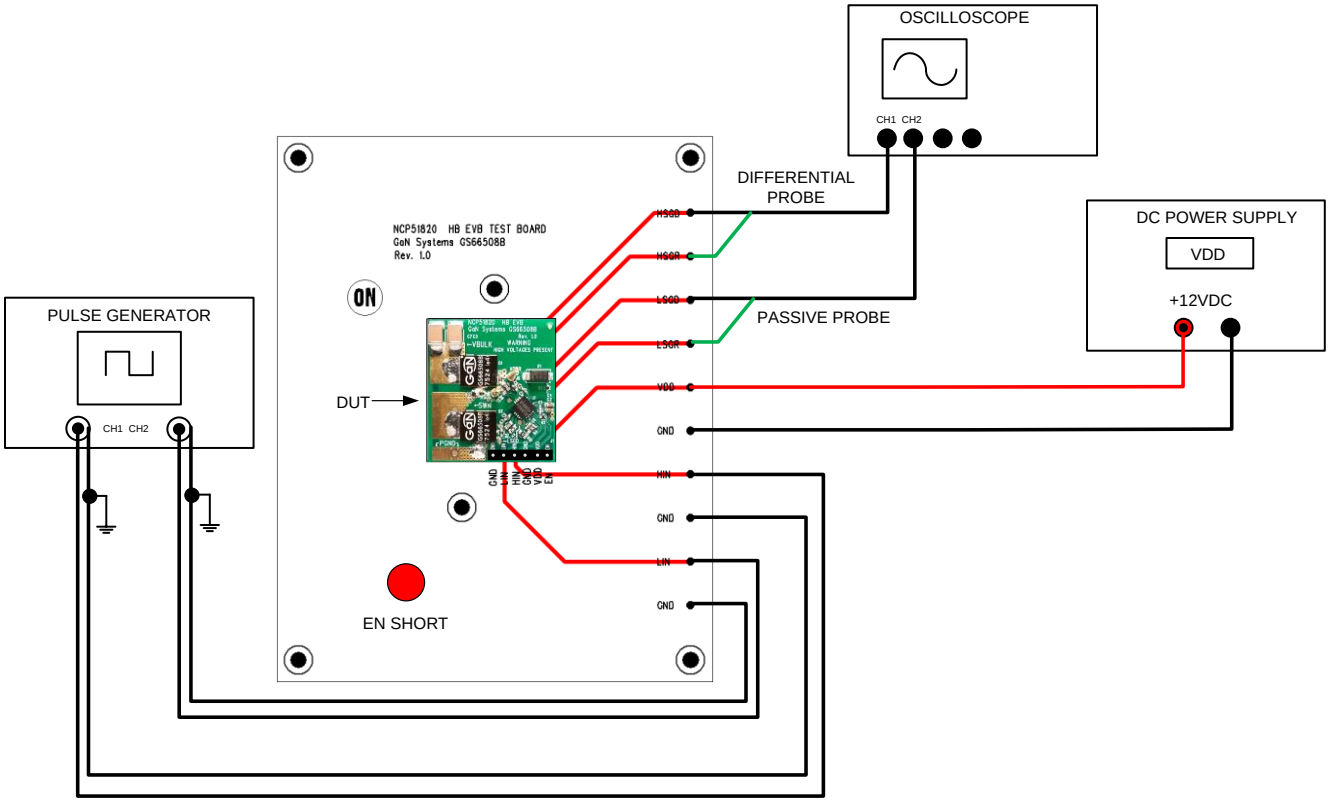

Figure 4. Test setup connections for NCP51820 GaN DRIVER EVB

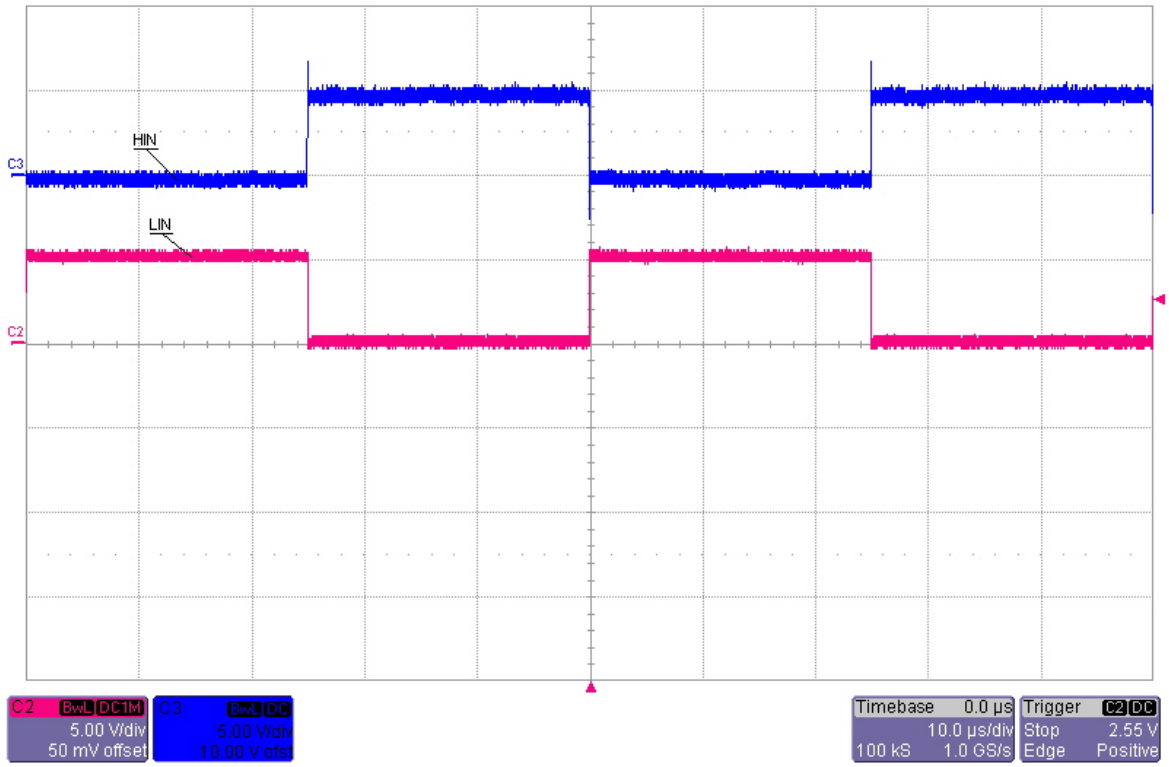

Figure 5. HIN and LIN signals from pulse generator

Power on and test sequence:

1) Place DUT on tester. It will be necessary to press down lightly on the DUT to make sure the test pins make contact.
2) Turn on VDD (+12VDC).
3) Turn on pulse generator.
4) Observe the HSGD and LSGD waveforms. They should look like the waveforms in Figure 6.
5) While the DUT is operating, push the EN SHORT button. The outputs should go to 0V. When the button is released, the outputs should return.
6) Test complete. Turn off pulse generator and VDD. Remove the DUT.

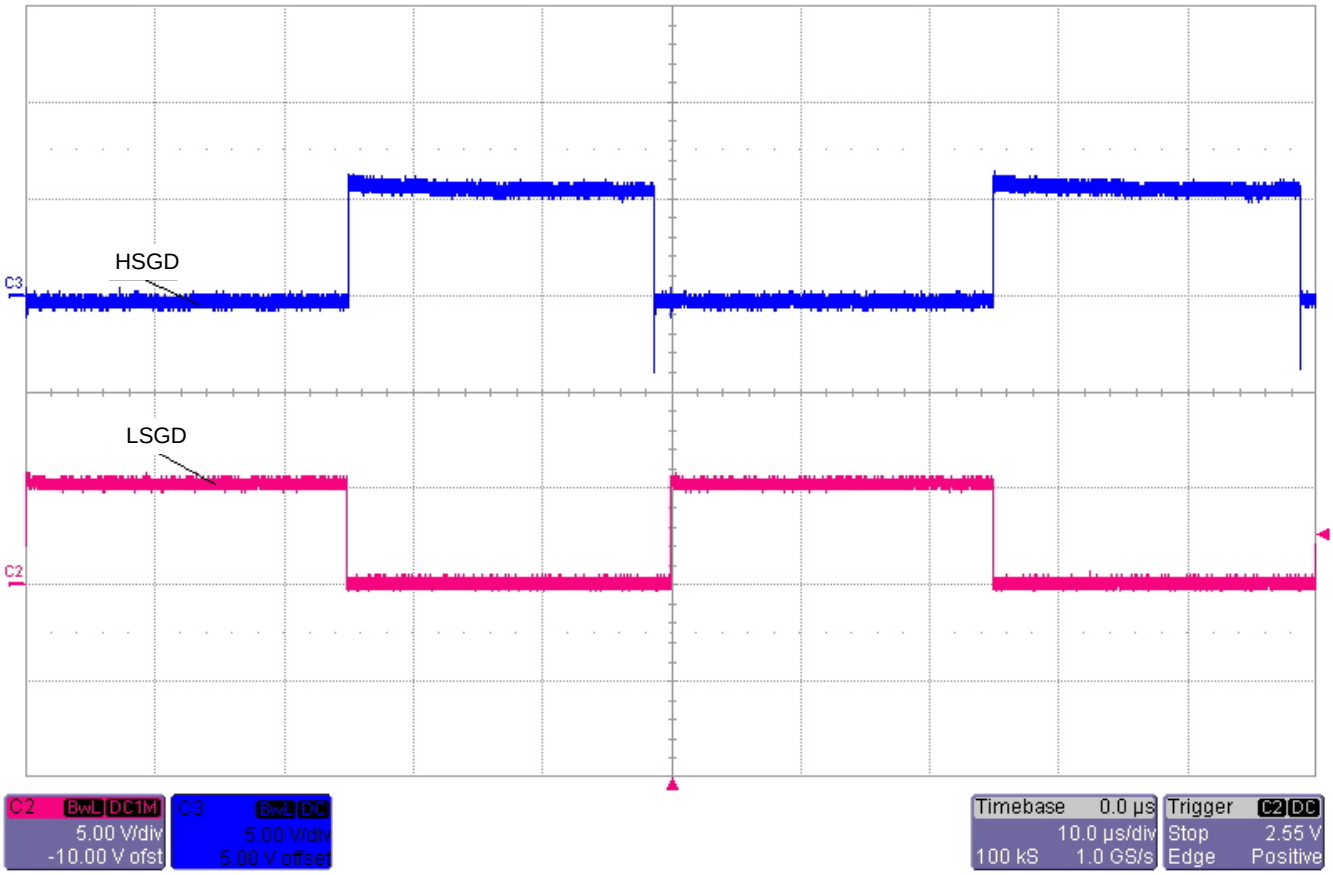

Figure 6. VGS (HI) and VGS (LO) waveforms

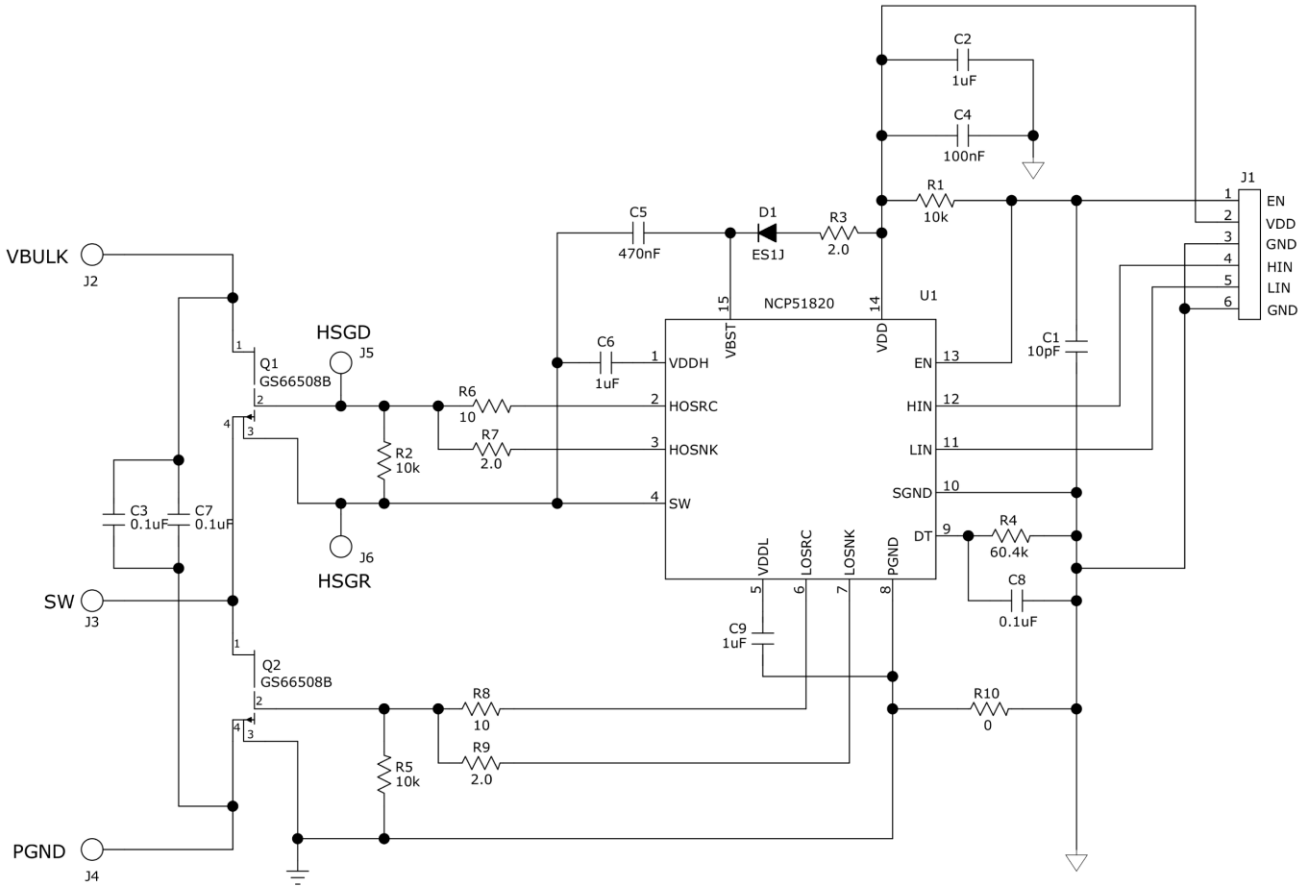

Figure 7. NCP51820 HB EVB Schematic

NCP51820 HB EVB Bill of materials:

Item	Qty	Reference	Value	Part Number	Description	Manufacturer	Pkg Type
1	1	C1	10 pF	CC0402JRNPO9BN100	CAP, SMD, CERAMIC, 50 V, NPO	Yageo	402
2	1	C2	1 µF	CL10B105KA8NNNC	CAP, SMD, CERAMIC, 25 V, X7R	Samsung	603
3	1	C4	100 nF	CGA3E2X7R1E104K080AA	CAP, SMD, CERAMIC, 25 V, X7R	TDK	603
4	1	C5	470 nF	CL05A474KA5NNNC	CAP, SMD, CERAMIC, 25 V, X5R	Samsung	402
5	1	C8	0.1 µF	CC0402KRX7R8BB104	CAP, SMD, CERAMIC, 25 V, X7R	Yageo	402
6	2	C3,C7	0.1 µF	C4532X7R2J104K230KA	CAP, SMD, CERAMIC, 630 V, X7R	TDK	1812
7	2	C6,C9	1 µF	CGB2A1X5R1E105K033BC	CAP, SMD, CERAMIC, 25 V, X5R	TDK	402
8	1	D1		ES1J	DIODE FAST REC 1 A 600 V	ON Semiconductor	SMA
9	1	J1		61300611121	Connector, Header, 100Mil spacing	Wurth	Thru-Hole
10	5	J2-6		1352-1	Testpin, Gold, 40mil	Keystone	Thru-Hole
11	2	Q1-2		GS66508B	GaN, 650V, E-mode, 30 A, 50 mΩ	GaN Systems	7.1x8.5 mm
12	1	R3	2 Ω	RC1005F2R0CS	RES, SMD, 1/16 W	Samsung	402
13	1	R4(1)	60.4 kΩ	RC0603FR-0760K4L	RES, SMD, 1/10 W	Yageo	603
14	1	R10(2)	0 Ω	RC0603JR-070RL	RES, SMD, 1/10 W	Yageo	603
15	3	R1-2,R5	10 k Ω	RC0402FR-0710KL	RES, SMD, 1/16 W	Yageo	402
16	2	R6,R8	10 Ω	RC0603FR-0710RL	RES, SMD, 1/10 W	Yageo	603
17	2	R7,R9	2 Ω	RC0603FR-072RL	RES, SMD, 1/10 W	Yageo	603
18	1	U1		NCP51820	High Speed Half Bridge GaN Driver	ON Semiconductor	MLP 4 x4-15
19	1			658-60AB	Heatsink (optional)	Wakefield-Vette	1.1 x 1.1 in.
20	1			LI98-28-28-0.25	Adhesive thermal isolator (optional)	T-Global Technology	28 x28 mm