NCP1030, NCP1031

Integrated DC-DC Converter - Power over Ethernet and Telecom

The NCP1030 and NCP1031 are a family of miniature high−voltage monolithic switching regulators with on−chip Power Switch and Startup Circuits. The NCP103x family incorporates in a single IC all the active power, control logic and protection circuitry required to implement, with minimal external components, several switching regulator applications, such as a secondary side bias supply or a low power dc−dc converter. This controller family is ideally suited for 48 V telecom, 42 V automotive and 12 V input applications. The NCP103x can be configured in any single−ended topology such as forward or flyback. The NCP1030 is targeted for applications requiring up to 3 W, and the NCP1031 is targeted for applications requiring up to 6 W.

The internal error amplifier allows the NCP103x family to be easily configured for secondary or primary side regulation operation in isolated and non−isolated configurations. The fixed frequency oscillator is optimized for operation up to 1 MHz and is capable of external frequency synchronization, providing additional design flexibility. In addition, the NCP103x incorporates individual line undervoltage and overvoltage detectors, cycle by cycle current limit and thermal shutdown to protect the controller under fault conditions. The preset current limit thresholds eliminate the need for external sensing components.

Features

- On Chip High 200 V Power Switch Circuit and Startup Circuit
- Internal Startup Regulator with Auxiliary Winding Override
- Operation up to 1 MHz
- External Frequency Synchronization Capability
- Frequency Fold−down Under Fault Conditions
- Trimmed ±2% Internal Reference
- Line Undervoltage and Overvoltage Detectors
- Cycle by Cycle Current Limit Using SENSEFET®
- Active LEB Circuit
- Overtemperature Protection
- Internal Error Amplifier
- Pb−Free Packages are Available

Typical Applications

- POE (Power Over Ethernet)/PD. Refer to Application Note AND8247.
- Secondary Side Bias Supply for Isolated dc−dc Converters
- Stand Alone Low Power dc−dc Converter
- Low Power Bias Supply
- Low Power Boost Converter

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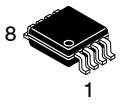
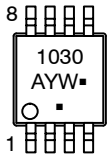
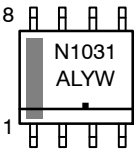
MARKING DIAGRAMS

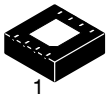


Micro8™
DM SUFFIX
CASE 846A

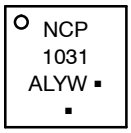


SO−8
D SUFFIX
CASE 751



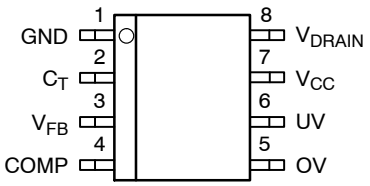


DFN−8
MN SUFFIX
CASE 488AF

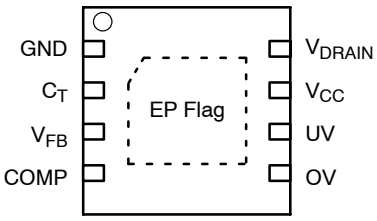


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 19 of this data sheet.

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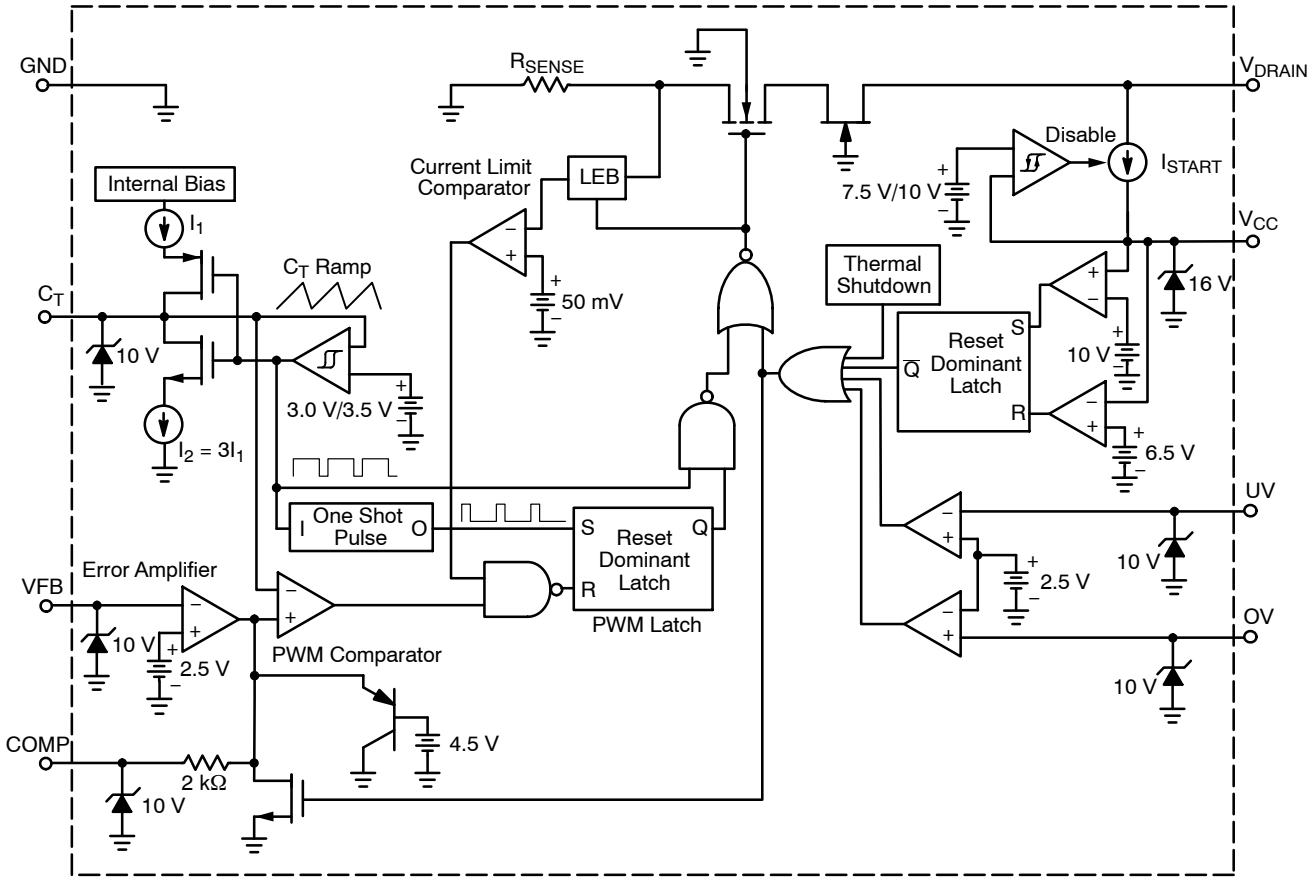

Figure 1. NCP1030/31 Functional Block Diagram

FUNCTIONAL PIN DESCRIPTION

Pin	Name	Function	Description
1	GND	Ground	Ground reference pin for the circuit.
2	C_T	Oscillator Frequency Selection	An external capacitor connected to this pin sets the oscillator frequency up to 1 MHz. The oscillator can be synchronized to a higher frequency by charging or discharging C_T to trip the internal 3.0 V/3.5 V comparator. If a fault condition exists, the power switch is disabled and the frequency is reduced by a factor of 7.
3	V_{FB}	Feedback Input	The regulated voltage is scaled down to 2.5 V by means of a resistor divider. Regulation is achieved by comparing the scaled voltage to an internal 2.5 V reference.
4	COMP	Error Amplifier Compensation	Requires external compensation network between COMP and V_{FB} pins. This pin is effectively grounded if faults are present.
5	OV	Line Overvoltage Shutdown	Line voltage (V_{in}) is scaled down using an external resistor divider such that the OV voltage reaches 2.5 V when line voltage reaches its maximum operating voltage.
6	UV	Line Undervoltage Shutdown	Line voltage is scaled down using an external resistor divider such that the UV voltage reaches 2.5 V when line voltage reaches its minimum operating voltage.
7	V_{CC}	Supply Voltage	This pin is connected to an external capacitor for energy storage. During Turn−On, the startup circuit sources current to charge the capacitor connected to this pin. When the supply voltage reaches $V_{CC(on)}$, the startup circuit turns OFF and the power switch is enabled if no faults are present. An external winding is used to supply power after initial startup to reduce power dissipation. V_{CC} should not exceed 16 V.
8	V_{DRAIN}	Power Switch and Startup Circuits	This pin directly connects the Power Switch and Startup Circuits to one of the transformer windings. The internal High Voltage Power Switch Circuit is connected between this pin and ground. V_{DRAIN} should not exceed 200 V.

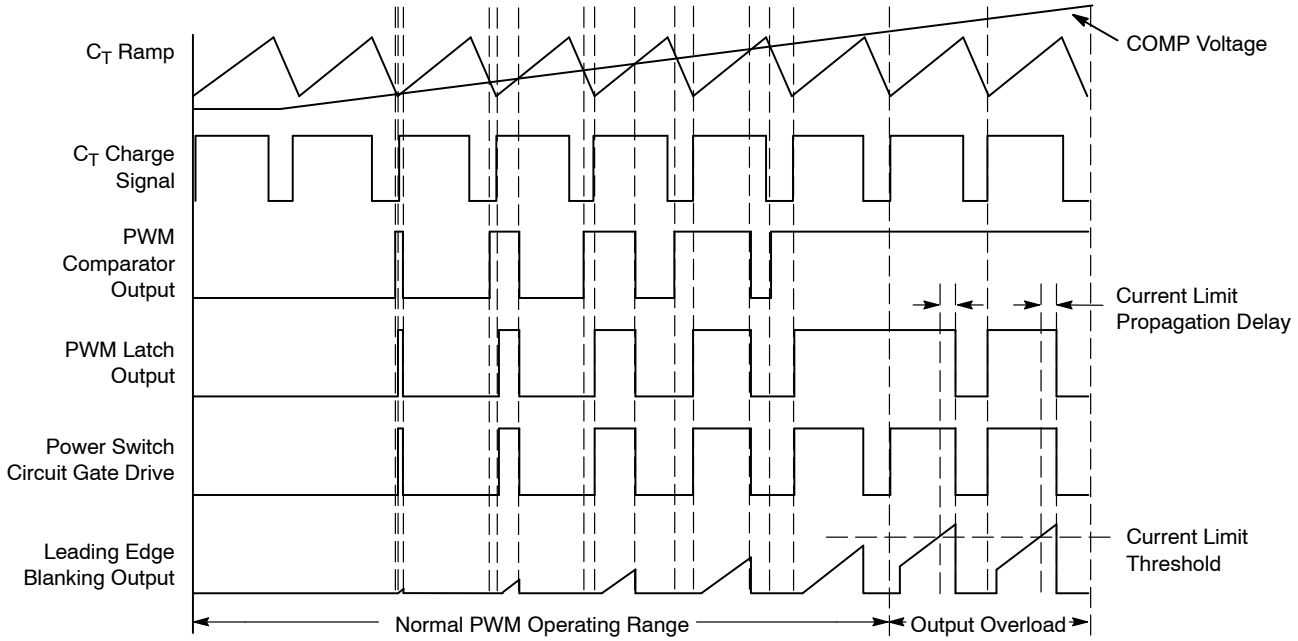

Figure 2. Pulse Width Modulation Timing Diagram

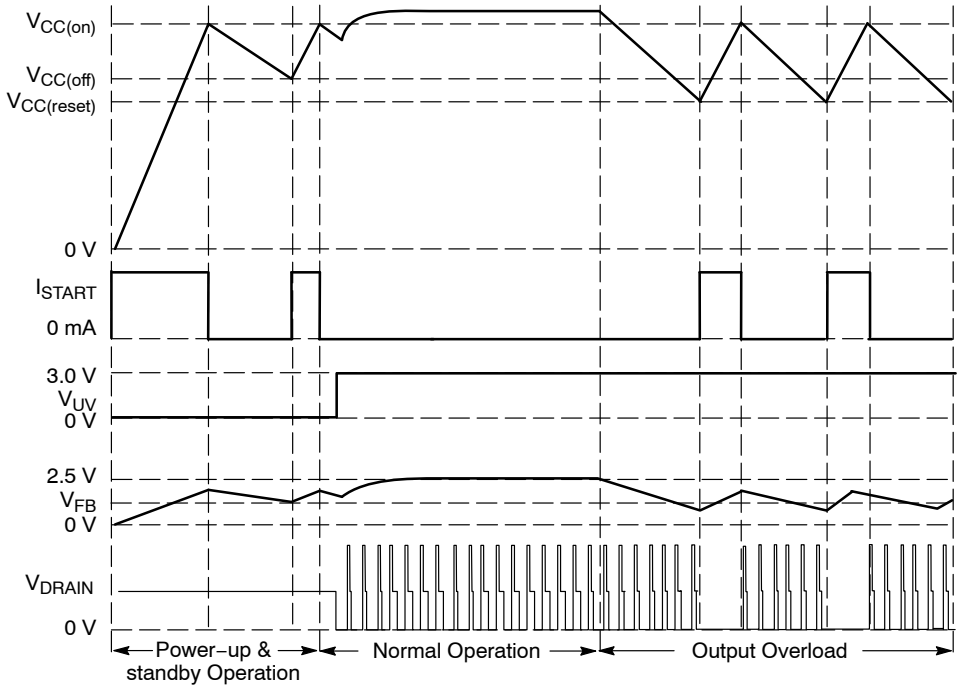

Figure 3. Auxiliary Winding Operation with Output Overload Timing Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Switch and Startup Circuits Voltage	V_{DRAIN}	−0.3 to 200	V
Power Switch and Startup Circuits Input Current − NCP1030 − NCP1031	I_{DRAIN}	 1.0 2.0	A
V_{CC} Voltage Range	V_{CC}	−0.3 to 16	V
All Other Inputs/Outputs Voltage Range	V_{IO}	−0.3 to 10	V
V_{CC} and All Other Inputs/Outputs Current	I_{IO}	100	mA
Operating Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	T_{stg}	−55 to 150	°C
Power Dissipation (T_J = 25°C, 2.0 Oz., 1.0 Sq Inch Printed Circuit Copper Clad) DM Suffix, Plastic Package Case 846A D Suffix, Plastic Package Case 751 MN Suffix, Plastic Package Case 488AF		 0.582 0.893 1.453	W
Thermal Resistance, Junction to Air (2.0 Oz., 1.0 Sq Inch Printed Circuit Copper Clad) DM Suffix, Plastic Package Case 846A D Suffix, Plastic Package Case 751 MN Suffix, Plastic Package Case 488AF	$R_{\theta JA}$	 172 112 69	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

A. This device contains ESD protection circuitry and exceeds the following tests:
   Pins 1−7: Human Body Model 2000V per MIL−STD−883, Method 3015.
   Machine Model Method 200 V.
   Pin 8 is connected to the High Voltage Startup and Power Switch Circuits and rated only to the maximum voltage rating of the part, or 200 V.

B. This device contains Latchup protection and exceeds ±100 mA per JEDEC Standard JESD78.

DC ELECTRICAL CHARACTERISTICS (V_{DRAIN} = 48 V, V_{CC} = 12 V, C_T = 560 pF, V_{UV} = 3 V, V_{OV} = 2 V, V_{FB} = 2.3 V, V_{COMP} = 2.5 V, T_J = −40°C to 125°C, typical values shown are for T_J = 25°C unless otherwise noted.) (Note 1)

Characteristics	Symbol	Min	Typ	Max	Unit
STARTUP CONTROL					
Startup Circuit Output Current (V_{FB} = V_{COMP})	I_{START}				mA
NCP1030					
T_J = 25°C					
V_{CC} = 0 V		10	12.5	15	
V_{CC} = $V_{CC(on)}$ − 0.2 V		6.0	8.6	12	
T_J = −40°C to 125°C					
V_{CC} = 0 V		8.0	–	16	
V_{CC} = $V_{CC(on)}$ − 0.2 V		2.0	–	13	
NCP1031					
T_J = 25°C					
V_{CC} = 0 V		13	16	19	
V_{CC} = $V_{CC(on)}$ − 0.2 V		8.0	12	16	
T_J = −40°C to 125°C					
V_{CC} = 0 V		11	–	21	
V_{CC} = $V_{CC(on)}$ − 0.2 V		4.0	–	18	
V_{CC} Supply Monitor (V_{FB} = 2.7 V)					V
Startup Threshold Voltage (V_{CC} Increasing)	$V_{CC(on)}$	9.6	10.2	10.6	
Minimum Operating V_{CC} After Turn−on (V_{CC} Increasing)	$V_{CC(off)}$	7.0	7.6	8.0	
Hysteresis Voltage	$V_{CC(hys)}$	–	2.6	–	
Undervoltage Lockout Threshold Voltage, V_{CC} Decreasing (V_{FB} = V_{COMP})	$V_{CC(reset)}$	6.0	6.6	7.0	V
Minimum Startup Voltage (Pin 8)	$V_{START(min)}$				V
I_{START} = 0.5 mA, V_{CC} = $V_{CC(on)}$ − 0.2 V		–	16.8	18.5	
ERROR AMPLIFIER					
Reference Voltage (V_{COMP} = V_{FB}, Follower Mode)	V_{REF}				V
T_J = 25°C		2.45	2.5	2.55	
T_J = −40°C to 125°C		2.40	2.5	2.60	
Line Regulation (V_{CC} = 8 V to 16 V, T_J = 25°C)	REG_{LINE}	–	1.0	5.0	mV
Input Bias Current (V_{FB} = 2.3 V)	I_{VFB}	–	0.1	1.0	μA
COMP Source Current	I_{SRC}	80	110	140	μA
COMP Sink Current (V_{FB} = 2.7 V)	I_{SNK}	200	550	900	μA
COMP Maximum Voltage (I_{SRC} = 0 μA)	$V_{C(max)}$	4.5	–	–	V
COMP Minimum Voltage (I_{SNK} = 0 μA, V_{FB} = 2.7 V)	$V_{C(min)}$	–	–	1.0	V
Open Loop Voltage Gain	A_{VOL}	–	80	–	dB
Gain Bandwidth Product	GBW	–	1.0	–	MHz
LINE UNDER/OVERVOLTAGE DETECTOR					
Undervoltage Lockout (V_{FB} = V_{COMP})					
Voltage Threshold (V_{in} Increasing)	V_{UV}	2.400	2.550	2.700	V
Voltage Hysteresis	$V_{UV(hys)}$	0.075	0.175	0.275	V
Input Bias Current	I_{UV}	–	0	1.0	μA
Overvoltage Lockout (V_{FB} = V_{COMP})					
Voltage Threshold (V_{in} Increasing)	V_{OV}	2.400	2.550	2.700	V
Voltage Hysteresis	$V_{OV(hys)}$	0.075	0.175	0.275	V
Input Bias Current	I_{OV}	–	0	1.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Production testing for NCP1030DMR2 is performed at 25°C only; limits at −40°C and 125°C are guaranteed by design.

DC ELECTRICAL CHARACTERISTICS (V_{DRAIN} = 48 V, V_{CC} = 12 V, C_T = 560 pF, V_{UV} = 3 V, V_{OV} = 2 V, V_{FB} = 2.3 V, V_{COMP} = 2.5 V, T_J = −40°C to 125°C, typical values shown are for T_J = 25°C unless otherwise noted.) (Note 2)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (C_T = 560 pF, Note 3) T_J = 25°C T_J = −40°C to 125°C	f_{OSC1}	 275 260	 300 –	 325 325	kHz
Frequency (C_T = 100 pF)	f_{OSC2}	–	800	–	kHz
Charge Current (V_{CT} = 3.25 V)	$I_{CT(C)}$	–	215	–	μA
Discharge Current (V_{CT} = 3.25 V)	$I_{CT(D)}$	–	645	–	μA
Oscillator Ramp Peak Valley	 Vrpk V_{rvly}	 – –	 3.5 3.0	 – –	V
PWM COMPARATOR					
Maximum Duty Cycle	DC_{MAX}	70	75	80	%
POWER SWITCH CIRCUIT					
Power Switch Circuit On−State Resistance (I_D = 100 mA) NCP1030 T_J = 25°C T_J = 125°C NCP1031 T_J = 25°C T_J = 125°C	$R_{DS(on)}$	 – – – –	 4.1 6.0 2.1 3.5	 7.0 12 3.0 6.0	Ω
Power Switch Circuit and Startup Circuit Breakdown Voltage (I_D = 100 μA, T_J = 25°C)	$V_{(BR)DS}$	200	–	–	V
Power Switch Circuit and Startup Circuit Off−State Leakage Current (V_{DRAIN} = 200 V, V_{UV} = 2.0 V) T_J = 25°C T_J = −40 to 125°C	$I_{DS(off)}$	 – –	 13 –	 25 50	μA
Switching Characteristics (V_{DS} = 48 V, R_L = 100 Ω) Rise Time Fall Time	 t_r t_f	 – –	 22 24	 – –	ns
CURRENT LIMIT AND OVER TEMPERATURE PROTECTION					
Current Limit Threshold (T_J = 25°C) NCP1030 (di/dt = 0.5 A/μs) NCP1031 (di/dt = 1.0 A/μs)	I_{LIM}	 350 700	 515 1050	 680 1360	mA
Propagation Delay, Current Limit Threshold to Power Switch Circuit Output (Leading Edge Blanking plus Current Limit Delay)	t_{PLH}	–	100	–	ns
Thermal Protection (Note 4) Shutdown Threshold (T_J Increasing) Hysteresis	 T_{SHDN} T_{HYS}	 – –	 150 45	 – –	°C
TOTAL DEVICE					
Supply Current After UV Turn−On Power Switch Enabled Power Switch Disabled Non−Fault condition (V_{FB} = 2.7 V) Fault Condition (V_{FB} = 2.7 V, V_{UV} = 2.0 V)	 I_{CC1} I_{CC2} I_{CC3}	 2.0 – –	 3.0 1.5 0.65	 4.0 2.0 1.2	mA

2. Production testing for NCP1030DMR2 is performed at 25°C only; limits at −40°C and 125°C are guaranteed by design.
3. Oscillator frequency can be externally synchronized to the maximum frequency of the device.
4. Guaranteed by design only.

TYPICAL CHARACTERISTICS

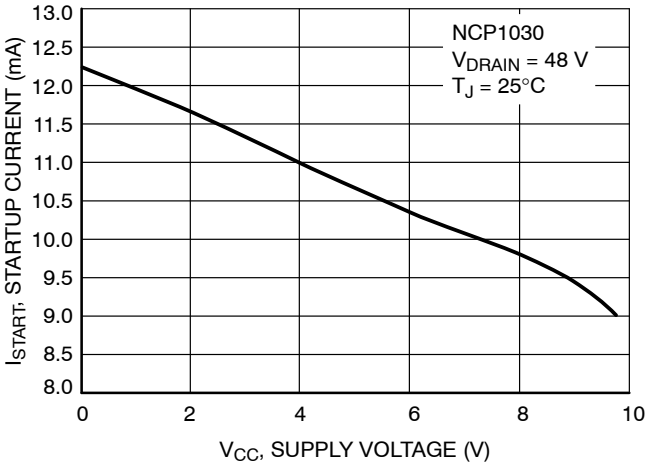

Figure 4. NCP1030 Startup Current vs. Supply Voltage

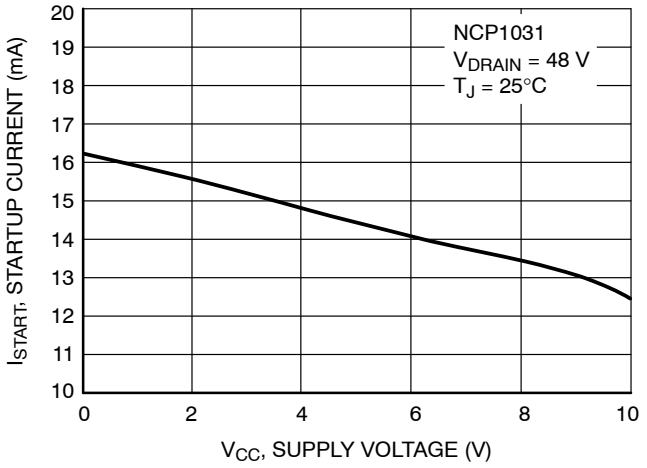

Figure 5. NCP1031 Startup Current vs. Supply Voltage

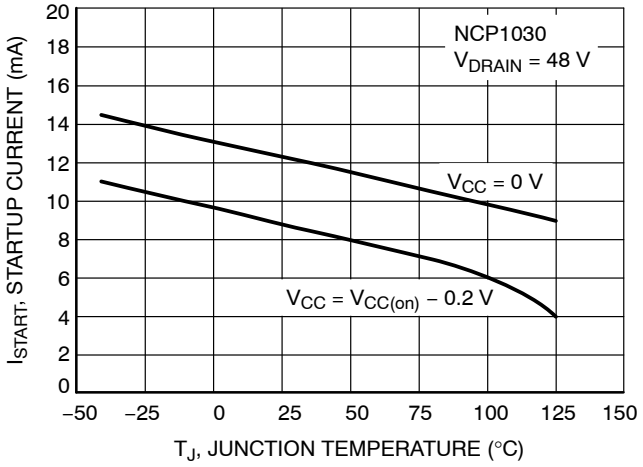

Figure 6. NCP1030 Startup Current vs. Junction Temperature

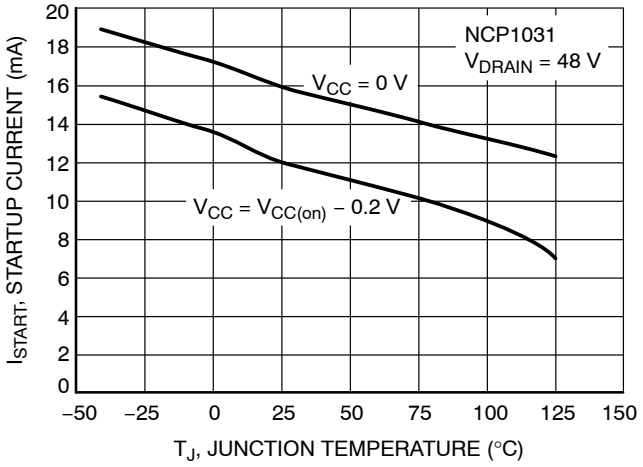

Figure 7. NCP1031 Startup Current vs. Junction Temperature

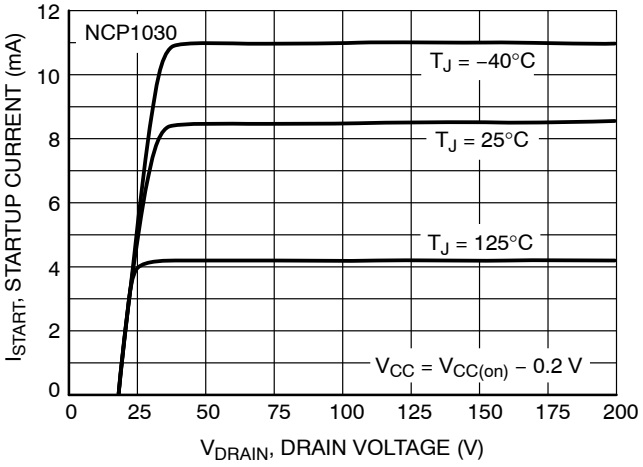

Figure 8. NCP1030 Startup Current vs. Drain Voltage

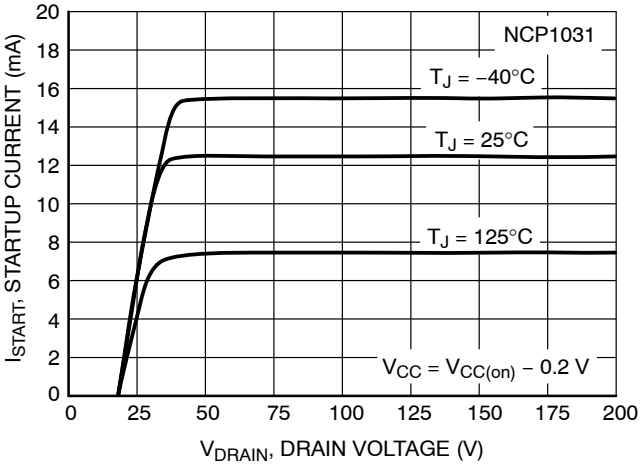

Figure 9. NCP1031 Startup Current vs. Drain Voltage

TYPICAL CHARACTERISTICS

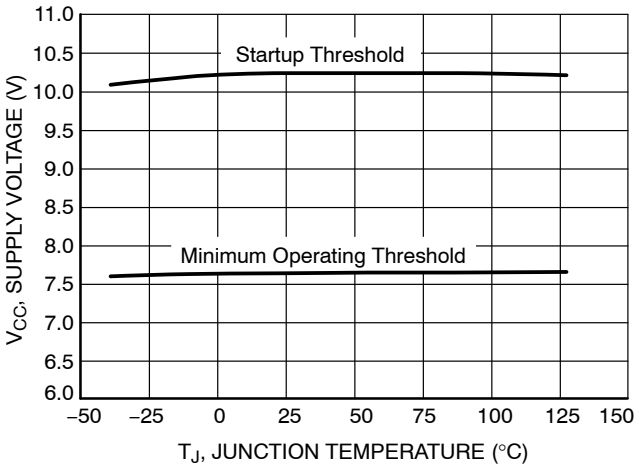

Figure 10. Supply Voltage Thresholds vs. Junction Temperature

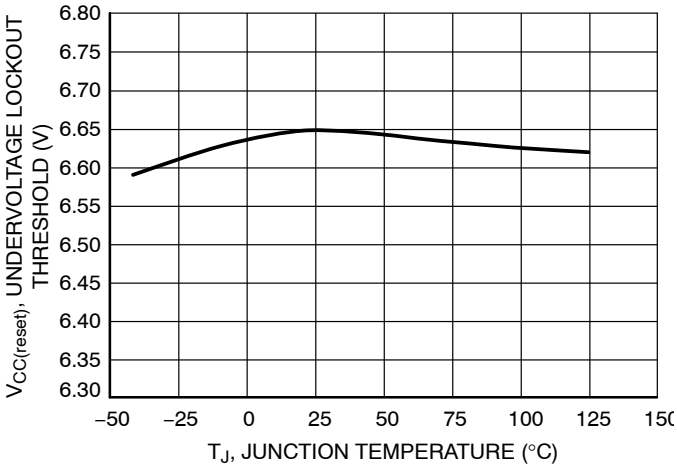

Figure 11. Undervoltage Lockout Threshold vs. Junction Temperature

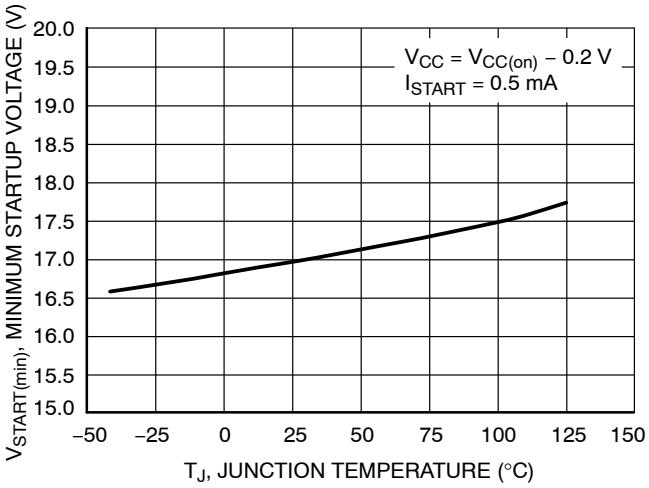

Figure 12. Minimum Startup Voltage vs. Junction Temperature

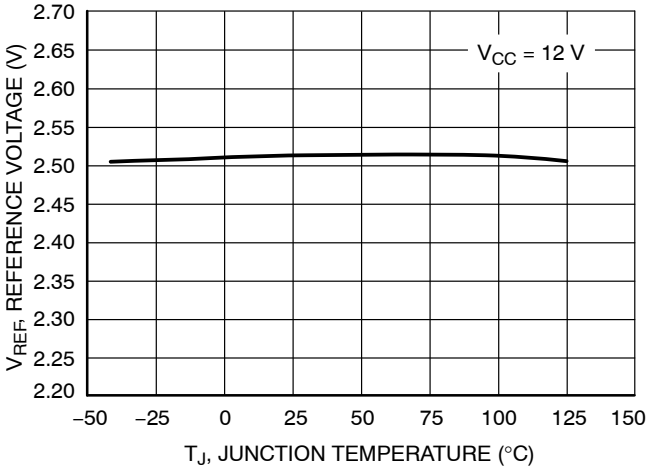

Figure 13. Reference Voltage vs. Junction Temperature

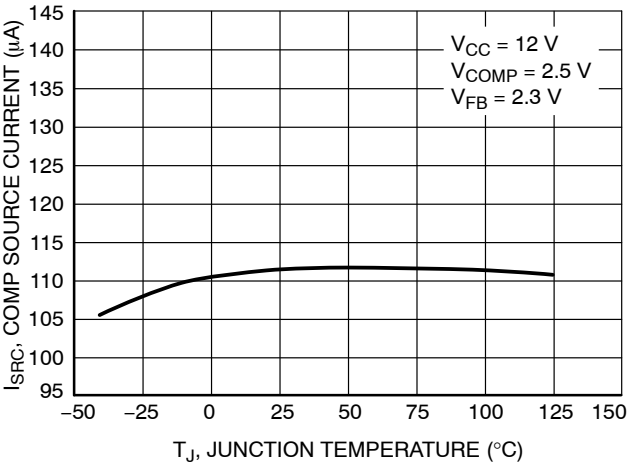

Figure 14. COMP Source Current vs. Junction Temperature

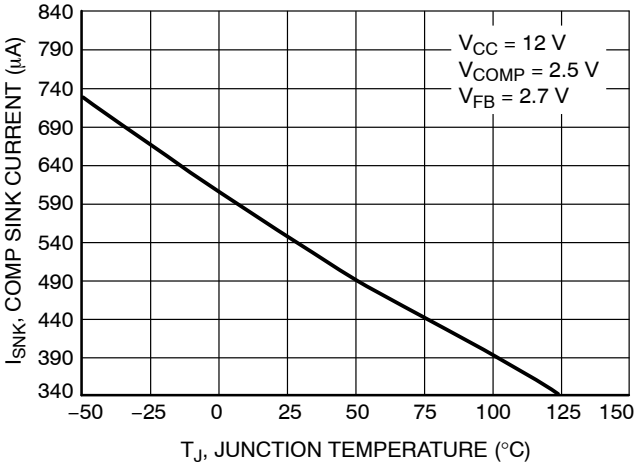

Figure 15. COMP Sink Current vs. Junction Temperature

TYPICAL CHARACTERISTICS

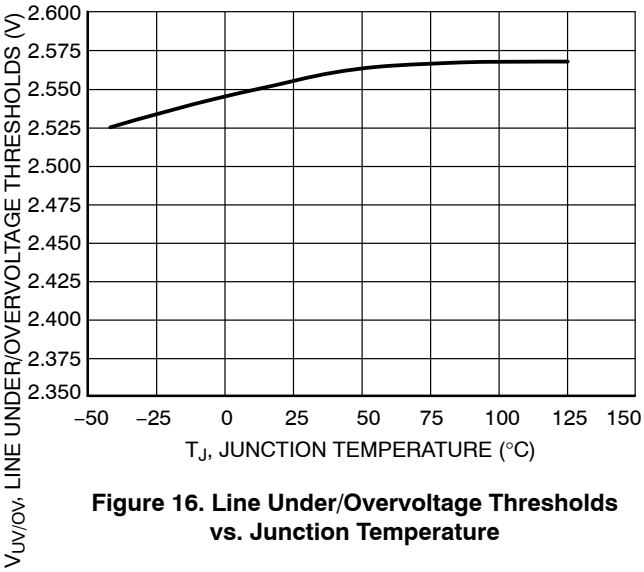

Figure 16. Line Under/Overvoltage Thresholds vs. Junction Temperature

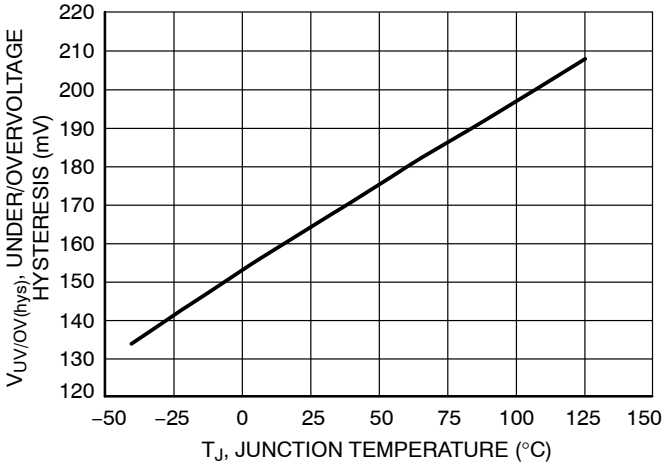

Figure 17. Line Under/Overvoltage Hysteresis vs. Junction Temperature

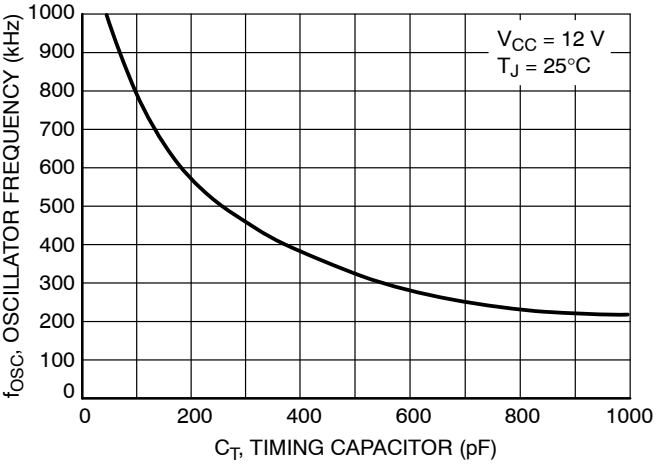

Figure 18. Oscillator Frequency vs. Timing Capacitor

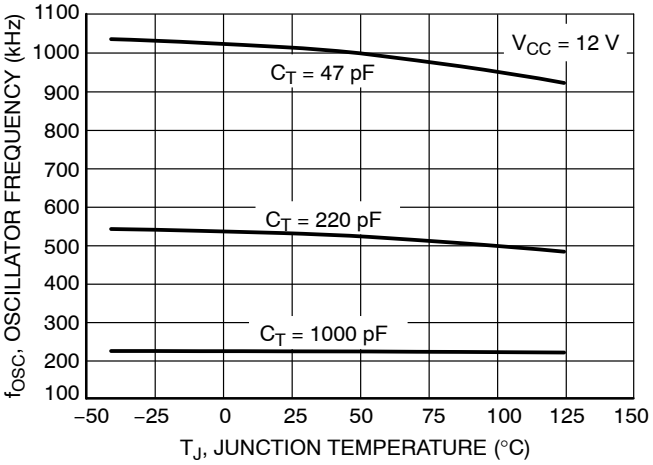

Figure 19. Oscillator Frequency vs. Junction Temperature

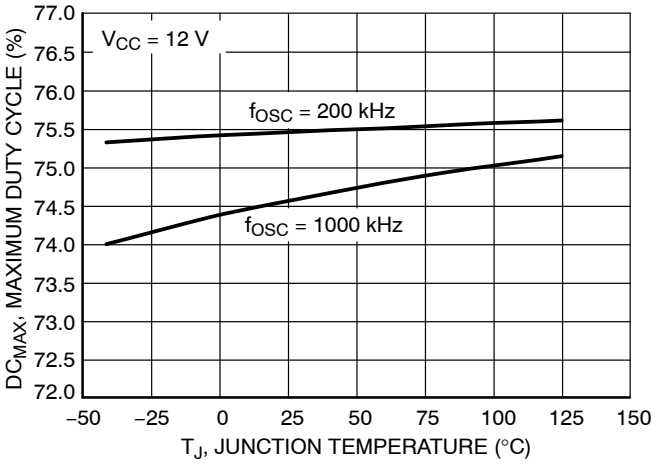

Figure 20. Maximum Duty Cycle vs. Junction Temperature

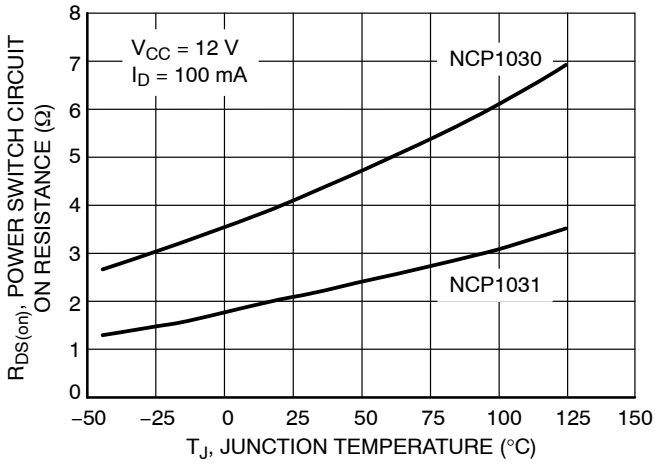

Figure 21. Power Switch Circuit On Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS

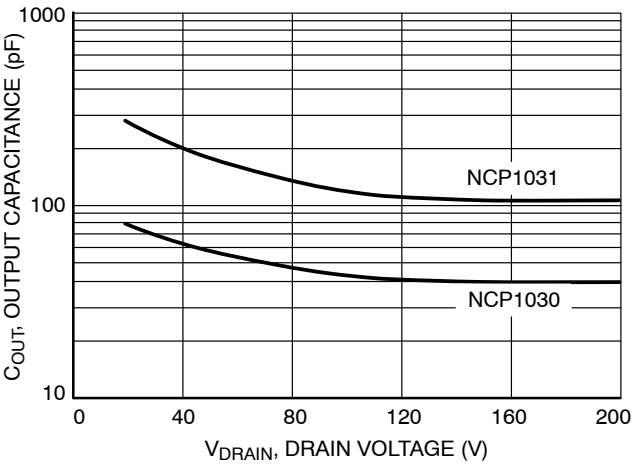

Figure 22. Power Switch Circuit Output Capacitance vs. Drain Voltage

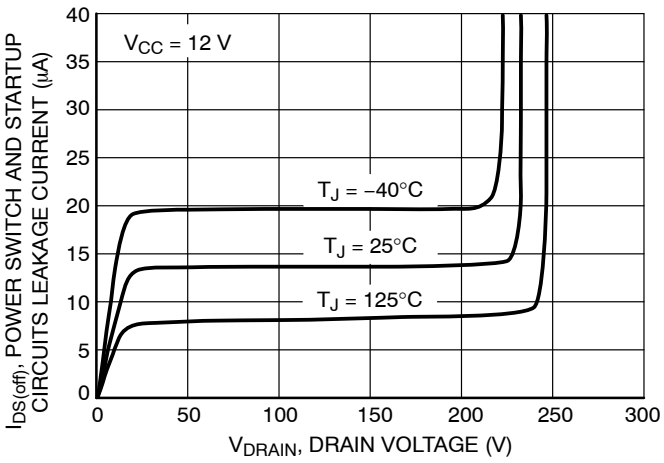

Figure 23. Power Switch Circuit and Startup Circuit Leakage Current vs. Drain Voltage

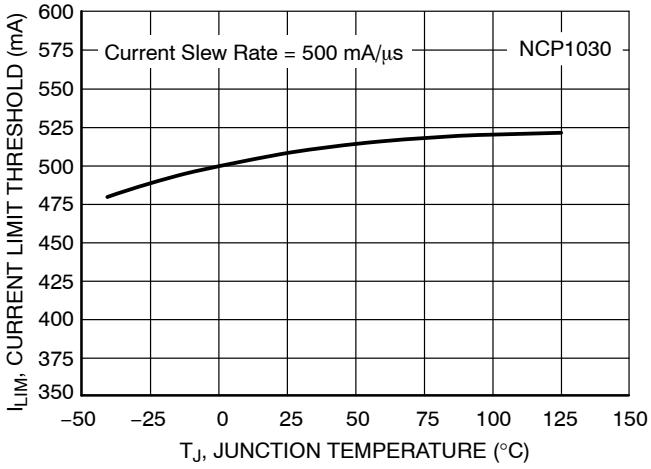

Figure 24. NCP1030 Current Limit Threshold vs. Junction Temperature

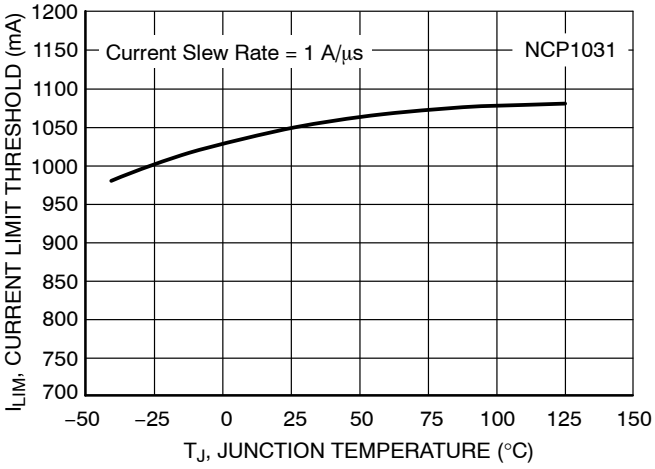

Figure 25. NCP1031 Current Limit Threshold vs. Junction Temperature

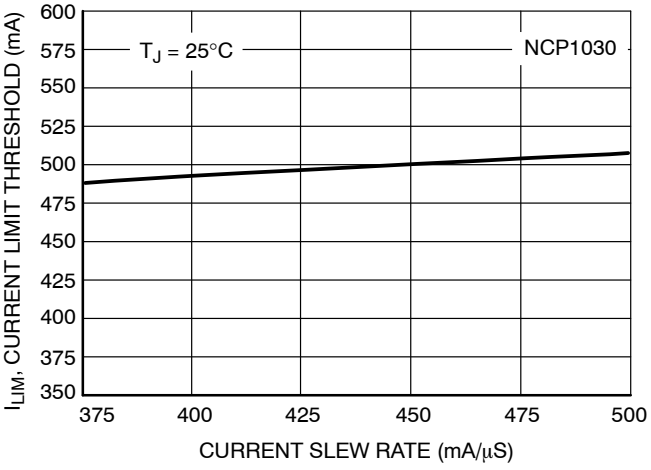

Figure 26. NCP1030 Current Limit Threshold vs. Current Slew Rate

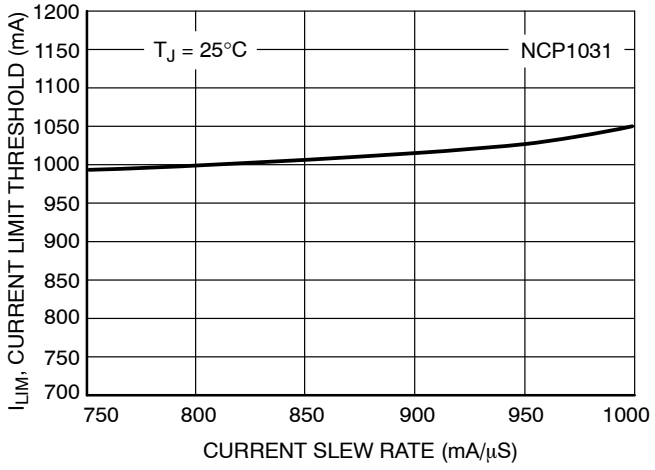

Figure 27. NCP1031 Current Limit Threshold vs. Current Slew Rate

TYPICAL CHARACTERISTICS

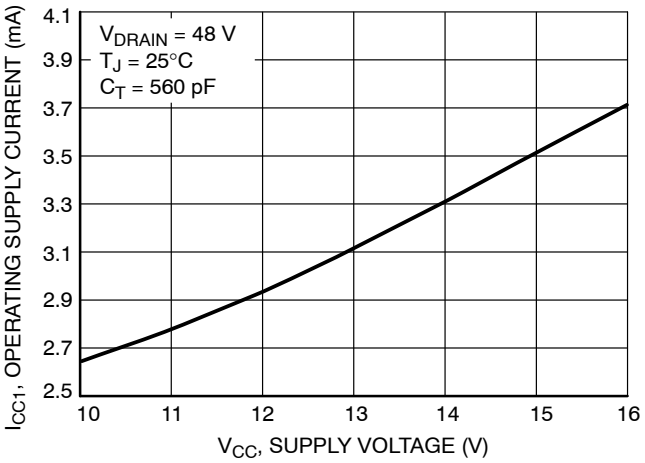

Figure 28. Operating Supply Current vs. Supply Voltage

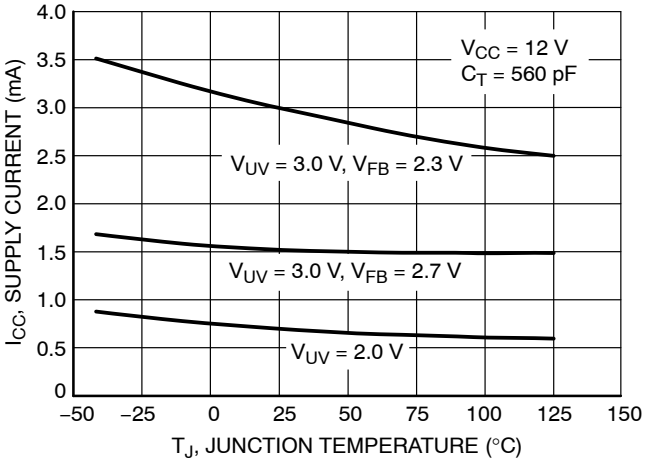

Figure 29. Supply Current vs. Junction Temperature

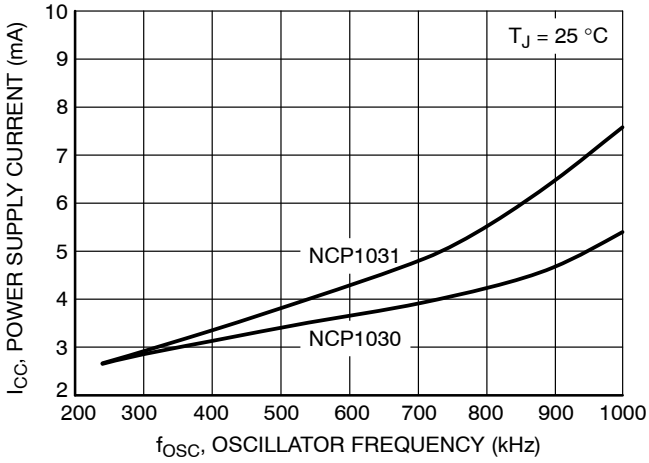

Figure 30. Operating Supply Current vs. Oscillator Frequency

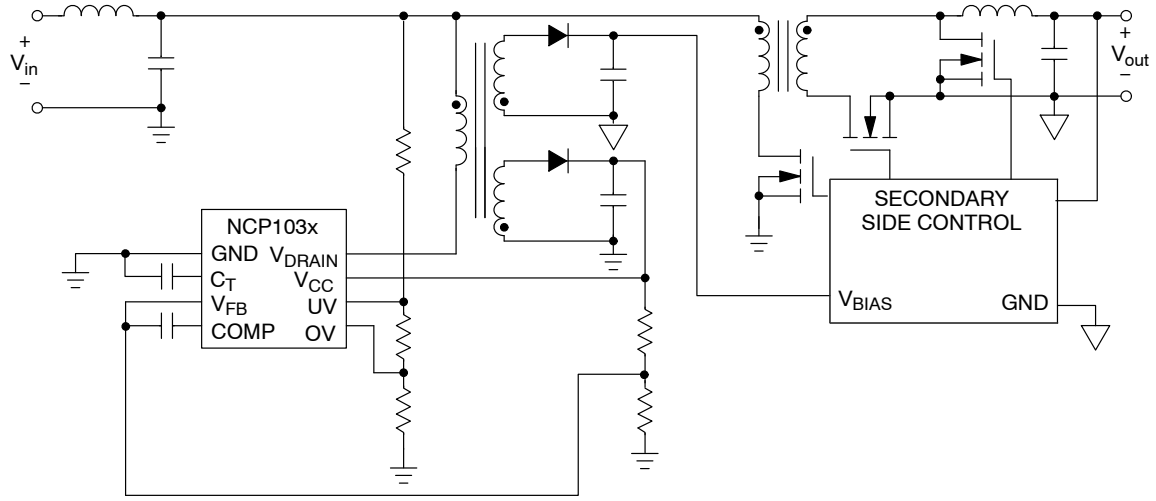

Figure 31. Secondary Side Bias Supply Configuration

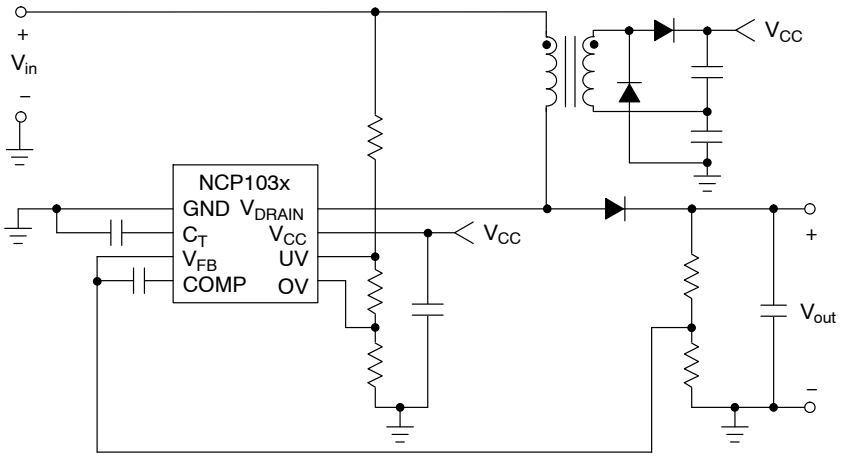

Figure 32. Boost Circuit Configuration

OPERATING DESCRIPTION

Introduction

The NCP1030 and NCP1031 are a family of miniature monolithic voltage−mode switching regulators designed for isolated and non−isolated bias supply applications. The internal startup circuit and the MOSFET are rated at 200 V, making them ideal for 48 V telecom and 42 V automotive applications. In addition, the NCP103x family can operate from an existing 12 V supply. This controller family is optimized for operation up to 1 MHz.

The NCP103x family incorporates in a single IC all the active power, control logic and protection circuitry required to implement, with a minimum of external components, several switching regulator applications, such as a secondary side bias supply or a low power dc−dc converter.

The NCP1030 is available in the space saving Micro8™ package and is targeted for applications requiring up to 3 W. The NCP1031 is targeted for applications up to 6 W and is available in the SO−8 package.

The NCP103x includes an extensive set of features including over temperature protection, cycle by cycle current limit, individual line under and overvoltage detection comparators with hysteresis, and regulator output undervoltage lockout with hysteresis, providing full protection during fault conditions. A description of each of the functional blocks is given below, and the representative block diagram is shown in Figure 2.

Startup Circuit and Undervoltage Lockout

The NCP103x contains an internal 200 V startup regulator that eliminates the need for external startup components. The startup regulator consists of a constant current source that supplies current from the input line (V_{in}) to the capacitor on the V_{CC} pin (C_{CC}). Once the V_{CC} voltage reaches approximately 10 V, the startup circuit is disabled and the Power Switch Circuit is enabled if no faults are present. During this self−bias mode, power to the NCP103x is supplied by the V_{CC} capacitor. The startup regulator turns ON again once V_{CC} reaches 7.5 V. This “7.5−10” mode of operation is known as Dynamic Self Supply (DSS). The NCP1030 and NCP1031 startup currents are 12 mA and 16 mA, respectively.

If V_{CC} falls below 7.5 V, the device enters a re−start mode. While in the re−start mode, the V_{CC} capacitor is allowed to discharge to 6.5 V while the Power Switch is enabled. Once the 6.5 V threshold is reached, the Power Switch Circuit is disabled and the startup regulator is enabled to charge the V_{CC} capacitor. The Power Switch is enabled again once the V_{CC} voltage reaches 10 V. Therefore, the external V_{CC} capacitor must be sized such that a voltage greater than 7.5 V is maintained on the V_{CC} capacitor while the converter output reaches regulation. Otherwise, the converter will enter the re−start mode. Equation (1) provides a guideline for the selection of the V_{CC} capacitor for a forward converter;

Forward:

$$C_{CC} = \frac{\cos^{-1}\left(1 - \frac{V_{OUT} \cdot N_P}{DC \cdot V_{in} \cdot N_S}\right) \times \sqrt{L_{OUT} C_{OUT}} \cdot I_{bias}}{2.6} \quad \text{(eq. 1)}$$

where, I_{bias} is the bias current supplied by the V_{CC} capacitor including the IC bias current (I_{CC1}) and any additional current used to bias the feedback resistors (if used).

After initial startup, the V_{CC} pin should be biased above $V_{CC(off)}$ using an auxiliary winding. This will prevent the startup regulator from turning ON and reduce power dissipation. Also, the load should not be directly connected to the V_{CC} capacitor. Otherwise, the load may override the startup circuit. Figure 33 shows the recommended configuration for a non−isolated flyback converter.

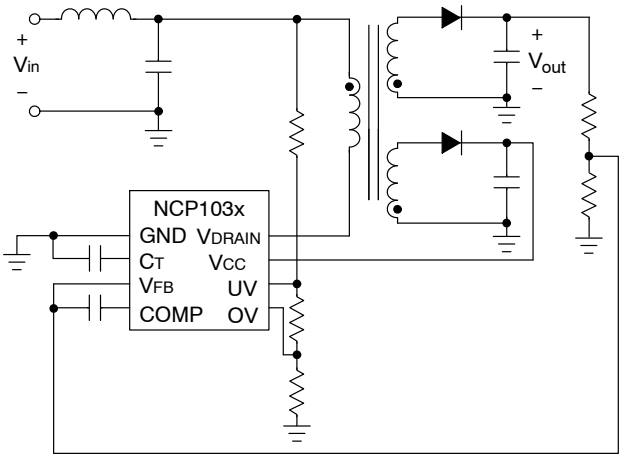

Figure 33. Non−Isolated Bias Supply Configuration

The maximum voltage rating of the startup circuit is 200 V. Power dissipation should be observed to avoid exceeding the maximum power dissipation of the package.

Error Amplifier

The internal error amplifier (EA) regulates the output voltage of the bias supply. It compares a scaled output voltage signal to an internal 2.5 V reference (V_{REF}) connected to its non−inverting input. The scaled signal is fed into the feedback pin (V_{FB}) which is the inverting input of the error amplifier.

The output of the error amplifier is available for frequency compensation and connection to the PWM comparator through the COMP pin. To insure normal operation, the EA compensation should be selected such that the EA frequency response crosses 0 dB below 80 kHz.

The error amplifier input bias current is less than 1 μA over the operating range. The output source and sink currents are typically 110 μA and 550 μA, respectively.

Under load transient conditions, COMP may need to move from the bottom to the top of the C_T Ramp. A large current is required to complete the COMP swing if small resistors or large capacitors are used to implement the compensation network. In which case, the COMP swing will

be limited by the EA sink current, typically 110 μA. Optimum transient response is obtained if the compensation components allow COMP to swing across its operating range in 1 cycle.

Line Under and Overvoltage Detector

The NCP103x incorporates individual line undervoltage (UV) and overvoltage (OV) shutdown circuits. The UV and OV thresholds are 2.5 V. A fault is present if the UV is below 2.5 V or if the OV voltage is above 2.5 V. The UV/OV detectors incorporate 175 mV hysteresis to prevent noise from triggering the shutdown circuits.

The UV/OV circuits can be biased using an external resistor divider from the input line as shown in Figure 34. The UV/OV pins should be bypassed using a capacitor to prevent triggering the UV or OV circuits during normal switching operation.

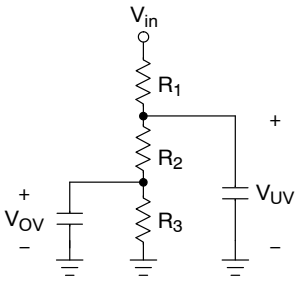

Figure 34. UV/OV Resistor Divider from the Input Line

The resistor divider must be sized to enable the controller once V_{in} is within the required operating range. While a UV or OV fault is present, switching is not allowed and the COMP pin is effectively grounded.

Either of these comparators can be used for a different function if UV or OV functions are not needed. For example, the UV/OV detectors can be used to implement an enable or disable function. If positive logic is used, the enable signal is applied to the UV pin while the OV pin is grounded. If negative logic is used, the disable signal is applied to the OV pin while biasing the UV pin from V_{CC} using a resistor divider.

Oscillator

The oscillator is optimized for operation up to 1 MHz and its frequency is set by the external timing capacitor (C_T) connected to the C_T pin. The oscillator has two modes of operation, free running and synchronized (sync). While in free running mode, an internal current source sequentially charges and discharges C_T generating a voltage ramp between 3.0 V and 3.5 V. Under normal operating conditions, the charge ($I_{CT(C)}$) and discharge ($I_{CT(D)}$) currents are typically 215 μA and 645 μA, respectively. The charge:discharge current ratio of 1:3 discharges C_T in 25 % of the total period. The Power Switch is disabled while C_T is discharging, guaranteeing a maximum duty cycle of 75 % as shown in Figure 35.

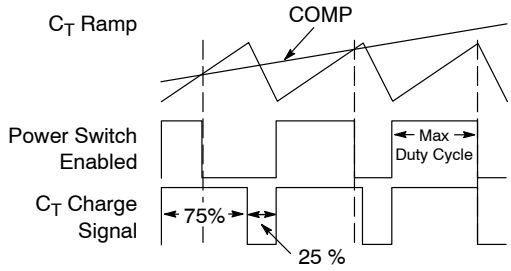

Figure 35. Maximum Duty Cycle vs COMP

Figure 18 shows the relationship between the operating frequency and C_T. If an UV fault is present, both $I_{CT(C)}$ and $I_{CT(D)}$ are reduced by a factor of 7, thus reducing the operating frequency by the same factor.

The oscillator can be synchronized to a higher frequency by capacitively coupling a synchronization pulse into the C_T pin. In sync mode, the voltage on the C_T pin needs to be driven above 3.5 V to trigger the internal comparator and complete the C_T charging period. However, pulsing the C_T pin before it reaches 3.5 V will reduce the p−p amplitude of the C_T Ramp as shown in Figure 36.

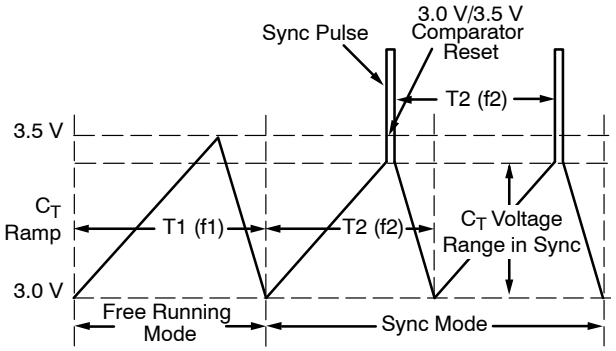

Figure 36. External Frequency Synchronization Waveforms

The oscillator frequency should be set no more that 25% below the target sync frequency to maintain an adequate voltage range and provide good noise immunity. A possible circuit to synchronize the oscillator is shown in Figure 37.

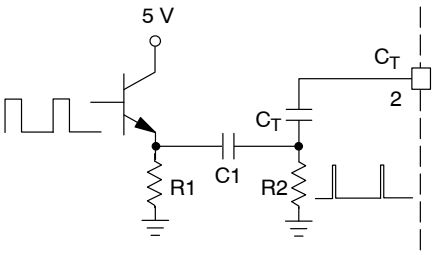

Figure 37. External Frequency Synchronization Circuit.

PWM Comparator and Latch

The Pulse Width Modulator (PWM) Comparator compares the error amplifier output (COMP) to the C_T Ramp and generates a proportional duty cycle. The Power Switch is enabled while the C_T Ramp is below COMP as shown in Figure 35. Once the C_T Ramp reaches COMP, the Power Switch is disabled. If COMP is at the bottom of the C_T Ramp, the converter operates at minimum duty cycle. While COMP increases, the duty cycle increases, until COMP reaches the peak of the C_T Ramp, at which point the controller operates at maximum duty cycle.

The C_T Charge Signal is filtered through a One Shot Pulse Generator to set the PWM Latch and enable switching at the beginning of each period. Switching is allowed while the C_T Ramp is below COMP and a current limit fault is not present.

The PWM Latch and Comparator propagation delay is typically 150 ns. If the system is designed to operate with a minimum ON time less than 150 ns, the converter will skip pulses. Skipping pulses is usually not a problem, unless operating at a frequency close to the audible range. Skipping pulses is more likely when operating at high frequencies during high line and minimum load condition.

A series resistor is included for ESD protection between the EA output and the COMP pin. Under normal operation, a 220 mV offset is observed between the C_T Ramp and the COMP crossing points. This is not a problem as the series resistor does not interact with the error amplifier transfer function.

Current Limit Comparator and Power Switch Circuit

The NCP103x monolithically integrates a 200 V Power Switch Circuit with control logic circuitry. The Power Switch Circuit is designed to directly drive the converter transformer. The characteristics of the Power Switch Circuit are well known. Therefore, the gate drive is tailored to control switching transitions and help limit electromagnetic interference (EMI). The Power Switch Circuit is capable of switching 200 V.

The Power Switch Circuit incorporates SENSEFET™ technology to monitor the drain current. A sense voltage is generated by driving a sense element, R_{SENSE}, with a current proportional to the drain current. The sense voltage is compared to an internal reference voltage on the non−inverting input of the Current Limit Comparator. If the sense voltage exceeds the reference level, the comparator resets the PWM Latch and switching is terminated. The NCP1030 and NCP1031 drain current limit thresholds are 0.5 A and 1.0 A, respectively.

Each time the Power Switch Circuit turns ON, a narrow voltage spike appears across R_{SENSE}. The spike is due to the Power Switch Circuit gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. This spike can cause a premature reset of the PWM Latch. A proprietary active Leading Edge Blanking (LEB) Circuit masks the current signal to prevent the voltage spike from resetting the PWM Latch. The active LEB masks the current signal until the Power Switch turn ON transition is complete. The adaptive LEB period provides better current limit control compared to a fixed blanking period.

The current limit propagation delay time is typically 100 ns. This time is measured from when an overcurrent fault appears at the Power Switch Circuit drain, to the start of the turn−off transition. Propagation delay must be factored in the transformer design to avoid transformer saturation.

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 150°C, the Power Switch Circuit is disabled. Once the junction temperature falls below 105°C, the NCP103x is allowed to resume normal operation. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

Application Considerations

A 2 W bias supply for a 48 V telecom system was designed using the NCP1030. The bias supply generates an isolated 12 V output. The circuit schematic is shown in Figure 38. Application Note AND8119/D describes the design of the bias supply.

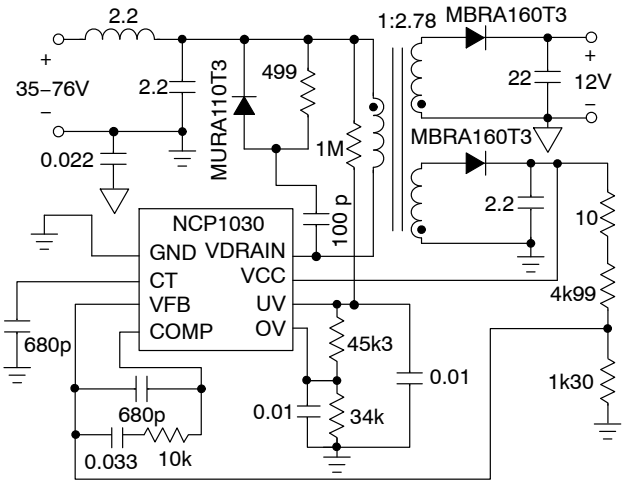

Figure 38. 2 W Isolated Bias Supply Schematic

VCC Excursion and Compensation

Some applications may regulate nodes that are not directly connected to VCC, such as the secondary or AUX1 shown in Figure 39. The regulation of another node can result in loose regulation of VCC. The result of loose regulation is that VCC can rise to unacceptable levels when a heavy load is applied to the regulated node and a relatively light load is applied to the VCC pin. The large voltage can lead to damage of the NCP1030/31 or other downstream parts.

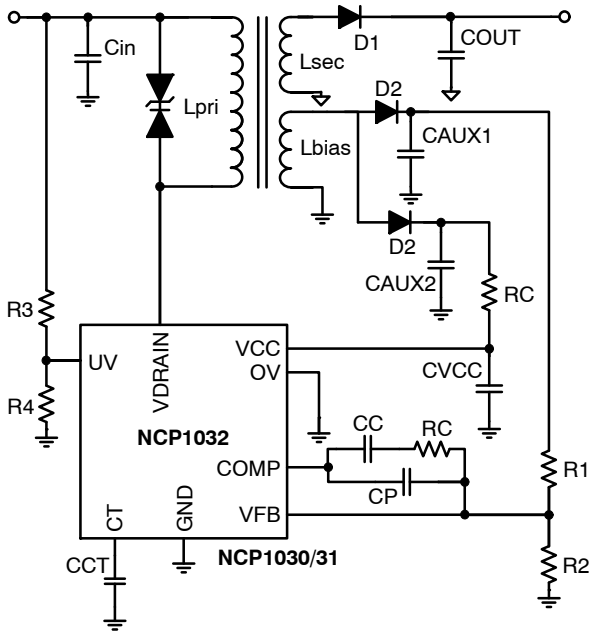

Figure 39. Typical Application with the Series Resistance Added to Control VCC

To reduce the problem, a series resistance can be added to allow the part to clamp VCC with the characteristic current draw of the regulator as the voltage increases. The resistor value required is such that it will not implead normal operation but will prevent damage to the device during transients, startup, current limits, and over loads. The proper sizing of the series resistance starts with an examination of the current draw by the NCP1031 at the desired operating frequency as shown in Figure 40. The resistor value should be such that it does not exceed the VCC maximum voltage of 16 V during the worst case overshoot. Further, the voltage must not fall below the VCC minimum operating voltage of 7 V during heavy loading, transients, or line disturbances. A series resistance calculated example of operation at 310 kHz is shown in Equation 2. In this case, a 1.96 kΩ resistor can be used to make the VCC node more robust.

Calculation of RC

$$16\ V \geq V_{OUTaux} - I_{C\_current} \cdot RC \geq 7.0\ V \qquad \text{(eq. 2)}$$

$$\frac{V_{OUTaux} - 16\ V}{I_{C\_current}} = RC$$

$$\frac{24\ V - 16\ V}{4.075\ mA} = 1.96\ k\Omega$$

$$\frac{12.5\ V - 7.0\ V}{2.65\ mA} = 2.07\ k\Omega$$

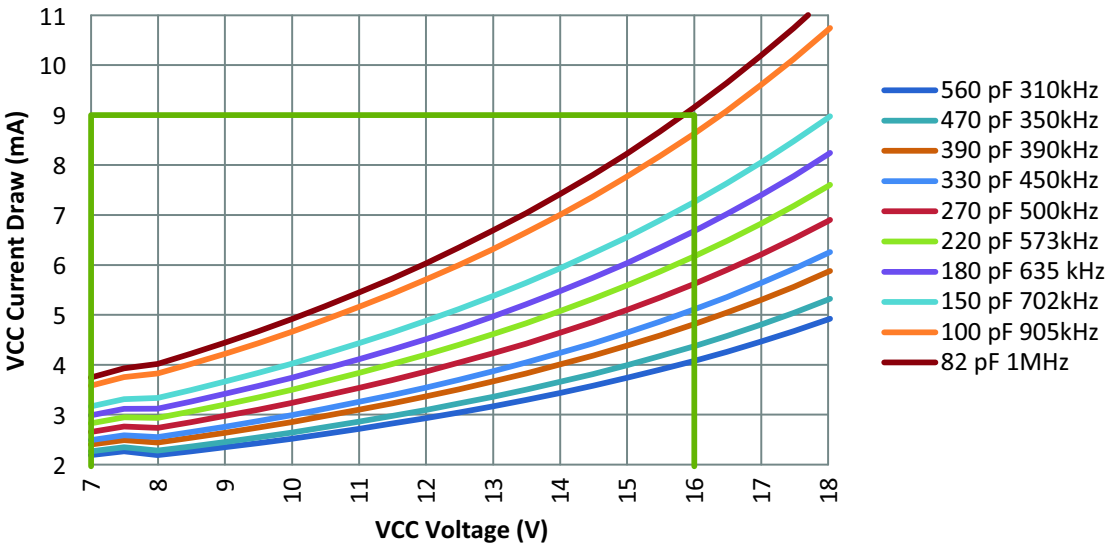

Figure 40. NCP1031 Current Draw vs. Frequency and VCC Voltage

The series resistor needs to be coupled with proper sizing of the auxiliary winding and VCC capacitance. The CAUX1 and CAUX2 should be approximately the same size where the CVCC should be between 1/10 to 1/100 the value of CAUX2. The smaller size of CVCC serves to reduce the amount of energy available to the internal clamping structures in the event of a large unforeseen over voltage. Proper sizing of capacitance and adding a series resistance can reduce the likelihood of an over voltage on the VCC, but cannot eliminate the possibility completely. A zener diode can be added along with the series resistance value calculated from Equation 2 which can be split into RC1 and RC2 as shown in Figure 41. If the OV pin is not used, it can be connected to the VCC node to monitor the voltage and suspend switching if the voltage exceeds a predefined level. The addition of the ROV1 and ROV2 will add a current draw from VAUX and will increase the voltage drop across RC.

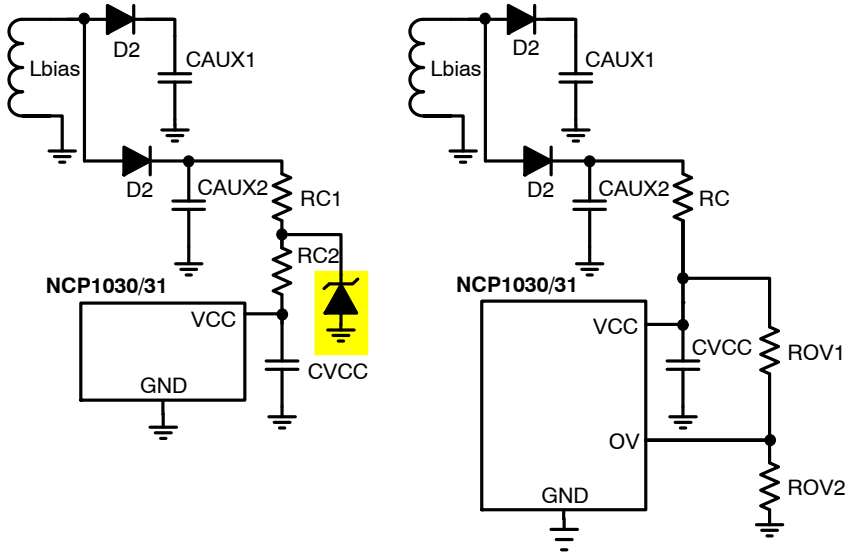

Figure 41. Zener Clamp or OV Protection

The compensation of the NCP1031/30 should be completed with the loop response, the transient response, and the amplifier in mind. The amplifier can source 110 μA and sink 550 μA typical. Internally the current sink that pulls down the amplifier has an on resistance of 2.45 kΩ and an ESD resistance of 1.74 kΩ as shown in Figure 42. The two resistances combine to create a maximum pull down current that changes with comp voltage as shown in Figure 43 and Figure 44.

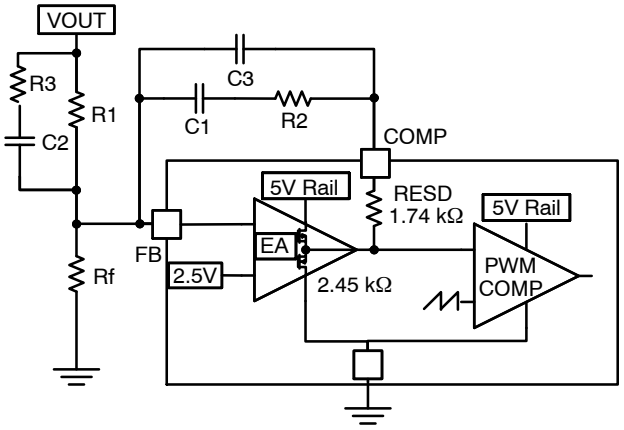

Figure 42. Internal Error Amplifier Structure

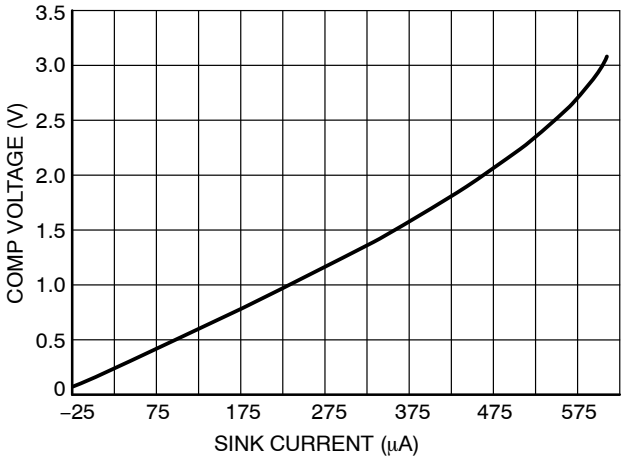

Figure 43. Sink Current vs. Comp Voltage

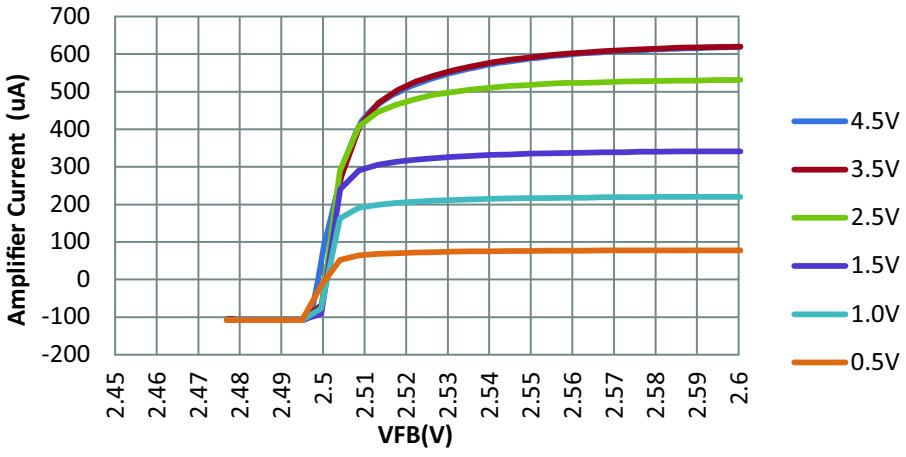

Figure 44. Amplifier Sink Current with Comp at Steady Voltage vs Feedback Voltage

One source of overshoot in the system can occur during startup where the reference voltage starts at 2.5 V and the system PWM regulates to the desired output voltage. The power is limited to the system by the internally set current limit. Since the voltage feedback loop sees the output voltage is lower than it should be, the COMP voltage slews up to increase the duty cycle, but the duty cycle is controlled by the pulse by pulse current limit. Once regulated output voltage is reached, the current loop will maintain control for the time it takes the COMP pin to slew from 5 V to 3.25 V where the voltage loop takes control and the pulse by pulse current limit is no longer limiting the system. The same is true for an overload or current limit. If the COMP voltage has reached a steady state value of 5 V, the required compensation value needed to slew from 5 V to 3.25 V is shown in Equation 3. Equation 3 is true if the feedback node has very low impedance at 2.5 V. For comparison, the decay from 5 V to 3.25 V in network A occurs in 259 ns and network B occurs in 12.2 μs although they have a very similar frequency response.

$$RC1 = \frac{V_{COMP\_INIT} - V_{COMP\_FINAL}}{I_{PULL\_DOWN}} \quad \text{(eq. 3)}$$

$$3.5\ k\Omega = \frac{5\ V - 3.25\ V}{500\ \mu A}$$

$$Time = CP \cdot \frac{V_{COMP\_INIT} - V_{COMP\_FINAL}}{I_{PULL\_DOWN}}$$

$$300\ ns = 100\ pF \cdot \frac{5\ V - 3.25\ V}{500\ \mu A}$$

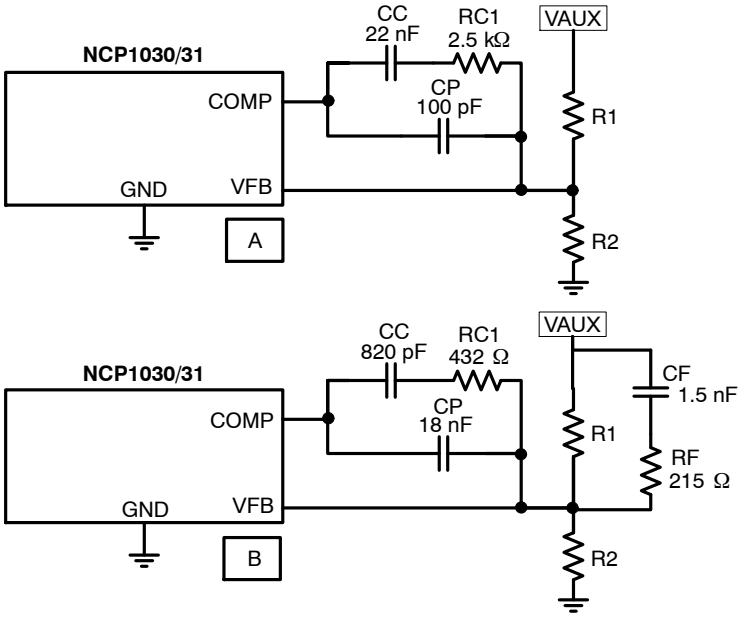

Figure 45. Compensation for Good Transient Response

When considering compensation and overshoot, the designer should follow a few rules for a better result.

1. If the current flowing through R1 and R2 is 10X larger than 620 μA then the RF and CF contribution to the large signal is small.
   a.) If RF is small (1 Ω -100 Ω) there is only a small DC shift from RC1.
   b.) To create a large DC shift down, increase RF (1 kΩ -10 kΩ).
2. Keep CP small (CP < 1 nF) or it will slow the large signal response of the converter.
3. CF should be less than 22 nF.
4. RC1 should be 2.7 k < RC1 < 100 k.

ORDERING INFORMATION

Device	Package	Shipping†
NCP1030DMR2	Micro8	4000 / Tape & Reel
NCP1030DMR2G	Micro8 (Pb−Free)	4000 / Tape & Reel
NCP1031DR2	SOIC−8	2500 / Tape & Reel
NCP1031DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1031MNTXG	DFN8 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

Micro8 is a trademark of International Rectifier.
SENSEFET is a registered trademark of Semiconductor Components Industries, LLC.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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CASE 488AF−01
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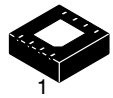

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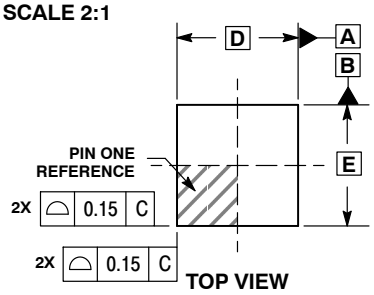
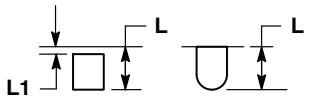
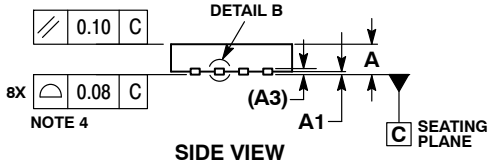
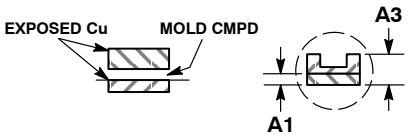


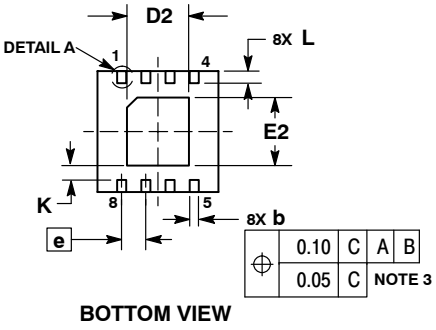




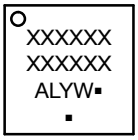


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL CONSTRUCTIONS FOR TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	1.91	2.21
E	4.00 BSC	
E2	2.09	2.39
e	0.80 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15



GENERIC MARKING DIAGRAM*

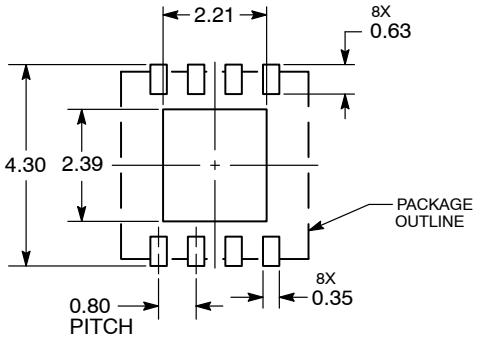


XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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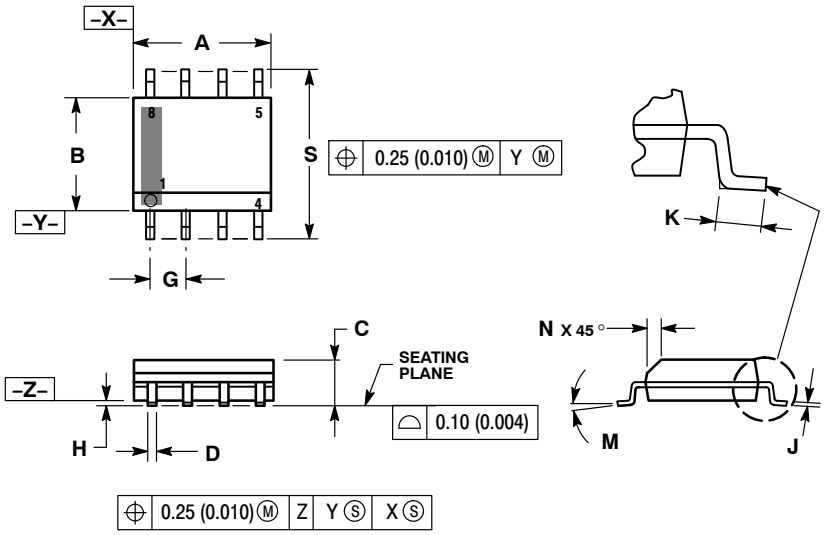
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

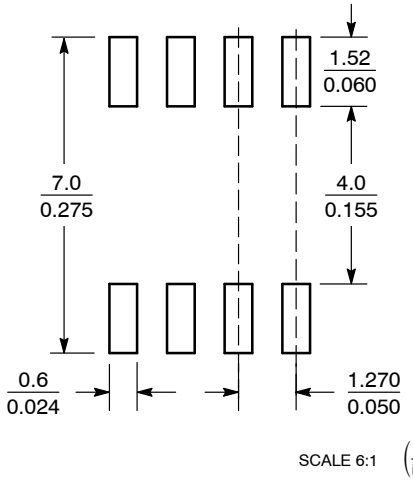
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

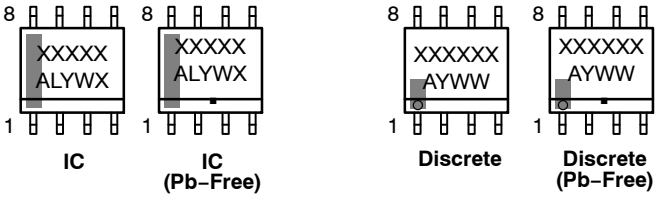
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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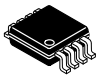
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

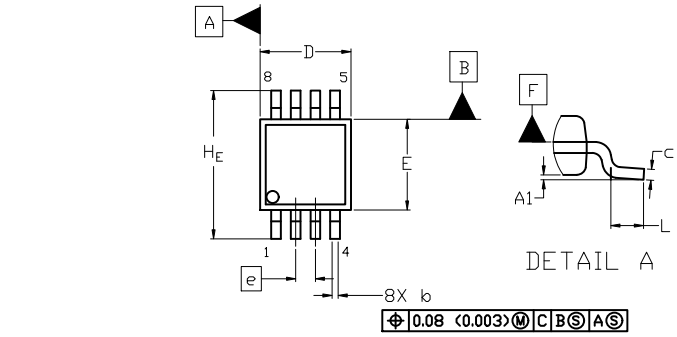
ON Semiconductor®

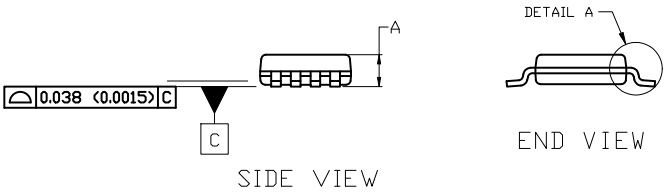


SCALE 2:1

Micro8
CASE 846A−02
ISSUE K

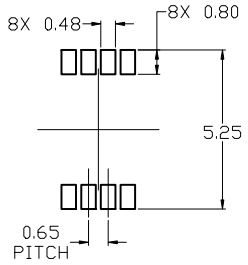
DATE 16 JUL 2020





NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

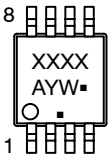


RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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