

NTD5802N, NVD5802N

MOSFET – Power, Single, N-Channel, DPAK 40 V, 101 A

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- MSL 1/260°C
- 100% Avalanche Tested
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Applications

- CPU Power Delivery
- DC-DC Converters
- Motor Driver

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit		
Drain-to-Source Voltage	V_{DS}	40	V		
Gate-to-Source Voltage	V_{GS}	± 20	V		
Continuous Drain Current ($R_{\theta JC}$) (Note 1)	I_D	$T_C = 25^\circ\text{C}$	101	A	
		$T_C = 85^\circ\text{C}$	78		
Power Dissipation ($R_{\theta JC}$) (Note 1)	P_D	$T_C = 25^\circ\text{C}$	93.75	W	
		$T_A = 25^\circ\text{C}$	16.4	A	
Continuous Drain Current ($R_{\theta JA}$) (Note 1)	I_D	$T_A = 25^\circ\text{C}$	16.4	A	
		$T_A = 85^\circ\text{C}$	12.7		
Power Dissipation ($R_{\theta JA}$) (Note 1)	P_D	$T_A = 25^\circ\text{C}$	2.5	W	
		$T_A = 25^\circ\text{C}$	2.5		
Pulsed Drain Current	$t_p = 10\mu\text{s}$	$T_A = 25^\circ\text{C}$	I_{DM}	300	A
Current Limited by Package	$T_A = 25^\circ\text{C}$	$I_{DmaxPkg}$	45	A	
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to 175		$^\circ\text{C}$	
Source Current (Body Diode)	I_S	50		A	
Drain to Source dV/dt	dV/dt	6.0		V/ns	
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 32\text{ V}$, $V_{GS} = 10\text{ V}$, $L = 0.3\text{ mH}$, $I_{L(pk)} = 40\text{ A}$, $R_G = 25\ \Omega$)	E_{AS}	240		mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260		$^\circ\text{C}$	

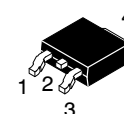
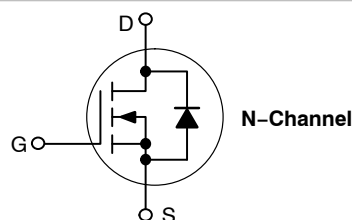
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



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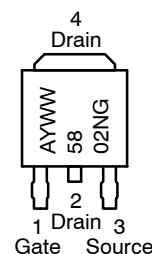
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
40 V	4.4 m Ω @ 10 V	101 A
	7.8 m Ω @ 5.0 V	50 A



CASE 369C
DPAK
(Bent Lead)
STYLE 2

MARKING DIAGRAMS & PIN ASSIGNMENT



A = Assembly Location*
Y = Year
WW = Work Week
5802N = Device Code
G = Pb-Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	1.6	°C/W
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	60	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	105	

- Surface-mounted on FR4 board using 1 in sq pad size, 1 oz Cu.
- Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 10\ \mu\text{A}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			40		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 150^\circ\text{C}$		50	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.5		3.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-7.4		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		3.6	4.4	m Ω
		$V_{GS} = 5.0\text{ V}, I_D = 50\text{ A}$		6.5	7.8	
Forward Transconductance	gFS	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		16.8		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 12\text{ V}$		5300		pF
Output Capacitance	C_{oss}			850		
Reverse Transfer Capacitance	C_{rss}			550		
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$		5025		pF
Output Capacitance	C_{oss}			580		
Reverse Transfer Capacitance	C_{rss}			400		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 50\text{ A}$		75	100	nC
Threshold Gate Charge	$Q_{G(TH)}$			6.0		
Gate-to-Source Charge	Q_{GS}			18		
Gate-to-Drain Charge	Q_{GD}			15		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V}, I_D = 50\text{ A}, R_G = 2.0\ \Omega$		14		ns
Rise Time	t_r			52		
Turn-Off Delay Time	$t_{d(off)}$			39		
Fall Time	t_f			8.5		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = 50\text{ A}$		0.9	1.2	V
		$V_{GS} = 0\text{ V},$ $I_S = 20\text{ A}$		0.8	1.0	
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V},$ $dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 50\text{ A}$		25		ns
Charge Time	t_a			15		
Discharge Time	t_b			10		
Reverse Recovery Charge	Q_{RR}			15		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CHARACTERISTICS

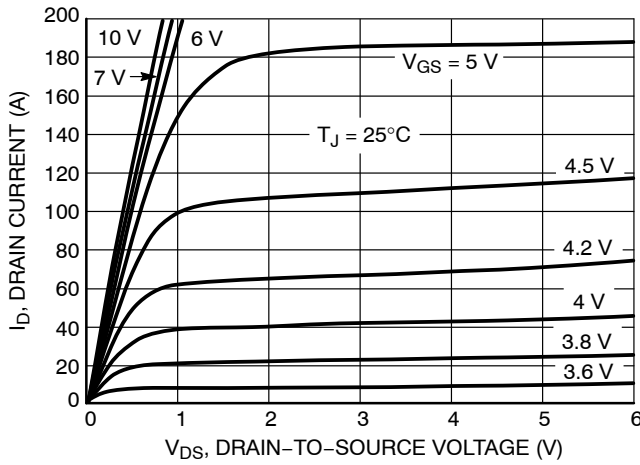


Figure 1. On-Region Characteristics

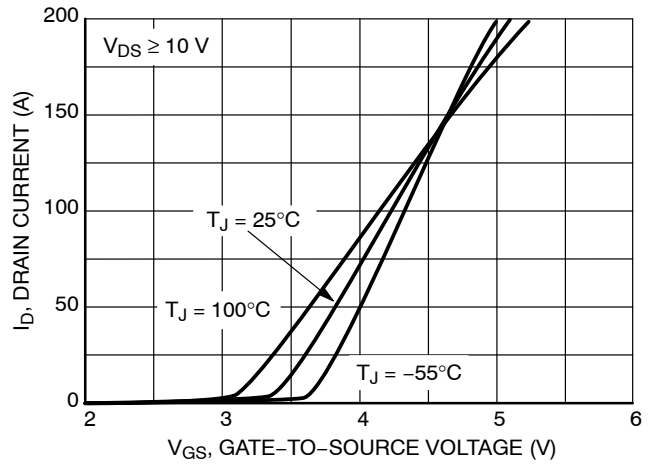


Figure 2. Transfer Characteristics

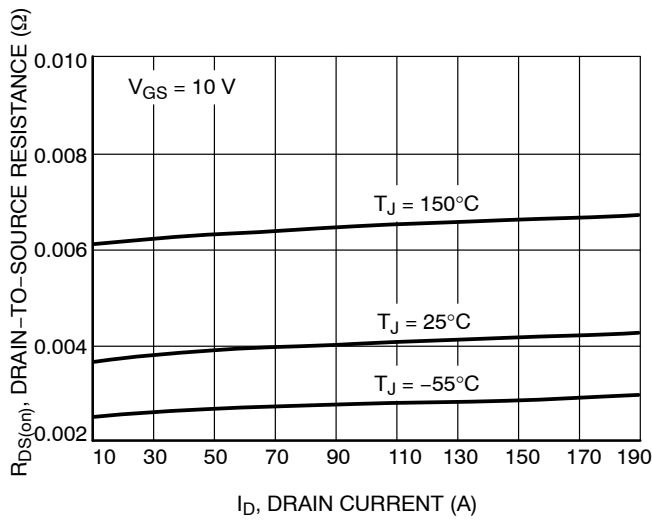


Figure 3. On-Resistance vs. Drain Current

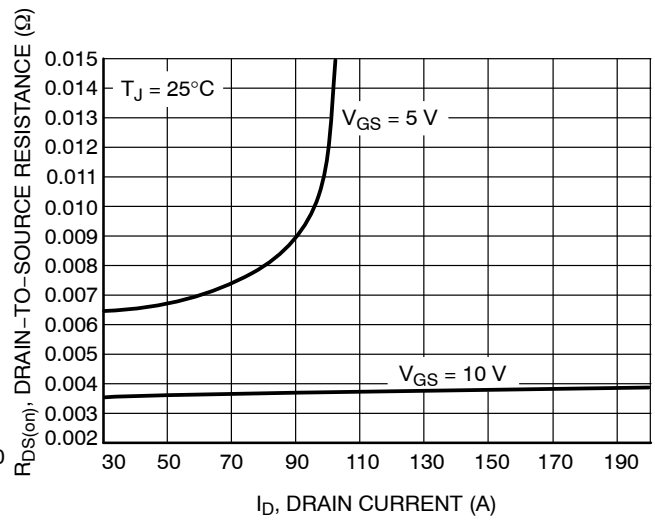


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

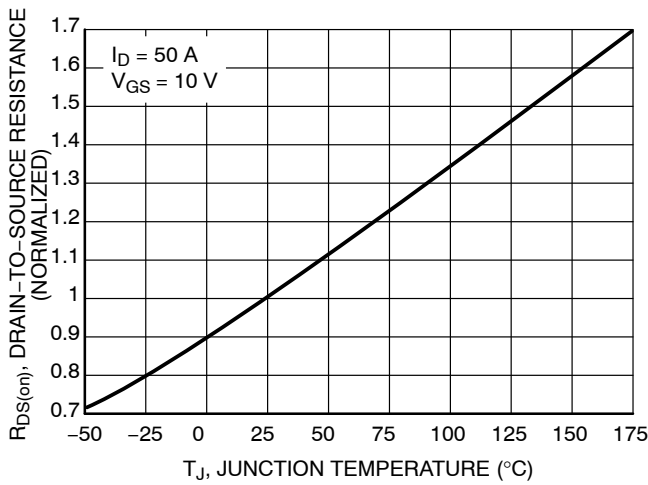


Figure 5. On-Resistance Variation with Temperature

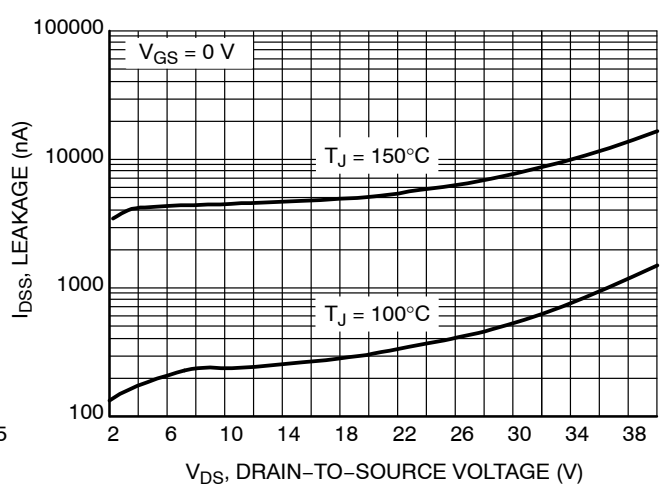


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

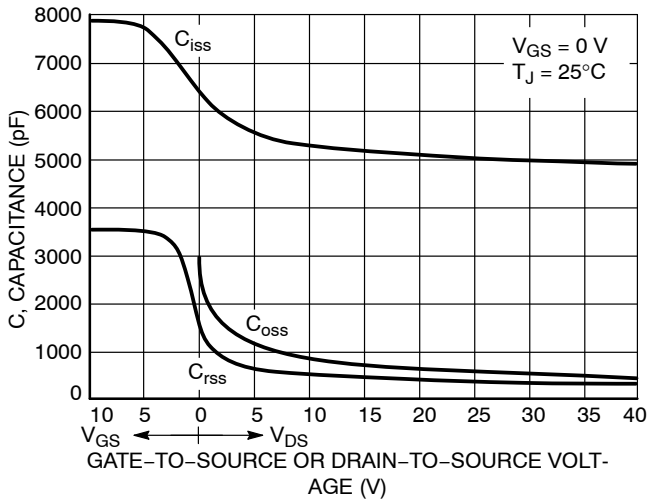


Figure 7. Capacitance Variation

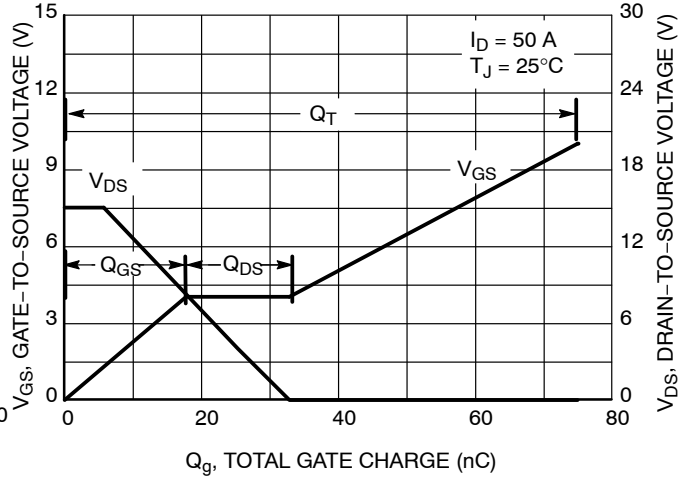


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

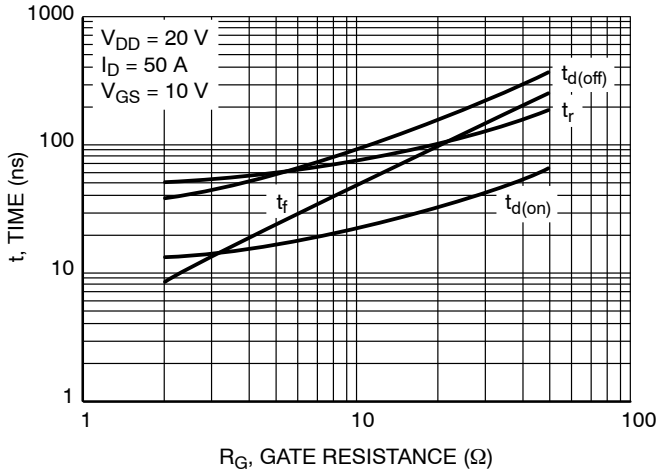


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

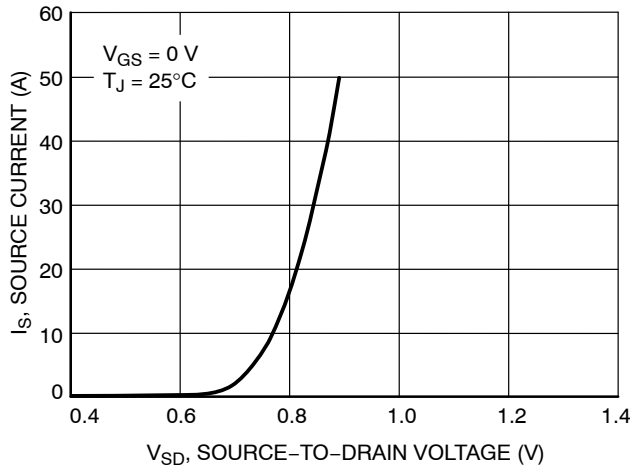


Figure 10. Diode Forward Voltage vs. Current

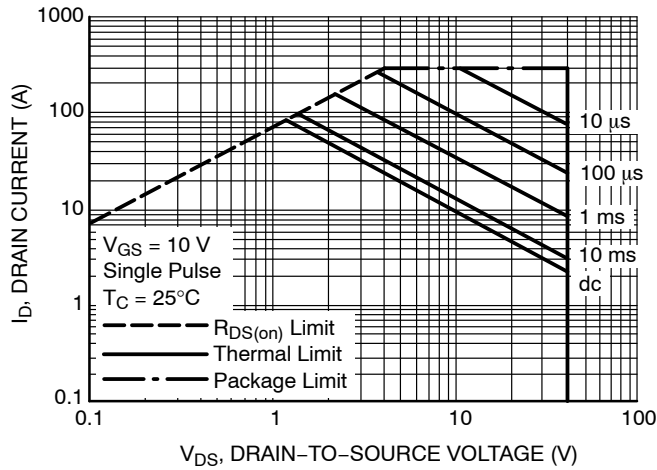


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL PERFORMANCE CHARACTERISTICS

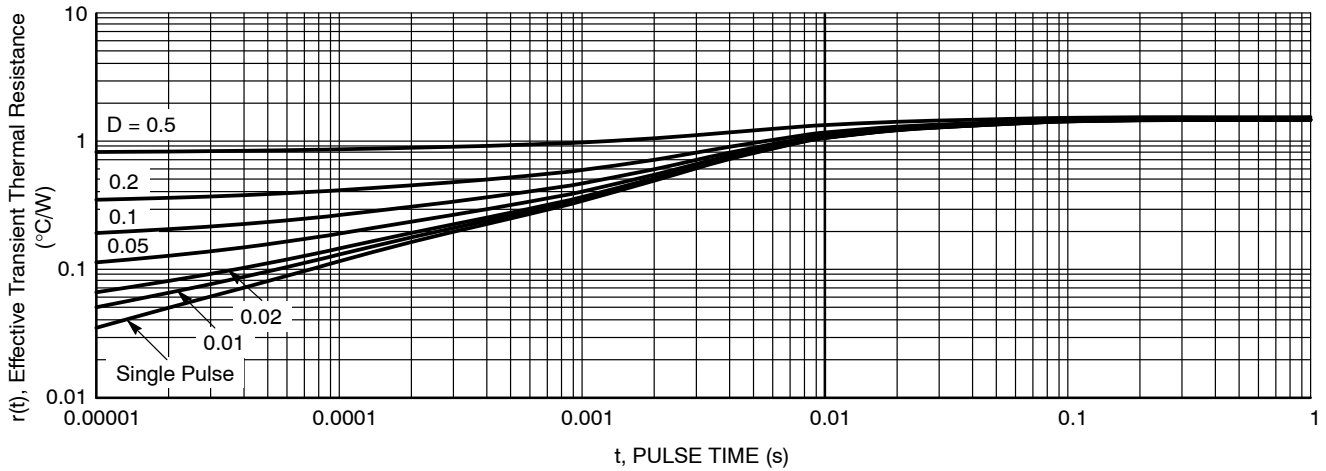


Figure 12. Thermal Response

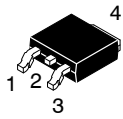
ORDERING INFORMATION

Order Number	Package	Shipping†
NTD5802NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NVD5802NT4G*	DPAK (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

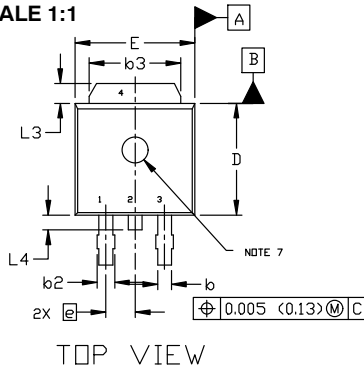
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



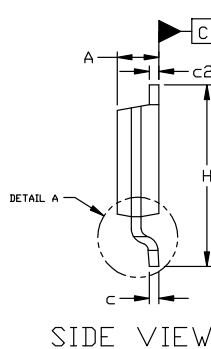
DPAK (SINGLE GAUGE) CASE 369C ISSUE G

DATE 31 MAY 2023

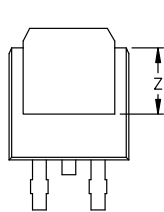
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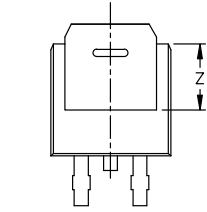
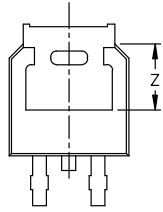
TOP VIEW



SIDE VIEW

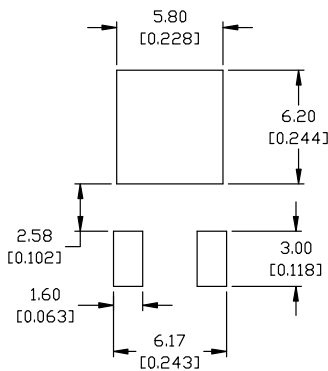


BOTTOM VIEW



BOTTOM VIEW

ALTERNATE CONSTRUCTIONS



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

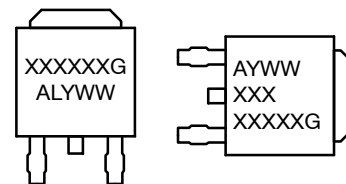
- | | | | | |
|--|--|---|---|--|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE | STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE | STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE |
| STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2 | STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE | STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE | STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE |

NOTES:

- DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
- OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---

GENERIC MARKING DIAGRAM*



- IC**
- XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

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