Evaluating the ADG1412L 1.5 Ω R_{ON}, Quad SPST Switch with 1.2 V and 1.8 V JEDEC Logic Compliance

FEATURES

- Single inline headers provide flexibility for the field programmable gate array or microcontroller 1.2 V or 1.8V logic-input signals
- Surface-mount device pin resistor or capacitor sockets available for the addition of passive components
- SMB connector sockets provide flexibility for the input and output signals

EVALUATION KIT CONTENTS

- EVAL-ADG1412LEBZ evaluation board

DOCUMENTS NEEDED

- ADG1412L data sheet
- EVAL-ADG1412LEBZ user guide

EQUIPMENT NEEDED

- DC voltage source (V_{DD}/V_{SS})
  - ±15 V for dual supply
- Optional digital logic supply (V_L)
  - 1.1 V to 1.3 V for 1.2 V logic
  - 1.65 V to 1.95 V for 1.8 V logic
- Analog signal source
- Method to measure voltage, such as a digital multimeter

GENERAL DESCRIPTION

The EVAL-ADG1412LEBZ is the evaluation board for the ADG1412L. The ADG1412L contains four independent SPST switches, and these switches are turned on with Logic 1. Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

An external V_L supply pin provides logic-control flexibility for lower logic controls. The ADG1412L is both 1.2 V and 1.8 V JEDEC standard compliant.

Figure 1 shows the EVAL-ADG1412LEBZ in a typical evaluation setup. The EVAL-ADG1412LEBZ is located in the center of the evaluation board. Four test points and Subminiature Version B (SMB) sockets are provided to connect to each of the source pins. Three screw terminals power the device. A 5-pin header is provided for the user-defined digital voltage, if required.

Full specifications on the ADG1412L are available in the ADG1412L data sheet available from Analog Devices, Inc., and must be consulted in conjunction with this user guide when using the EVAL-ADG1412LEBZ.

TABLE OF CONTENTS

REVISION HISTORY

8/2022—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH

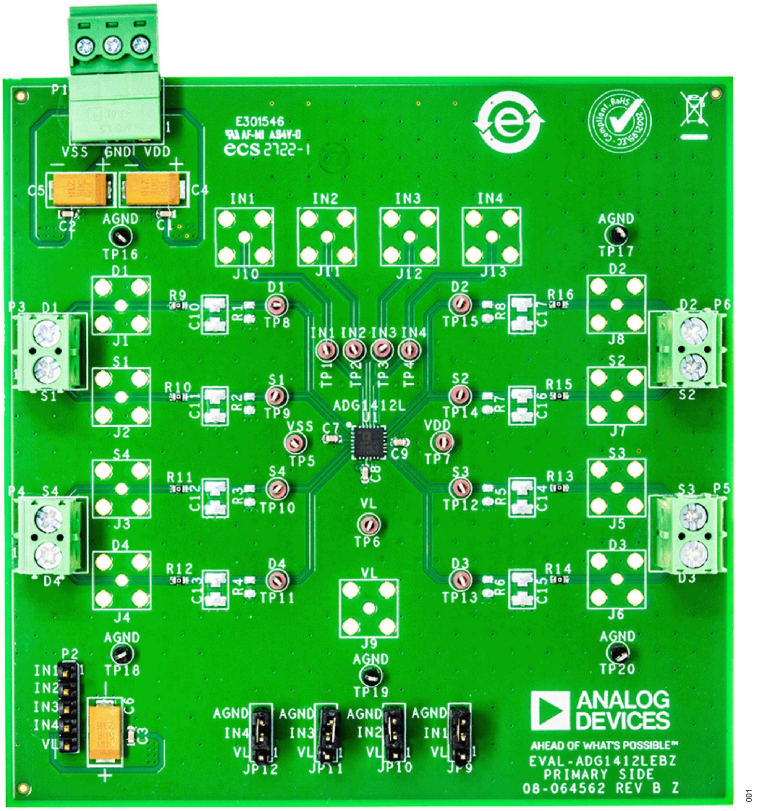

Figure 1. EVAL-ADG1412LEBZ Photograph

EVALUATION BOARD HARDWARE

POWER SUPPLY

Connector P1 provides access to the supply pins on the ADG1412L. V_{DD}, GND, and V_{SS} on P1 link to the appropriate pins on the ADG1412L. For dual-supply voltages, the EVAL-ADG1412LEBZ can be powered at ±15 V. For single-supply voltages, the GND and V_{SS} terminals must be connected and power by the EVAL-ADG1412LEBZ with 5 V or 12 V. Additionally, 1.1 V to 1.95 V is supplied to the V_L pin of the ADG1412L.

LINK HEADERS

A number of link options are provided on the EVAL-ADG1412LEBZ that must be set for the required operating conditions before using. Table 1 summarizes the link headers and how these headers are used on the EVAL-ADG1412LEBZ. The functions of these link options are described in detail in Table 2.

Table 1. Link Header Descriptions

Link	Position	Description
JP9 to JP12	A	VL
	B	AGND

Table 2. Link Header Functions

Link	Function
JP9 to JP12	This link selects the source of the INx voltage supplied to the ADG1412L. Position A selects VL from P2. Position B selects 0 V or AGND.

SMB CONNECTORS

The parallel interface of the ADG1412L is controlled manually using the link headers of JP9 to JP12, or it can be accessed using the SMB connectors, IN1 to IN4. To use the SMB connectors, remove the JP9 to JP12 link headers.

INPUT SIGNALS

The 2-pin terminal blocks, P3, P4, P5, and P6, are provided to connect to both the source and drain pins of the ADG1412L. Additional SMB connector pads are available if extra connections are required.

Each trace on the source and drain side includes two sets of 0603 pads, which can place a load on the signal path to ground. A 0 Ω resistor is placed in the signal path and can be replaced with a user-defined value. The resistor combined with the 0603 pads can create a simple RC filter.

EVALUATION BOARD SCHEMATIC AND ARTWORK

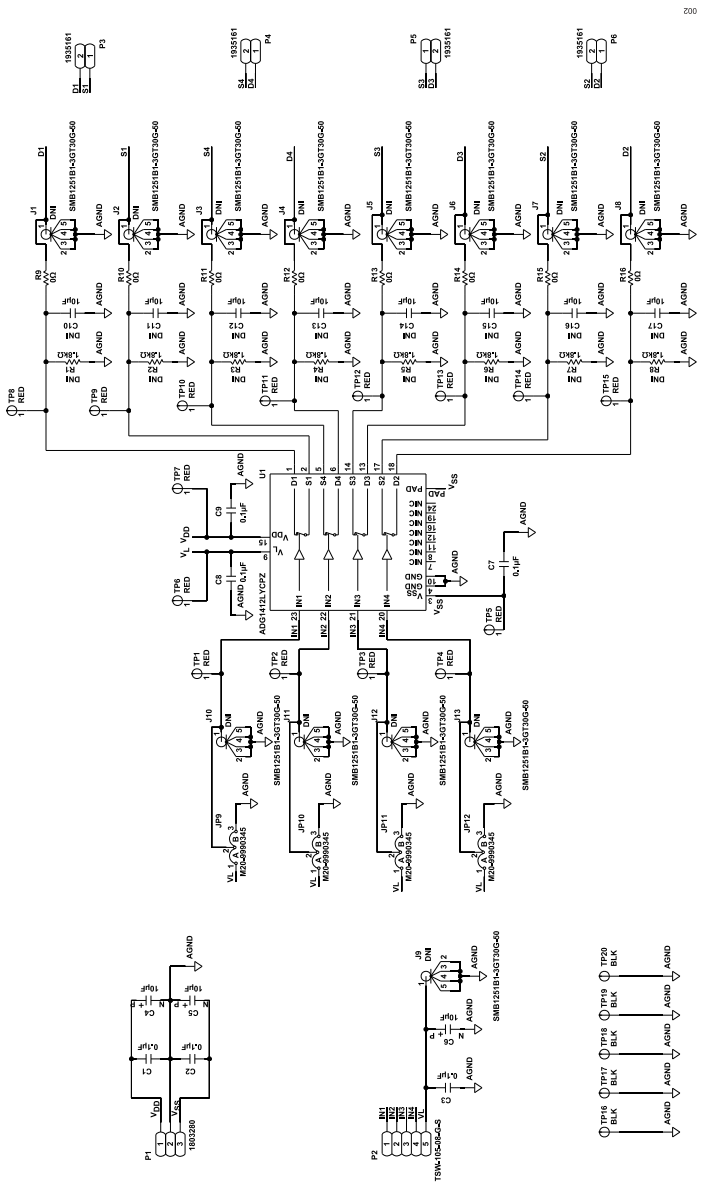

Figure 2. EVAL-ADG1412LEBZ Evaluation Board Schematic, Part 1

EVALUATION BOARD SCHEMATIC AND ARTWORK

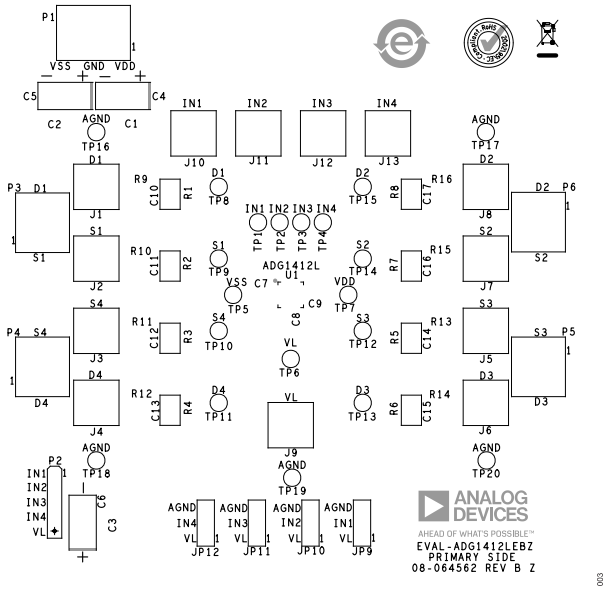

Figure 3. EVAL-ADG1412LEBZ Silkscreen

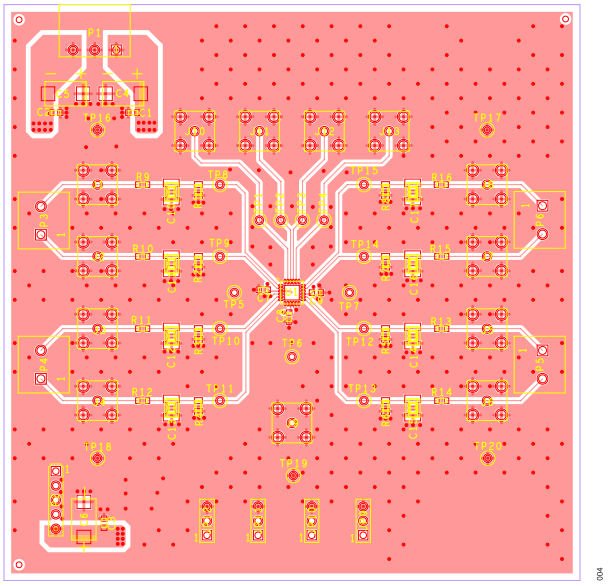

Figure 4. EVAL-ADG1412LEBZ Top Layer

EVALUATION BOARD SCHEMATIC AND ARTWORK

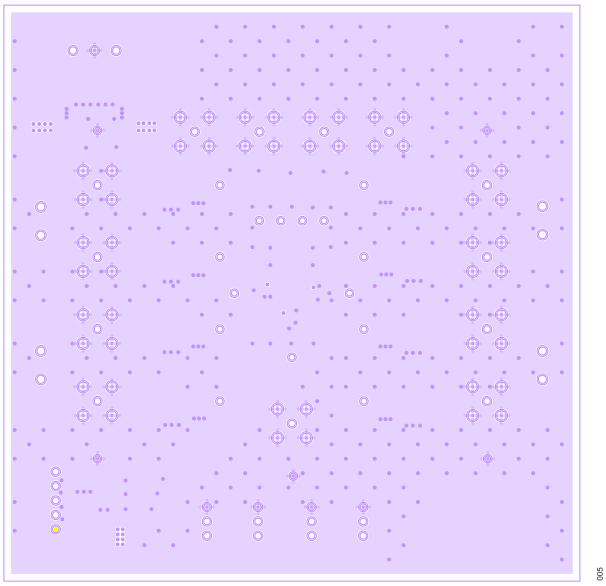

Figure 5. EVAL-ADG1412LEBZ Layer 2

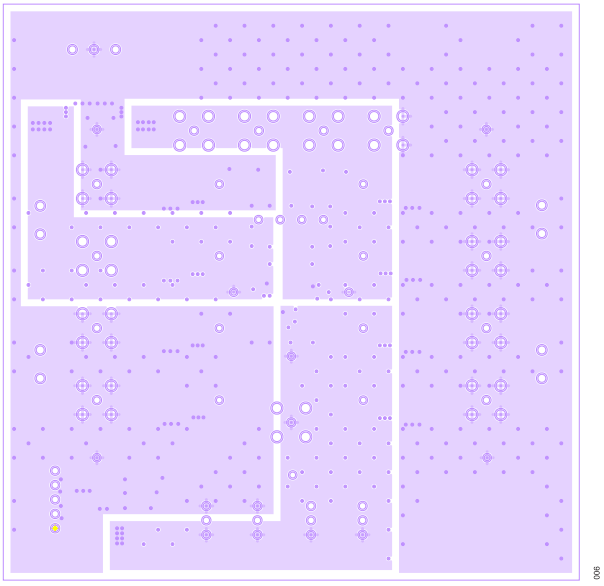

Figure 6. EVAL-ADG1412LEBZ Layer 3

EVALUATION BOARD SCHEMATIC AND ARTWORK

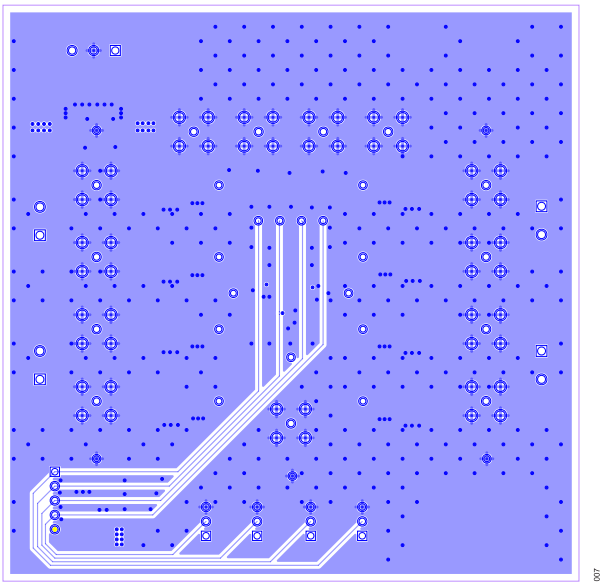

Figure 7. EVAL-ADG1412LEBZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 3. Bill of Materials

Reference Designator	Description	Manufacturer	Part Number
C4 to C6	50 V tantalum capacitors, 10 µF, Size D	Kemet	T491D106K050AT
C1 to C3, C7 to C9	50 V, X7R multilayer ceramic capacitors, 0.1 µF, 0603	TDK	CGA3E2X7R1H104K080AA
C10 to C17	Do not insert (DNI)	Not applicable	Not applicable
R1 to R8	DNI	Not applicable	Not applicable
R9 to R16	Resistors, 0 Ω, 0603, 1%	Yageo	RC0603JR-070RL
J1 to J13	50 Ω, SMB sockets, DNI	Amphenol	SMB1251B1-3GT30G-50
T1 to T15	Red test points	Keystone Electronics	5000
TP16 to TP20	Black test points	Keystone Electronics	5001
P1	Header, right angle, 3.81 mm with plug	Phoenix Contact	1803280
P2	Through-hole header, 5-position	Samtec	TSW-106-08-G-S
P3 to P6	2-pin terminal blocks, 5 mm	Phoenix Contact	1935161
JP9 to JP12	3-pin single inline headers and shorting links	Harwin	M20-9990345
U1	ADG1412L, 1.5 Ω R_{ON}, quad SPST switch with 1.2 V and 1.8 V JEDEC logic compliance	Analog Devices Inc.	ADG1412L

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.