

LUCID SDR

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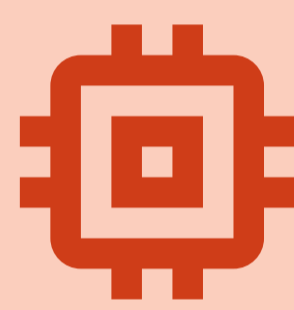
Lucid SDR is a real-time processing engine for RF signals in frequency ranges between **75 MHz to 6 GHz** with **168 MHz** bandwidth. **Lucid SDR** is equipped with an **efficiently integrated FPGA** based on a **Zynq family chip**. Our SDR is integrated with **three ultra-fast RF transceivers**. **B4 Limits** full product range consists of stable **multiphase power supply**, multiple **communication interfaces**, **fast RAM**, **flash memory** and **full duplex RF input and output paths**.



75(RX)-6000 MHz
47(TX)-6000 MHz



3x RX RF inputs
3x TX RF outputs
in the range up to 6 GHz each



Dual ARM Cortex-A9
@800MHz Zynq-7030 FPGA SoC
with 125 K logic cells

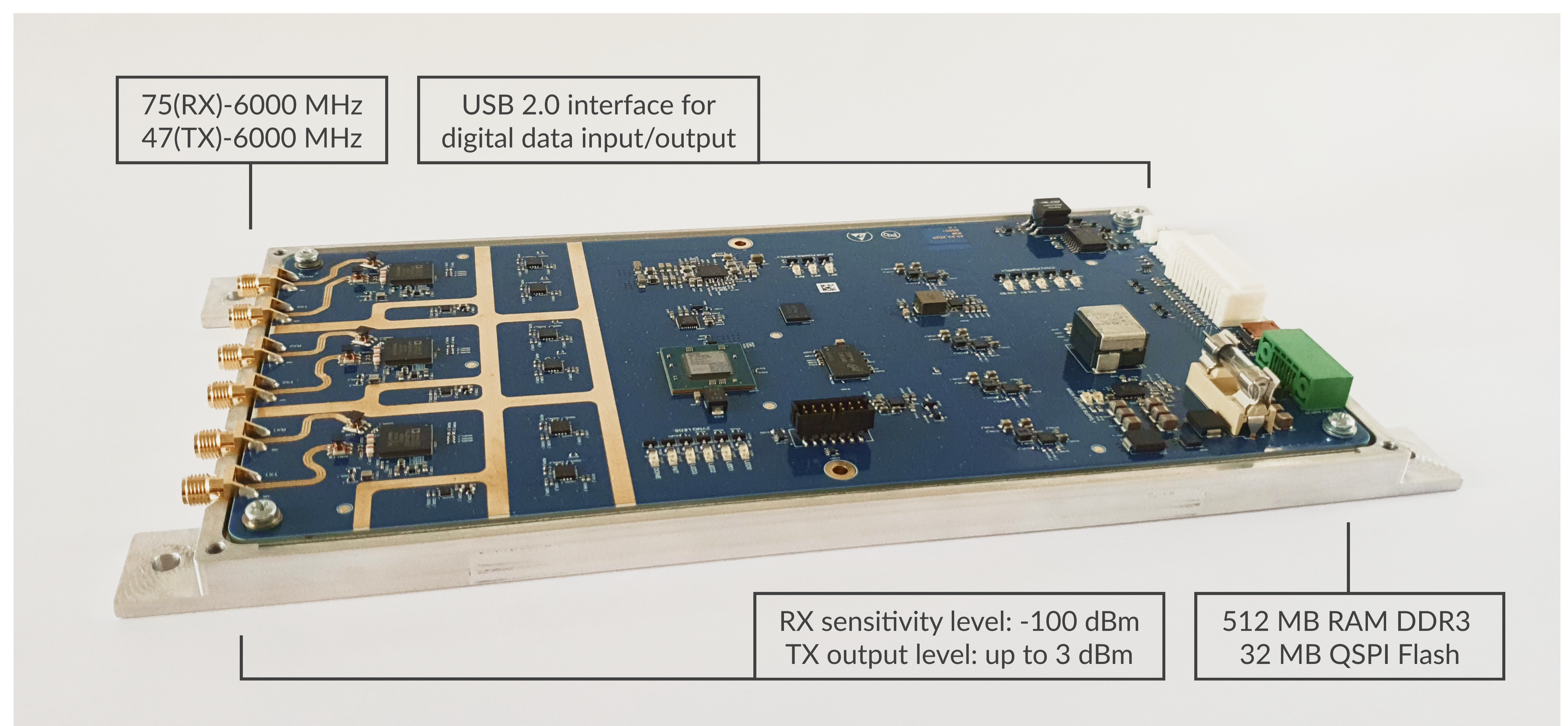


Bandwidth: 168 MHz
(3x56 MHz)

ABOUT B4 LIMITS

B4 Limits highly qualified and experienced PhD level team created our **signal processing SDR platform** offering **full flexibility** of use. Our platform can be applied for solutions ranging from **vector signal generator**, **BTS**, **spectrum analyzer**, **jamming** and **repeater applications** to **uplink activity detection/decoding**.

B4 Limits team also developed **state of the art solutions** around our base product: **Software Defined Radio Platform**. The entire range of products consists of mainly support devices: **power amplifier controller**, **smart system controller** and the heart of the system **B4 Limits produced SDR**.





SHORT SPECIFICATION

POWER	FEATURES
Supply voltage: 12 V	GNU Radio sink and source blocks
Maximum current consumption: 4 A	Libiio, a C, C++, C#, and Python API
Digital signals of voltage levels 1.8 V	
PHYSICAL	APPLICATIONS
Operating temperature: -30 to 85 °C	Vector signal generator
PCB dimensions (L x W): 235 x 120 mm	Spectrum analyzer
Housing dimensions (L x W x H): 245 x 130 x 40 mm	Uplink activity detection/decoding (2G/3G/4G/5G, UHF/VHF, WiFi 2.4/5.0)
PCB weight: 0.5 kg	Jamming and repeater applications
Optional aluminium housing weight: 1.0 kg	BTS
RF PERFORMANCE	DIGITAL SPECIFICATION
RX/TX isolation level: 50 dBm	Dual ARM Cortex-A9 @800 MHz
RX sensitivity level: - 100 dBm	Zynq-7030 FPGA SoC with 125 K logic cells
RX to TX response time: 36 µs	3 communication interfaces: CAN, USB, UART
TX output level up to 3 dBm	RAM: 512 MB
CONVERSION PERFORMANCE	CUSTOMISATION
Processing speed: 6 Gb/s	Customised projects upon request
Sampling speed: 61.22 MS/s	On your own via GNU platform
18 configurable digital IOs (4 PS, 14 PL)	With B4 Limits

LUCID SDR VERSIONS

V1 – equipped with 1 transceiver

V2 – equipped with 2 transceivers

V3 – equipped with 3 transceivers

LUCID SDR

