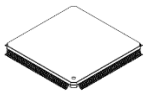
CMOS Digital Integrated Circuit Silicon Monolithic

TXZ+ Family TMPM4G Group(1)



LQFP176(20x20mm, 0.4mm pitch)
LQFP144(20x20mm, 0.5mm pitch)
LQFP100(14x14mm, 0.5mm pitch)

VFBGA177(13x13mm, 0.8mm pitch)
VFBGA145(12x12mm, 0.8mm pitch)

General Description

- Arm® Cortex®-M4 (with FPU)
- Operating frequency: 1 to 200 MHz, Operating voltage: 2.7 to 3.6 V
- Code Flash: 512 KB to 2048 KB, Data Flash: 32KB
- Built-in high speed 12-bit AD converter and plenty of timers/serial channels

Applications

TXZ+ family TMPM4G group(1) integrates widely used for the equipment in which high speed data procedure is required, such as OA/digital products, industrial equipment, and others.

Features

- Arm Cortex-M4(with FPU)
  - Operating frequency: 1 to 200 MHz
  - Memory Protection Unit (MPU)
- Supply voltage and power consumption
  - Operating voltage: 2.7 to 3.6 V
  - Low-power consumption operation: IDLE, STOP1, and STOP2
- Operating temperature:

  - 40 to +85°C @ operating frequency 1 to 200 MHz
- Internal memory
  - Code Flash: 512 KB to 2048 KB, rewritable up to 100,000 times
  - Data Flash: 32 KB, rewritable up to 100,000 times
  - Data Flash is rewritable during instruction execution
  - RAM: 192 KB to 256 KB and Backup RAM: 2 KB (all products)
- Clock
  - External high speed oscillator: 8 MHz to 20 MHz (Ceramic and Crystal)
  - External high speed clock input: 8 to 24 MHz
  - Internal high speed oscillator1 (IHOSC1):10 MHz, user trimming function
  - Internal high speed oscillator2 (IHOSC2):10 MHz
  - PLL: 200 MHz output
  - External low speed oscillator: 32.768 kHz
- Oscillation frequency detector (OFD): Abnormal system clock detection
- Voltage detection (LVD): 7 levels. selection between interrupts and reset outputs
- Interrupt
  - External factors: 12 to 16

    (External pins: 17 to 32 pins , with DNF)
  - Internal factors: 109 to 145
- I/O ports: 91 to 155 (Input: 4, Output: 1)
  - Enable to select Pull-up/Pull-down resistor, Open-drain
  - 5V tolerant, 3V tolerant
- On-chip debug (JTAG/SW) and NBDIF (RAM monitor)
- Trigger selector (TRGSEL)
  - Expand trigger requests for DMA Controller, Timer counter, and others.
- DMA controller: 3 units
  - MDMAC: 1 unit, DMA requests: 30 to 32 factors, internal/external triggers
  - HDMAC: 2 units, DMA requests: 13 to 15 factors, internal/external triggers
- External bus interface (EBIF)
  - Expandable to 64MB (Program/data)
  - External data bus (separate bus/multiplexed bus): 8/16 bit width
  - Chip select controller: 4 channels
- Asynchronous serial communication
  - UART: 3 to 6 channels, up tp 5.0 Mbps, FIFO (Transmission 8 stages and Reception 8 stages)
  - FUART: 1 or 2 channels, up to 2.5 Mbps. FIFO (Transmission 32 stages and Reception 32 stages) and IrDA up to 115.2Kbps.
- Serial peripheral interface (TSPI): 5 to 9 channels
  - SIO/SPI mode, up to 25 MHz
  - FIFO (Transmission 16bit x 8 stages and Reception 16bit x 8 stages)
  - Frame mode/Sector mode

Start of commercial production
2021-07

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- Synchronous serial interface (TSSI): 2 channels
  - Transmitter/reciever can communicate independently. Full-duplex communication is possible by cooperative operation.
  - FIFO (Transmission 32bit x 4 stages and Reception 32bit x 4 stages)
- I^2C interface
  - I^2C Interface (I2C): 3 to 5 channels
    Multi master, Standard mode/Fast mode available
    7-bit addressing format available
  - I^2C Interface version A(EI2C): 3 to 5 channels
    Multi master, Standard mode/Fast mode/Fast mode Plus available
    7/10-bit addressing format available

  Note: I2C and EI2C can be used exclusively.
- Serial memory interface (SMIF): 1 channel
  - Up to two serial memories can be connected
  - Memory capacity 64 KB to 128 MB
  - SPI, Quad, QPI, Octal, OPI
- Consumer electronics control Circuit (CEC): 1 channel
- 8-bit DA converter (DAC): 2 channels
- 12-bit AD converter (ADC): 16 to 24 channel inputs
  - Sample and hold circuit
  - Conversion time: 1.0 μs @f_{ADCLK} = 60 MHz
- Advanced programmable motor control circuit (A-PMD): 1 channel
  - 3 phase PWM output, Synchronized with 12-bit ADC
  - Emergency stop function by external inputs (EMG0 pin and OVV0 pin)
- 32-bit timer event counter (T32A)
  - 32 channels as 16-bit timer, 16 channels as 32-bit timer
  - Interval timer, event counter, input capture, phase difference input, PPG output, Sync Start, Trigger start
- Interval sensor detection circuit (ISD): 3 units
  - 4 inputs per unit
  - Sampling up to 12 inputs simultaneously in unit synchronous mode
  - Low speed oscillator (32.768 kHz) and 32-bit timer output can be used as sampling clock
- I^2S Interface (I2S): 2 channels
  - Audio data format: I^2S stereo,/LR stereo/ PCM monaural
  - Sampling frequency: Stereo up to 192 kHz, monaural up to 384 kHz
- FIR calculation circuit (FIR): 1 channel
  - Dedicated function for I^2S Interface
  - Sum-of-products processing of audio data
- Long term timer (LTTMR): 1 channel
  - Interval time of 0.1 μs to 6553.5 μs can be set
- Real-time clock (RTC): 1 channel
- Clock selective watchdog timer (SIWDT): 1 channel
  - Clocks, not the system clock can be selected.
  - Clear window, interrupts and reset outputs
- Remote control signal preprocessor (RMC): 1 to 2channels
- Supports boundary scan (BSC)

Products Lists Categorized by Functions

The product under development is contained in this table.
For the newest status of each product, please contact your sales representative.

Table 1.1 TMPM4GR (1/2)

Built-in Functions		TMPM4GRF20FG	TMPM4GRF15FG	TMPM4GRF10FG	TMPM4GRFDFG
Memory	Code Flash (KB)	2048	1536	1024	512
	Data Flash (KB)	32	32	32	32
	RAM (KB)	256	256	256	192
	Backup RAM (KB)	2	2	2	2
I/O port	PORT (pin)	155	155	155	155
External interrupt	Factor	16	16	16	16
	Pin	32	32	32	32
External bus	EBIF	Separate bus /Multiplexed bus	Separate bus /Multiplexed bus	Separate bus /Multiplexed bus	Separate bus /Multiplexed bus
DMAC	MDMAC (ch)	32	32	32	32
	HDMAC (ch)	15	15	15	15
Timer function	T32A (ch)	16	16	16	16
	LTTMR (ch)	1	1	1	1
	RTC (ch)	1	1	1	1
Serial communication function	UART (ch)	6	6	6	6
	FUART (ch)	2	2	2	2
	I2C/EI2C (ch)	5/5	5/5	5/5	5/5
	TSPI (ch)	9	9	9	9
	TSSI (ch)	2	2	2	2
	SMIF (ch)	1	1	1	1
	CEC (ch)	1	1	1	1
Analog function	12-bit ADC (ch)	24	24	24	24
	8-bit DAC (ch)	2	2	2	2
Motor control function	A-PMD (ch)	1	1	1	1
Remote Control preprocessor	RMC (ch)	2	2	2	2
Interval Sensor Detection	ISD (unit)	3	3	3	3
Inter-IC Sound	I2S (ch)	2	2	2	2
Finite Impulse Response	FIR (ch)	1	1	1	1
System function	LVD (ch)	1	1	1	1
	SIWDT (ch)	1	1	1	1
	OFD (ch)	1	1	1	1
	POR	1	1	1	1
Debug interface	Debug	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF
Package	Package type	LQFP176 (20 mm x 20 mm, 0.4 mm pitch)			

Table 1.2 TMPM4GR (2/2)

Built-in Functions		TMPM4GRF20XBG	TMPM4GRF15XBG	TMPM4GRF10XBG	TMPM4GRFDXBG
Memory	Code Flash (KB)	2048	1536	1024	512
	Data Flash (KB)	32	32	32	32
	RAM (KB)	256	256	256	192
	Backup RAM (KB)	2	2	2	2
I/O port	PORT (pin)	155	155	155	155
External interrupt	Factor	16	16	16	16
	Pin	32	32	32	32
External bus	EBIF	Separate bus /Multiplexed bus	Separate bus /Multiplexed bus	Separate bus /Multiplexed bus	Separate bus /Multiplexed bus
DMAC	MDMAC (ch)	32	32	32	32
	HDMAC (ch)	15	15	15	15
Timer function	T32A (ch)	16	16	16	16
	LTTMR (ch)	1	1	1	1
	RTC (ch)	1	1	1	1
Serial communication function	UART (ch)	6	6	6	6
	FUART (ch)	2	2	2	2
	I2C/EI2C (ch)	5/5	5/5	5/5	5/5
	TSPI (ch)	9	9	9	9
	TSSI (ch)	2	2	2	2
	SMIF (ch)	1	1	1	1
	CEC (ch)	1	1	1	1
Analog function	12-bit ADC (ch)	24	24	24	24
	8-bit DAC (ch)	2	2	2	2
Motor control function	A-PMD (ch)	1	1	1	1
Remote Control preprocessor	RMC (ch)	2	2	2	2
Interval Sensor Detection	ISD (unit)	3	3	3	3
Inter-IC Sound	I2S (ch)	2	2	2	2
Finite Impulse Response	FIR (ch)	1	1	1	1
System function	LVD (ch)	1	1	1	1
	SIWDT (ch)	1	1	1	1
	OFD (ch)	1	1	1	1
	POR	1	1	1	1
Debug interface	Debug	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF
Package	Package type	VFBGA177 (13 mm x 13 mm, 0.8 mm pitch)			

Table 1.3 TMPM4GQ (1/2)

Built-in Functions		TMPM4GQF20FG	TMPM4GQF15FG	TMPM4GQF10FG	TMPM4GQFDFG
Memory	Code Flash (KB)	2048	1536	1024	512
	Data Flash (KB)	32	32	32	32
	RAM (KB)	256	256	256	192
	Backup RAM (KB)	2	2	2	2
I/O port	PORT (pin)	127	127	127	127
External interrupt	Factor	16	16	16	16
	Pin	25	25	25	25
External bus	EBIF	Separate bus /Multiplexed bus	Separate bus /Multiplexed bus	Separate bus /Multiplexed bus	Separate bus /Multiplexed bus
DMAC	MDMAC (ch)	32	32	32	32
	HDMAC (ch)	15	15	15	15
Timer function	T32A (ch)	16	16	16	16
	LTTMR (ch)	1	1	1	1
	RTC (ch)	1	1	1	1
Serial communication function	UART (ch)	5	5	5	5
	FUART (ch)	2	2	2	2
	I2C/EI2C (ch)	5/5	5/5	5/5	5/5
	TSPI (ch)	8	8	8	8
	TSSI (ch)	1	1	1	1
	SMIF (ch)	1	1	1	1
	CEC (ch)	1	1	1	1
Analog function	12-bit ADC (ch)	24	24	24	24
	8-bit DAC (ch)	2	2	2	2
Motor control function	A-PMD (ch)	1	1	1	1
Remote Control preprocessor	RMC (ch)	2	2	2	2
Interval Sensor Detection	ISD (unit)	2	2	2	2
Inter-IC Sound	I2S (ch)	2	2	2	2
Finite Impulse Response	FIR (ch)	1	1	1	1
System function	LVD (ch)	1	1	1	1
	SIWDT (ch)	1	1	1	1
	OFD (ch)	1	1	1	1
	POR	1	1	1	1
Debug interface	Debug	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF
Package	Package type	LQFP144 (20 mm x 20 mm, 0.5 mm pitch)			

Table 1.4 TMPM4GQ (2/2)

Built-in Functions		TMPM4GQF20XBG	TMPM4GQF15XBG	TMPM4GQF10XBG	TMPM4GQFDXBG
Memory	Code Flash (KB)	2048	1536	1024	512
	Data Flash (KB)	32	32	32	32
	RAM (KB)	256	256	256	192
	Backup RAM (KB)	2	2	2	2
I/O port	PORT (pin)	127	127	127	127
External interrupt	Factor	16	16	16	16
	Pin	25	25	25	25
External bus	EBIF	Separate bus / Multiplexed bus	Separate bus / Multiplexed bus	Separate bus / Multiplexed bus	Separate bus / Multiplexed bus
DMAC	MDMAC (ch)	32	32	32	32
	HDMAC (ch)	15	15	15	15
Timer function	T32A (ch)	16	16	16	16
	LTTMR (ch)	1	1	1	1
	RTC (ch)	1	1	1	1
Serial communication function	UART (ch)	5	5	5	5
	FUART (ch)	2	2	2	2
	I2C / EI2C (ch)	5 / 5	5 / 5	5 / 5	5 / 5
	TSPI (ch)	8	8	8	8
	TSSI (ch)	1	1	1	1
	SMIF (ch)	1	1	1	1
	CEC (ch)	1	1	1	1
Analog function	12-bit ADC (ch)	24	24	24	24
	8-bit DAC (ch)	2	2	2	2
Motor control function	A-PMD (ch)	1	1	1	1
Remote Control preprocessor	RMC (ch)	2	2	2	2
Interval Sensor Detection	ISD (unit)	2	2	2	2
Inter-IC Sound	I2S (ch)	2	2	2	2
Finite Impulse Response	FIR (ch)	1	1	1	1
System function	LVD (ch)	1	1	1	1
	SIWDT (ch)	1	1	1	1
	OFD (ch)	1	1	1	1
	POR	1	1	1	1
Debug interface	Debug	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF
Package	Package type	VFBGA145 (12 mm x 12 mm, 0.8 mm pitch)			

Table 1.5 TMPM4GN (1/1)

Built-in Functions		TMPM4GNF20FG	TMPM4GNF15FG	TMPM4GNF10FG	TMPM4GNFDFG
Memory	Code Flash (KB)	2048	1536	1024	512
	Data Flash (KB)	32	32	32	32
	RAM (KB)	256	256	256	192
	Backup RAM (KB)	2	2	2	2
I/O port	PORT (pin)	91	91	91	91
External interrupt	Factor	12	12	12	12
	Pin	17	17	17	17
External bus	EBIF	Separate bus /Multiplexed bus	Separate bus /Multiplexed bus	Separate bus /Multiplexed bus	Separate bus /Multiplexed bus
DMAC	MDMAC (ch)	30	30	30	30
	HDMAC (ch)	13	13	13	13
Timer function	T32A (ch)	16	16	16	16
	LTTMR (ch)	1	1	1	1
	RTC (ch)	1	1	1	1
Serial communication function	UART (ch)	3	3	3	3
	FUART (ch)	1	1	1	1
	I2C/EI2C (ch)	3/3	3/3	3/3	3/3
	TSPI (ch)	5	5	5	5
	TSSI (ch)	1	1	1	1
	SMIF (ch)	1	1	1	1
	CEC (ch)	1	1	1	1
Analog function	12-bit ADC (ch)	16	16	16	16
	8-bit DAC (ch)	2	2	2	2
Motor control function	A-PMD (ch)	1	1	1	1
Remote Control preprocessor	RMC (ch)	1	1	1	1
Interval Sensor Detection	ISD (unit)	1	1	1	1
Inter-IC Sound	I2S (ch)	2	2	2	2
Finite Impulse Response	FIR (ch)	1	1	1	1
System function	LVD (ch)	1	1	1	1
	SIWDT (ch)	1	1	1	1
	OFD (ch)	1	1	1	1
	POR	1	1	1	1
Debug interface	Debug	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF
Package	Package type	LQFP100 (14 mm x 14 mm, 0.5 mm pitch)			

Contents

List of Figures

List of Tables

Preface

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C . . .
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] →[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 . . .
  Example: [***T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

The following words are terms or abbreviations mainly used in this datasheet.

ADC	Analog to Digital Converter
A-PMD	Advanced Programmable Motor Control Circuit
BSC	Boundary Scan
CEC	Consumer Electronics Control
DAC	Digital to Analog Converter
DNF	Digital Noise Filter
EBIF	External Bus Interface
EHOSC	External High Speed Oscillator
EI2C	I^2C Interface Version A
ELOSC	External Low Speed Oscillator
FIR	Finite Impulse Response
FUART	Full Universal Asynchronous Receiver Transmitter
HDMAC	High Speed DMAC
IHOSC	Internal High Speed Oscillator
INT	Interrupt
I2C	Inter-Integrated Circuit
EI2C	I^2C interface version A
I2S	Inter-IC Sound
ISD	Interval Sensor Detection Circuit
LTTMR	Long Term Timer
LVD	Voltage Detection Circuit
MDMAC	Multi-Function DMA Controller
NBDIF	Non Break Debug Interface
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
POR	Power On Reset Circuit
RMC	Remote Control Signal Preprocessor
RTC	Real Time Clock
SMIF	Serial Memory Interface
SIWDT	Clock Selective Watchdog Timer
TRGSEL	Trigger Selection circuit
TRM	Trimming Circuit
TSPI	Serial Peripheral Interface
TSSI	Synchronized Serial Interface
T32A	32-bit Timer Event Counter
UART	Universal Asynchronous Receiver Transmitter

1. Block Diagram

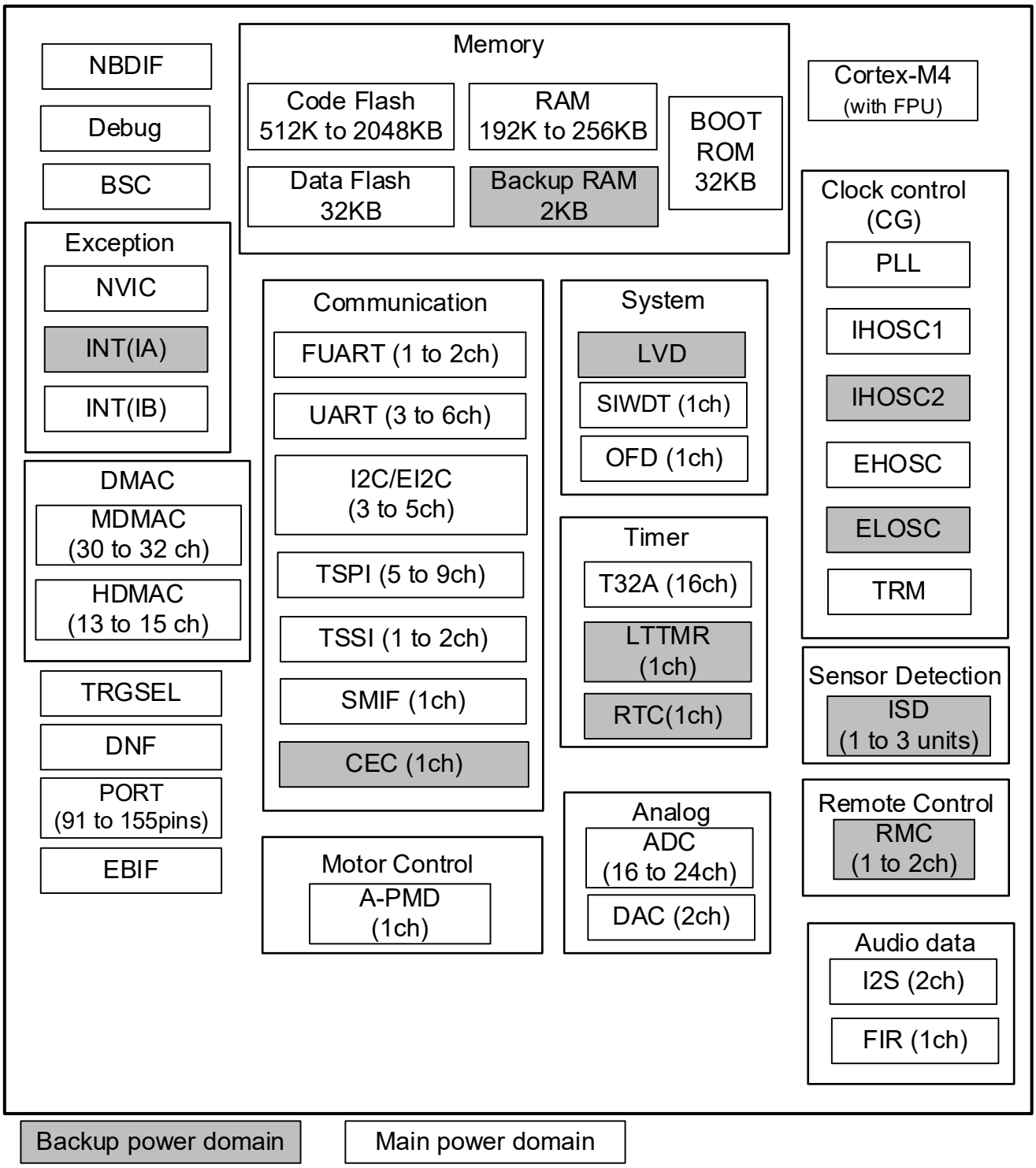
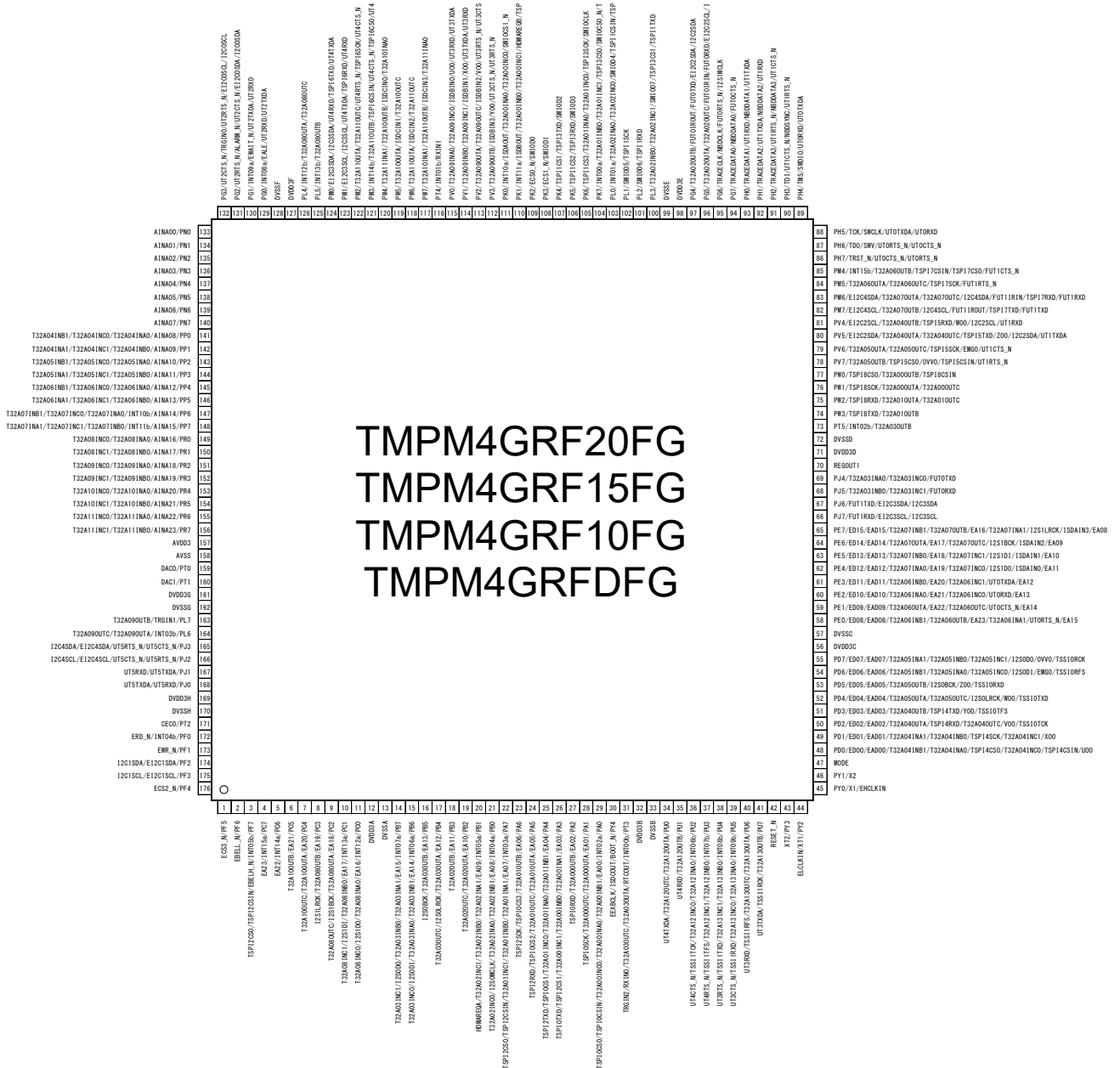


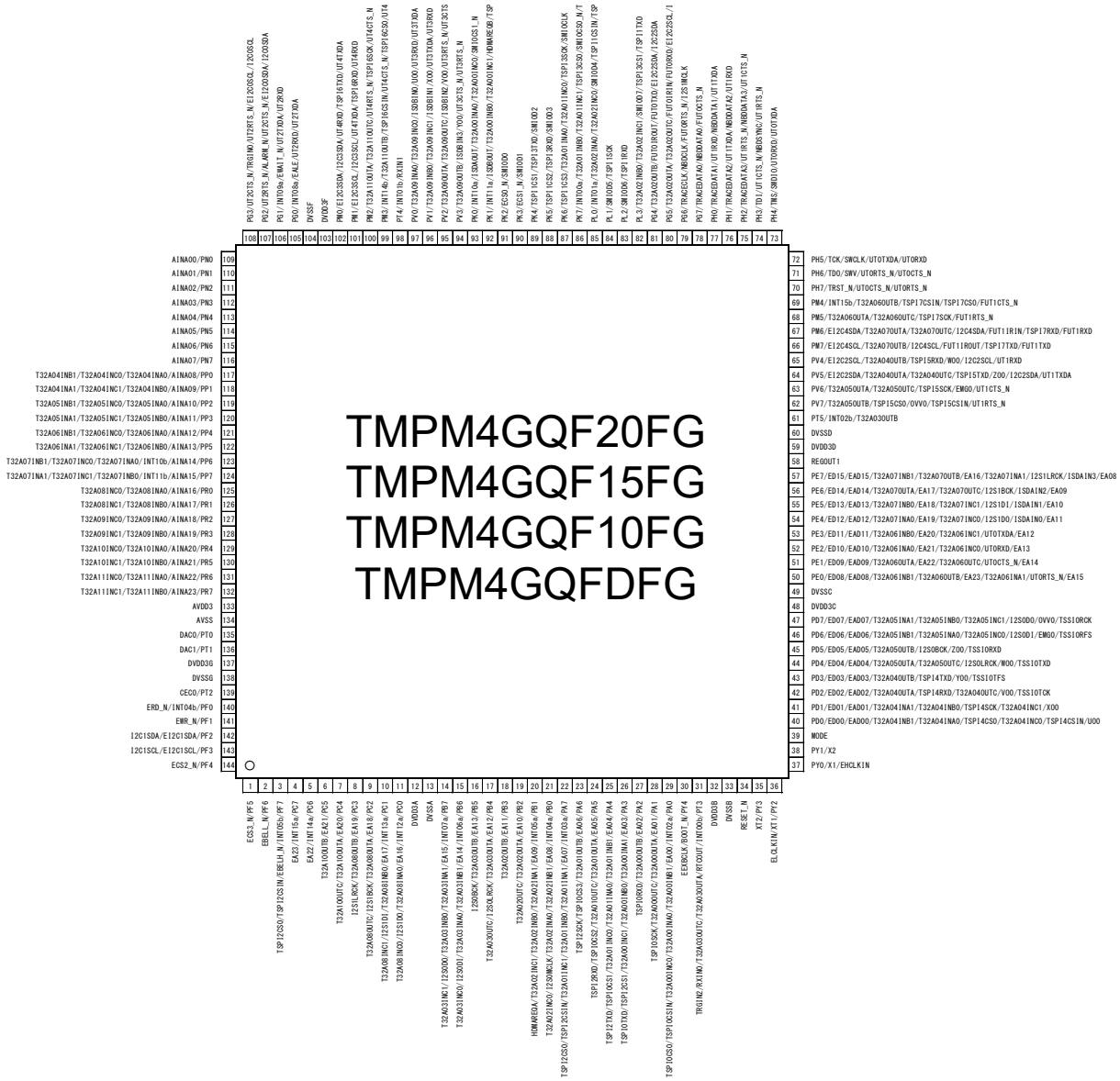
Figure 1.1 Block diagram of the TMPM4G Group (1)

2. Pin Assignment

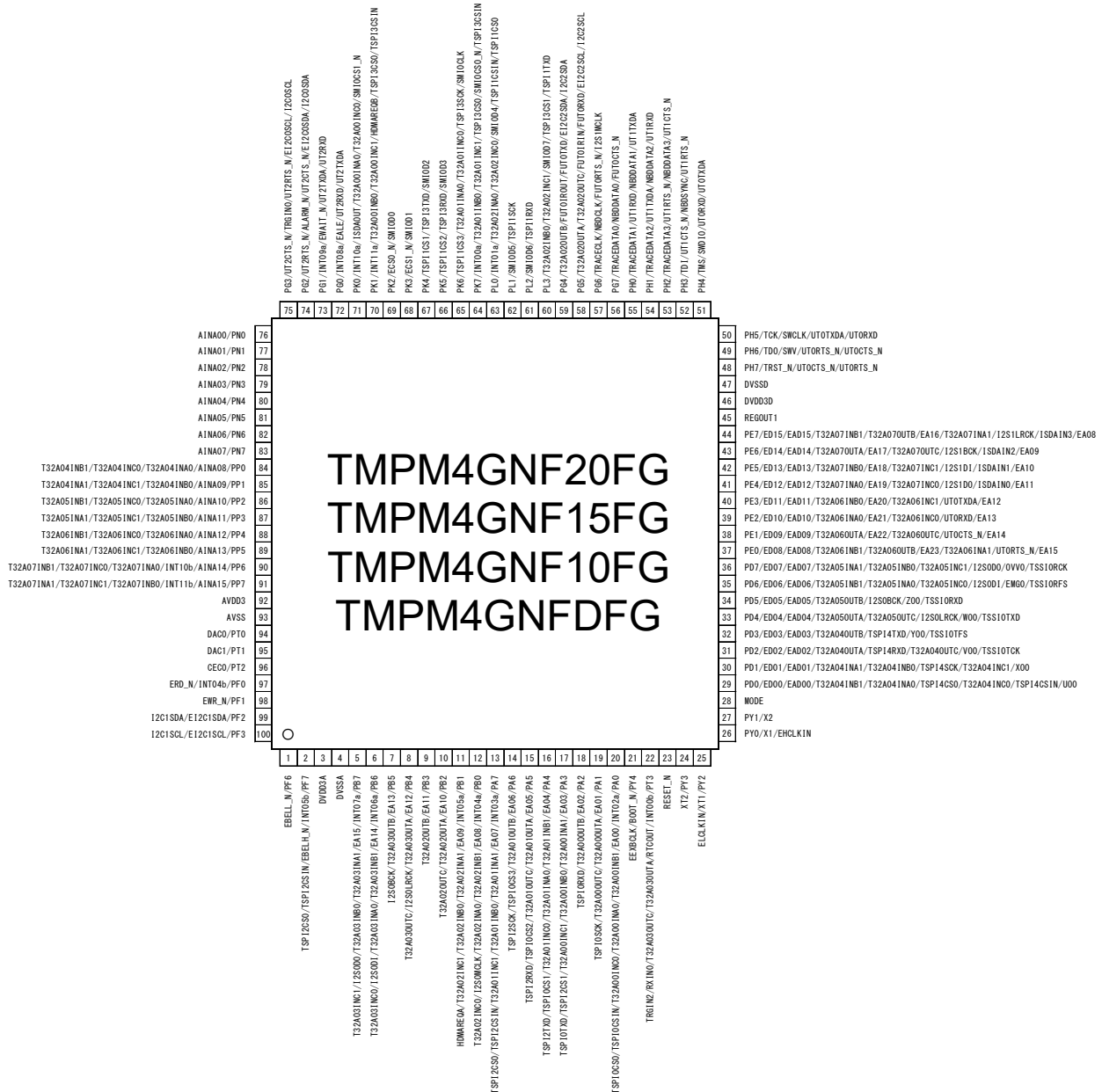
2.1. LQFP176



2.2. LQFP144



2.3. LQFP100


TMPM4GNF20FG
TMPM4GNF15FG
TMPM4GNF10FG
TMPM4GNFDFG
1 EBELL_N/PF6
2 TSP12CS0/TSP12CS1N/EBELL_N/INT05b/PF7
3 DVDD3A
4 DVSSA
5 T32A031NC1/12SDDO/T32A031NB0/T32A031NA1/EA15/INT07a/PB7
6 T32A031NC0/12SDDI/T32A031NA0/T32A031NB1/EA14/INT06a/PB6
7 12SBCK/T32A030UTB/EA13/PB5
8 T32A030UTC/12SOLRCK/T32A030UTA/EA12/PB4
9 T32A020UTB/EA11/PB3
10 T32A020UTC/T32A020UTA/EA10/PB2
11 HDMAREQA/T32A021NC1/T32A021NB0/T32A021NA1/EA09/INT05a/PB1
12 T32A021NC0/12SMCLK/T32A021NA0/T32A021NB1/EA08/INT04a/PB0
13 TSP12CS0/TSP12CS1N/T32A011NB0/T32A011NA1/EA07/INT03a/PA7
14 TSP12SCK/TSP10CS3/T32A010UTB/EA06/PA6
15 TSP12RXD/TSP10CS2/T32A010UTC/T32A010UTA/EA05/PA5
16 TSP12TXD/TSP10CS1/T32A011NC0/T32A011NA0/T32A011NB1/EA04/PA4
17 TSP10TXD/TSP12CS1/T32A001NC1/T32A001NB0/T32A001NA1/EA03/PA3
18 TSP10RXD/T32A000UTB/EA02/PA2
19 TSP10SCK/T32A000UTC/T32A000UTA/EA01/PA1
20 TSP10CS0/TSP10CS1N/T32A001NC0/T32A001NA0/T32A001NB1/EA00/INT02a/PA0
21 EEXBCLK/BOOT_N/PY4
22 TRGIN2/RXIN0/T32A030UTC/T32A030UTA/RTCOUT/INT00b/PT3
23 RESET_N
24 XT2/PY3
25 ELCLKIN/XT1/PY2
26 PY0/X1/EHCLKIN
27 PY1/X2
28 MODE
29 PD0/ED00/EAD00/T32A041NB1/T32A041NA0/TSP14CS0/T32A041NC0/TSP14CS1N/U00
30 PD1/ED01/EAD01/T32A041NA1/T32A041NB0/TSP14SCK/T32A041NC1/X00
31 PD2/ED02/EAD02/T32A040UTA/TSPI4RXD/T32A040UTC/V00/TSSI0TCK
32 PD3/ED03/EAD03/T32A040UTB/TSPI4TXD/Y00/TSSI0TFS
33 PD4/ED04/EAD04/T32A050UTA/T32A050UTC/12SOLRCK/W00/TSSI0TXD
34 PD5/ED05/EAD05/T32A050UTB/12SOBCK/Z00/TSSI0RXD
35 PD6/ED06/EAD06/T32A051NB1/T32A051NA0/T32A051NC0/12SOD1/EMG0/TSSI0RFS
36 PD7/ED07/EAD07/T32A051NA1/T32A051NB0/T32A051NC1/12SODO/OVV0/TSSI0RCK
37 PE0/ED08/EAD08/T32A061NB1/T32A060UTB/EA23/T32A061NA1/UTORTS_N/EA15
38 PE1/ED09/EAD09/T32A060UTA/EA22/T32A060UTC/UTOCTS_N/EA14
39 PE2/ED10/EAD10/T32A061NA0/EA21/T32A061NC0/UTORXD/EA13
40 PE3/ED11/EAD11/T32A061NB0/EA20/T32A061NC1/UTOTXDA/EA12
41 PE4/ED12/EAD12/T32A071NA0/EA19/T32A071NC0/12S1DO/ISDAIN0/EA11
42 PE5/ED13/EAD13/T32A071NB0/EA18/T32A071NC1/12S1DI/ISDAIN1/EA10
43 PE6/ED14/EAD14/T32A070UTA/EA17/T32A070UTC/12S1BCK/ISDAIN2/EA09
44 PE7/ED15/EAD15/T32A071NB1/T32A070UTB/EA16/T32A071NA1/12S1LRCK/ISDAIN3/EA08
45 REGOUT1
46 DVDD3D
47 DVSSD
48 PH7/TRST_N/UTOCTS_N/UTORTS_N
49 PH6/TDO/SWV/UTORTS_N/UTOCTS_N
50 PH5/TCK/SWCLK/UTOTXDA/UTORXD
51 PH4/TMS/SWDIO/UTORXD/UTOTXDA
52 PH3/TDI/UT1CTS_N/NBBSYNC/UT1RTS_N
53 PH2/TRACEDATA3/UT1RTS_N/NBEDDATA3/UT1CTS_N
54 PH1/TRACEDATA2/UT1TXDA/NBEDDATA2/UT1RXD
55 PH0/TRACEDATA1/UT1RXD/NBEDDATA1/UT1TXDA
56 PG7/TRACEDATA0/NBEDDATA0/FUTOCTS_N
57 PG6/TRACEECLK/NBECLK/FUTORTS_N/I2S1MCLK
58 PG5/T32A020UTA/T32A020UTC/FUTO1RIN/FUTORXD/E12C2SCL/I2C2SCL
59 PG4/T32A020UTB/FUTO1ROUT/FUTOTXD/E12C2SDA/I2C2SDA
60 PL3/T32A021NB0/T32A021NC1/SMI007/TSPI13CS1/TSPI1TXD
61 PL2/SMI006/TSPI1RXD
62 PL1/SMI005/TSPI1SCK
63 PL0/INT01a/T32A021NA0/T32A021NC0/SMI004/TSPI1CS1N/TSPI1CS0
64 PK7/INT00a/T32A011NB0/T32A011NC1/TSPI3CS0/SMI0CS0_N/TSPI3CS1N
65 PK6/TSPI1CS3/T32A011NA0/T32A011NC0/TSPI3SCK/SMI0CLK
66 PK5/TSPI1CS2/TSPI3RXD/SMI003
67 PK4/TSPI1CS1/TSPI3TXD/SMI002
68 PK3/ECS1_N/SMI001
69 PK2/ECS0_N/SMI000
70 PK1/INT11a/T32A001NB0/T32A001NC1/HDMAREQB/TSPI3CS0/TSPI3CS1N
71 PK0/INT10a/ISDAOUT/T32A001NA0/T32A001NC0/SMI0CS1_N
72 PG0/INT08a/EALE/UT2RXD/UT2TXDA
73 PG1/INT09a/EWAIT_N/UT2TXDA/UT2RXD
74 PG2/UT2RTS_N/ALARM_N/UT2CTS_N/E12C0SDA/I2C0SDA
75 PG3/UT2CTS_N/TRGIN0/UT2RTS_N/E12C0SCL/I2C0SCL
76 AINA00/PN0
77 AINA01/PN1
78 AINA02/PN2
79 AINA03/PN3
80 AINA04/PN4
81 AINA05/PN5
82 AINA06/PN6
83 AINA07/PN7
84 T32A041NB1/T32A041NC0/T32A041NA0/AINA08/PP0
85 T32A041NA1/T32A041NC1/T32A041NB0/AINA09/PP1
86 T32A051NB1/T32A051NC0/T32A051NA0/AINA10/PP2
87 T32A051NA1/T32A051NC1/T32A051NB0/AINA11/PP3
88 T32A061NB1/T32A061NC0/T32A061NA0/AINA12/PP4
89 T32A061NA1/T32A061NC1/T32A061NB0/AINA13/PP5
90 T32A071NB1/T32A071NC0/T32A071NA0/INT10b/AINA14/PP6
91 T32A071NA1/T32A071NC1/T32A071NB0/INT11b/AINA15/PP7
92 AVDD3
93 AVSS
94 DAC0/PT0
95 DAC1/PT1
96 CEC0/PT2
97 ERD_N/INT04b/PF0
98 EWR_N/PF1
99 I2C1SDA/E12C1SDA/PF2
100 I2C1SCL/E12C1SCL/PF3

2.4. VFBGA177

TMPM4GRF20XBG/TMPM4GRF15XBG/TMPM4GRF10XBG/TMPM4GRFDXBG

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	DVDD3A	PF4	PF3	PF1	PT1	PT0	AVDD3	PR4	PR3	PP7	PP3	PN7	PN5	PN3	PN1	DVSSF
B	PF7	PF6	PF5	PF2	PJ0	PJ1	AVSS	PR5	PR2	PP6	PP2	PN6	PN4	PN2	PN0	PG3
C	PC4	PC5	–	–	–	–	–	–	–	–	–	–	–	–	PG2	PG1
D	PC2	PC3	–	PC7	PF0	PJ2	PJ3	PR7	PR1	PP5	PP1	PP0	DVSSE	–	PG0	PL4
E	PB4	PB5	–	PC6	DVSSH	PT2	PL6	PL7	PR6	PR0	PP4	DVSSD	PM3	–	PL5	PM0
F	PB2	PB3	–	PC0	PC1	DVSSG	–	–	–	–	–	PV0	PT4	–	PM1	PM2
G	PB0	PB1	–	PB6	PB7	–	–	–	–	–	–	PV2	PV1	–	PW4	PW5
H	PA6	PA7	–	PU0	PT3	–	–	–	–	–	–	PK0	PV3	–	PW6	PW7
J	PA4	PA5	–	PU1	PU2	–	–	–	–	–	–	PK1	PK2	–	PK4	PK6
K	PA2	PA3	–	PU3	PU4	–	–	–	–	–	–	PK7	PK3	–	PK5	PL1
L	PA0	PA1	–	PU6	PU5	–	–	–	–	–	–	PG4	PL0	–	PL2	PL3
M	DVSSA	PY4	–	PU7	DVDD3G	PD1	PD3	PD5	PD7	PW2	PW0	DVDD3D	PG5	–	PG7	PG6
N	PY3/XT2	DVSSB	–	DVDD3H	PD0	PD2	PD4	PD6	PJ7	PW3	PW1	PM4	DVDD3E	–	PH1	PH0
P	PY2/XT1	DVSSC	–	–	–	–	–	–	–	–	–	–	–	–	PH3	PH2
R	RESET_N	DVDD3B	DVDD3C	PE0	PE1	PE4	PE5	PJ6	PJ5	PT5	PV7	PV4	PM6	PH7	PH6	PH4
T	MODE	PY0/X1	PY1/X2	DVDD3F	PE2	PE3	PE6	PE7	PJ4	REGOUT1	PV6	PV5	PM7	PM5	PH5	BSC

2.5. VFBGA145

TMPM4GQF20XBG/TMPM4GQF15XBG/TMPM4GQF10XBG/TMPM4GQFDXBG

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	DVDD3A	PF4	PF3	PT1	PT0	AVDD3	PR3	PP7	PP3	PN7	PN5	PN3	PN1	DVSSF
B	PF7	PF6	PF5	PF2	PF1	AVSS	PR2	PP6	PP2	PN6	PN4	PN2	PN0	PG3
C	PC4	PC5	–	–	–	–	–	–	–	–	–	–	PG2	PG1
D	PC2	PC3	–	PC7	PF0	PR7	PR4	PR0	PP4	PP1	PP0	–	PG0	PM0
E	PB4	PB5	–	PC6	PT2	PR6	PR5	PR1	PP5	DVSSD DVSSE	PT4	–	PM1	PM2
F	PB2	PB3	–	PC0	PC1	DVSSG DVSSH	–	–	–	PV0	PV1	–	PM3	PK2
G	PA5	PA6	–	PB6	PB7	–	–	–	–	PV3	PV2	–	PK3	PK4
H	PA3	PA4	–	PB0	PB1	–	–	–	–	PK0	PK1	–	PK5	PK6
J	PA1	PA2	–	PA0	PA7	–	–	–	–	PK7	PL0	–	PL2	PL1
K	DVSSA	PY4	–	PT3	DVDD3G DVDD3H	PD2	PD5	PD6	PT5	DVDD3D DVDD3E	PG5	–	PG4	PL3
L	PY3/XT2	DVSSB	–	PD0	PD1	PD3	PD4	PD7	PV7	PM4	PH0	–	PG7	PG6
M	PY2/XT1	DVSSC	–	–	–	–	–	–	–	–	–	–	PH1	PH2
N	RESET_N	DVDD3B	DVDD3C	PE0	PE1	PE3	PE6	PE7	PV6	PV4	PM6	PH7	PH3	PH4
P	MODE	PY0/X1	PY1/X2	DVDD3F	PE2	PE4	PE5	REGOUT1	PV5	PM7	PM5	PH6	PH5	BSC

3. Memory Map

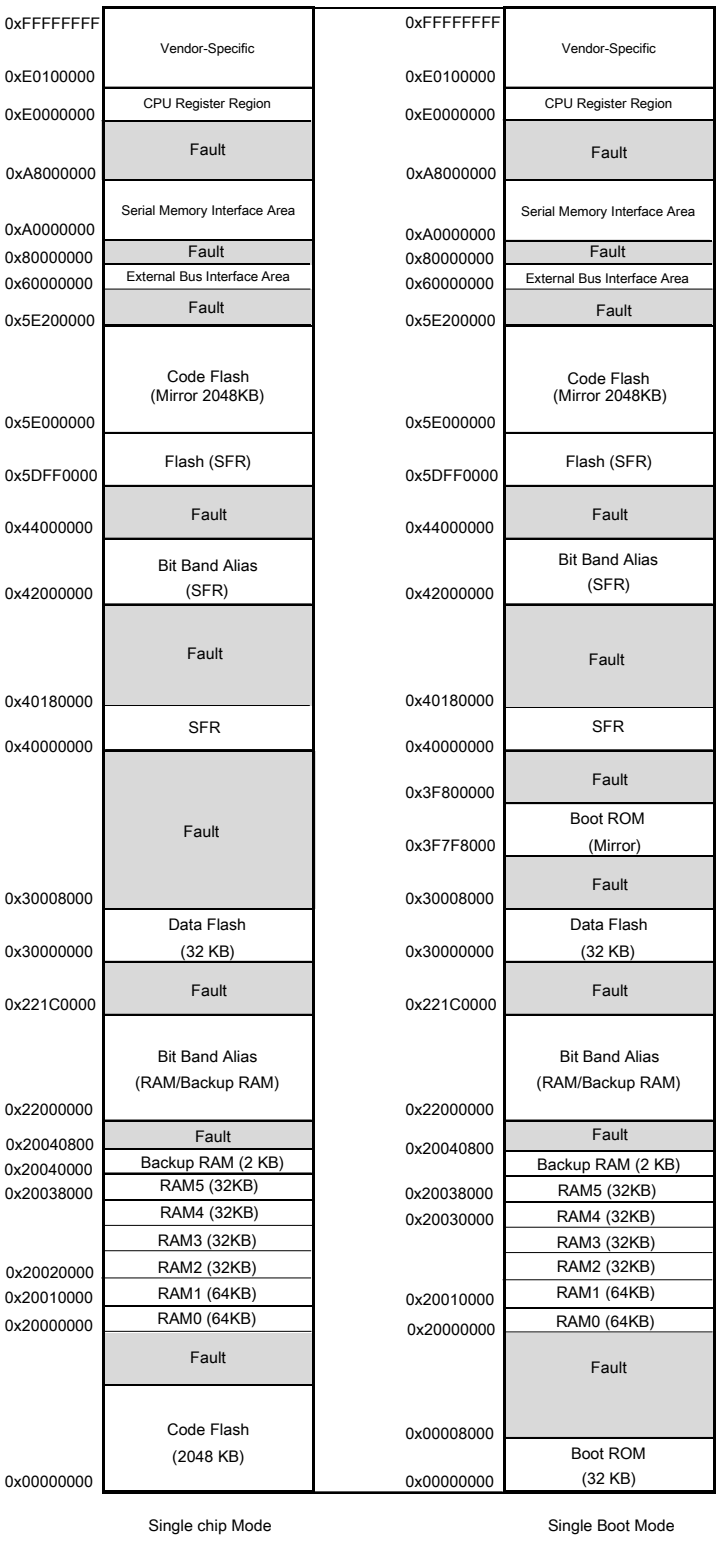


Figure 3.1 Example of the memory map of TMPM4GRF20

Note1: Fault and Reserved areas should not be accessed.

Note2: For details of Single Chip Mode and Single Boot Mode, refer to the Reference Manual "Flash Memory".

3.1. List of Memory Sizes

Table 3.1 Memory sizes and addresses

Products			TMPM4GRF20FG TMPM4GRF20XBG TMPM4GQF20FG TMPM4GQF20XBG TMPM4GNF20FG	TMPM4GRF15FG TMPM4GRF15XBG TMPM4GQF15FG TMPM4GQF15XBG TMPM4GNF15FG	TMPM4GRF10FG TMPM4GRF10XBG TMPM4GQF10FG TMPM4GQF10XBG TMPM4GNF10FG	TMPM4GRFDFG TMPM4GRFDXBG TMPM4GQFDFG TMPM4GQFDXBG TMPM4GNFDFG
Peripheral region	Code Flash (Mirror)	START	0x5E000000	0x5E000000	0x5E000000	0x5E000000
		END	0x5E1FFFFF	0x5E17FFFF	0x5E0FFFFF	0x5E07FFFF
SRAM region	Data Flash	Size	32 KB			
		START	0x30000000			
		END	0x30007FFF			
	Backup RAM	Size	2 KB			
		START	0x20040000			
		END	0x200407FF			
	RAM	Size	256 KB			192 KB
		START(0)	0x20000000			
		END(0)	0x2000FFFF			
		START(1)	0x20010000			
		END(1)	0x2001FFFF			
		START(2)	0x20020000			-
		END(2)	0x20027FFF			-
		START(3)	0x20028000			-
		END(3)	0x2002FFFF			-
		START(4)	0x20030000			
		END(4)	0x20037FFF			
		START(5)	0x20038000			
		END(5)	0x2003FFFF			
Code region	Code Flash	Size	2048 KB	1536KB	1024 KB	512 KB
		START	0x00000000	0x00000000	0x00000000	0x00000000
		END	0x001FFFFF	0x0017FFFF	0x000FFFFF	0x0007FFFF

4. Pin Description

4.1. Functional Pin Name and Function

4.1.1. Peripheral Function Pins

Table 4.1 Pin names and functions of peripheral pins (1/3)

Peripheral function	Pin name	Input or Output	Function
Interrupt control	INTx	Input	External interrupt input pin External input pin provides the noise filter (filter width: typ. 30 ns).
32-bit Timer event counter (T32A)	T32AxINA0	Input	16-bit timer A input capture input pin 0
	T32AxINA1	Input	16-bit timer A input capture input pin 1
	T32AxOUTA	Output	16-bit timer A output pin
	T32AxINB0	Input	16-bit timer B input capture input pin 0
	T32AxINB1	Input	16-bit timer B input capture input pin 1
	T32AxOUTB	Output	16-bit timer B output pin
	T32AxINC0	Input	32-bit timer C input capture input pin 0
	T32AxINC1	Input	32-bit timer C input capture input pin 1
	T32AxOUTC	Output	32-bit timer C output pin
Serial peripheral interface (TSPI)	TSPIxRXD	Input	Data input pin
	TSPIxTXD	Output	Data output pin
	TSPIxSCK	I/O	Clock input/output pin
	TSPIxCS0	Output	Chip select output pin 0
	TSPIxCS1	Output	Chip select output pin 1
	TSPIxCS2	Output	Chip select output pin 2
	TSPIxCS3	Output	Chip select output pin 3
	TSPIxCSIN	Input	Chip select input pin
Synchronous serial interface (TSSI)	TSSIxTCK	I/O	Transmit clock input/output pin
	TSSIxTFS	I/O	Transmit frame synchronization signal input/output pin
	TSSIxTXD	Output	Transmit data output pin
	TSSIxRCK	I/O	Receive clock input/output pin
	TSSIxRFS	I/O	Receive frame synchronization signal input/output pin
	TSSIxRXD	Input	Receive data input pin

Note: "x" means channel number, unit number, or interrupt number.

Table 4.2 Pin names and functions of peripheral pins (2/3)

Peripheral function	Pin name	Input or Output	Function
Serial Memory Interface (SMIF)	SMIxCLK	Output	Clock output pin
	SMIxD0	I/O	Data input/output pin 0
	SMIxD1	I/O	Data input/output pin 1
	SMIxD2	I/O	Data input/output pin 2
	SMIxD3	I/O	Data input/output pin 3
	SMIxD4	I/O	Data input/output pin 4
	SMIxD5	I/O	Data input/output pin 5
	SMIxD6	I/O	Data input/output pin 6
	SMIxD7	I/O	Data input/output pin 7
	SMIxCSx_N	Output	Chip select output pin
Asynchronous serial communication circuit (UART)	UTxTXDA	Output	Data output pin A
	UTxRXD	Input	Data input pin
	UTxCTS_N	Input	Clear to send signal pin
	UTxRTS_N	Output	Request to send signal pin
Full Universal Asynchronous Receiver Transmitter circuit (FUART)	FUTxTXD	Output	Data output pin
	FUTxRXD	Input	Data input pin
	FUTxCTS_N	Input	Transmission control input pin
	FUTxRTS_N	Output	Transmission request output pin
	FUTxIROUT	Output	IrDA 1.0 Data output pin
	FUTxIRIN	Input	IrDA 1.0 Data input pin
I^2C Interface (I2C/EI2C)	I2CxSDA /EI2CxSDA	I/O	Data input/output pin
	I2CxSCL /EI2CxSCL	I/O	Clock input/output pin
High speed DMA Controller (HDMAC)	HDMAREQx	Input	HDMA request input pin
Interval Sensor Detection circuit (ISD)	ISDxIN0	Input	Data input pin 0
	ISDxIN1	Input	Data input pin 1
	ISDxIN2	Input	Data input pin 2
	ISDxIN3	Input	Data input pin 3
	ISDxOUT	Output	Data output pin

Note: "x" means channel number, unit number, or interrupt number.

Table 4.3 Pin names and functions of peripheral pins (3/3)

Peripheral function	Pin name	Input or Output	Function
I²S interface (I2S)	I2SxBCK	I/O	Bit clock input/output pin
	I2SxLRCK	I/O	LR clock input/output pin
	I2SxDI	Input	Audio input serial data pin
	I2SxDO	Output	Audio output serial data pin
	I2SxMCLK	I/O	External master clock input/output pin
Consumer Electronics Control Circuit (CEC)	CECx	I/O	Data input/output pin
External bus interface (EBIF)	EAx	Output	Address bus output pin
	EDx	I/O	Data bus input/output pin
	EADx	I/O	Address/Data bus input/output pin
	ERD_N	Output	Read strobe output pin
	EWR_N	Output	Write strobe output pin
	ECSx_N	Output	Chip select output pin
	EBELL_N	Output	Byte enable output pin
	EBELH_N	Output	Byte enable output pin
	EALE	Output	Address latch enable output pin
	EWAIT_N	Input	Wait input pin
	EEXBCLK	Output	Clock output pin
Advanced Programmable Motor control circuit (A-PMD)	XOx	Output	X-phase output pin
	YOx	Output	Y-phase output pin
	ZOx	Output	Z-phase output pin
	UOx	Output	U-phase output pin
	VOx	Output	V-phase output pin
	WOx	Output	W-phase output pin
	EMGx	Input	Emergency state detection input pin
	OVVx	Input	Overvoltage detection input pin
Trigger input (TRGSEL)	TRGINx	Input	External trigger input pin (MDMAC/ADC)
Analog to digital converter (ADC)	AINAx	Input	Analog input pin
Digital to analog converter (DAC)	DACx	Output	DAC output pin
Remote Control Signal Preprocessor (RMC)	RXINx	Input	Remote Signaling Data input pin
Real Time Clock (RTC)	ALARM_N	Output	Alarm output pin
	RTCOUT	Output	1Hz clock output pin

Note: "x" means channel number, unit number, or interrupt number.

4.1.2. Debug Pins

There are the special pins which output internal information using TRACE and NBDIF as well as basic debug pins of JTAG/SWD.

Table 4.4 Debug pin names and functions

Debug Function	Pin name	Input or Output	Function
JTAG	TMS	Input	JTAG test mode selection input pin
	TCK	Input	JTAG serial clock input pin
	TDO	Output	JTAG serial data output pin
	TDI	Input	JTAG serial data input pin
	TRST_N	Input	JTAG test reset input pin JTAG test reset input pin has noise filter (filter width: typ.30ns).
SW	SWDIO	I/O	Serial wire data input/output pin
	SWCLK	Input	Serial wire clock input pin
	SWV	Output	Serial wire viewer output pin
TRACE	TRACECLK	Output	Trace clock output pin
	TRACEDATA0	Output	Trace data output pin 0
	TRACEDATA1	Output	Trace data output pin 1
	TRACEDATA2	Output	Trace data output pin 2
	TRACEDATA3	Output	Trace data output pin 3
NBDIF	NBDSYNC	Input	Non-break debug synchronous input pin
	NBDCLK	Input	Non-break debug clock input pin
	NBDDATA0	I/O	Non-break debug data input/output pin 0
	NBDDATA1	I/O	Non-break debug data input/output pin 1
	NBDDATA2	I/O	Non-break debug data input/output pin 2
	NBDDATA3	I/O	Non-break debug data input/output pin 3

4.1.3. Control Pins

Table 4.5 Control pin names and functions

	Pin name	Input or Output	Function
Control pin	X1	Input	High speed oscillator connection pin, External clock input pin
	X2	Output	High speed oscillator connection pin
	XT1	Input	Low speed oscillator connection pin, Low clock input pin
	XT2	Output	Low speed oscillator connection pin
	MODE	Input	Mode pin This pin must be fixed to "Low" level.
	RESET_N	Input	Reset signal input pin Reset signal input pin has noise filter(filter width: Typ.30ns)
	BOOT_N	Input	BOOT mode control pin The BOOT mode control pin is sampled at the rising edge of the RESET_N pin input or the rising edge of POR, whichever is slower. It's not sampled by internal Reset factor. If the BOOT mode control pin is "Low" level, the MCU enters single Boot mode. If it is "High", the MCU enters single chip mode. For details, refer to the reference manual "Flash Memory".
	BSC	Input	Boundary-scan mode control pin

4.1.4. Power Supply Pins

Table 4.6 Power supply pin names and functions

Power Supply	Pin name	Function
Power	DVDD3A (Note1) DVDD3B (Note1) DVDD3C (Note1) DVDD3D (Note1) DVDD3E (Note1) DVDD3F (Note1) DVDD3G (Note1) DVDD3H (Note1)	Power supply pin for digital DVDD3A/B/C/D/E/F/G/H pins supply the power to the following pins: PA to PH, PJ to PM, PT(PT2 to PT5), PU to PW, PY, X1, X2, XT1, XT2, MODE, RESET_N, BOOT_N,BSC
	DVSSA (Note2) DVSSB (Note2) DVSSC (Note2) DVSSD (Note2) DVSSE (Note2) DVSSF (Note2) DVSSG (Note2) DVSSH (Note2)	GND pin for digital
	REGOUT1 (Note3)	Capacitor for a regulator connection pin (Note4)
	AVDD3	Power supply pin and Reference power pin (VREFH) for analog circuits The AVDD3 supplies the power to the following pins: PN, PP, PR, PT (PT0, PT1)
	AVSS	GND pin and Reference GND (VREFL) pin for analog circuits

Note1: Apply the voltage to DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, and DVDD3H at the same potential except the case that the pins are not provided.

Note2: Apply the external voltage to DVSSA, DVSSB, DVSSC, DVSSD, DVSSE, DVSSF, DVSSG, and DVSSH at the same potential except the case that the pins are not provided.

Note3: For REGOUT1, do not cause a short circuit with DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H, DVSSA, DVSSB, DVSSC, DVSSD, DVSSE, DVSSF, DVSSG, or DVSSH

Note4: For the capacitor value, refer to the "Electrical Characteristics"

4.2. Functional Pin and Port Assignment (Pin Number)

Following table shows a pin number of the port assignment and each product which were seen from the functional pin.

"-" means that does not have a pin or there is no assignment of a function.

Table 4.7 List of signal connections: UART ch 0, 1

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
UART ch 0	UT0RXD	PE2	60	52	39	T5	P5
		PH4	89	73	51	R16	N14
		PH5	88	72	50	T15	P13
	UT0TXDA	PE3	61	53	40	T6	N6
		PH4	89	73	51	R16	N14
		PH5	88	72	50	T15	P13
	UT0CTS_N	PE1	59	51	38	R5	N5
		PH6	87	71	49	R15	P12
		PH7	86	70	48	R14	N12
	UT0RTS_N	PE0	58	50	37	R4	N4
		PH6	87	71	49	R15	P12
		PH7	86	70	48	R14	N12
UART ch 1	UT1RXD	PH0	93	77	55	N16	L11
		PH1	92	76	54	N15	M13
		PV4	81	65	-	R12	N10
	UT1TXDA	PH0	93	77	55	N16	L11
		PH1	92	76	54	N15	M13
		PV5	80	64	-	T12	P9
	UT1CTS_N	PH2	91	75	53	P16	M14
		PH3	90	74	52	P15	N13
		PV6	79	63	-	T11	N9
	UT1RTS_N	PH2	91	75	53	P16	M14
		PH3	90	74	52	P15	N13
		PV7	78	62	-	R11	L9

Table 4.8 List of signal connections: UART ch 2, 3, 4

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
UART ch 2	UT2RXD	PG0	129	105	72	D15	D13
		PG1	130	106	73	C16	C14
	UT2TXDA	PG0	129	105	72	D15	D13
		PG1	130	106	73	C16	C14
	UT2CTS_N	PG2	131	107	74	C15	C13
		PG3	132	108	75	B16	B14
	UT2RTS_N	PG2	131	107	74	C15	C13
		PG3	132	108	75	B16	B14
UART ch 3	UT3RXD	PU6	40	-	-	L4	-
		PV0	115	97	-	F12	F10
		PV1	114	96	-	G13	F11
	UT3TXDA	PU7	41	-	-	M4	-
		PV0	115	97	-	F12	F10
		PV1	114	96	-	G13	F11
	UT3CTS_N	PU5	39	-	-	L5	-
		PV2	113	95	-	G12	G11
		PV3	112	94	-	H13	G10
	UT3RTS_N	PU4	38	-	-	K5	-
		PV2	113	95	-	G12	G11
		PV3	112	94	-	H13	G10
UART ch 4	UT4RXD	PM0	124	102	-	E16	D14
		PM1	123	101	-	F15	E13
		PU1	35	-	-	J4	-
	UT4TXDA	PM0	124	102	-	E16	D14
		PM1	123	101	-	F15	E13
		PU0	34	-	-	H4	-
	UT4CTS_N	PM2	122	100	-	F16	E14
		PM3	121	99	-	E13	F13
		PU2	36	-	-	J5	-
	UT4RTS_N	PM2	122	100	-	F16	E14
		PM3	121	99	-	E13	F13
		PU3	37	-	-	K4	-

Table 4.9 List of signal connections: UART ch 5/FUART ch0, 1/I2C ch 0, 1, 2/EI2C ch 0, 1, 2

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
UART ch 5	UT5RXD	PJ0	168	-	-	B5	-
		PJ1	167	-	-	B6	-
	UT5TXDA	PJ0	168	-	-	B5	-
		PJ1	167	-	-	B6	-
	UT5CTS_N	PJ2	166	-	-	D6	-
		PJ3	165	-	-	D7	-
	UT5RTS_N	PJ2	166	-	-	D6	-
		PJ3	165	-	-	D7	-
FUART ch 0	FUT0RXD	PG5	96	80	58	M13	K11
		PJ5	68	-	-	R9	-
	FUT0TXD	PG4	97	81	59	L12	K13
		PJ4	69	-	-	T9	-
	FUT0CTS_N	PG7	94	78	56	M15	L13
	FUT0RTS_N	PG6	95	79	57	M16	L14
	FUT0IROUT	PG4	97	81	59	L12	K13
	FUT0IRIN	PG5	96	80	58	M13	K11
FUART ch 1	FUT1RXD	PJ7	66	-	-	N9	-
		PM6	83	67	-	R13	N11
	FUT1TXD	PJ6	67	-	-	R8	-
		PM7	82	66	-	T13	P10
	FUT1CTS_N	PM4	85	69	-	N12	L10
	FUT1RTS_N	PM5	84	68	-	T14	P11
	FUT1IROUT	PM7	82	66	-	T13	P10
	FUT1IRIN	PM6	83	67	-	R13	N11
I2C/EI2C ch 0	I2C0SDA /EI2C0SDA	PG2	131	107	74	C15	C13
	I2C0SCL /EI2C0SCL	PG3	132	108	75	B16	B14
I2C/EI2C ch 1	I2C1SDA /EI2C1SDA	PF2	174	142	99	B4	B4
	I2C1SCL /EI2C1SCL	PF3	175	143	100	A3	A3
I2C/EI2C ch 2	I2C2SDA /EI2C2SDA	PG4	97	81	59	L12	K13
		PV5	80	64	-	T12	P9
	I2C2SCL /EI2C2SCL	PG5	96	80	58	M13	K11
		PV4	81	65	-	R12	N10

Table 4.10 List of signal connections: I2C ch 3, 4/EI2C ch 3, 4/ISD unit A, B, C/I2S ch 0

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
I2C/EI2C ch 3	I2C3SDA /EI2C3SDA	PJ6	67	-	-	R8	-
		PM0	124	102	-	E16	D14
	I2C3SCL /EI2C3SCL	PJ7	66	-	-	N9	-
		PM1	123	101	-	F15	E13
I2C/EI2C ch 4	I2C4SDA /EI2C4SDA	PJ3	165	-	-	D7	-
		PM6	83	67	-	R13	N11
	I2C4SCL /EI2C4SCL	PJ2	166	-	-	D6	-
		PM7	82	66	-	T13	P10
ISD unit A	ISDAIN0	PE4	62	54	41	R6	P6
	ISDAIN1	PE5	63	55	42	R7	P7
	ISDAIN2	PE6	64	56	43	T7	N7
	ISDAIN3	PE7	65	57	44	T8	N8
	ISDAOUT	PK0	111	93	71	H12	H10
ISD unit B	ISDBIN0	PV0	115	97	-	F12	F10
	ISDBIN1	PV1	114	96	-	G13	F11
	ISDBIN2	PV2	113	95	-	G12	G11
	ISDBIN3	PV3	112	94	-	H13	G10
	ISDBOUT	PK1	110	92	70	J12	H11
ISD unit C	ISDCIN0	PW4	120	-	-	G15	-
	ISDCIN1	PW5	119	-	-	G16	-
	ISDCIN2	PW6	118	-	-	H15	-
	ISDCIN3	PW7	117	-	-	H16	-
	ISDCOUT	PY4	30	-	-	M2	-
I2S ch 0	I2S0MCLK	PB0	21	21	12	G1	H4
	I2S0LRCK	PB4	17	17	8	E1	E1
		PD4	52	44	33	N7	L7
	I2S0BCK	PB5	16	16	7	E2	E2
		PD5	53	45	34	M8	K7
	I2S0DO	PB7	14	14	5	G5	G5
		PD7	55	47	36	M9	L8
	I2S0DI	PB6	15	15	6	G4	G4
		PD6	54	46	35	N8	K8

Table 4.11 List of signal connections: I2S ch 1/TSPI ch 0, 1, 2

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
I2S ch 1	I2S1MCLK	PG6	95	79	57	M16	L14
	I2S1LRCK	PC3	8	8	-	D2	D2
		PE7	65	57	44	T8	N8
	I2S1BCK	PC2	9	9	-	D1	D1
		PE6	64	56	43	T7	N7
	I2S1DO	PC0	11	11	-	F4	F4
		PE4	62	54	41	R6	P6
	I2S1DI	PC1	10	10	-	F5	F5
		PE5	63	55	42	R7	P7
TSPI ch 0	TSPI0CSIN	PA0	29	29	20	L1	J4
	TSPI0CS0	PA0	29	29	20	L1	J4
	TSPI0CS1	PA4	25	25	16	J1	H2
	TSPI0CS2	PA5	24	24	15	J2	G1
	TSPI0CS3	PA6	23	23	14	H1	G2
	TSPI0RXD	PA2	27	27	18	K1	J2
	TSPI0TXD	PA3	26	26	17	K2	H1
	TSPI0SCK	PA1	28	28	19	L2	J1
TSPI ch 1	TSPI1CSIN	PL0	103	85	63	L13	J11
	TSPI1CS0	PL0	103	85	63	L13	J11
	TSPI1CS1	PK4	107	89	67	J15	G14
	TSPI1CS2	PK5	106	88	66	K15	H13
	TSPI1CS3	PK6	105	87	65	J16	H14
	TSPI1RXD	PL2	101	83	61	L15	J13
	TSPI1TXD	PL3	100	82	60	L16	K14
	TSPI1SCK	PL1	102	84	62	K16	J14
TSPI ch 2	TSPI2CSIN	PA7	22	22	13	H2	J5
		PF7	3	3	2	B1	B1
	TSPI2CS0	PA7	22	22	13	H2	J5
		PF7	3	3	2	B1	B1
	TSPI2CS1	PA3	26	26	17	K2	H1
	TSPI2RXD	PA5	24	24	15	J2	G1
	TSPI2TXD	PA4	25	25	16	J1	H2
	TSPI2SCK	PA6	23	23	14	H1	G2

Table 4.12 List of signal connections: TSPI ch 3, 4, 5, 6, 7, 8

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
TSPI ch 3	TSPI3CSIN	PK1	110	92	70	J12	H11
		PK7	104	86	64	K12	J10
	TSPI3CS0	PK1	110	92	70	J12	H11
		PK7	104	86	64	K12	J10
	TSPI3CS1	PL3	100	82	60	L16	K14
	TSPI3RXD	PK5	106	88	66	K15	H13
	TSPI3TXD	PK4	107	89	67	J15	G14
	TSPI3SCK	PK6	105	87	65	J16	H14
TSPI ch 4	TSPI4CSIN	PD0	48	40	29	N5	L4
	TSPI4CS0	PD0	48	40	29	N5	L4
	TSPI4RXD	PD2	50	42	31	N6	K6
	TSPI4TXD	PD3	51	43	32	M7	L6
	TSPI4SCK	PD1	49	41	30	M6	L5
TSPI ch 5	TSPI5CSIN	PV7	78	62	-	R11	L9
	TSPI5CS0	PV7	78	62	-	R11	L9
	TSPI5RXD	PV4	81	65	-	R12	N10
	TSPI5TXD	PV5	80	64	-	T12	P9
	TSPI5SCK	PV6	79	63	-	T11	N9
TSPI ch 6	TSPI6CSIN	PM3	121	99	-	E13	F13
	TSPI6CS0	PM3	121	99	-	E13	F13
	TSPI6RXD	PM1	123	101	-	F15	E13
	TSPI6TXD	PM0	124	102	-	E16	D14
	TSPI6SCK	PM2	122	100	-	F16	E14
TSPI ch 7	TSPI7CSIN	PM4	85	69	-	N12	L10
	TSPI7CS0	PM4	85	69	-	N12	L10
	TSPI7RXD	PM6	83	67	-	R13	N11
	TSPI7TXD	PM7	82	66	-	T13	P10
	TSPI7SCK	PM5	84	68	-	T14	P11
TSPI ch 8	TSPI8CSIN	PW0	77	-	-	M11	-
	TSPI8CS0	PW0	77	-	-	M11	-
	TSPI8RXD	PW2	75	-	-	M10	-
	TSPI8TXD	PW3	74	-	-	N10	-
	TSPI8SCK	PW1	76	-	-	N11	-

Table 4.13 List of signal connections: TSSI ch 0, 1/SMIF ch 0

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
TSSI ch 0	TSSI0TCK	PD2	50	42	31	N6	K6
	TSSI0TFS	PD3	51	43	32	M7	L6
	TSSI0TXD	PD4	52	44	33	N7	L7
	TSSI0RCK	PD7	55	47	36	M9	L8
	TSSI0RFS	PD6	54	46	35	N8	K8
	TSSI0RXD	PD5	53	45	34	M8	K7
TSSI ch 1	TSSI1TCK	PU2	36	-	-	J5	-
	TSSI1TFS	PU3	37	-	-	K4	-
	TSSI1TXD	PU4	38	-	-	K5	-
	TSSI1RCK	PU7	41	-	-	M4	-
	TSSI1RFS	PU6	40	-	-	L4	-
	TSSI1RXD	PU5	39	-	-	L5	-
SMIF ch 0	SMI0CS1_N	PK0	111	93	71	H12	H10
	SMI0D0	PK2	109	91	69	J13	F14
	SMI0D1	PK3	108	90	68	K13	G13
	SMI0D2	PK4	107	89	67	J15	G14
	SMI0D3	PK5	106	88	66	K15	H13
	SMI0D4	PL0	103	85	63	L13	J11
	SMI0D5	PL1	102	84	62	K16	J14
	SMI0D6	PL2	101	83	61	L15	J13
	SMI0D7	PL3	100	82	60	L16	K14
	SMI0CLK	PK6	105	87	65	J16	H14
	SMI0CS0_N	PK7	104	86	64	K12	J10

Table 4.14 List of signal connections: T32A ch 0, 1

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
T32A ch 0	T32A00INA0	PA0	29	29	20	L1	J4
		PK0	111	93	71	H12	H10
	T32A00INA1	PA3	26	26	17	K2	H1
	T32A00OUTA	PA1	28	28	19	L2	J1
		PW1	76	-	-	N11	-
	T32A00INB0	PA3	26	26	17	K2	H1
		PK1	110	92	70	J12	H11
	T32A00INB1	PA0	29	29	20	L1	J4
	T32A00OUTB	PA2	27	27	18	K1	J2
		PW0	77	-	-	M11	-
	T32A00INC0	PA0	29	29	20	L1	J4
		PK0	111	93	71	H12	H10
	T32A00INC1	PA3	26	26	17	K2	H1
		PK1	110	92	70	J12	H11
	T32A00OUTC	PA1	28	28	19	L2	J1
		PW1	76	-	-	N11	-
T32A ch 1	T32A01INA0	PA4	25	25	16	J1	H2
		PK6	105	87	65	J16	H14
	T32A01INA1	PA7	22	22	13	H2	J5
	T32A01OUTA	PA5	24	24	15	J2	G1
		PW2	75	-	-	M10	-
	T32A01INB0	PA7	22	22	13	H2	J5
		PK7	104	86	64	K12	J10
	T32A01INB1	PA4	25	25	16	J1	H2
	T32A01OUTB	PA6	23	23	14	H1	G2
		PW3	74	-	-	N10	-
	T32A01INC0	PA4	25	25	16	J1	H2
		PK6	105	87	65	J16	H14
	T32A01INC1	PA7	22	22	13	H2	J5
		PK7	104	86	64	K12	J10
	T32A01OUTC	PA5	24	24	15	J2	G1
		PW2	75	-	-	M10	-

Table 4.15 List of signal connections: T32A ch 2, 3

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
T32A ch 2	T32A02INA0	PB0	21	21	12	G1	H4
		PL0	103	85	63	L13	J11
	T32A02INA1	PB1	20	20	11	G2	H5
	T32A02OUTA	PB2	19	19	10	F1	F1
		PG5	96	80	58	M13	K11
	T32A02INB0	PB1	20	20	11	G2	H5
		PL3	100	82	60	L16	K14
	T32A02INB1	PB0	21	21	12	G1	H4
	T32A02OUTB	PB3	18	18	9	F2	F2
		PG4	97	81	59	L12	K13
	T32A02INC0	PB0	21	21	12	G1	H4
		PL0	103	85	63	L13	J11
	T32A02INC1	PB1	20	20	11	G2	H5
		PL3	100	82	60	L16	K14
	T32A02OUTC	PB2	19	19	10	F1	F1
		PG5	96	80	58	M13	K11
T32A ch 3	T32A03INA0	PB6	15	15	6	G4	G4
		PJ4	69	-	-	T9	-
	T32A03INA1	PB7	14	14	5	G5	G5
	T32A03OUTA	PB4	17	17	8	E1	E1
		PT3	31	31	22	H5	K4
	T32A03INB0	PB7	14	14	5	G5	G5
		PJ5	68	-	-	R9	-
	T32A03INB1	PB6	15	15	6	G4	G4
	T32A03OUTB	PB5	16	16	7	E2	E2
		PT5	73	61	-	R10	K9
	T32A03INC0	PB6	15	15	6	G4	G4
		PJ4	69	-	-	T9	-
	T32A03INC1	PB7	14	14	5	G5	G5
		PJ5	68	-	-	R9	-
	T32A03OUTC	PB4	17	17	8	E1	E1
		PT3	31	31	22	H5	K4

Table 4.16 List of signal connections: T32A ch 4, 5

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
T32A ch 4	T32A04INA0	PD0	48	40	29	N5	L4
		PP0	141	117	84	D12	D11
	T32A04INA1	PD1	49	41	30	M6	L5
		PP1	142	118	85	D11	D10
	T32A04OUTA	PD2	50	42	31	N6	K6
		PV5	80	64	-	T12	P9
	T32A04INB0	PD1	49	41	30	M6	L5
		PP1	142	118	85	D11	D10
	T32A04INB1	PD0	48	40	29	N5	L4
		PP0	141	117	84	D12	D11
	T32A04OUTB	PD3	51	43	32	M7	L6
		PV4	81	65	-	R12	N10
	T32A04INC0	PD0	48	40	29	N5	L4
		PP0	141	117	84	D12	D11
	T32A04INC1	PD1	49	41	30	M6	L5
		PP1	142	118	85	D11	D10
	T32A04OUTC	PD2	50	42	31	N6	K6
		PV5	80	64	-	T12	P9
T32A ch 5	T32A05INA0	PD6	54	46	35	N8	K8
		PP2	143	119	86	B11	B9
	T32A05INA1	PD7	55	47	36	M9	L8
		PP3	144	120	87	A11	A9
	T32A05OUTA	PD4	52	44	33	N7	L7
		PV6	79	63	-	T11	N9
	T32A05INB0	PD7	55	47	36	M9	L8
		PP3	144	120	87	A11	A9
	T32A05INB1	PD6	54	46	35	N8	K8
		PP2	143	119	86	B11	B9
	T32A05OUTB	PD5	53	45	34	M8	K7
		PV7	78	62	-	R11	L9
	T32A05INC0	PD6	54	46	35	N8	K8
		PP2	143	119	86	B11	B9
	T32A05INC1	PD7	55	47	36	M9	L8
		PP3	144	120	87	A11	A9
	T32A05OUTC	PD4	52	44	33	N7	L7
		PV6	79	63	-	T11	N9

Table 4.17 List of signal connections: T32A ch 6, 7

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
T32A ch 6	T32A06INA0	PE2	60	52	39	T5	P5
		PP4	145	121	88	E11	D9
	T32A06INA1	PE0	58	50	37	R4	N4
		PP5	146	122	89	D10	E9
	T32A06OUTA	PE1	59	51	38	R5	N5
		PM5	84	68	-	T14	P11
	T32A06INB0	PE3	61	53	40	T6	N6
		PP5	146	122	89	D10	E9
	T32A06INB1	PE0	58	50	37	R4	N4
		PP4	145	121	88	E11	D9
	T32A06OUTB	PE0	58	50	37	R4	N4
		PM4	85	69	-	N12	L10
	T32A06INC0	PE2	60	52	39	T5	P5
		PP4	145	121	88	E11	D9
	T32A06INC1	PE3	61	53	40	T6	N6
		PP5	146	122	89	D10	E9
	T32A06OUTC	PE1	59	51	38	R5	N5
		PM5	84	68	-	T14	P11
T32A ch 7	T32A07INA0	PE4	62	54	41	R6	P6
		PP6	147	123	90	B10	B8
	T32A07INA1	PE7	65	57	44	T8	N8
		PP7	148	124	91	A10	A8
	T32A07OUTA	PE6	64	56	43	T7	N7
		PM6	83	67	-	R13	N11
	T32A07INB0	PE5	63	55	42	R7	P7
		PP7	148	124	91	A10	A8
	T32A07INB1	PE7	65	57	44	T8	N8
		PP6	147	123	90	B10	B8
	T32A07OUTB	PE7	65	57	44	T8	N8
		PM7	82	66	-	T13	P10
	T32A07INC0	PE4	62	54	41	R6	P6
		PP6	147	123	90	B10	B8
	T32A07INC1	PE5	63	55	42	R7	P7
		PP7	148	124	91	A10	A8
	T32A07OUTC	PE6	64	56	43	T7	N7
		PM6	83	67	-	R13	N11

Table 4.18 List of signal connections: T32A ch 8, 9

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
T32A ch 8	T32A08INA0	PC0	11	11	-	F4	F4
		PR0	149	125	-	E10	D8
	T32A08OUTA	PC2	9	9	-	D1	D1
		PL4	126	-	-	D16	-
	T32A08INB0	PC1	10	10	-	F5	F5
		PR1	150	126	-	D9	E8
	T32A08OUTB	PC3	8	8	-	D2	D2
		PL5	125	-	-	E15	-
	T32A08INC0	PC0	11	11	-	F4	F4
		PR0	149	125	-	E10	D8
	T32A08INC1	PC1	10	10	-	F5	F5
		PR1	150	126	-	D9	E8
	T32A08OUTC	PC2	9	9	-	D1	D1
		PL4	126	-	-	D16	-
T32A ch 9	T32A09INA0	PR2	151	127	-	B9	B7
		PV0	115	97	-	F12	F10
	T32A09OUTA	PL6	164	-	-	E7	-
		PV2	113	95	-	G12	G11
	T32A09INB0	PR3	152	128	-	A9	A7
		PV1	114	96	-	G13	F11
	T32A09OUTB	PL7	163	-	-	E8	-
		PV3	112	94	-	H13	G10
	T32A09INC0	PR2	151	127	-	B9	B7
		PV0	115	97	-	F12	F10
	T32A09INC1	PR3	152	128	-	A9	A7
		PV1	114	96	-	G13	F11
	T32A09OUTC	PL6	164	-	-	E7	-
		PV2	113	95	-	G12	G11

Table 4.19 List of signal connections: T32A ch 10, 11

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
T32A ch 10	T32A10INA0	PR4	153	129	-	A8	D7
		PW4	120	-	-	G15	-
	T32A10INA1	PW7	117	-	-	H16	-
	T32A10OUTA	PC4	7	7	-	C1	C1
		PW5	119	-	-	G16	-
	T32A10INB0	PR5	154	130	-	B8	E7
	T32A10OUTB	PC5	6	6	-	C2	C2
		PW4	120	-	-	G15	-
	T32A10INC0	PR4	153	129	-	A8	D7
	T32A10INC1	PR5	154	130	-	B8	E7
	T32A10OUTC	PC4	7	7	-	C1	C1
		PW5	119	-	-	G16	-
T32A ch 11	T32A11INA0	PR6	155	131	-	E9	E6
		PW7	117	-	-	H16	-
	T32A11INA1	PW4	120	-	-	G15	-
	T32A11OUTA	PM2	122	100	-	F16	E14
		PW6	118	-	-	H15	-
	T32A11INB0	PR7	156	132	-	D8	D6
	T32A11OUTB	PM3	121	99	-	E13	F13
		PW7	117	-	-	H16	-
	T32A11INC0	PR6	155	131	-	E9	E6
	T32A11INC1	PR7	156	132	-	D8	D6
	T32A11OUTC	PM2	122	100	-	F16	E14
		PW6	118	-	-	H15	-

Table 4.20 List of signal connections: T32A ch 12, 13/EBIF (1/3)

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
T32A ch 12	T32A12INA0	PU2	36	-	-	J5	-
	T32A12OUTA	PU0	34	-	-	H4	-
	T32A12INB0	PU3	37	-	-	K4	-
	T32A12OUTB	PU1	35	-	-	J4	-
	T32A12INC0	PU2	36	-	-	J5	-
	T32A12INC1	PU3	37	-	-	K4	-
	T32A12OUTC	PU0	34	-	-	H4	-
T32A ch 13	T32A13INA0	PU5	39	-	-	L5	-
	T32A13OUTA	PU6	40	-	-	L4	-
	T32A13INB0	PU4	38	-	-	K5	-
	T32A13OUTB	PU7	41	-	-	M4	-
	T32A13INC0	PU5	39	-	-	L5	-
	T32A13INC1	PU4	38	-	-	K5	-
	T32A13OUTC	PU6	40	-	-	L4	-
EBIF	EA00	PA0	29	29	20	L1	J4
	EA01	PA1	28	28	19	L2	J1
	EA02	PA2	27	27	18	K1	J2
	EA03	PA3	26	26	17	K2	H1
	EA04	PA4	25	25	16	J1	H2
	EA05	PA5	24	24	15	J2	G1
	EA06	PA6	23	23	14	H1	G2
	EA07	PA7	22	22	13	H2	J5

Table 4.21 List of signal connections: EBIF (2/3)

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
EBIF	EA08	PB0	21	21	12	G1	H4
		PE7	65	57	44	T8	N8
	EA09	PB1	20	20	11	G2	H5
		PE6	64	56	43	T7	N7
	EA10	PB2	19	19	10	F1	F1
		PE5	63	55	42	R7	P7
	EA11	PB3	18	18	9	F2	F2
		PE4	62	54	41	R6	P6
	EA12	PB4	17	17	8	E1	E1
		PE3	61	53	40	T6	N6
	EA13	PB5	16	16	7	E2	E2
		PE2	60	52	39	T5	P5
	EA14	PB6	15	15	6	G4	G4
		PE1	59	51	38	R5	N5
	EA15	PB7	14	14	5	G5	G5
		PE0	58	50	37	R4	N4
	EA16	PC0	11	11	-	F4	F4
		PE7	65	57	44	T8	N8
	EA17	PC1	10	10	-	F5	F5
		PE6	64	56	43	T7	N7
	EA18	PC2	9	9	-	D1	D1
		PE5	63	55	42	R7	P7
	EA19	PC3	8	8	-	D2	D2
		PE4	62	54	41	R6	P6
	EA20	PC4	7	7	-	C1	C1
		PE3	61	53	40	T6	N6
	EA21	PC5	6	6	-	C2	C2
		PE2	60	52	39	T5	P5
	EA22	PC6	5	5	-	E4	E4
		PE1	59	51	38	R5	N5
	EA23	PC7	4	4	-	D4	D4
		PE0	58	50	37	R4	N4

Table 4.22 List of signal connections: EBIF (3/3)/NBDIF

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
EBIF	ED00/EAD00	PD0	48	40	29	N5	L4
	ED01/EAD01	PD1	49	41	30	M6	L5
	ED02/EAD02	PD2	50	42	31	N6	K6
	ED03/EAD03	PD3	51	43	32	M7	L6
	ED04/EAD04	PD4	52	44	33	N7	L7
	ED05/EAD05	PD5	53	45	34	M8	K7
	ED06/EAD06	PD6	54	46	35	N8	K8
	ED07/EAD07	PD7	55	47	36	M9	L8
	ED08/EAD08	PE0	58	50	37	R4	N4
	ED09/EAD09	PE1	59	51	38	R5	N5
	ED10/EAD10	PE2	60	52	39	T5	P5
	ED11/EAD11	PE3	61	53	40	T6	N6
	ED12/EAD12	PE4	62	54	41	R6	P6
	ED13/EAD13	PE5	63	55	42	R7	P7
	ED14/EAD14	PE6	64	56	43	T7	N7
	ED15/EAD15	PE7	65	57	44	T8	N8
	ERD_N	PF0	172	140	97	D5	D5
	EWR_N	PF1	173	141	98	A4	B5
	ECS0_N	PK2	109	91	69	J13	F14
	ECS1_N	PK3	108	90	68	K13	G13
	ECS2_N	PF4	176	144	-	A2	A2
	ECS3_N	PF5	1	1	-	B3	B3
	EBELL_N	PF6	2	2	1	B2	B2
	EBELH_N	PF7	3	3	2	B1	B1
	EALE	PG0	129	105	72	D15	D13
	EWAIT_N	PG1	130	106	73	C16	C14
	EEXBCLK	PY4	30	30	21	M2	K2
NBDIF	NBDCLK	PG6	95	79	57	M16	L14
	NBDDATA0	PG7	94	78	56	M15	L13
	NBDDATA1	PH0	93	77	55	N16	L11
	NBDDATA2	PH1	92	76	54	N15	M13
	NBDDATA3	PH2	91	75	53	P16	M14
	NBDSYNC	PH3	90	74	52	P15	N13

Table 4.23 List of signal connections: ADC unit A/DAC ch 0, 1/TRGSEL

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
ADC unit A	AINA00	PN0	133	109	76	B15	B13
	AINA01	PN1	134	110	77	A15	A13
	AINA02	PN2	135	111	78	B14	B12
	AINA03	PN3	136	112	79	A14	A12
	AINA04	PN4	137	113	80	B13	B11
	AINA05	PN5	138	114	81	A13	A11
	AINA06	PN6	139	115	82	B12	B10
	AINA07	PN7	140	116	83	A12	A10
	AINA08	PP0	141	117	84	D12	D11
	AINA09	PP1	142	118	85	D11	D10
	AINA10	PP2	143	119	86	B11	B9
	AINA11	PP3	144	120	87	A11	A9
	AINA12	PP4	145	121	88	E11	D9
	AINA13	PP5	146	122	89	D10	E9
	AINA14	PP6	147	123	90	B10	B8
	AINA15	PP7	148	124	91	A10	A8
	AINA16	PR0	149	125	-	E10	D8
	AINA17	PR1	150	126	-	D9	E8
	AINA18	PR2	151	127	-	B9	B7
	AINA19	PR3	152	128	-	A9	A7
	AINA20	PR4	153	129	-	A8	D7
	AINA21	PR5	154	130	-	B8	E7
	AINA22	PR6	155	131	-	E9	E6
	AINA23	PR7	156	132	-	D8	D6
DAC ch 0, 1	DAC0	PT0	159	135	94	A6	A5
	DAC1	PT1	160	136	95	A5	A4
TRGSEL	TRGIN0	PG3	132	108	75	B16	B14
	TRGIN1	PL7	163	-	-	E8	-
	TRGIN2	PT3	31	31	22	H5	K4

Table 4.24 List of signal connections: A-PMD ch0/ CEC ch0/RTC/RMC ch 0, 1/HDMAC unit A, B /JTAG/SW/TRACE

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
A-PMD ch 0	EMG0	PD6	54	46	35	N8	K8
		PV6	79	63	-	T11	N9
	OVV0	PD7	55	47	36	M9	L8
		PV7	78	62	-	R11	L9
	UO0	PD0	48	40	29	N5	L4
		PV0	115	97	-	F12	F10
	VO0	PD2	50	42	31	N6	K6
		PV2	113	95	-	G12	G11
	WO0	PD4	52	44	33	N7	L7
		PV4	81	65	-	R12	N10
	XO0	PD1	49	41	30	M6	L5
		PV1	114	96	-	G13	F11
	YO0	PD3	51	43	32	M7	L6
		PV3	112	94	-	H13	G10
	ZO0	PD5	53	45	34	M8	K7
		PV5	80	64	-	T12	P9
CEC ch 0	CEC0	PT2	171	139	96	E6	E5
RTC	ALARM_N	PG2	131	107	74	C15	C13
	RTCOUT	PT3	31	31	22	H5	K4
RMC ch 0, 1	RXIN0	PT3	31	31	22	H5	K4
	RXIN1	PT4	116	98	-	F13	E11
HDMC unit A, B	HDMAREQA	PB1	20	20	11	G2	H5
	HDMAREQB	PK1	110	92	70	J12	H11
JTAG	TMS	PH4	89	73	51	R16	N14
	TCK	PH5	88	72	50	T15	P13
	TDO	PH6	87	71	49	R15	P12
	TDI	PH3	90	74	52	P15	N13
	TRST_N	PH7	86	70	48	R14	N12
SW	SWDIO	PH4	89	73	51	R16	N14
	SWCLK	PH5	88	72	50	T15	P13
	SWV	PH6	87	71	49	R15	P12
TRACE	TRACECLK	PG6	95	79	57	M16	L14
	TRACEDATA0	PG7	94	78	56	M15	L13
	TRACEDATA1	PH0	93	77	55	N16	L11
	TRACEDATA2	PH1	92	76	54	N15	M13
	TRACEDATA3	PH2	91	75	53	P16	M14

Table 4.25 List of signal connections: INT

Function	Combination functional pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
INT	INT00a	PK7	104	86	64	K12	J10
	INT00b	PT3	31	31	22	H5	K4
	INT01a	PL0	103	85	63	L13	J11
	INT01b	PT4	116	98	-	F13	E11
	INT02a	PA0	29	29	20	L1	J4
	INT02b	PT5	73	61	-	R10	K9
	INT03a	PA7	22	22	13	H2	J5
	INT03b	PL6	164	-	-	E7	-
	INT04a	PB0	21	21	12	G1	H4
	INT04b	PF0	172	140	97	D5	D5
	INT05a	PB1	20	20	11	G2	H5
	INT05b	PF7	3	3	2	B1	B1
	INT06a	PB6	15	15	6	G4	G4
	INT06b	PU2	36	-	-	J5	-
	INT07a	PB7	14	14	5	G5	G5
	INT07b	PU3	37	-	-	K4	-
	INT08a	PG0	129	105	72	D15	D13
	INT08b	PU4	38	-	-	K5	-
	INT09a	PG1	130	106	73	C16	C14
	INT09b	PU5	39	-	-	L5	-
	INT10a	PK0	111	93	71	H12	H10
	INT10b	PP6	147	123	90	B10	B8
	INT11a	PK1	110	92	70	J12	H11
	INT11b	PP7	148	124	91	A10	A8
	INT12a	PC0	11	11	-	F4	F4
	INT12b	PL4	126	-	-	D16	-
	INT13a	PC1	10	10	-	F5	F5
	INT13b	PL5	125	-	-	E15	-
	INT14a	PC6	5	5	-	E4	E4
	INT14b	PM3	121	99	-	E13	F13
	INT15a	PC7	4	4	-	D4	D4
	INT15b	PM4	85	69	-	N12	L10

Table 4.26 List of signal connections: Control/Power

Function	Combination functional pin name or Dedicated pin name	Port name	M4GR (LQFP176)	M4GQ (LQFP144)	M4GN (LQFP100)	M4GR (BGA177)	M4GQ (BGA145)
Control	X1	PY0	45	37	26	T2	P2
	X2	PY1	46	38	27	T3	P3
	XT1	PY2	44	36	25	P1	M1
	XT2	PY3	43	35	24	N1	L1
	BOOT_N	PY4	30	30	21	M2	K2
	EHCLKIN	PY0	45	37	26	T2	P2
	ELCLKIN	PY2	44	36	25	P1	M1
	RESET_N		42	34	23	R1	N1
	MODE		47	39	28	T1	P1
	BSC		-	-	-	T16	P14
Power	DVDD3A		12	12	3	A1	A1
	DVDD3B		32	32	-	R2	N2
	DVDD3C		56	48	-	R3	N3
	DVDD3D		71	59	46	M12	K10
	DVDD3E		98	-	-	N13	K10
	DVDD3F		127	103	-	T4	P4
	DVDD3G		161	137	-	M5	K5
	DVDD3H		169	-	-	N4	K5
	DVSSA		13	13	4	M1	K1
	DVSSB		33	33	-	N2	L2
	DVSSC		57	49	-	P2	M2
	DVSSD		72	60	47	E12	E10
	DVSSE		99	-	-	D13	E10
	DVSSF		128	104	-	A16	A14
	DVSSG		162	138	-	F6	F6
	DVSSH		170	-	-	E5	F6
	REGOUT1		70	58	45	T10	P8
	AVDD3		157	133	92	A7	A6
	AVSS		158	134	93	B7	B6

4.3. Ports

The symbols of each table of port have the following meanings.

- Input/Output: Input and/or Output of Port
  Input: Input port
  Output: Output port
  I/O: Input/output port

- PU/PD: Programmable pull-up/pull-down
  PU: Programmable pull-up is selectable
  PD: Programmable pull-down is selectable

- OD: Programmable open-drain output
  YES: Support
  NO: Non support

- 5VT/3VT: Tolerant
  5VT: 5V-tolerant
  3VT: 3V-tolerant
  N/A: Not available

- SMT/CMOS: Input gate
  SMT: Schmitt trigger input
  CMOS: CMOS input

- Under Reset: Port state under Reset
  Hi-Z: High impedance
  PU: Pull-up
  PD: Pull-down

- After Reset: Port state after Reset
  Hi-Z: High impedance
  PU: Pull-up
  PD: Pull-down

4.3.1. Port Specifications Table

Table 4.27 Port names, and specifications of Port A, B, C, D

Port Name	Input/Output	PU/PD	OD	5VT/3VT	SMT/ CMOS	Under Reset	After Reset
PA0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PA1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PA2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PA3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PA4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PA5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PA6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PA7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z

Table 4.28 Port names, and specifications of Port E, F, G, H

Port Name	Input/Output	PU/PD	OD	5VT/3VT	SMT/ CMOS	Under Reset	After Reset
PE0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF2	I/O	PU/PD	YES	5VT	SMT	Hi-Z	Hi-Z
PF3	I/O	PU/PD	YES	5VT	SMT	Hi-Z	Hi-Z
PF4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG2	I/O	PU/PD	YES	5VT	SMT	Hi-Z	Hi-Z
PG3	I/O	PU/PD	YES	5VT	SMT	Hi-Z	Hi-Z
PG4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH3	I/O	PU/PD	YES	N/A	SMT	PU	PU
PH4	I/O	PU/PD	YES	N/A	SMT	PU	PU
PH5	I/O	PU/PD	YES	N/A	SMT	PD	PD
PH6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH7	I/O	PU/PD	YES	N/A	SMT	PU	PU

Table 4.29 Port names, and specifications of Port J, K, L, M

Port Name	Input/Output	PU/PD	OD	5VT/3VT	SMT/ CMOS	Under Reset	After Reset
PJ0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PL0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PL1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PL2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PL3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PL4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PL5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PL6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PL7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z

Table 4.30 Port names, and specifications of Port N, P, R, T

Port Name	Input/Output	PU/PD	OD	5VT/3VT	SMT/ CMOS	Under Reset	After Reset
PN0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT2	I/O	PU/PD	YES	3VT	SMT	Hi-Z	Hi-Z
PT3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z

Table 4.31 Port names, and specifications of Port U, V, W, Y

Port Name	Input/Output	PU/PD	OD	5VT/3VT	SMT/ CMOS	Under Reset	After Reset
PU0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PW0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PW1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PW2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PW3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PW4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PW5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PW6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PW7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PY0	Input	PU/PD	N/A	N/A	SMT	Hi-Z	Hi-Z
PY1	Input	PU/PD	N/A	N/A	SMT	Hi-Z	Hi-Z
PY2	Input	PU/PD	N/A	N/A	SMT	Hi-Z	Hi-Z
PY3	Input	PU/PD	N/A	N/A	SMT	Hi-Z	Hi-Z
PY4	Output	PU/PD	YES	N/A	SMT	Hi-Z(Note)	Hi-Z

Note: This pin is shared by BOOT_N pin. During the reset period by the reset pin (RESET_N) and POR, ***[PYPUP]*** is enabled ("1") and the BOOT_N signal can be input. When RESET_N pin = High, if internal reset other than POR is asserted, it is Hi-Z state.

5. Functional Description and Operation Description

For the details of the functions, refer to Reference manuals.

5.1. Reference Manuals

For more information on product of TMPM4G Group (1), please refer to Reference Manuals below;

Table 5.1 Reference Manuals for TMPM4G Group (1)

Reference Manual	IP Symbol	Category
Input/Output Ports (TMPM4G Group(1))	PORT-M4G(1)	System
Exception (TMPM4G Group(1))	EXCEPT-M4G(1)	System
Clock Control and Operation Mode (TMPM4G Group(1))	CG-M4G(1)-C	System
Product Information (TMPM4G Group(1))	PINFO-M4G(1)	System
Flash Memory (Code Flash:2.0MB/1.5MB/1.0MB/512KB, Data Flash 32KB, USB single boot supported)	FLASH20MUD32-C	Peripheral
Trimming Circuit	TRM-B	Peripheral
Oscillation Frequency Detector	OFD-A	Peripheral
Voltage Detection Circuit	LVD-E	Peripheral
Digital Noise Filter Circuit	DNF-A	Peripheral
Debug Interface	DEBUG-A	Peripheral
Non Break Debug Interface	NBDIF-A	Peripheral
Interval Sensor Detection Circuit	ISD-A	Peripheral
I^2S Interface	I2S-A	Peripheral
FIR Calculation circuit	FIR-A	Peripheral
Multi-Function DMA Controller	MDMAC-B	Peripheral
High Speed DMA Controller	HDMAC-A	Peripheral
External Bus Interface	EBIF-A	Peripheral
Serial Memory Interface	SMIF-B	Peripheral
Asynchronous Serial Communication Circuit	UART-C	Peripheral
Full Universal Asynchronous Receiver Transmitter Circuit	FUART-B	Peripheral
Serial Peripheral Interface	TSPI-E	Peripheral
Synchronous serial interface	TSSI-A	Peripheral
I^2C Interface	I2C-B	Peripheral
I^2C Interface Version A	EI2C-A	Peripheral
Consumer Electronics Control Circuit	CEC-A	Peripheral
12-bit Analog to Digital Converter	ADC-H	Peripheral
8-bit Digital to Analog Converter	DAC-B	Peripheral
Advanced Programmable Motor Control Circuit	A-PMD-C	Peripheral
32-bit Timer Event Counter	T32A-B	Peripheral
Long Term Timer	LTTMR-A	Peripheral
Real Time Clock	RTC-A	Peripheral
Clock Selective Watchdog Timer	SIWDT-A	Peripheral
Remote Control Signal Preprocessor	RMC-B	Peripheral
Boundary Scan	BSC-A	Peripheral

5.2. Processor Core

TMPM4G Group (1) incorporates a high-performance 32-bit processor core (Arm Cortex-M4 (with FPU)).

For the operation of the processor core, refer to the "Arm documentation set of the Arm "Cortex-M" series processors". This section explains the product-specific information.

5.2.1. Core Information

The Cortex-M4 (with FPU) core revision used in TMPM4G Group (1) is shown as below:
For details of the CPU core and the architecture, refer to the Arm documentation in the following URL:
http://infocenter.arm.com/help/index.jsp

Table 5.2 Core revision

Group name	Core revision
TMPM4G Group (1)	r0p1

5.2.2. Configurable Options

In the Cortex-M4 (with FPU) core, some blocks can be selected to implement. The following table shows the configurations of TMPM4G Group (1).

Table 5.3 Configurable options and their implementations

Configurable option	Implementation
FWB	Literal comparator: 2 Instruction comparator: 6
DWT	Comparator: 4
ITM	Available
MPU	Available
ETM	Available
AHB-AP	Available
AHB trace macro cell interface	Not available
TPIU	Available
WIC	Not available
Debug port	JTAG/Serial wire
Bit band	Available
Sequential control of AHB	Not available

5.3. Clock Control and Operation Mode (CG)

The CG selects a clock gear ratio and the prescaler clock, or warm up time of the oscillator.

There are NORMAL mode and low power consumption mode as operation modes. Power consumption can be reduced by mode transition.

The system clock consists of "High speed system clock" and "Middle speed system clock". The former is a high speed oscillation clock and the latter is generated by dividing High speed system clock.

The outline of the clock control circuit is as follows:

- Internal high speed oscillation circuit 1: 10 MHz
- Internal high speed oscillation circuit 2: 10 MHz
- Selectable from the external high speed oscillation circuit or internal high speed oscillation circuit.
- PLL (Clock Multiplication Circuit):

  Capable of 200 MHz output by changing the multiplication ratio according to the frequency of the high speed oscillation circuit
- Clock gear:

  The high speed clock can be divided by 1, 2, 4, 8, or 16 and the clock is used as the system clock (fsys).
- Low power consumption mode:

  IDLE: Only the CPU is stopped in this mode. Each peripheral circuit can be enabled or disabled in the IDLE mode.

  STOP1: Except some peripheral circuits, all the internal circuits including the internal oscillator are brought to a stop in STOP1 mode.
  The low frequency oscillator can be supplied to RTC, RMC CEC and ISD by the corresponding setting. LTTMR can be worked by enabling of IHOSC2.

  STOP2: This mode halts voltage supply, retaining some peripheral circuits operation. The low frequency clock can be supplied to RTC, RMC, CEC and ISD by the corresponding setting. LTTMR can be worked by enabling of IHOSC2.

5.4. Flash Memory (Code FLASH, Data FLASH)

The cord flash stores instruction code, and CPU reads instruction code and executes.

The code flash and data flash store data, and even if a power supply is off, data can be kept.

The flash memory has the dual mode that possible to write and erase a data flash while executing instructions on a code flash, and it's also possible to continue executing an application program while writing or erasing data flash.

While saving the data to the data flash, it can continue running the application program on the code flash.

It has protection function which prohibits write or erase by the block unit and it has the security function which prohibits the reading of the program code by outsiders.

5.5. Oscillation Circuit

External High Speed Oscillator (EHOSC):	Connect crystal resonator or ceramic resonator to terminals. Use clock source for System clock.
External Low Speed Oscillator (ELOSC):	Connect crystal resonator (32.768 kHz) to terminals. Use clock source for Real Time Clock or Power consumption mode.
Internal High Speed Oscillator 1 (IHOSC1):	Oscillation frequency is 10 MHz. Use clock source for System clock.
Internal High Speed Oscillator 2 (IHOSC2):	Oscillation frequency is 10 MHz. Use clock source for OFD, SIWDT and LTTMR.

The built-in oscillators in TMPM4G Group (1) are shown in the following table.

Table 5.4 Built-in Oscillator

	M4GR	M4GQ	M4GN
EHOSC	✓	✓	✓
ELOSC	✓	✓	✓
IHOSC1	✓	✓	✓
IHOSC2	✓	✓	✓

Note: ✓: Available, -: N/A

5.6. Trimming Circuit (TRM)

The trimming function can adjust frequency of the internal high speed oscillator1 (IHOSC1).
The built-in trimming circuit is integrated in TMPM4G Group (1) as shown in the following table.

Table 5.5 Built-in TRM

	M4GR	M4GQ	M4GN
TRM	✓	✓	✓

Note: ✓: Available, -: N/A

5.7. Oscillation Frequency Detector (OFD)

The oscillation frequency detection circuit (OFD) is a function that detects an abnormal state of the clock. It measures the external high speed oscillation (f_{EHOSC}) or high speed clock (fc) based on the internal reference clock (f_{IHOSC2}). If an oscillation or clock frequency is out of the specified range, a reset signal occurs.
The upper limit and the lower limit of detection frequency ranges can be specified.

Table 5.6 Built-in OFD

	M4GR	M4GQ	M4GN
OFD	✓	✓	✓

Note: ✓: Available, -: N/A

5.8. Voltage Detection Circuit (LVD)

The LVD is a peripheral function that detects whether a power supply voltage is lower or higher than the preset voltage. When a low voltage or higher voltage than the preset voltage is detected, the LVD generates an interrupt request or reset the MCU.

Setting voltage can be selected from seven levels. LVD is set to enable from the Reset state at the Power-on.

Table 5.7 Built-in LVD

	M4GR	M4GQ	M4GN
LVD	✓	✓	✓

Note: ✓: Available, -: N/A

5.9. Digital Noise Filter Circuit (DNF)

The digital noise filter circuit can eliminate noise of input signals from external interrupt pins at the certain range. The noise of the High level/Low level input of the external interrupt signal INTx is removed. The width of noise elimination can be selected from among 0.07 to 4.48 μs (fc=200 MHz) for each interrupt input pin independently.

TMPM4G Group (1) can have 17 to 32 external interrupt input pins.

Table 5.8 Number of External interrupt pins (Built-in DNF)

	M4GR	M4GQ	M4GN
External interrupt pins	32	25	17

5.10. Debug Interface (DEBUG)

TMPM4G Group (1) contains interface to connect debug tool, which is the Serial Wire Debug Port (SWCLK, SWDIO) and the JTAG Debug Port (TDI, TDO, TMS, TCK, TRST_N). These are connected with the Debug tool and used for program development. And also it contains the trace clock (TRACECLK) and data output (TRACEDATA0 to 3) to reduce the Debug Process.

TMPM4G Group (1) supports Serial Wire Debug Port, JTAG Debug Port and Trace outputs.

Table 5.9 Built-in Debug Interface

	Port	M4GR	M4GQ	M4GN
TMS/SWDIO	PH4	✓	✓	✓
TCK/SWCLK	PH5	✓	✓	✓
TDO/SWV	PH6	✓	✓	✓
TDI	PH3	✓	✓	✓
TRST_N	PH7	✓	✓	✓
TRACECLK	PG6	✓	✓	✓
TRACEDATA0	PG7	✓	✓	✓
TRACEDATA1	PH0	✓	✓	✓
TRACEDATA2	PH1	✓	✓	✓
TRACEDATA3	PH2	✓	✓	✓

Note: ✓: Available, -: N/A

5.11. Non Break Debug Interface (NBDIF)

Connecting debug tools supporting NBD interface can provide RAM monitor function.

Table 5.10 Built-in NBDIF

	M4GR	M4GQ	M4GN
NBDSYNC	✓	✓	✓
NBDCLK	✓	✓	✓
NBDDATA0	✓	✓	✓
NBDDATA1	✓	✓	✓
NBDDATA2	✓	✓	✓
NBDDATA3	✓	✓	✓

Note: ✓: Available, -: N/A

5.12. Interval Sensor Detection Circuit (ISD)

ISD can generate an interrupt when the value of the sensor input changes (High level, Low level, High to Low transition, and Low to High transition). And the low power consumption mode can be released by the input signal detection interrupt.

Table 5.11 Built-in ISD

UNIT	M4GR	M4GQ	M4GN
Unit A	✓	✓	✓
Unit B	✓	✓	-
Unit C	✓	-	-

Note: ✓: Available, -: N/A

5.13. I²S Interface (I2S)

I2S can transmit and receive audio data. The audio data format can be selected from I²S stereo/LR stereo/PCM monaural, and the sampling frequency is up to 192 kHz for stereo and up to 384 kHz for monaural.

Table 5.12 Built-in I2S

Channel	M4GR	M4GQ	M4GN
Channel 0	✓	✓	✓
Channel 1	✓	✓	✓

Note: ✓: Available, -: N/A

5.14. FIR Calculation circuit (FIR)

The FIR calculation circuit (FIR) is a dedicated function for I²S Interface (I2S). When the data is written to the data buffer, sum-of-products arithmetic operation are performed with a pre-set filter coefficient. FIR can be operated in cooperation with I2S and MDMAC.

Table 5.13 Built-in FIR

Channel	M4GR	M4GQ	M4GN
Channel 0	✓	✓	✓

Note: ✓: Available, -: N/A

5.15. DMA Controller

5.15.1. Multi-Function DMA Controller (MDMAC)

MDMAC transfers data from peripheral function to memory, from memory to peripheral function and between memories. These operations are performed separately from the CPU control. The CPU load can be greatly reduced by using it. The transfer count can be set infinitely by using chain transfer.

TMPM4G Group (1) has one unit of MDMAC. There are 32 channel requests per unit. The inputs of channels 0 to 31 pass via the trigger selector (TRGSEL). They can be used as startup factors which are assigned to TSPI, TSSI, UART, FUART, I2C/EI2C, I2S, FIR, T32A, ADC, A-PMD, external trigger input via the trigger selector (TRGSEL).

Table 5.14 Built-in MDMAC

UNIT	M4GR	M4GQ	M4GN
Unit A	✓	✓	✓

Note: ✓: Available, -: N/A

5.15.2. High Speed DMA Controller (HDMAC)

HDMAC transfers data from peripheral function to memory, from memory to peripheral function and between memories. High speed transfer of up to 4095 counts is possible. These operations are performed separately from the CPU control. The CPU load can be greatly reduced by using it.

TMPM4G Group (1) has two units of HDMAC. SMIF, TSPI, External trigger pin can be startup factors of HDMAC.

Table 5.15 Built-in HDMAC

UNIT	M4GR	M4GQ	M4GN
Unit A	✓	✓	✓
Unit B	✓	✓	✓

Note: ✓: Available, -: N/A

5.16. External Bus Interface (EBIF)

EBIF (External bus interface) connects external memories, external I/O’s, and others.
Two modes (Separate bus mode and Multiplex bus mode) are available and EBIF supports 64 MB access space (16 MB × 4 channels) at maximum. The data bus width can be set to 8 bits or 16 bits per channel.

Table 5.16 Built-in EBIF

	M4GR	M4GQ	M4GN
EBIF	✓	✓	✓

Note: ✓: Available, -: N/A

5.17. Serial Memory Interface (SMIF)

SMIF is an interface for connecting to devices (SPI Flash memory and others) with serial I/O or multiple I/O communication interface devices . Up to two serial memories can be connected per channel. The access method supports direct access and indirect access. For communication between SMIF and SPI memory, read / write is supported for STR-SPI (Standard SPI compatible), STR-Quad, STR-QPI, STR-Octal, and STR-OPI.

Table 5.17 Built-in SMIF

Channel	M4GR	M4GQ	M4GN
Channel 0	✓	✓	✓

Note: ✓: Available, -: N/A

5.18. Asynchronous Serial Communication Circuit

5.18.1. Asynchronous Serial Communication Circuit (UART)

The UART is asynchronous serial communication function. It can choose the data length of 7, 8 or 9 bits, parity existence, and a STOP bit length function. Moreover, selection of the MSB first/LSB first and reversal of data polarity can be performed and Terminal exchanged of TXD/RXD can be performed in a Port setting.

The FIFO buffer supports data communication on 8 stage at transmission; and on 8 stage at reception.

The telecommunication control by CTS/RTS are supported.

Table 5.18 Built-in UART

Channel	M4GR	M4GQ	M4GN
Channel 0	✓	✓	✓
Channel 1	✓	✓	✓
Channel 2	✓	✓	✓
Channel 3	✓	✓	-
Channel 4	✓	✓	-
Channel 5	✓	-	-

Note1: ✓: Available, -: N/A
Note2: External pins are not same by product. Please refer to "2. Pin Assignment".

5.18.2. Full Universal Asynchronous Receiver Transmitter Circuit (FUART)

FUART is asynchronous serial communication function. It can choose a data length of 5, 6, 7, or 8 bits, parity existence, and a STOP bit length.

The FIFO buffer contains data communication on 32 stage at transmission and on 32 stage at reception. The communication control by CTS/RTS, IrDA 1.0 function, and DMA are supported.

Table 5.19 Built-in FUART

Channel	M4GR	M4GQ	M4GN
Channel 0	✓	✓	✓
Channel 1	✓	✓	–

Note1: ✓: Available, -: N/A
Note2: External pins are not same by product. Please refer to "2. Pin Assignment".

5.19. Serial Peripheral Interface (TSPI)

The TSPI supports two communication methods and enables serial communication to perform between this device and other devices at high speed. The SPI bus type, which uses a CS (Chip Select) signal at communications, and SIO bus type, which does not use a CS signal at communications can be selected.

The data length can be changed from 7 bits (with a parity bit) to 32 bits (without a parity bit) in the unit of one bit. There are an 8 stage 16-bit FIFO for reception and transmission, each. The TSPI supports the master and slave communications. In addition, frame mode (frame length (8 to 32 bits)) or sector mode (frame length (8 to 128 bits) consisting of 2 to 4 sectors) can be used.

Table 5.20 Built-in TSPI

Channel	M4GR	M4GQ	M4GN
Channel 0	✓	✓	✓
Channel 1	✓	✓	✓
Channel 2	✓	✓	✓
Channel 3	✓	✓	✓
Channel 4	✓	✓	✓
Channel 5	✓	✓	-
Channel 6	✓	✓	-
Channel 7	✓	✓	-
Channel 8	✓	-	-

Note1: ✓: Available, -: N/A
Note2: External pins are not same by product. Please refer to "2. Pin Assignment".

5.20. Synchronous serial interface (TSSI)

The synchronous serial interface (TSSI) can be used synchronous serial communication independently for the transmitter and the receiver. Transmit and receive (full duplex communication) is also possible by the cooperative operation of the transmitter and receiver. Each of the transmitter and receiver has a 32-bit x 4stages FIFO.

Table 5.21 Built-in TSSI

Channel	M4GR	M4GQ	M4GN
Channel 0	✓	✓	✓
Channel 1	✓	-	-

Note1: ✓: Available, -: N/A
Note2: External pin are not same by product. Please refer to "2. Pin Assignment".

5.21. I^2C Interface

The following table shows the list of I^2C interfaces.
Use the I^2C interface (I2C) and I^2C interface version A (EI2C) exclusively.

Table 5.22 Built-in I2C/EI2C

Channel	M4GR	M4GQ	M4GN
Channel 0	✓	✓	✓
Channel 1	✓	✓	✓
Channel 2	✓	✓	✓
Channel 3	✓	✓	-
Channel 4	✓	✓	-

Note: ✓: Available, -: N/A

5.21.1. I^2C Interface (I2C)

I2C is two-wire bi-directional serial communications between Master and Slave device. The mode in which two or more masters can exist on the same bus called a multi-master is supported. It supports Standard mode (up to 100kHz), Fast mode (up to 400kHz). The slave address supports the 7-bit addressing format.

5.21.2. I^2C Interface Version A (EI2C)

EI2C is two-wire bi-directional serial communications between Master and Slave device. The mode in which two or more masters can exist on the same bus called a multi-master is supported. It supports Standard mode (up to 100kHz), Fast mode (up to 400kHz), Fast mode Plus (up to 1MHz). The slave address supports the 7-bit and 10-bit addressing format.

5.22. Consumer Electronics Control Circuit (CEC)

CEC (Consumer Electronics Control) transfers data compliant with HDMI standard Version 1.3a.

Table 5.23 Built-in CEC

Channel	M4GR	M4GQ	M4GN
Channel 0	✓	✓	✓

Note: ✓: Available, -: N/A

5.23. 8-bit Digital to Analog Converter (DAC)

The DAC is an R-2R type 8-bit digital to analog converter that can output the specified voltage. A buffer amplifier is not incorporated.

Table 5.24 Built-in DAC

Channel	M4GR	M4GQ	M4GN
Channel 0	✓	✓	✓
Channel 1	✓	✓	✓

Note: ✓: Available, -: N/A

5.24. 12-bit Analog to Digital Converter (ADC)

The ADC is a successive-approximation analog to digital converter. It supports maximum 24 analog inputs. The combination of conversion result register and analog input can be programmed for each AD conversion start factor, and it can be selected the highest startup factor / general purpose startup factor or sampling period. A startup trigger for ADC can be selected from software or peripheral functions (timer/event counter outputs, port inputs).

The monitor function is also available and it can generate an interrupt request when the compare conditions are matched.

Table 5.25 Built-in ADC

UNIT	M4GR	M4GQ	M4GN
Unit A	✓	✓	✓

Note: ✓: Available, -: N/A

Table 5.26 Number of analog inputs for ADC

	M4GR	M4GQ	M4GN
Analog inputs pin count	24	24	16

5.25. Advanced Programmable Motor Control Circuit (A-PMD)

The Advanced Programmable Motor control circuit (A-PMD) can control motors easily. It incorporates a three-phase pulse modulation circuit and a dead-time circuit, and easily generates waveforms for motor control.

Table 5.27 Built-in A-PMD

Channel	M4GR	M4GQ	M4GN
Channel 0	✓	✓	✓

Note: ✓: Available, -: N/A

5.26. 32-bit Timer Event Counter (T32A)

The T32A is a timer event counter that can operate as a 32-bit timer or two 16-bit timers. 16-bit Timer or 32-bit Timer can be selected. In 16-bit Timer, the T32A is comprised of Timer A and Timer B incorporating a 16-bit counter. In 32-bit Timer, the T32A operates as Timer C incorporating a 32-bit counter.

The T32A has an interval timer, event counter, input capture, 2-phase counter input, PPG output, Synchronous Start, and Trigger start/stop functions.

Table 5.28 Built-in T32A

Channel	M4GR	M4GQ	M4GN
Channel 0	✓	✓	✓
Channel 1	✓	✓	✓
Channel 2	✓	✓	✓
Channel 3	✓	✓	✓
Channel 4	✓	✓	✓
Channel 5	✓	✓	✓
Channel 6	✓	✓	✓
Channel 7	✓	✓	✓
Channel 8	✓	✓	✓
Channel 9	✓	✓	✓
Channel 10	✓	✓	✓
Channel 11	✓	✓	✓
Channel 12	✓	✓	✓
Channel 13	✓	✓	✓
Channel 14	✓	✓	✓
Channel 15	✓	✓	✓

Note1: ✓: Available, -: N/A
Note2: External pins are not same by product. Please refer to "2. Pin Assignment".

5.27. Long Term Timer (LTTMR)

The long term timer (LTTMR) notifies an interrupt request at a constant period. The period is generated based on the frequency of the internal oscillator 2 (IHOSC2). The interrupt cycle can be generated in the range of 0.1 μs to 6553.5 μs. The output of LTTMR can be used as the source clock of RMC and CEC.

Table 5.29 Built-in LTTMR

Channel	M4GR	M4GQ	M4GN
LTTMR	✓	✓	✓

Note: ✓: Available, -: N/A

5.28. Real Time Clock (RTC)

The RTC is a peripheral function that has a second counter, clock function, and leap year calendar function. It also has the alarm function that generates an interrupt request on a specified time and date.

Since the RTC operates on a low speed external oscillation clock, it can operate in low power consumption mode such as IDLE, STOP1 or STOP2 mode. In addition, the MCU can be returned from low power consumption mode by an interrupt request of the RTC.

The RTC easily corrects a gain/loss of the clock caused by an error of low speed oscillation frequency using the clock correction function.

Table 5.30 Built-in RTC

	M4GR	M4GQ	M4GN
RTC	✓	✓	✓

Note: ✓: Available, -: N/A

5.29. Clock Selective Watchdog Timer (SIWDT)

The SIWDT is a peripheral function that detects an overflow of the binary counter and generates an interrupt request or resets the MCU. This state occurs when a binary counter cannot be cleared within the preset detection time.

The count clock can be selected from three clocks: system clock (fsys / 4), internal high speed oscillator 1 clock (f_{IHOSC1}), or internal high speed oscillator 2 clock (f_{IHOSC2}).

It also provides the count-clear window function that can clear the count only for the specified period.

Moreover, change of a register can be forbidden by setting to protected mode (the count-clear function is possible).

Table 5.31 Built-in SIWDT

	M4GR	M4GQ	M4GN
SIWDT	✓	✓	✓

Note: ✓: Available, -: N/A

5.30. Remote Control Signal Preprocessor (RMC)

The RMC is a peripheral function that receives signals excluding carrier signal from remote control reception signals. The RMC detects a leader signal to receive 72 bits data in a collective manner. Two data formats can be received: synchronous format and fixed-synchronous phase format.

In addition, it contains a digital noise canceller to avoid external noise. The interval of the leader signals can be also measured using the timer event counter.

Since the RMC operates on a low speed clock, it can operate in low power consumption mode, such as IDLE mode, STOP1 mode or STOP2 mode according to the setting. The MCU can also be returned from low power consumption mode by an interrupt request of the RMC.

Table 5.32 Built-in RMC

Channel	M4GR	M4GQ	M4GN
Channel0	✓	✓	✓
Channel1	✓	✓	-

Note: ✓: Available, -: N/A

5.31. Boundary Scan (BSC)

A boundary-scan supports the on-board Test. The TMPM4G group (1) provides a boundary-scan interface that is compatible with Joint Test Action Group (JTAG) specifications and uses the industry-standard JTAG protocol (IEEE Standard 1149.1·1990 (includes IEEE Standard 1149.1a·1993)).

Table 5.33 Built-in BSC

	M4GR	M4GQ	M4GN
Boundary-scan	✓	✓	-

Note1: ✓: Available, -: N/A

Note2: M4GR and M4GQ are implemented only VFBGA177 and VFBGA145.

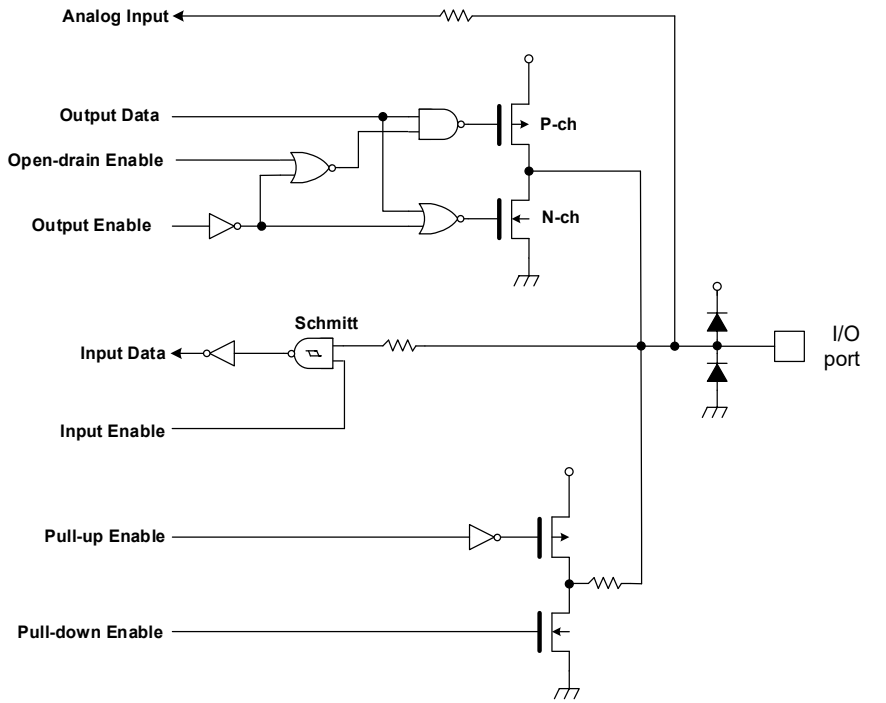
6. Equivalent Circuit

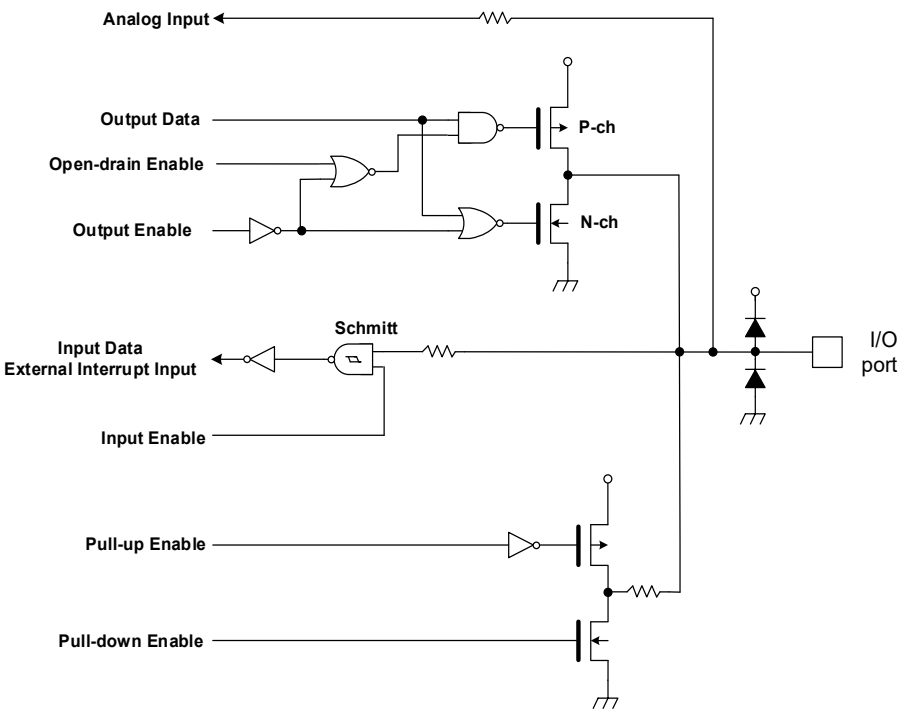
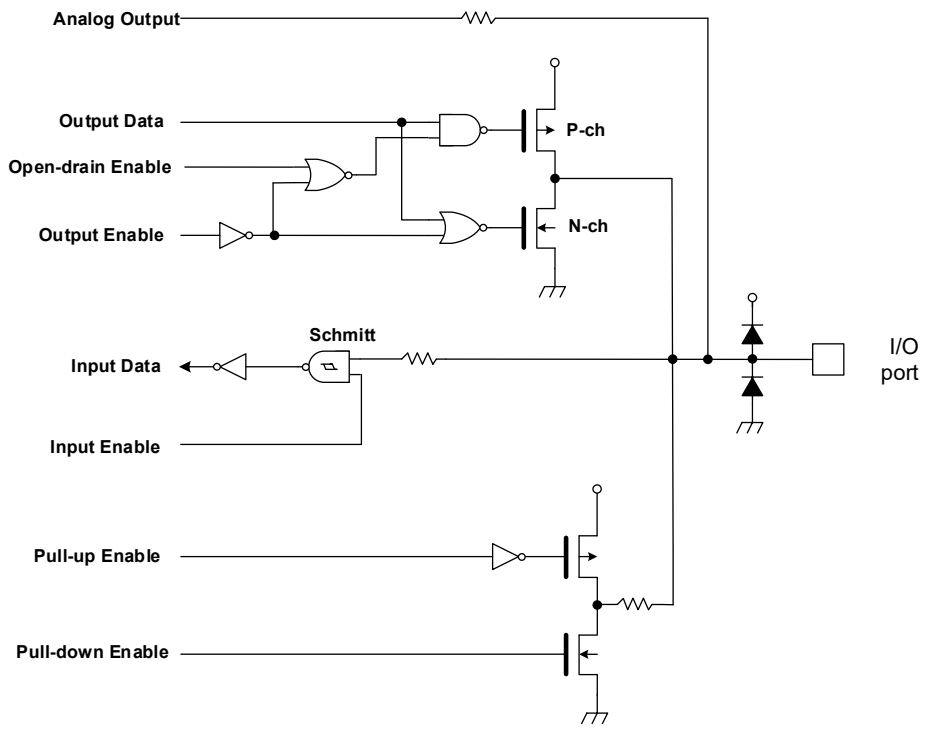
Basically, the gate symbols written are the same as those used for the standard CMOS logic IC [74HCXX] series.

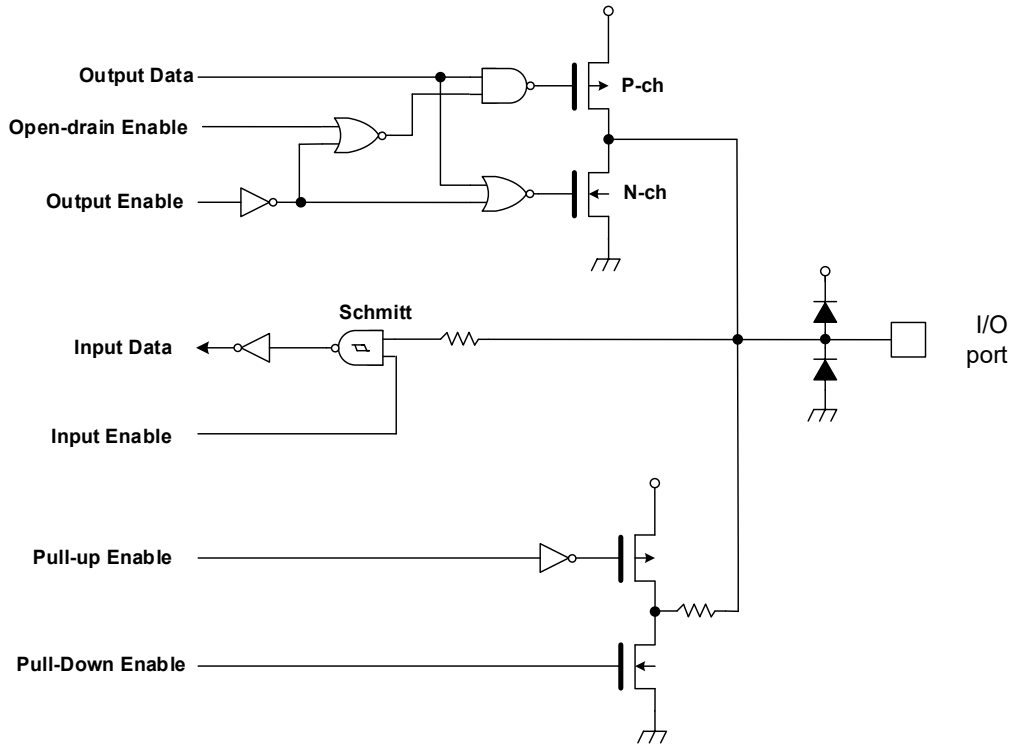
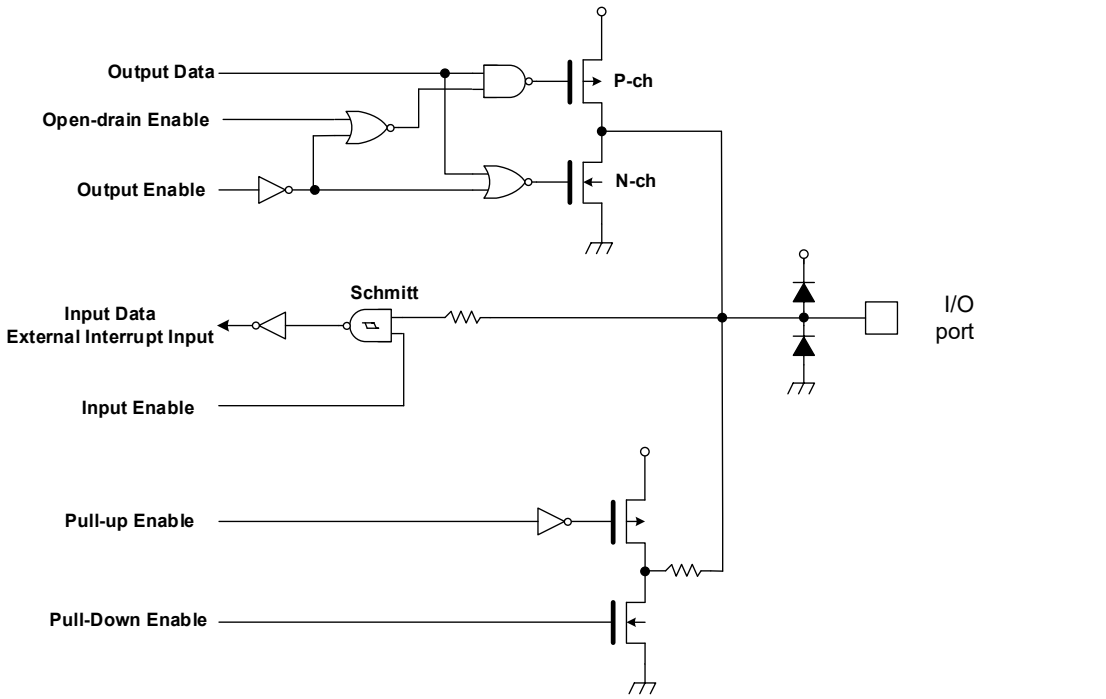
The input protection resistance ranges from several tens of Ω to several hundreds of Ω, Feedback resistor and Damping resistor are shown with a typical value.

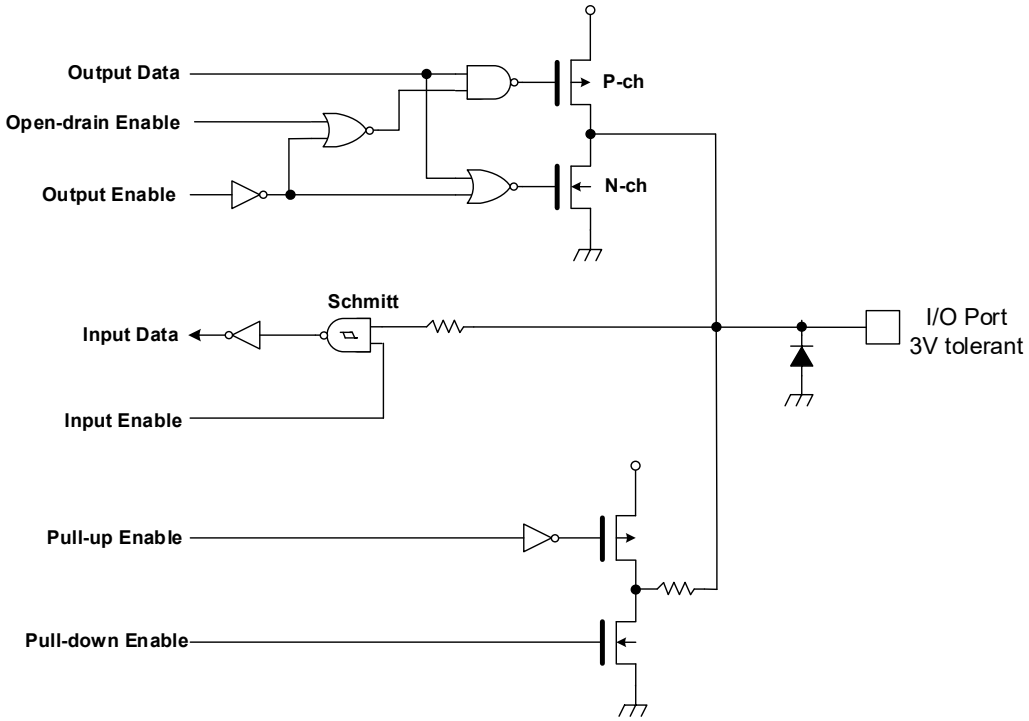
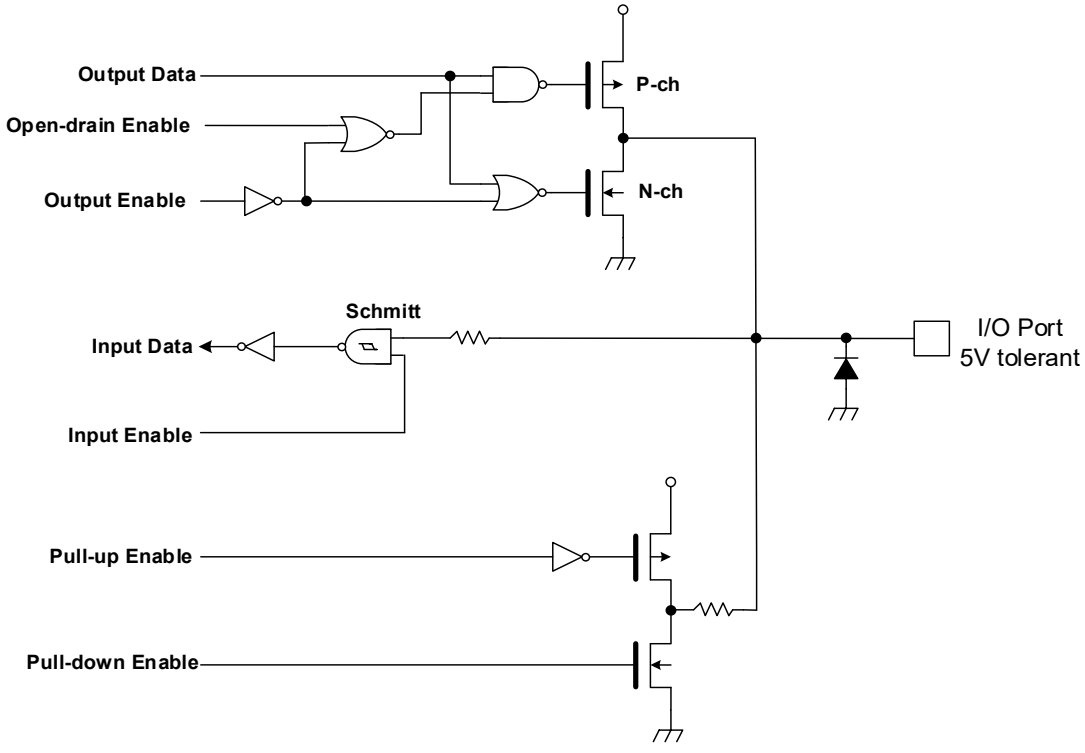
Note: The resistance without the statement of the numerical value in the figure shows input protection resistance.

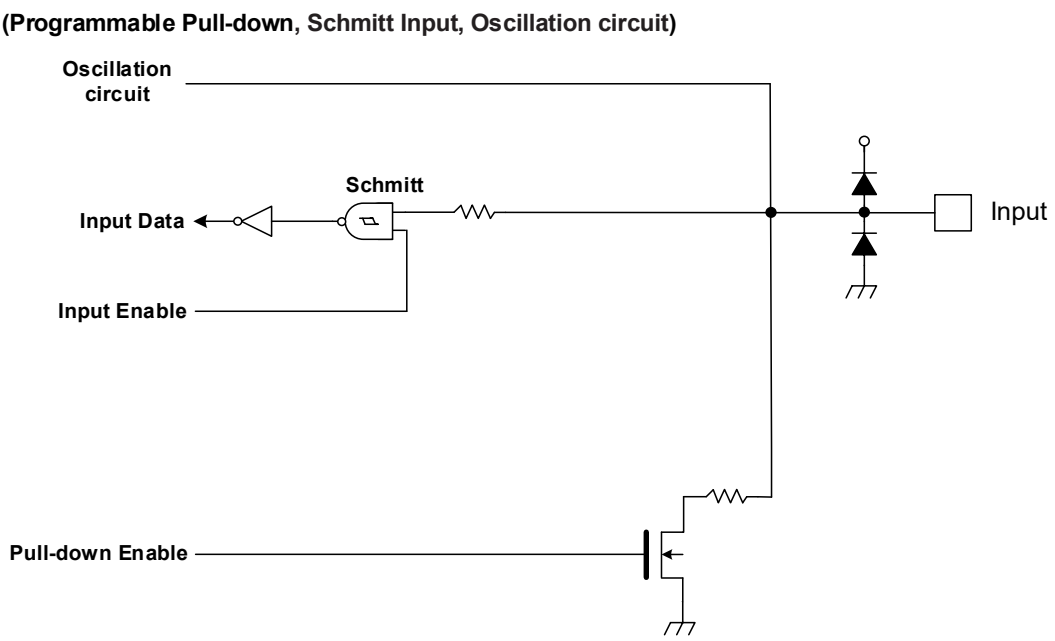
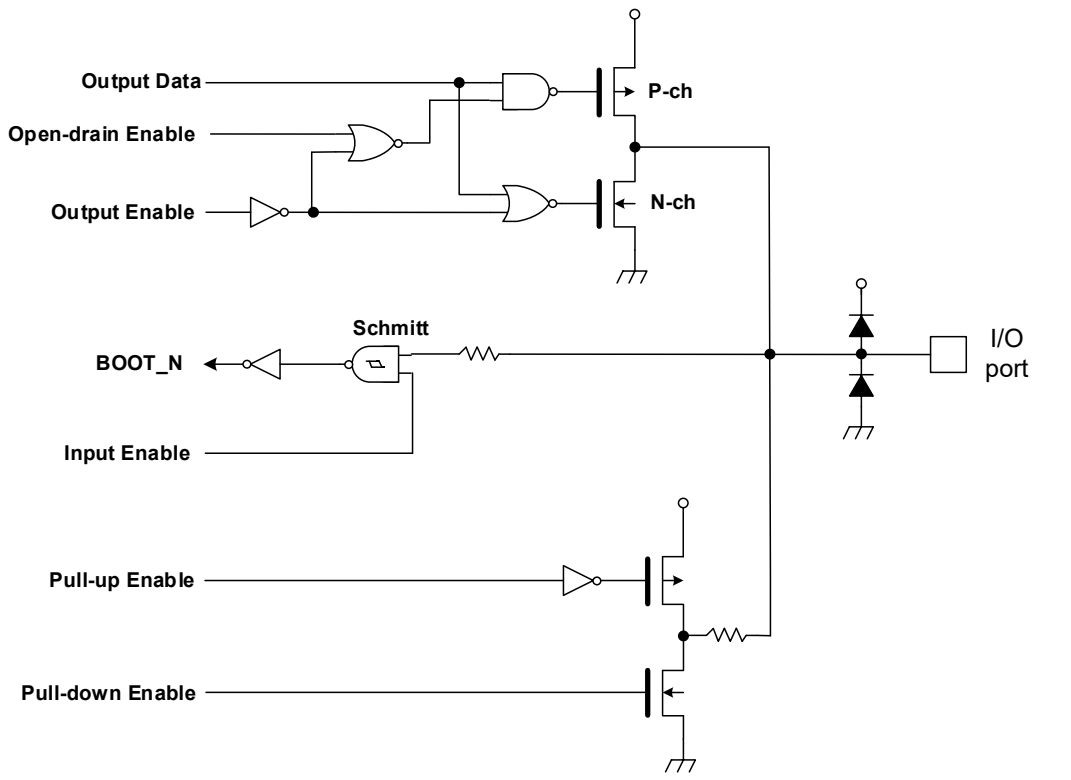
6.1. Port

PN0 to PN7, PP0 to PP5, PR0 to PR7	**(Programmable pull-up/pull-down, Programmable Open-drain output, Schmitt Input, Analog Input)** 

PP6, PP7	**(Programmable pull-up/pull-down, Programmable Open-drain output, Schmitt Input, Analog Input, External Interrupt input)** 
PT0, PT1	**(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input, Analog Output)** 

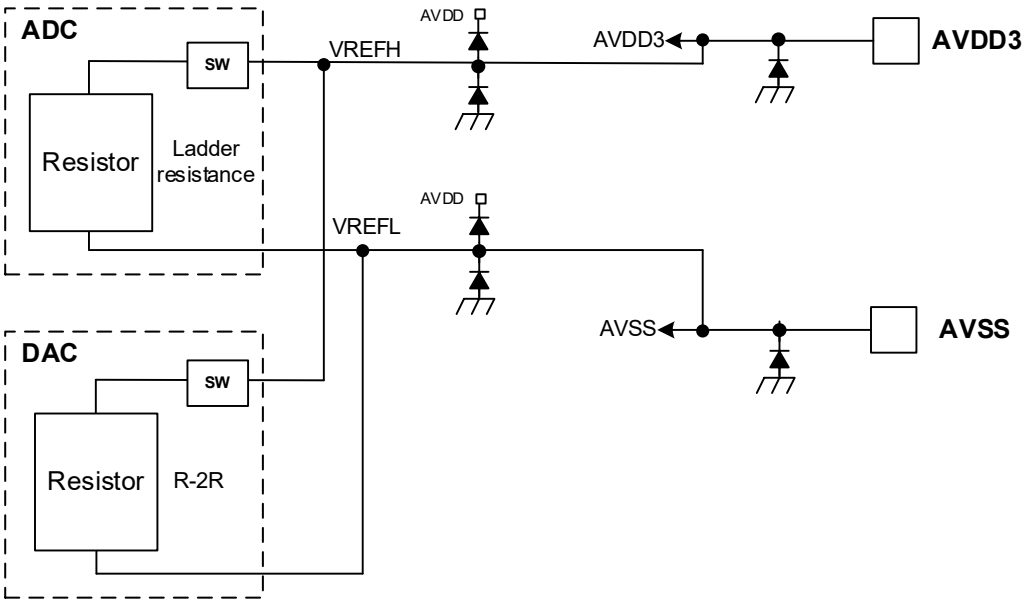
PA1 to PA6, PB2 to PB5, PC2 to PC5, PD0 to PD7, PE0 to PE7, PF1, PF4 to PF6, PG4 to PG7, PH0 to PH7, PJ0 to PJ7, PK2 to PK6, PL1 to PL3, PL7, PM0 to PM2, PM5 to PM7, PU0, PU1, PU6, PU7, PV0 to PV7, PW0 to PW7	**(Programmable Pull-up/Pill-down, Programmable Open-drain Output, Schmitt Input)** 
PA0, PA7, PB0, PB1, PB6, PB7, PC0, PC1, PC6, PC7, PF0, PF7, PG0, PG1, PK0, PK1, PK7, PL0, PL4 to PL6, PM3, PM4, PT3 to PT5, PU2 to PU5	**(Programmable Pull-up/Pill-down, Programmable Open-drain Output, Schmitt Input, External Interrupt Input)** 

PT2	**(3V-tolerant, Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input)** 
PF2, PF3, PG2, PG3	**(5V tolerant, Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input)** 

PY0 to PY3	
PY4/ BOOT_N	

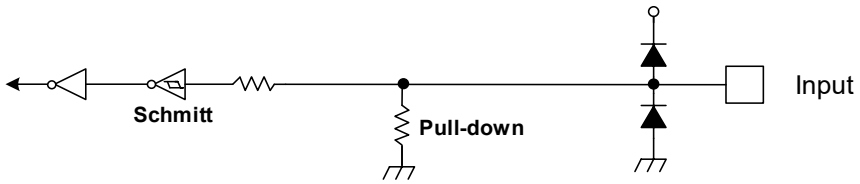
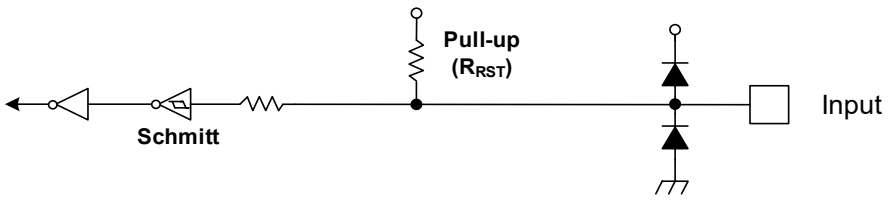
Note: Although, this port is input during pin reset period and POR period, it can be used for output port when use as port.

6.2. Analog Power pin

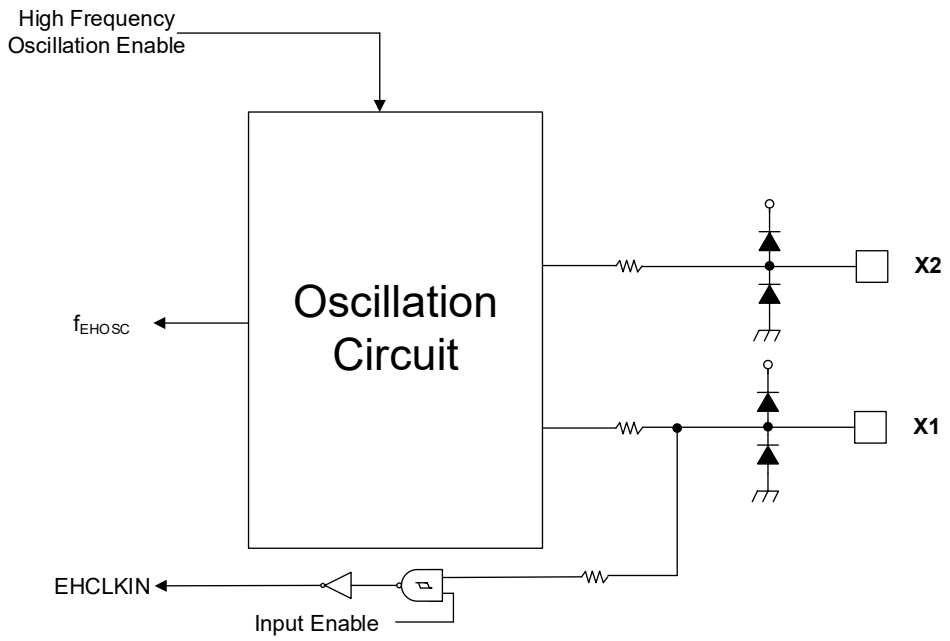
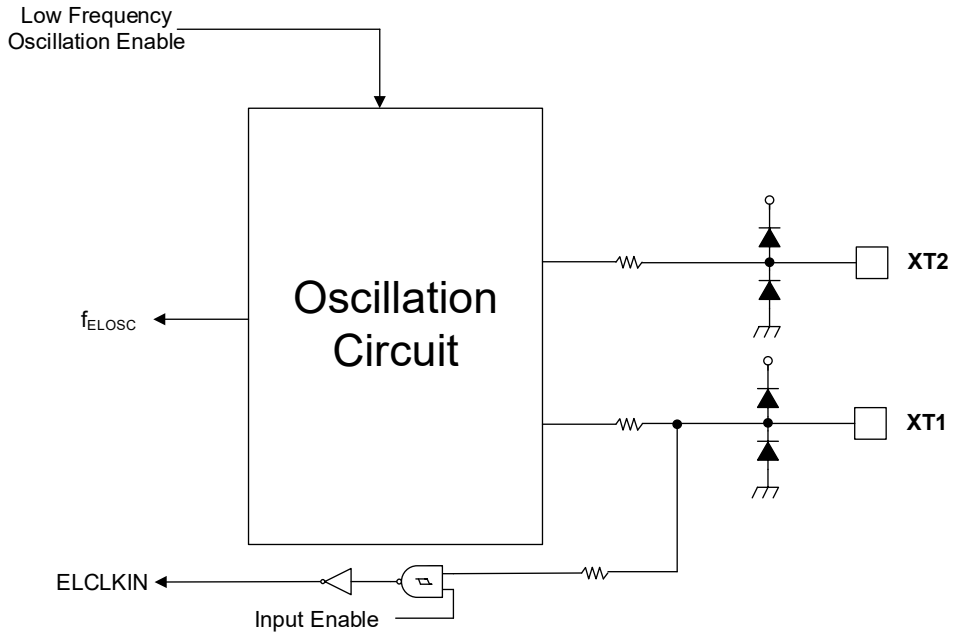
AVDD3, AVSS	

Note: SW: ON/OFF Switch Circuit

6.3. Control Pin

MODE, BSC	 **MODE pin must be connected to GND**
RESET_N	

6.4. Clock control

X1, X2	
XT1, XT2	

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

Table 7.1 Absolute maximum ratings

Parameter		Symbol	Rating	Unit
Power supply voltage		DVDD3A to DVDD3H	-0.3 to 3.9	V
		AVDD3	-0.3 to 3.9	
Input voltage	PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PF0, PF1, PF4 to PF7, PG0, PG1, PG4 to PG7, PH0 to PH7, PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7, PT3 to PT5, PU0 to PU7, PV0 to PV7, PW0 to PW7, PY0 to PY3, MODE, RESET_N, BOOT_N, BSC	V_{IN1}	-0.3 to DVDD3+0.3 (≤ 3.9V) (Note1)	V
	PN0 to PN7, PP0 to PP7, PR0 to PR7, PT0, PT1	V_{IN2}	-0.3 to AVDD3+0.3 (≤ 3.9V)	
	PF2, PF3, PG2, PG3	V_{IN3}	-0.3 to 5.5	
	PT2	V_{IN4}	-0.3 to 3.9	
Low level output current	PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PF0, PF1, PF4 to PF7, PG0, PG1, PG4 to PG7, PH0 to PH7, PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PN0 to PN7, PM0 to PM7, PP0 to PP7, PR0 to PR7, PT0 to PT5, PU0 to PU7, PV0 to PV7, PW0 to PW7, PY4	I_{OL1}	5	mA
	PF2, PF3, PG2, PG3	I_{OL2}	25	
	Total	ΣI_{OL}	50	
High level output current	PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PF0 to PF7, PG0 to PG7, PH0 to PH7, PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PN0 to PN7, PM0 to PM7, PP0 to PP7, PR0 to PR7, PT0 to PT5, PU0 to PU7, PV0 to PV7, PW0 to PW7, PY4	I_{OH1}	-5	
	Total	ΣI_{OH}	-50	
Power consumption (Ta= 85°C)		PD	600	mW
Soldering temperature		T_{SOLDER}	260	°C
Storage temperature		T_{STG}	-55 to 125	°C
Operating temperature	fsys ≤ 200MHz	T_{OPR1}	-40 to 85	°C

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

Note2: Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions. The equipment manufacturer should design so that no Absolute maximum rating value is exceeded with respect to current, voltage, power consumption, temperature, etc. Exposure to conditions beyond those listed above may cause permanent damage to the device or affect device reliability, which could increase potential risks of personal injury due to IC blow up and/or burning.

7.2. DC Electrical Characteristics (1/2)

DVDD3 = AVDD3 = 2.7V to 3.6V
DVSS = AVSS = 0V
Ta= -40 to 85°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Power supply voltage	DVDD3A to DVDD3H AVDD3	VDD	f_{OSC} = 8 to 24MHz f_{sys} =1 to 200MHz fs = 30 to 34kHz	2.7	-	3.6	V
Low level Input voltage	PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PF0, PF1, PF4 to PF7, PG0, PG1, PG4 to PG7, PH0 to PH7, PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7, PT3 to PT5, PU0 to PU7, PV0 to PV7, PW0 to PW7, PY0 to PY3, MODE, RESET_N, BOOT_N, BSC	V_{IL2}	-	-0.3	-	DVDD3×0.25	V
	PN0 to PN7, PP0 to PP7, PR0 to PR7, PT0, PT1	V_{IL3}	-			AVDD3×0.25	
	PF2, PF3, PG2, PG3, PT2	V_{IL4}	-			DVDD3×0.3	
High level Input voltage	PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PF0, PF1, PF4 to PF7, PG0, PG1, PG4 to PG7, PH0 to PH7, PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7, PT3 to PT5, PU0 to PU7, PV0 to PV7, PW0 to PW7, PY0 to PY3, MODE, RESET_N, BOOT_N, BSC	V_{IH2}	-	DVDD3×0.75	-	DVDD3+0.3	V
	PN0 to PN7, PP0 to PP7, PR0 to PR7, PT0, PT1	V_{IH3}	-	AVDD3×0.75		AVDD3+0.3	
	PF2, PF3, PG2, PG3, PT2	V_{IH4}	-	DVDD3×0.7		DVDD3+0.3	

DVDD3 = AVDD3 = 2.7V to 3.6V
DVSS = AVSS = 0V
Ta= -40 to 85°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Low level output voltage	PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PF0, PF1, PF4 to PF7, PG0, PG1, PG6, PG7, PH0 to PH7, PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7, PN0 to PN7, PP0 to PP7, PR0 to PR7, PT0 to PT2, PT4, PU0 to PU7, PV0 to PV7, PW0 to PW7, PY4	V_{OL1}	DVDD3=AVDD3=2.7V I_{OL} = 1.6mA	-	-	0.4	V
	PG4, PG5, PT3, PT5	V_{OL2}	DVDD3=2.7V I_{OL}=8mA	-	-	0.4	
	PF2, PF3, PG2, PG3	V_{OL3}	DVDD3=2.7V I_{OL}=12mA	-	-	1.0	
High level output voltage	PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PF0, PF1, PF4 to PF7, PG0, PG1, PG6, PG7, PH0 to PH7, PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7, PN0 to PN7, PP0 to PP7, PR0 to PR7, PT0 to PT2, PT4, PU0 to PU7, PV0 to PV7, PW0 to PW7, PY4	V_{OH1}	DVDD3=AVDD3=2.7V I_{OH} = -1.6mA	DVDD3-0.4 AVDD3-0.4	-	-	V
	PG4, PG5, PT3, PT5	V_{OH2}	DVDD3=2.7V I_{OH}= -8mA	DVDD3-0.4	-	-	
	PF2, PF3, PG2, PG3	V_{OH3}	DVDD3=2.7V I_{OH}= -1.0mA	DVDD3-0.4	-	-	

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.
Note2: Typ. value is in Ta = 25 °C, DVDD3 = AVDD3 = 3.3V, unless otherwise noted.
Note3: Apply same voltage to DVDD3 and AVDD3.

DVDD3=AVDD3=2.7V to 3.6V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Input leak current		I_{LI}	0V ≤ VIN ≤ DVDD3 0V ≤ VIN ≤ AVDD3	-	0.05	±5	μA
Output leak current		I_{LO}	0.2 ≤ VIN ≤ DVDD3-0.2 0.2 ≤ VIN ≤ AVDD3-0.2	-	0.05	±10	
Schmitt trigger Input width		VTH	-	-	0.8	-	V
Reset pull-up resistor		R_{RST}	-	25	45	100	kΩ
Programmable pull-up/pull-down resistor	Other than the following	P_{KH}	Pull-up	25	45	100	kΩ
			Pull-down	25	55	100	
	5V tolerant	P_{KH5}	Pull-up	40	70	150	
			Pull-down	40	70	150	
	3V tolerant	P_{KH3}	Pull-up	30	47	200	
			Pull-down	30	47	200	
Pin capacity (except power supply pin)		C_{IO}	fc =1MHz	-	-	10	pF
Low level output current	Per pin PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PF0, PF1, PF4 to PF7 PG0, PG1, PG6, PG7, PH0 to PH7, PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7, PN0 to PN7, PP0 to PP7, PR0 to PR7, PT0 to PT2, PT4, PU0 to PU7, PV0 to PV7, PW0 to PW7, PY4	I_{OL1}	DVDD3=3V AVDD3=3V	-	-	1.6	mA
	Per pin PG4, PG5, PT3, PT5	I_{OL2}	DVDD3=3V	-	-	8	
	Per pin PF2, PF3, PG2, PG3	I_{OL3}	DVDD3=3V	-	-	12	
	Total of PA0 to PA7, PB0 to PB7, PT3, PY4	ΣI_{OL1}	DVDD3=3V	-	-	35	
	Total of PD0 to PD7, PE0 to PE7, PJ4 to PJ7, PU0 to PU7	ΣI_{OL2}	DVDD3=3V	-	-	35	
	Total of PC0 to PC7, PF0 to PF7, PJ0 to PJ3, PL6, PL7, PT2	ΣI_{OL3}	DVDD3=3V	-	-	35	
	Total of PG4 to PG7, PH0 to PH7, PM4 to PM7, PV4 to PV7, PW0 to PW3, PT5	ΣI_{OL4}	DVDD3=3V	-	-	35	

	Total of PG0 to PG3, PK0 to PK7, PL0 to PL5, PM0 to PM3, PV0 to PV3, PW4 to PW7, PT4	ΣI_{OL5}	DVDD3=3V	-	-	35	
	Total of PN0 to PN7, PP0 to PP7, PR0 to PR7, PT0, PT1	ΣI_{OL6}	AVDD3=3V	-	-	35	
High level output current	per Pin PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PF0, PF1, PF4 to PF7, PG0, PG1, PG6, PG7 PH0 to PH7, PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7, PN0 to PN7, PP0 to PP7, PR0 to PR7, PT0 to PT2, PT4, PU0 to PU7, PV0 to PV7, PW0 to PW7, PY4	I_{OH1}	DVDD3=3V AVDD3=3V	-2.0	-	-	mA
	per Pin PG4, PG5, PT3, PT5	I_{OH2}	DVDD3=3V	-8	-	-	
	per Pin PF2, PF3, PG2, PG3	I_{OH3}	DVDD3=3V	-1.0	-	-	
	Total of PA0 to PA7, PB0 to PB7, PT3, PY4	ΣI_{OH1}	DVDD3=3V	-35	-	-	
	Total of PD0 to PD7, PE0 to PE7, PJ4 to PJ7, PU0 to PU7	ΣI_{OH2}	DVDD3=3V	-35	-	-	
	Total of PC0 to PC7, PF0 to PF7, PJ0 to PJ3, PL6, PL7, PT2	ΣI_{OH3}	DVDD3=3V	-35	-	-	
	Total of PG4 to PG7, PH0 to PH7, PM4 to PM7, PV4 to PV7, PW0 to PW3, PT5	ΣI_{OH4}	DVDD3=3V	-35	-	-	
	Total of PG0 to PG3, PK0 to PK7, PL0 to PL5, PM0 to PM3, PV0 to PV3, PW4 to PW7, PT4	ΣI_{OH5}	DVDD3=3V	-35	-	-	
	Total of PN0 to PN7, PP0 to PP7, PR0 to PR7, PT0, PT1	ΣI_{OH6}	AVDD3=3V	-35	-	-	

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.
Note2: Typ. value is in Ta = 25 °C, DVDD3 = AVDD3 = 3.3V, unless otherwise noted.
Note3: Apply same voltage to DVDD3 and AVDD3.

7.3. DC Electrical Characteristics (2/2) (Current consumption)

Ta= -40 to 85°C

Parameter	Symbol	Conditions				Min	Typ.	Max	Unit
		Supply voltage	High speed oscillator	Low speed oscillator	Operating condition				
Normal	I_{DD}	DVDD3= AVDD3= 3.6V	Refer to the "Table 7.2" and "Table 7.3" for measuring condition			-	40	120	mA
			Oscillation	Stop	CPU only	-	25	90	
IDLE			Refer to "Table 7.2" and "Table 7.3" for measuring condition			-	8	75	
STOP1			Stop	Oscillation	Refer to "Table 7.2" and "Table 7.3" for measuring condition	-	2	70	
STOP2						-	7	160	µA
				Stop		-	6	160	

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H
Note2: Typ. value is in Ta=25 °C, DVDD3=AVDD3=3.3V, unless otherwise noted.
Note3: Apply same voltage to DVDD3 and AVDD3.
Note4: Input pin is fixed level, Output pin is open.

Table 7.2 IDD measuring condition (Pin setting, Oscillation Circuit)

		NORMAL	IDLE	STOP1	STOP2
				LOSC run	LOSC stop
Pin setting	DVDD3= AVDD3=	3.3V(Typ.), 3.6V(max)			
	X1,X2	Oscillator connected (10MHz)			
	XT1,XT2	Oscillator connected (32.768kHz)			
	Input pins	Fixed			
	Output pins	Open			
Operating condition (Oscillation Circuit)	System clock (fsys)	High speed 200MHz Middle speed 100MHz		Stop	
	External High speed oscillator (EHOSC)	Oscillation		Stop	
	Internal High speed oscillator 1 (IHOSC1)	Stop			
	PLL	run(20 times)		Stop	
	External Low speed oscillator (ELOSC)	Oscillation			Stop

Table 7.3 IDD measuringt condition (CPU, Peripheral)

Peripheral	Number of built-in circuits	NORMAL	IDLE	STOP1	STOP2	
				LOSC run	LOSC run RTC, RMC run	LOSC stop
CPU	1	Run (Dhrystone Ver.2.1)	Stop			
HDMAC	2	Unit A (software startup of ch1, memory to memory transmission) / Unit B (software startup of ch0,memory to peripheral (EBIF) transmission)	Stop			
MDMAC	1	Unit A (software startup, memory to memory transmission)	Stop			
ADC	1	Run (1.15μs, Repeated conversion)	Stop			
DAC	2	Run	Stop			
EBIF	1	Run (Asynchronous separate mode, Internal 4 wait access)	Stop			
T32A	14	All Ch: Run	Stop			
A-PMD	1	Run	Stop			
A-ENC	1	Run	Stop			
RTC	1	Run	Run			Stop
SIWDT	1	Run	Stop			
UART	6	Data Transmission (5Mbps)	Stop			
FUART	2	Data Transmission (2.5Mbps)	Stop			
I2C/EI2C	5	Run only clock (fprsck = 5MHz)	Stop			
TSPI	9	Transfer Clock ch0 to ch3: 25MHz ch4 to ch8: 10MHz	Stop			
TSSI	2	Data Transmission (10MHz)	Stop			
I2S	2	Data Transmission (12.288MHz)	Stop			
SMIF	1	Run	Stop			
ISD	3	Run	Run		Stop	
LTTMR	1	Run	Stop			
CEC	1	Run, Transmission	Stop (supply only clock)	Stop		
RMC	2	Run	Run			Stop
LVD	1	Stop	Stop			
OFD	1	Run (OFD reset output disable)	Stop			
PORT	-	Stop	Stop			

fsysm=100MHz
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Current consumption (ADC and DAC run)	I_{AVDD}	AVDD3=3.3V	-	1.0	2.0	mA

7.4. 12-bit AD Converter Characteristics

DVDD3 = AVDD3 = 2.7V to 3.6V
DVSS = AVSS = 0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog reference voltage (+)	VREFH (AVDD3)	-	-	AVDD3	-	V
Analog input voltage	VAIN	-	AVSS (VREFL)	-	AVDD3 (VREFH)	V
Integral nonlinearity error (INL)	-	2.7V ≤ AVDD3 ≤ 3.6V AIN load resistor ≤ 600Ω AIN load capacity ≥ 0.1μF Conversion time ≥ 1.0μs	-6	-	+6	LSB
Differential nonlinearity error (DNL)			-5	-	+5	
Zero-scale error			-6	-	+6	
Full-scale error			-6	-	+6	
Total errors			-7	-	+7	
Stable time	t_{sta}	***[ADAMOD0]***<DACON>= 1 is set	3	-	-	μs
Conversion time	t_{conv}	2.7V ≤ AVDD3 ≤ 3.6V	1.0	-	5.0	μs

7.5. 8-bit DA Converter Characteristics

DVDD3 = AVDD3 = 2.7V to 3.6V
DVSS = AVSS = 0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog reference voltage(+)	VREFH (AVDD3)	-	-	AVDD3	-	V
Integral nonlinearity error(INL)	-	2.7V ≤ AVDD3 ≤ 3.6V Rload= 10MΩ	-2	-	+2	LSB
Differential nonlinearity error(DNL)			-1	-	+1	
Total errors			-2	-	+2	
Stable time	t_{sta}	Cload = 20pF	4.5	-	-	μs

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.
Note2: Typ. value is in Ta=25 °C, DVDD3=AVDD3=3.3V, unless otherwise noted.
Note3: 1LSB = (AVDD3 (VREFH) - AVSS (VREFL)) / 256 [V]
Note4: This is the characteristic in case only DA converter is operating.

7.6. Characteristics of Internal processing at RESET

DVSS = AVSS = 0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Internal initialization time	t_{IINIT}	Power-on	-	-	1.0	ms
Internal processing time for Reset	t_{IRST}	STOP2 released by RESET with RESET_N or LVD.	-	-	0.8	
		STOP2 released by Interrupt	-	-	0.5	
		Reset operation except STOP2 releasing	0.15	-	0.8	
Waiting time till CPU running (Note)	t_{CPUWT}	Power-on Reset operation by LVD in STOP1 or STOP2 mode Reset operation by RESET_N pin in STOP1 or STOP2 mode	10	-	20	µs
		Reset operation by LVD in NORMAL or IDLE mode Reset operation by RESET_N pin in NORMAL or IDLE mode Reset operation by WDT, OFD, LOCKUP, or SYSRESET in NORMAL or IDLE mode	150	-	165	
Power gradient	V_{PON}	Rising slope	1.33	-	100	mV/µs
	V_{POFF}	Falling slope	-	-	5	

Note: Except reset operation by WDT, OFD, LOCKUP, or SYSRESET, when reset factor repeats, t_{CPUWT} (Waiting time till CPU running) starts measuring elapse time after releasing this factor.

7.7. Characteristics of Power on Reset

DVSS = AVSS = 0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{PREL}	Power-up	2.22	2.33	2.44	V
	V_{PRED}	Power-down	2.17	2.28	2.39	
Detection pulse width	T_{PDET}	-	30	-	-	µs

7.8. Characteristics of PORF

DVSS = AVSS = 0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{PORFL}	Power-up	2.55	2.61	2.67	V
	V_{PORFD}	Power-down	2.50	2.56	2.62	
Detection pulse width	T_{PDET}	-	50	-	-	µs

7.9. Characteristics of Voltage Detection Circuit

DVDD3 = AVDD3 = 2.7V to 3.6V
DVSS = AVSS = 0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{LVL0}	Power-up (releasing)	2.58	2.64	2.70	V
		Power-down (detecting)	2.53	2.59	2.65	
	V_{LVL1}	Power-up (releasing)	2.63	2.69	2.75	V
		Power-down (detecting)	2.58	2.64	2.70	
	V_{LVL2}	Power-up (releasing)	2.69	2.75	2.81	V
		Power-down (detecting)	2.64	2.7	2.76	
	V_{LVL3}	Power-up (releasing)	2.79	2.85	2.91	V
		Power-down (detecting)	2.74	2.8	2.86	
	V_{LVL4}	Power-up (releasing)	2.89	2.95	3.01	V
		Power-down (detecting)	2.84	2.9	2.96	
	V_{LVL5}	Power-up (releasing)	2.99	3.05	3.11	V
		Power-down (detecting)	2.94	3.0	3.06	
	V_{LVL6}	Power-up (releasing)	3.09	3.15	3.21	V
		Power-down (detecting)	3.04	3.1	3.16	
Detection response time	t_{VDDT1}	Power-down	-	-	200	μs
Detection release time	t_{VDDT2}	Power-up	-	-	250	
setup time	t_{LVDEN}	-	-	-	100	
Detection Minimum pulse width	t_{LVDPW}	-	200	-	-	

7.10. AC Electrical Characteristics

7.10.1. Serial Peripheral Interface (TSPI)

7.10.1.1. Conditions

The conditions for AC characteristics are as follows:

- DVDD3=AVDD3=2.7V to 3.6V
- Ta = -40 to 85°C (fsys ≤ 200MHz)
- Output level: High = 0.8×DVDD3, Low = 0.2×DVDD3
- Input level: High = 0.75×DVDD3, Low = 0.25×DVDD3
- Load capacity: CL = 30pF

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.10.1.2. AC Electrical Characteristics

"T" indicates an operation clock cycle of the TSPI. This operation clock has the same cycle of the system clock (fsys). This cycle depends on the clock gear setting.

The number of cycles can be 1 to 16. It is specified with TSPIxSCK. The value of k1 is specified with ***[TSPIxFMTR0]***<CSSCKDL[3:0]>; the value of k2 is specified with ***[TSPIxFMTR0]***<SCKCSDL[3:0]>. These values are 1 to 16.

(1) Master mode

k1=k2=1

Parameter	Symbol	Equation		fsysh = 100MHz (Note2) ch0 to 3		fsys = 80MHz (Note3) ch4 to 8		Unit
		Min	Max	Min	Max	Min	Max	
TSPIxSCK output frequency (Note1)	f_{CYC}	-	ch0 to 3: 25	-	25	-	-	MHz
			ch4 to 8: 10	-	-	-	10	
TSPIxSCK output cycle	t_{CYC}	-	-	40	-	100	-	ns
TSPIxSCK low level output pulse width	t_{WL}	ch0 to 3: (t_{CYC}/2)-11	-	9	-	-	-	
		ch4 to 8: (t_{CYC}/2)-12		-	-	38	-	
TSPIxSCK high level output pulse width	t_{WH}	ch0 to 3: (t_{CYC}/2)-11	-	9	-	-	-	
		ch4 to 8: (t_{CYC}/2)-12		-	-	38	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSUM}	ch0 to 2: (t_{CYC}×k1)-15	ch0 to 3: (t_{CYC}×k1)+15	25	55	-	-	
		ch3: (t_{CYC}×k1)-18		22	55			
		ch4 to 8: (t_{CYC}×k1)-15	ch4 to 8: (t_{CYC}×k1)+13	-	-	85	113	
TSPIxSCK rise/fall time → TSPIxCSn hold time	t_{CHD}	ch0 to 3: (t_{CYC}×(k2+0.5)-15	-	45	-	-	-	
		ch4 to 8: (t_{CYC}×(k2+0.5)-15		-	-	135	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	ch0 to 3: 23-Ndly×T	-	3	-	-	-	
		ch4 to 8: 30- Ndly×T		-	-	5	-	
TSPIxSCK rise/fall time → TSPIxRXD hold time	t_{DHD}	Ndly×T (Note4)	-	20	-	25	-	
TSPIxSCK rise/fall time → TSPIxTXD hold time	t_{ODLY1}	ch0 to 3: -7	-	-7	-	-	-	
		ch4 to 8: -10		-	-	-10	-	
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY2}	-	ch0 to 3: 7	-	7	-	-	
			ch4 to 8: 13	-	-	-	13	
TSPIxCSIN fall → TSPIxTXD delay time	t_{ODLY3}	ch0 to 3: (t_{CYC}×(k1-0.5))-20	(t_{CYC}×(k1-0.5))+9	0	29	-	-	
		ch4 to 8: (t_{CYC}×(k1-0.5))-50		-	-	0	59	

Note1: The output frequency is determined by the setting value of ***[TSPIxBR]***<BRCK><BRS>. Please set the output frequency within the range not exceeding the Max value of the Equation.

Note2: Although the maximum frequency of fsysh is 200MHz, it is described as an example of fsysh = 100MHz so as to show of outputting the maximum frequency (25 MHz) of TSPIxSCK

Note3: ch4 and ch5 is shown fsysh(200MHz maximum), and ch6 to ch8 is shown fsysm(100MHz maximum).

Note4: Ndly has a value of ***[TSPIxCR2]***<RXDLY[2:0]> + 1. In this example, Ndly = 2.

(2) Slave mode

Parameter	Symbol	Equation		fsysh = 100MHz ch0 to 3		fsys = 80MHz (Note) ch4 to 8		Unit
		Min	Max	Min	Max	Min	Max	
TSPIxSCK Input frequency	f_{CYC}	-	ch0 to 3: 20	-	20	-	-	MHz
			ch4 to 8: 10	-	-	-	10	
TSPIxSCK Input cycle	t_{CYC}	$1/f_{CYC}$	-	50	-	100	-	ns
TSPIxSCK low level Input pulse width	t_{WL}	ch0 to 3: 15	-	15	-	-	-	
		ch4 to 8: 40		-	-	40	-	
TSPIxSCK High level Input pulse width	t_{WH}	ch0 to 3: 15	-	15	-	-	-	
		ch4 to 8: 40		-	-	40	-	
TSPIxCSIN Input ← TSPIxSCK rise/fall time	t_{CSU1}	ch0 to 3: 40	-	40	-	-	-	
		ch4 to 8: 90		-	-	90	-	
TSPIxCSIN Input ← TSPIxSCK rise/fall time	t_{CSU2}	ch0 to 3: 40	-	40	-	-	-	
		ch4 to 8: 90		-	-	90	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time	t_{CHD}	ch0 to 3: 40	-	40	-	-	-	
		ch4 to 8: 90		-	-	90	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	ch0 to 3: 3	-	3	-	-	-	
		ch4 to 8: 16		-	-	16	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	ch0 to 3: 8	-	8	-	-	-	
		ch4 to 8: 6		-	-	6	-	
TSPIxSCK rise/fall → TSPIxTXD hold time	t_{ODLY1}	2	-	2	-	2	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	ch0 to 3: 25	-	-	25	-	-	
		ch4 to 8: 35		-	-	-	35	
TSPIxCSIN fall → TSPIxTXD delay time	t_{ODLY3}	ch0 to 3: 25	-	-	25	-	-	
		ch4 to 8: 38		-	-	-	38	
TSPIxCSIN high level input pulse width (1st)	t_{WDIS}	T×5+10	-	60	-	73	-	
TSPIxCSIN high level input pulse width (2nd)	t_{WDIS}	T×2+10	-	30	-	35	-	

Note: ch4 and ch5 is shown fsysh(200MHz maximum), and ch6 to ch8 is shown fsysm(100MHz maximum).

(1) 1st clock edge sampling (Master)

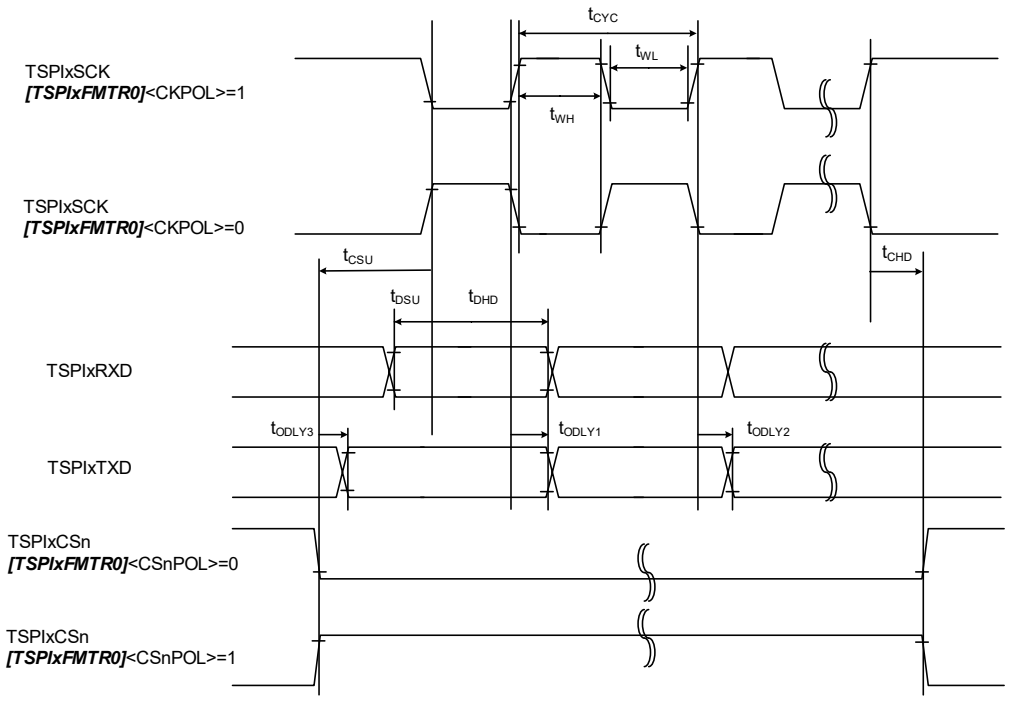


Figure 7.1 1st clock edge sampling (Master)

(2) 2nd clock edge sampling (Master)

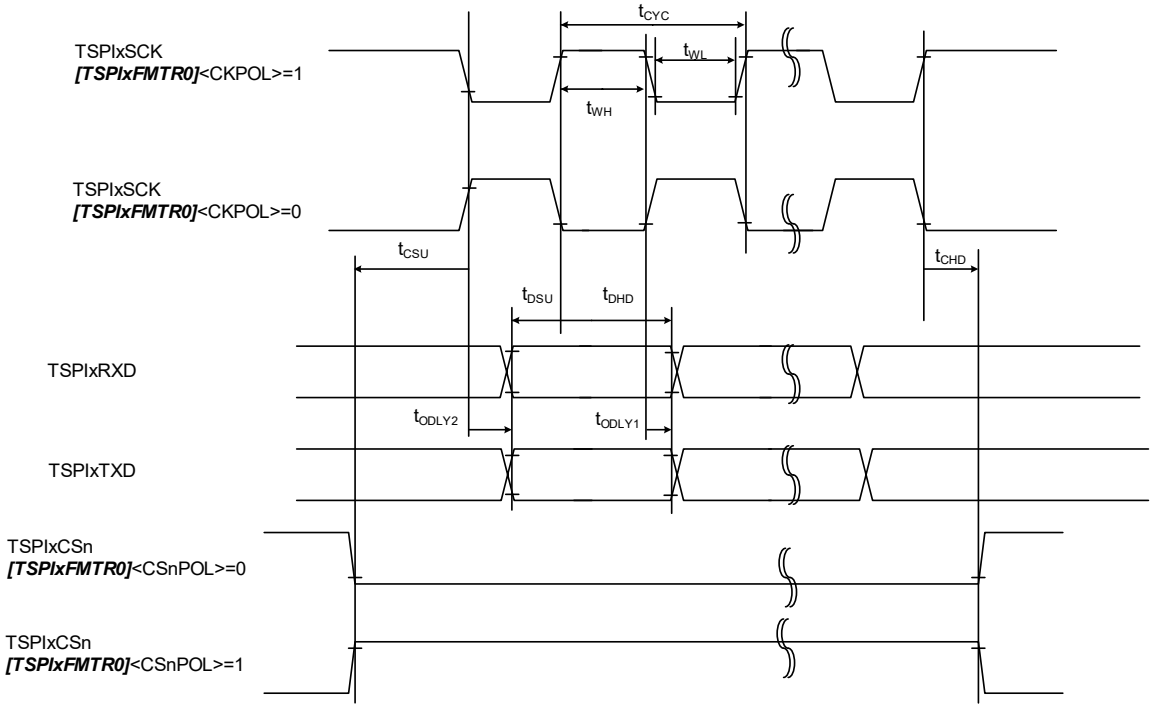


Figure 7.2 2nd clock edge sampling (Master)

(3) 1st clock edge sampling (Slave)

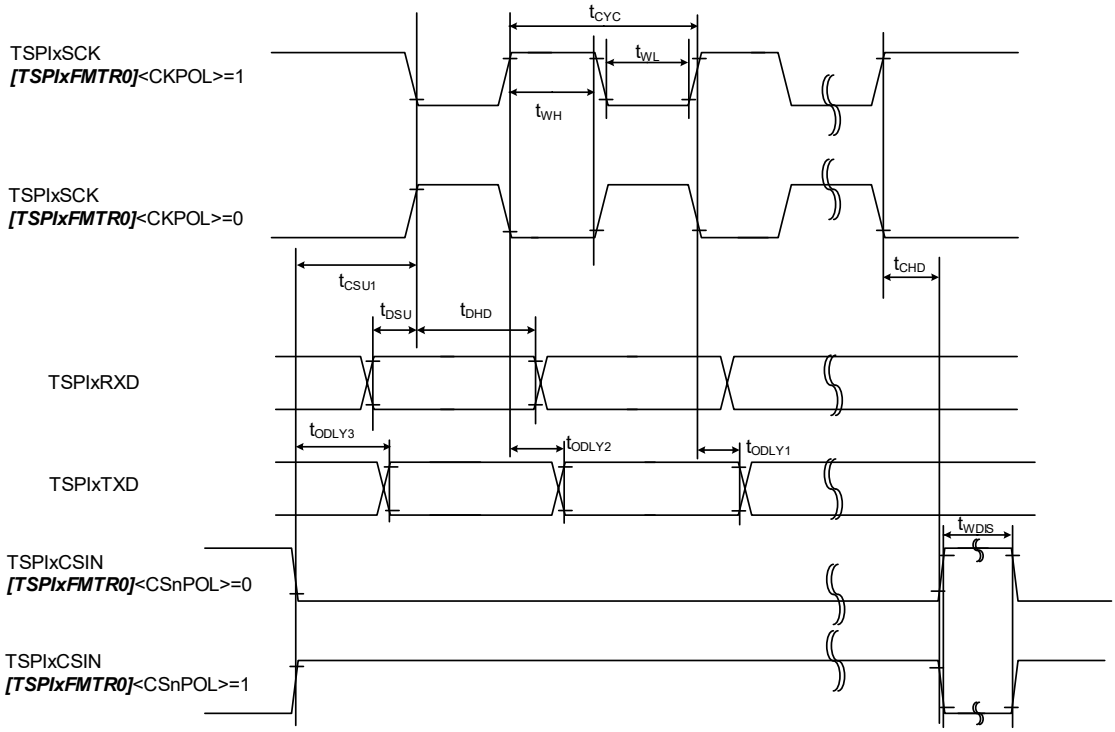


Figure 7.3 1st clock edge sampling (Slave)

(4) 2nd clock edge sampling (Slave)

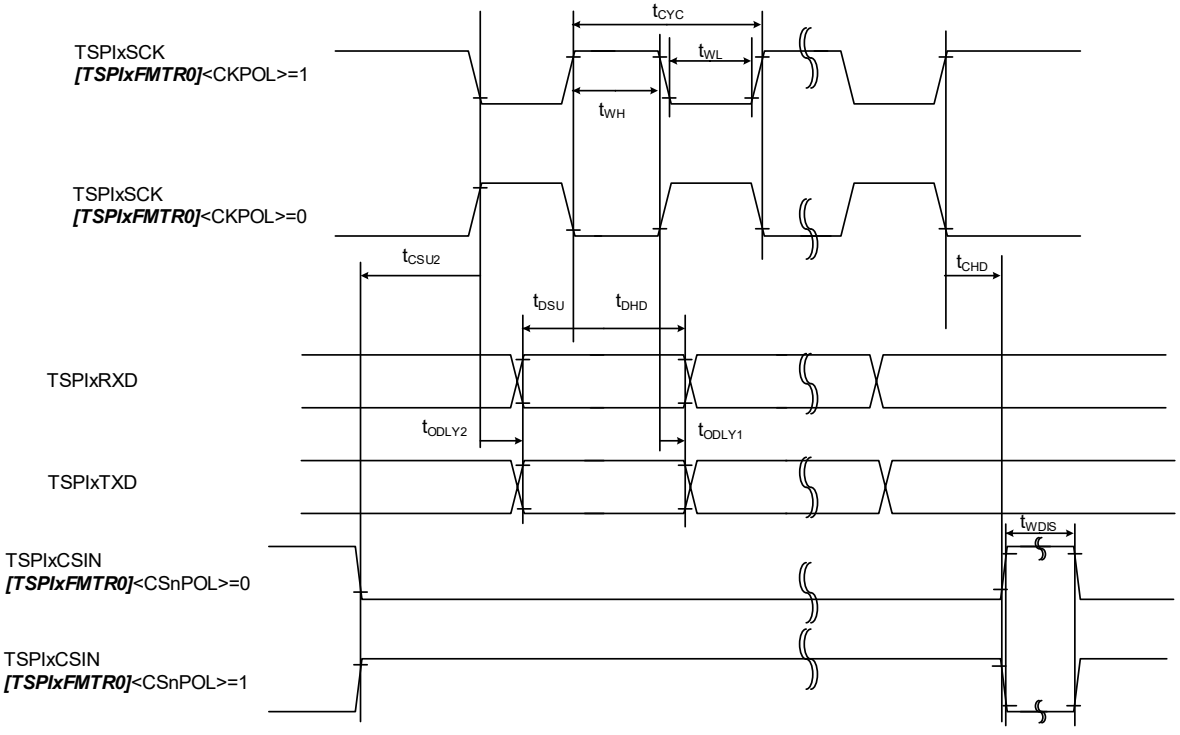


Figure 7.4 2nd clock edge sampling (Slave)

7.10.2. I²C Interface (I2C)

7.10.2.1. Conditions

The conditions for AC characteristics are as follows:

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C
- Output level: Low = 0.4V
- Input level: High = 0.7×DVDD3, Low = 0.3×DVDD3
- Load capacity: CL = 30pF
- External pull-up resistor: R_p = 2.2 kΩ

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.10.2.2. AC Electrical Characteristics

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Start condition hold time	$t_{HD;STA}$	4.0	-	0.6	-	μs
SCL clock Low width (Input) (Note1)	t_{LOW}	4.7	-	1.3	-	
SCL clock High width (Input) (Note1)	t_{HIGH}	4.0	-	0.6	-	
Re-start condition setup time (Note3)	$t_{SU;STA}$	4.7	-	0.6	-	
Data hold time (Input) (Note2)	$t_{HD;DAT}$	0	-	0	-	
Data setup time	$t_{SU;DAT}$	250	-	100	-	ns
Stop condition setup time	$t_{SU;STO}$	4.0	-	0.6	-	μs
Bus free time between stop condition and start condition (Note3)	t_{BUF}	4.7	-	1.3	-	

Note1: On I²C bus standard, the maximum speed of Standard mode/Fast mode is 100 kHz/400 kHz respectively. For the setting of the internal SCL clock frequency, refer to the calculation formula in Chapter 3.3.2 of the reference manual "I²C Interface".

Note2: On I²C bus standard, it is described that a data internal hold time should be set at least 300 ns to avoid unstable condition on the falling of the SCL when the SDA is input; however, this precaution is not supported in this MCU. Also, the edge slope control function for the SCL is not available. Therefore, when the customer designs the MCU, make sure to follow the data hold time (input) in the table above. Note that tr/tf on the SCL/SDA should be included in the data hold time.

Note3: Depends on software.

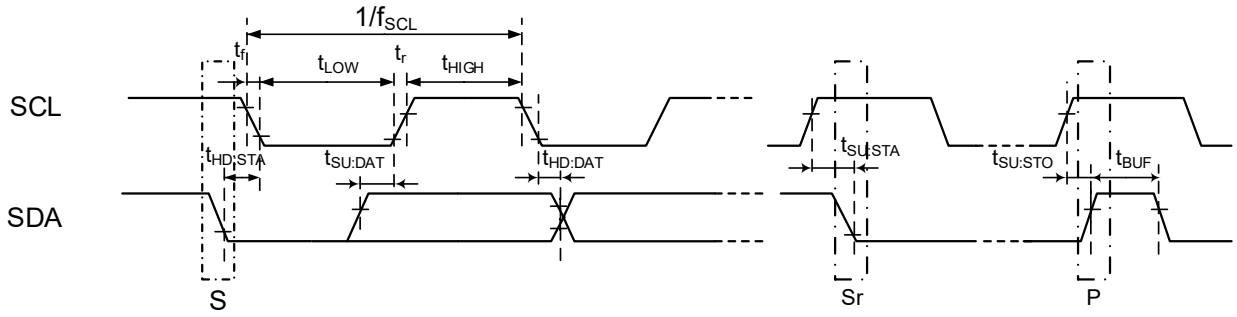


Figure 7.5 AC timing of I²C Interface

7.10.3. I²C Interface Version A (EI2C)

7.10.3.1. Conditions

The conditions for AC characteristics are as follows:

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C
- Output level: Low = 0.4V
- Input level: High = 0.7×DVDD3, Low = 0.3×DVDD3
- Load capacity: CL = 30pF
- External pull-up resistor: R_p = 2.2 kΩ

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.10.3.2. AC Electrical Characteristic

Parameter	記号	Standard mode		Fast mode		Fast mode Plus (ch0, 1 のみ)		Unit
		Min	Max	Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	0	1000	kHz
Start condition hold time	$t_{HD;STA}$	4.0	-	0.6	-	0.26	-	μs
SCL clock Low width (Input) (Note1)	t_{LOW}	4.7	-	1.3	-	0.5	-	
SCL clock High width (Input) (Note1)	t_{HIGH}	4.0	-	0.6	-	0.26	-	
Re-start condition setup time (Note3)	$t_{SU;STA}$	4.7	-	0.6	-	0.26	-	
Data hold time (Input) (Note2)	$t_{HD;DAT}$	0	-	0	-	0	-	
Data setup time	$t_{SU;DAT}$	250	-	100	-	50	-	ns
Stop condition setup time	$t_{SU;STO}$	4.0	-	0.6	-	0.26	-	μs
Bus free time between stop condition and start condition (Note3)	t_{BUF}	4.7	-	1.3	-	0.5	-	

Note1: On I²C bus standard, the maximum speed of Standard mode/Fast mode/Fast mode Plus is 100 kHz/400 kHz/1 MHz, respectively. For the setting of the internal SCL clock frequency, refer to the calculation formula in Chapter 3.3.1 of the reference manual "I²C Interface Version A".

Note2: On I²C bus standard, it is described that a data internal hold time should be set at least 300 ns to avoid unstable condition on the falling of the SCL when the SDA is input; however, this precaution is not supported in this MCU. Also, the edge slope control function for the SCL is not available. Therefore, when the customer designs the MCU, make sure to follow the data hold time (input) in the table above. Note that tr/tf on the SCL/SDA should be included in the data hold time.

Note3: Depends on software.

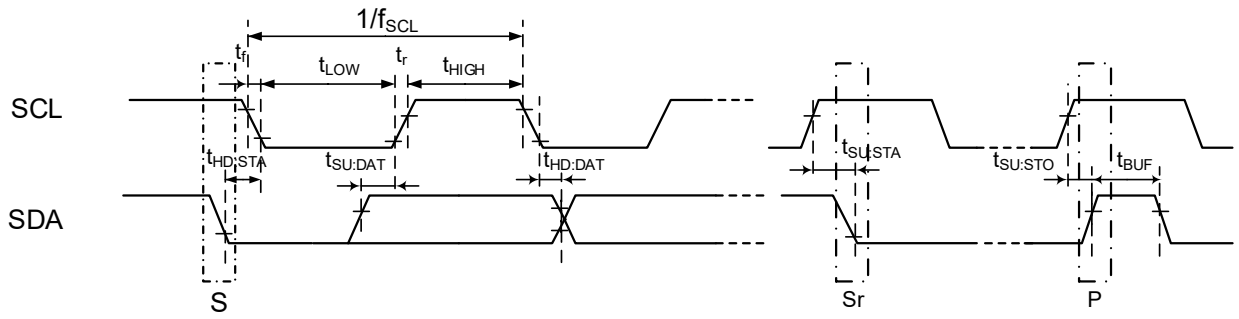


Figure 7.6 AC timing of I²C Interface Version A

7.10.4. 32-bit Timer Event Counter (T32A)

This section describes AC characteristics of T32AxINA0/A1, T32AxINB0/B1, and T32AxINC0/C1.

7.10.4.1. Conditions

The conditions for AC characteristics are as follows:

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C
- Input level: High = 0.75×DVDD3, Low = 0.25×DVDD3
- Load capacity: CL = 30pF

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.10.4.2. AC Characteristics

"T" in the table below indicates the operation clock cycle of the T32A. The operation clock of the T32A is the same cycle as the ΦT0m clock. This cycle depends on the Prescaler Clock setting.

(1) Operation other than the pulse count

Parameter	Symbol	Equation		ΦT0m=100MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{VCKL}	2T + 20	-	40	-	ns
High level pulse width	t_{VCKH}	2T + 20	-	40	-	

(2) At the pulse count

Parameter	Symbol	Equation		ΦT0m =100MHz		Unit
		Min	Max	Min	Max	
Pulse cycle	t_{DCYC}	1000	-	1000	-	ns
Low level pulse width	t_{PWL}	500	-	500	-	
High level pulse width	t_{PWH}	500	-	500	-	
Input setup	t_{ABS}	(NF+1)×T+20	-	30	-	
Input hold	t_{ABH}	(NF+1)×T+20	-	30	-	

NF Value depends on the ***[T32AxPLSCR]***<NF[1:0]> setting as following.

[T32AxPLSCR]<NF[1:0]>	NF Value of Formula
00	0
01	2
10	4
11	8

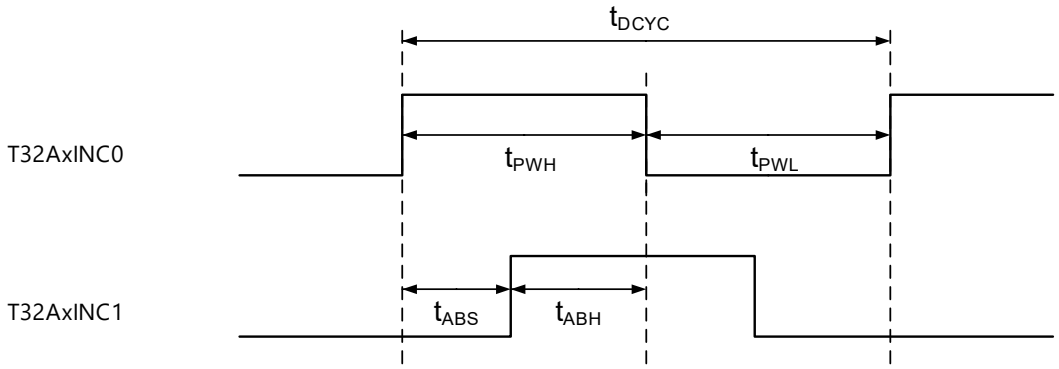


Figure 7.7 Count Pulse input

7.10.5. External Bus Interface(EBIF)

7.10.5.1. Conditions

The conditions for AC characteristics are as follows:

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C (fsys ≤ 200MHz)
- Output level: High = 0.8×DVDD3, Low = 0.2×DVDD3
- Input level: High = 0.75×DVDD3, Low = 0.25×DVDD3
- Load capacity: CL = 30pF

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.10.5.2. Variable Condition

- RWS: Number of setup cycle insertion before RD, WR asserted.: RWS = 0, 1, 2, 4
- TW: Number of internal wait insertion: TW = 0 to 15
- TWEX: Number of external wait insertion: TWEX = any
- RWH: Number of RD, WR recovery cycle insertion: RWH = 0 to 6 or 8
- CSH: Number of ECSx_N recovery cycle insertion: CSH = 0, 1, 2, 4

7.10.5.3. AC Electrical Characteristics (EEXBCLK asynchronous Separate Mode)

Variable Condition: fsysh = 100MHz RWS = 4, TW = 3, TWEX = 4, RWH = 4, CSH =1
fsysh = 200MHz RWS = 4, TW = 3, TWEX = 4, RWH = 4, CSH =2

Parameter	Symbol	Equation		fsysh = 100MHz		fsysh = 200MHz		Unit
		Min	Max	Min	Max	Min	Max	
System clock cycle (T)	t_{SYS}	T	–	10	-	5	-	ns
EA[0:23] valid → ERD_N, EWR_N fall	t_{AC}	T (1+RWS)−25	–	25	-	0	-	
ERD_N, EWR_N rise → EA[0:23] hold	t_{CAR}	T (1+RWH+CSH)−30	–	30	-	5	-	
EA[0:23] valid → ED[0:15] input	t_{AD}	–	T (2+RWS+TW+TWEX)−40	-	90	-	25	
ERD_N fall → ED[0:15] input	t_{RD}	–	T (1+TW+TWEX)−40	-	40	-	0	
ERD_N Low level pulse width	t_{RR}	T (1+TW+TWEX)−20	–	60	-	20	-	
ERD_N rise → ED[0:15] hold	t_{HR}	0	–	0	-	0	-	
ERD_N rise → EA[0:23] output	t_{RAE}	T (1+RWH+CSH)−30	–	30	-	5	-	
EWR_N Low level pulse width	t_{WW}	T (1+TW+TWEX)−20	–	60	-	20	-	
ED[0:15] valid → EWR_N rise	t_{DW}	T (1+TW+TWEX)−25	–	55	-	15	-	
EWR_N rise → ED[0:15] hold	t_{WD}	T (1+RWH)−30	–	20	-	-5	-	
ERD_N/EWR_N fall → EWAIT_N fall	t_{RWW}	–	T (TW)−40	-	-10	-	-25	
EWAIT_N rise → ERD_N/EWR_N rise	t_{WRW}	–	4T + 30	-	70	-	50	

1. Read cycle (minimum bus cycle)
(Neither Cycle expander, RD setup, Internal wait, CS recovery nor RD recovery are used)

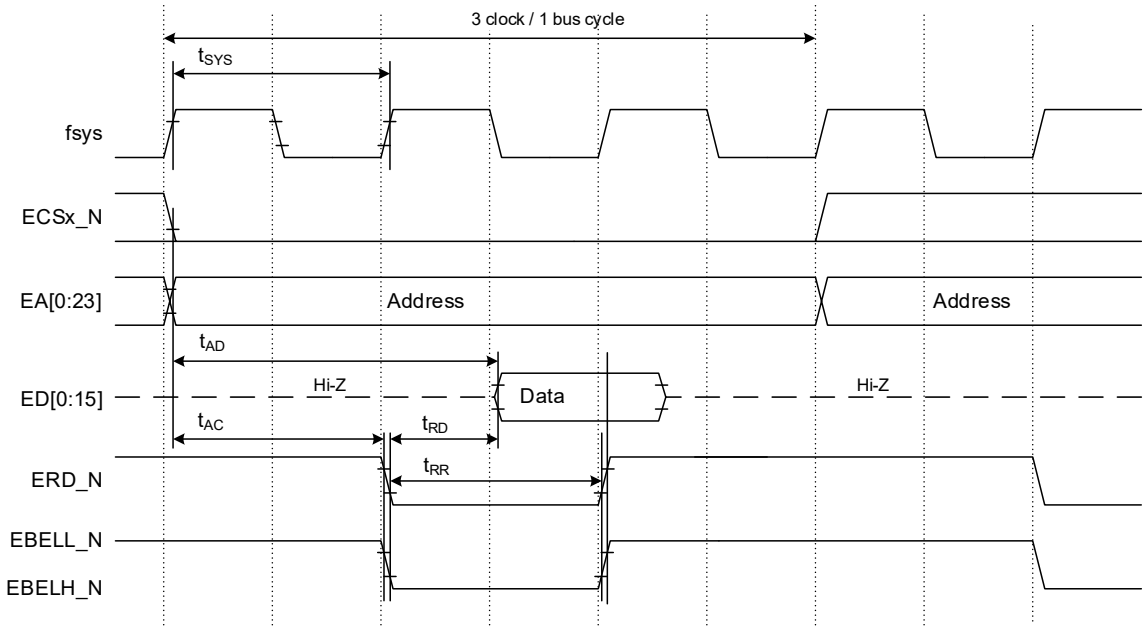


Figure 7.8 Read cycle timing (minimum bus cycle)

2. Read cycle (6 clock per 1 bus cycle)
(Cycle expander is not used, RD setup=1 cycle, Internal wait=1 cycle, CS recovery=1 cycle, RD recovery=1 cycle)

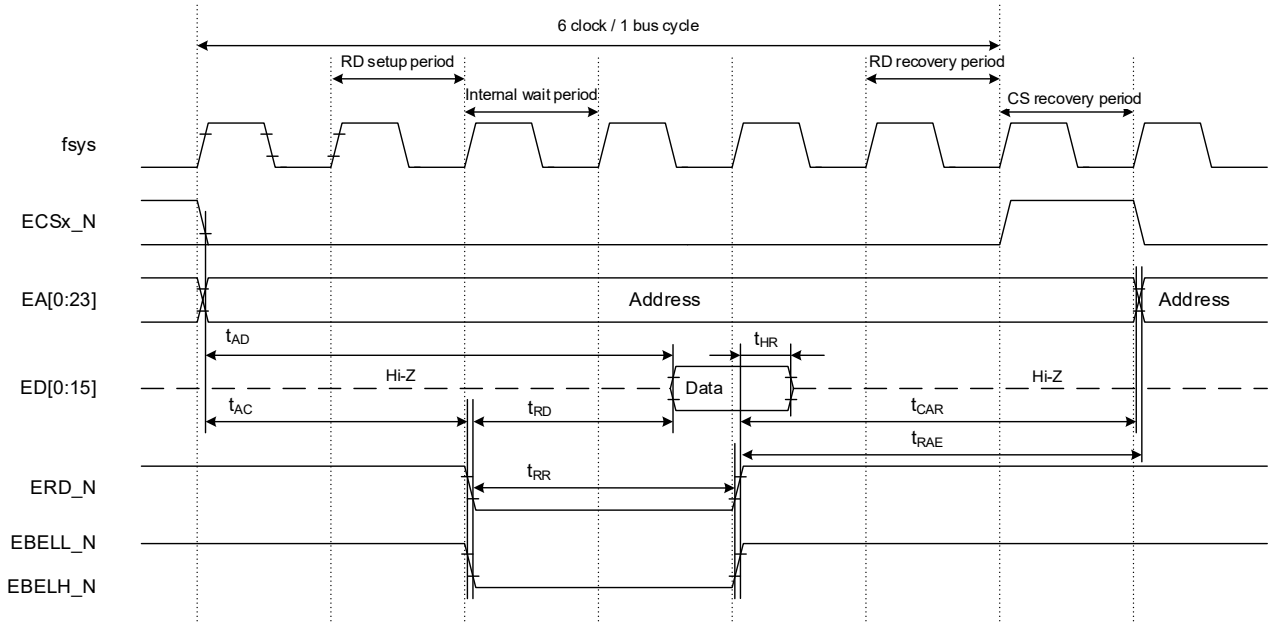


Figure 7.9 Read cycle timing (6 clock per 1 bus cycle)

3. Read cycle (external wait)
(Cycle expander is not used, RD setup=1 cycle, Internal wait=3 cycles, External wait=any, CS recovery=1 cycle, RD recovery=1 cycle)

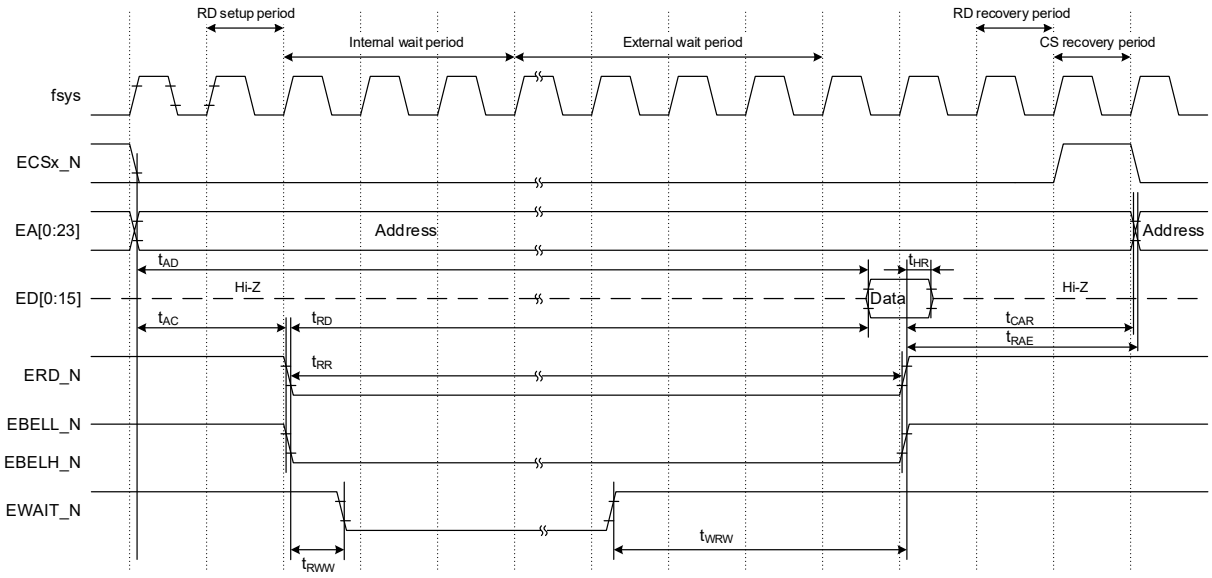


Figure 7.10 Read cycle timing (external wait)

4. Write cycle (minimum cycle)
(Neither Cycle expander, WR setup, Internal wait, CS recovery nor WR recovery are used)

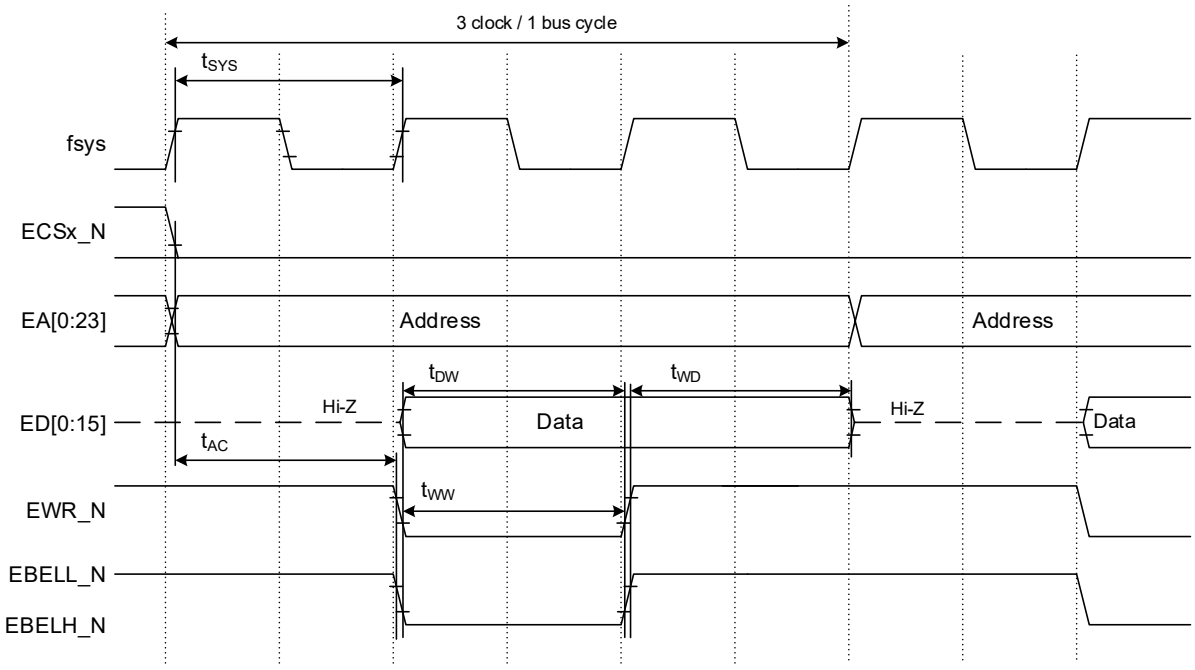


Figure 7.11 Write cycle timing (minimum cycle)

5. Write cycle (6 clock per 1 bus cycle)
(Cycle expander is not used, WR setup=1 cycle, Internal wait=1 cycle, CS recovery=1 cycle, WR recovery=1 cycle)

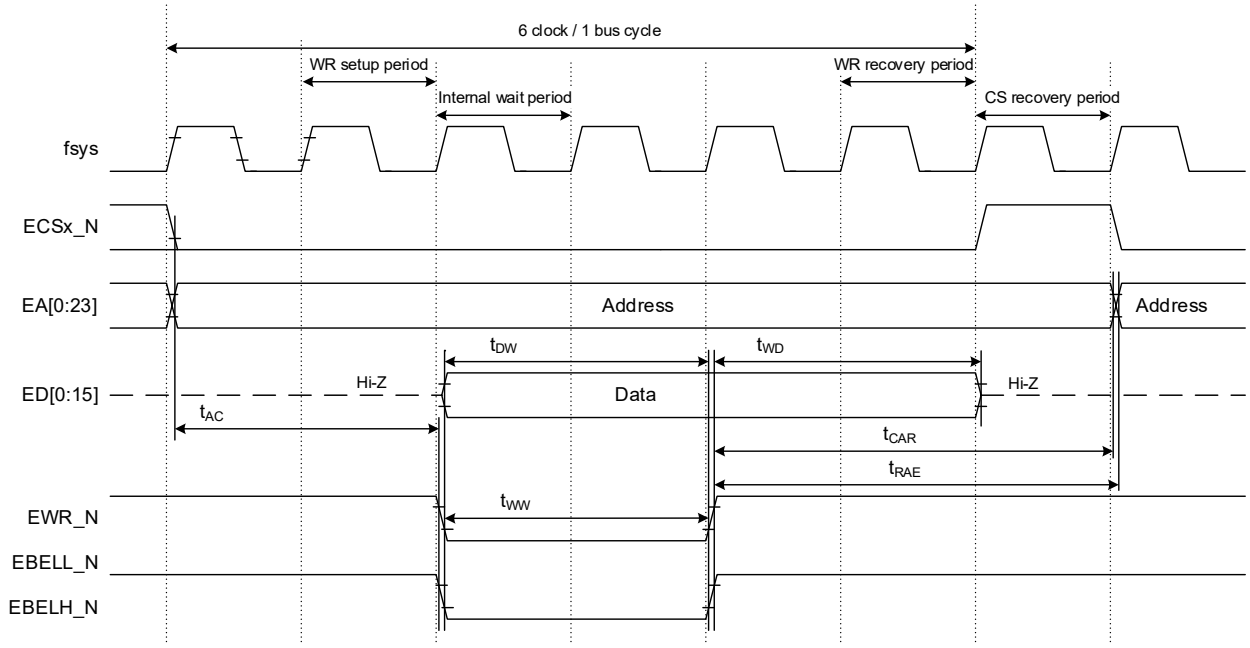


Figure 7.12 Write cycle timing (6 clock per 1 bus cycle)

6. Write cycle (external wait)
(Cycle expander is not used, WR setup=1 cycle, Internal wait=3 cycles, External wait=any, CS recovery=1 cycle, WR recovery=1 cycle)

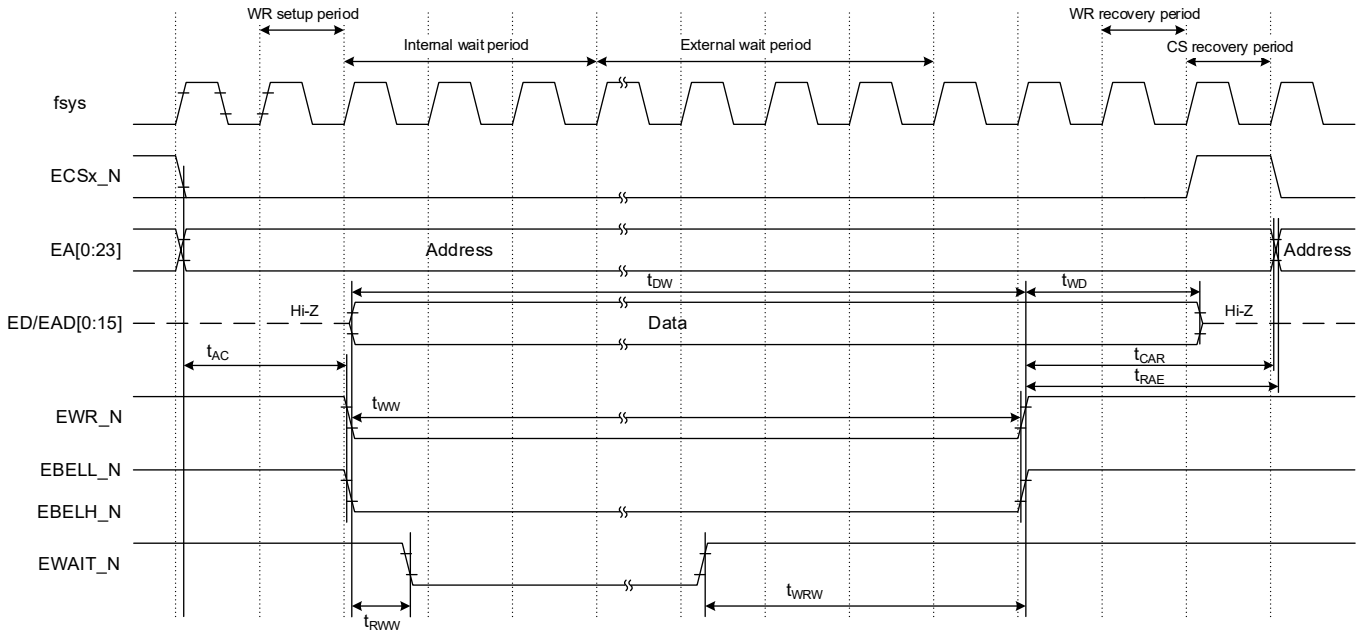


Figure 7.13 Write cycle timing (external wait)

7.10.5.4. AC Electrical Characteristics (EEXBCLK asynchronous multiplex bus mode)

Variable Condition: fsysh = 100MHz ALE = 2, RWS = 4, TW = 3, TWEX = 4, RWH = 4, CSH =1
fsysh = 200MHz ALE = 4, RWS = 4, TW = 3, TWEX = 4, RWH = 4, CSH =2

Parameter	Symbol	Equation		fsysh = 100MHz		fsysh = 200MHz		Unit
		Min	Max	Min	Max	Min	Max	
System clock cycle (T)	t_{SYS}	T	–	10	–	5	–	ns
EAD[0:15] valid → EALE fall	t_{AL}	T (1+ALE)-25	–	5	–	0	–	
EALE fall → EAD[0:15] hold	t_{LA}	T (1+RWS)-30	–	20	–	-5	–	
EALE High pulse width	t_{LL}	T (1+ALE)-16	–	14	–	9	–	
EALE fall → ERD_N, EWR_N fall	t_{LC}	T(1+RWS)-25	–	25	–	0	–	
ERD_N, EWR_N rise → EALE rise	t_{CL}	T (1+RWH+CSH)-25	–	35	–	10	–	
EAD[0:15] valid → ERD_N, EWR_N fall EA[16:23] valid → ERD_N, EWR_N fall	t_{ACL} t_{ACH}	T (2+ALE+RWH)-25	–	55	–	25	–	
ERD_N, EWR_N rise → EA[16:23] hold	t_{CAR}	T (1+RWH+CSH)-30	–	30	–	5	–	
EAD[0:15] valid → EAD[0:15] input EA[16:23] valid → EAD[0:15] input	t_{ADL} t_{ADH}	–	T (3+ALE+RWS+TW+TWEX)-40	–	120	–	50	
ERD_N fall → ED[0:15] input	t_{RD}	–	T (1+TW+TWEX)-40	–	40	–	00	
ERD_N Low level pulse width	t_{RR}	T (1+TW+TWEX)-20	–	60	–	20	–	
ERD_N rise → EAD[0:15] hold	t_{HR}	0	–	0	–	0	–	
ERD_N rise → EA[16:23] output	t_{RAE}	T (1+RWH+CSH)-30	–	30	–	5	–	
EWR_N Low pulse width	t_{WW}	T (1+TW+TWEX)-20	–	60	–	20	–	
EAD[0:15] valid → EWR_N rise	t_{DW}	T (1+TW+TWEX)-25	–	55	–	15	–	
EWR_N rise → EAD[0:15] hold	t_{WD}	T (1+RWH)-30	–	20	–	-5	–	
ERD_N/EWR_N fall → EWAIT_N fall	t_{RWW}	–	T (TW)−40	–	-10	–	-25	
EWAIT_N rise → ERD_N/EWR_N rise	t_{WRW}	–	4T + 30	–	70	–	50	

1. Read cycle (minimum cycle)
(Neither Cycle expander, ALE wait, RD setup, Internal wait, CS recovery nor RD recovery are used)

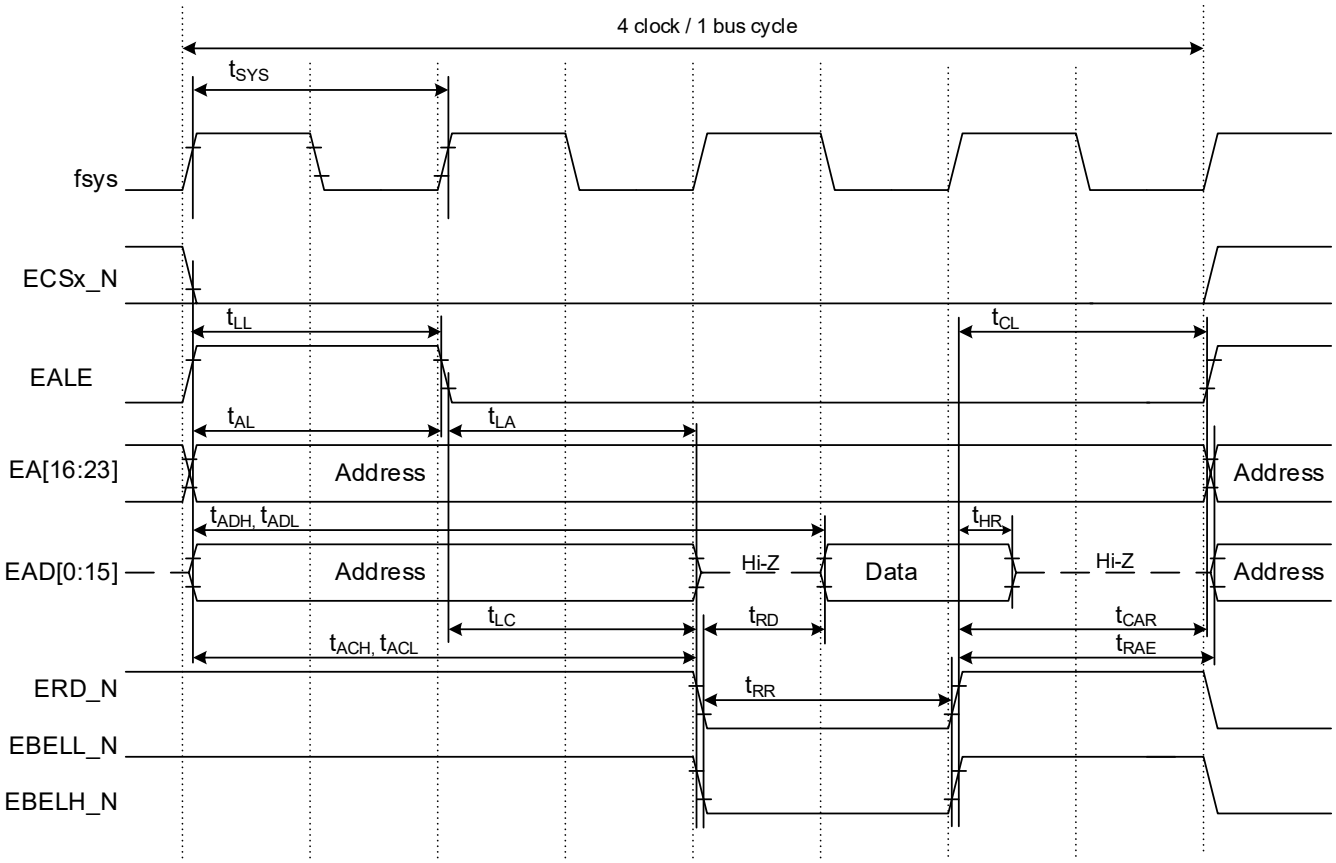


Figure 7.14 Read cycle timing (minimum cycle)

2. Read cycle (8 clock per 1 bus cycle)
(Cycle expander is not used, ALE wait=1 cycle, RD setup=1 cycle, Internal wait=1 cycle, CS recovery=1 cycle, RD recovery=1 cycle)

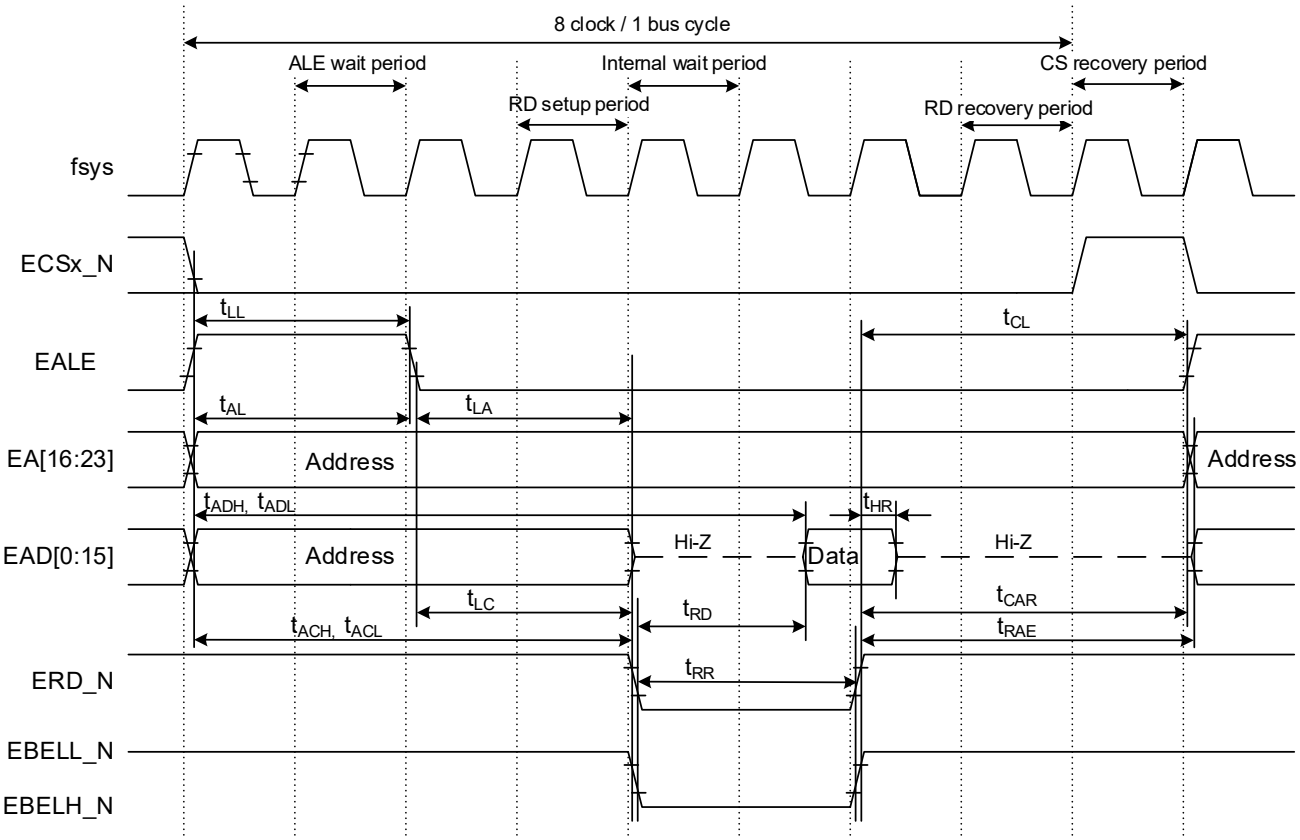


Figure 7.15 Read cycle timing (8 clock per 1 bus cycle)

3. Read cycle (10 clock per 1 bus cycle)
(Cycle expander=double, ALE wait=1 cycle, RD setup is not used, Internal wait=1 cycle, CS recovery=1 cycle, RD recovery=1 cycle)

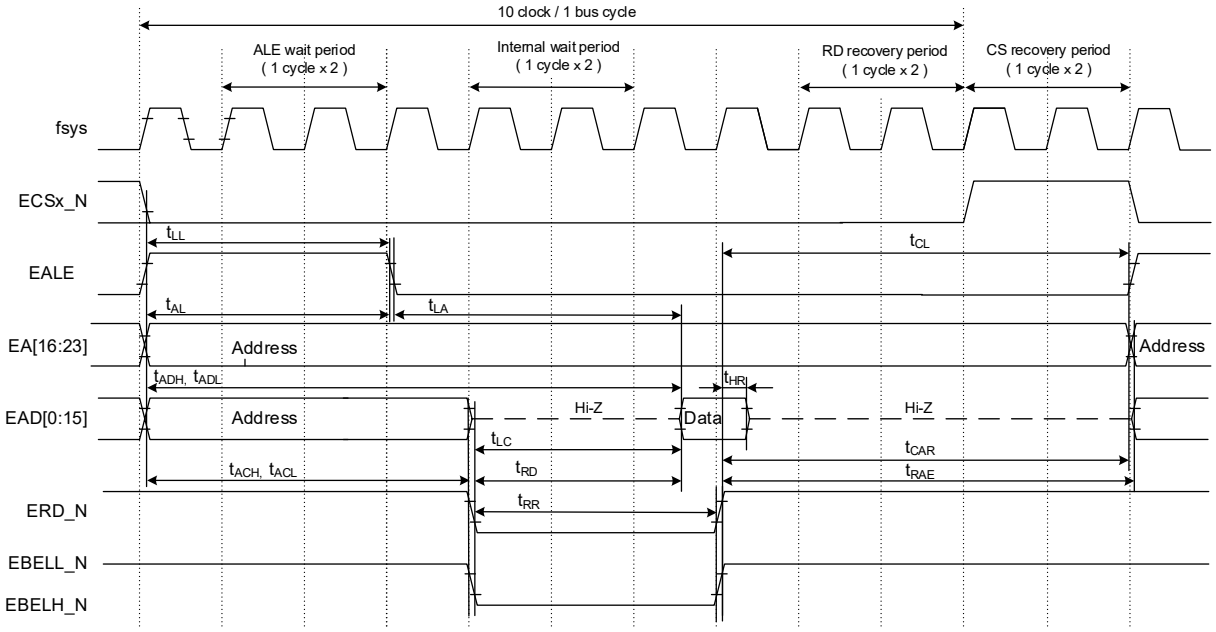


Figure 7.16 Read cycle timing (10 clock per 1 bus cycle)

4. Read cycle (external wait)
(Cycle expander is not used, ALE wait=1 cycle, RD setup=1 cycle, Internal wait=3 cycles, External wait=any, CS recovery=1 cycle, RD recovery=1 cycle)

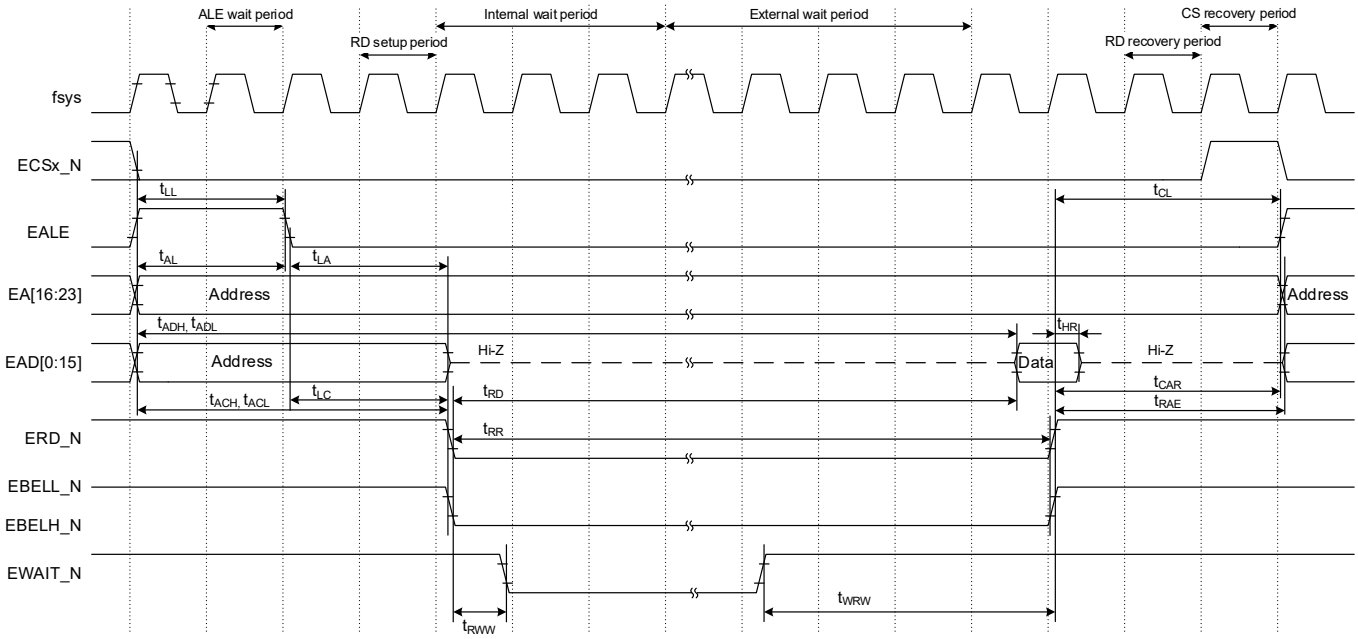


Figure 7.17 Read cycle timing (external wait)

5. Write cycle (minimum bus cycle)
(Neither Cycle expander, ALE wait, WR setup, Internal wait, CS recovery nor WR recovery are used.)

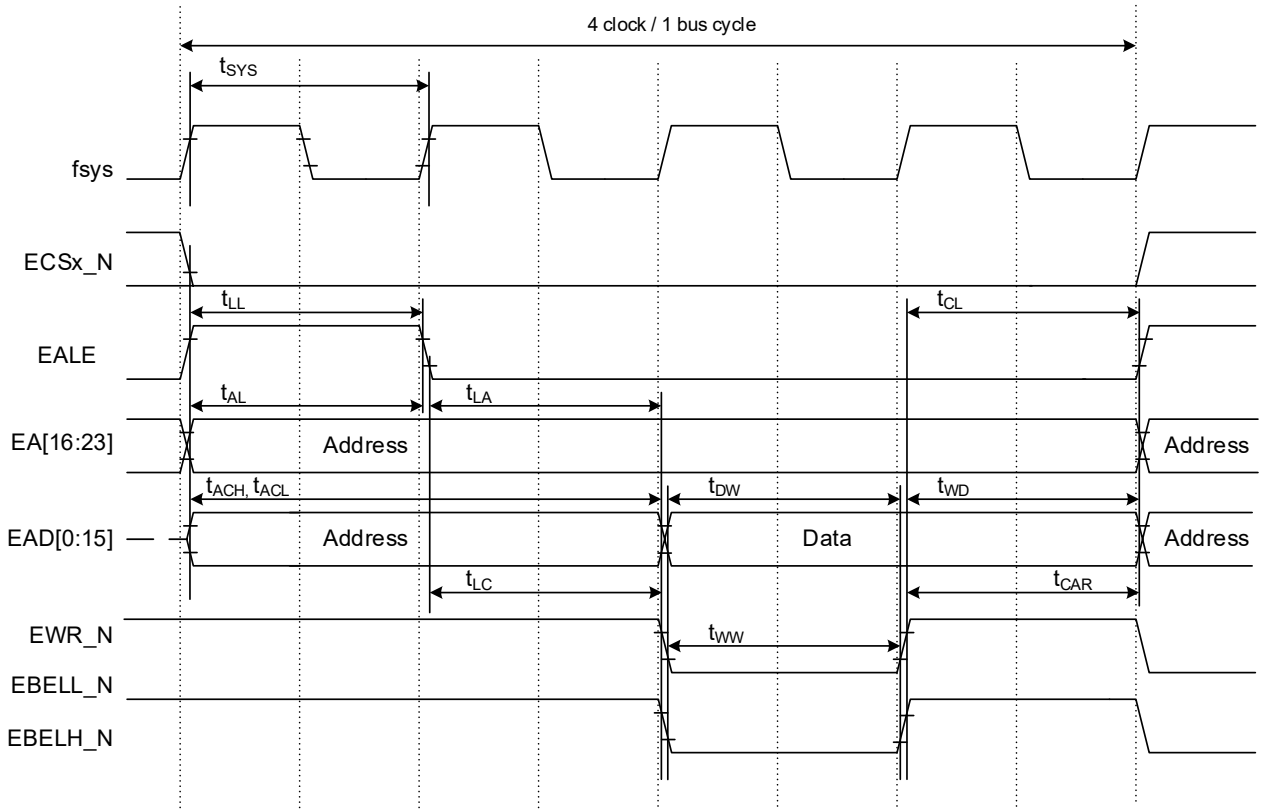


Figure 7.18 Write cycle timing (minimum bus cycle)

6. Write cycle (8 clock per 1 bus cycle)
(Cycle expander is not used, ALE wait=1 cycle, WR setup=1 cycle, Internal wait=1 cycle, CS recovery=1 cycle, WR recovery=1 cycle)

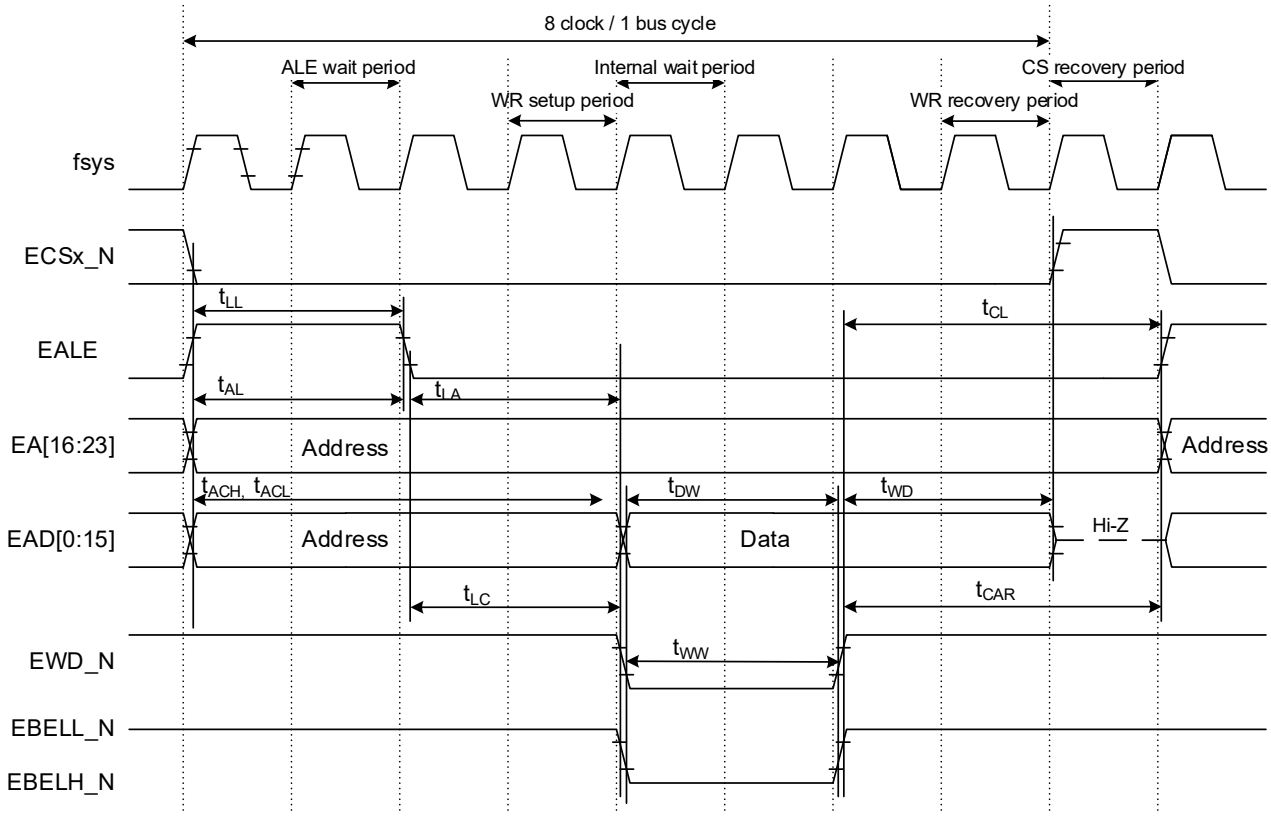


Figure 7.19 Write cycle timing (1 bus cycle per 8 clock)

7. Write cycle (external wait)
(Cycle expander is not used, ALE wait=1 cycle, WR setup=1 cycle, Internal wait=3 cycles, External wait=any, CS recovery=1 cycle, WR recovery=1 cycle)

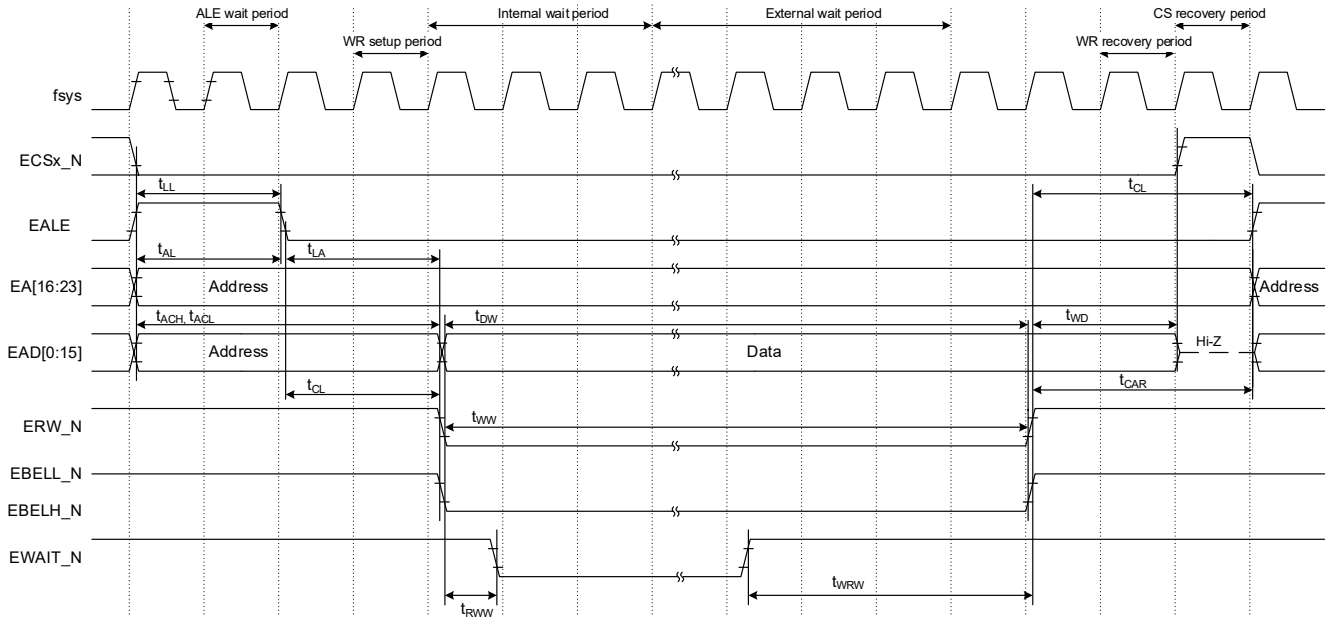


Figure 7.20 Write cycle timing (external wait)

7.10.5.5. AC Electrical Characteristics (EEXBCLK synchronous separate bus mode/multiplex bus mode)

The AC characteristics are as follows:

- Output level: High = 0.5×DVDD3, Low = 0.5×DVDD3
- Input level: High = 0.5×DVDD3, Low = 0.5×DVDD3

Parameter	Symbol	Equation		fsysh=200MHz		Unit
		Min	Max	Min	Max	
External bus clock cycle(EEXBCLK)	X	33.3	-	33.3	-	ns
Output pin valid → EEXBCLK fall	t_S	2	-	2	-	
EEXBCLK fall → Output pin hold	t_H	7	-	7	-	
ED/EAD[15:0] input valid → EEXBCLK rise	t_{DS}	20	-	20	-	
EEXBCLK rise → ED/EAD[15:0] input hold	t_{DH}	0	-	0	-	
EWAIT_N input valid → EEXBCLK rise	t_{WS}	20	-	20	-	
EEXBCLK rise → EWAIT_N input hold	t_{WH}	0	-	0	-	

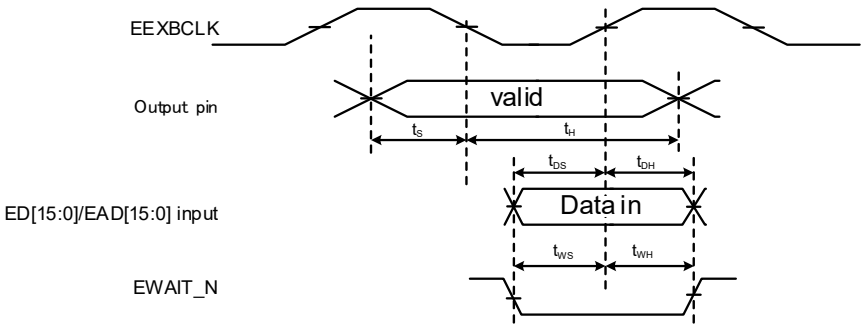


Figure 7.21 EEXBCLK synchronous separate bus mode/multiplex bus mode timing

7.10.6. Serial Memory Interface (SMIF)

7.10.6.1. Conditions

The conditions for AC characteristics are as follows:

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C (fsysh ≤ 200MHz)
- Output level: High = 0.8×DVDD3, Low = 0.2×DVDD3
- Input level: High = 0.75×DVDD3, Low = 0.25×DVDD3
- Load capacity: CL = 30pF

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

Parameter	Symbol	Equation	Min	Max	Unit
SMIxCLK clock frequency	f_{CK}	-	-	25	MHz
Data setup time	t_{SU}	-	31.2	-	ns
Data hold time	t_{HD}	-	0	-	
Output valid	t_V	-	-	14.5	
Output hold time	t_{HO}	-	-14.5	-	
CS Setup time	t_{CSS}	1.5T-20	40	-	
CS hold time	t_{CSH}	1.0T-20	20	-	

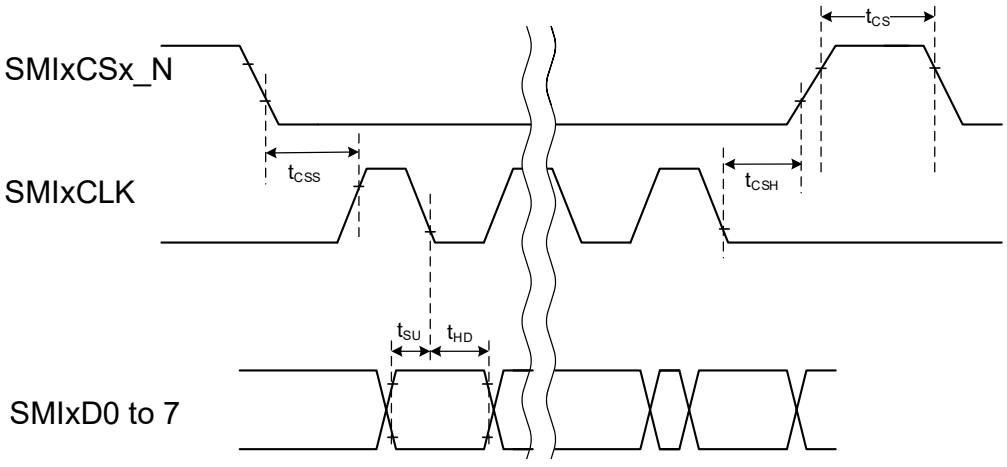


Figure 7.22 SMIF Input timing

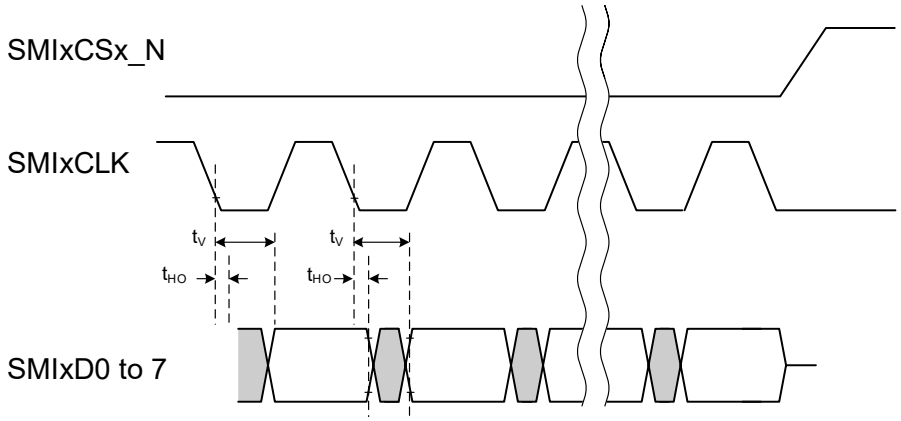


Figure 7.23 SMIF Output timing

7.10.7. I²S Interface (I2S)

7.10.7.1. Conditions

The conditions for AC characteristics are as follows:

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C (fsysh ≤ 200MHz)
- Output level: High = 0.5×DVDD3, Low = 0.5×DVDD3
- Input level: High = 0.5×DVDD3, Low = 0.5×DVDD3
- Load capacity: CL = 30pF

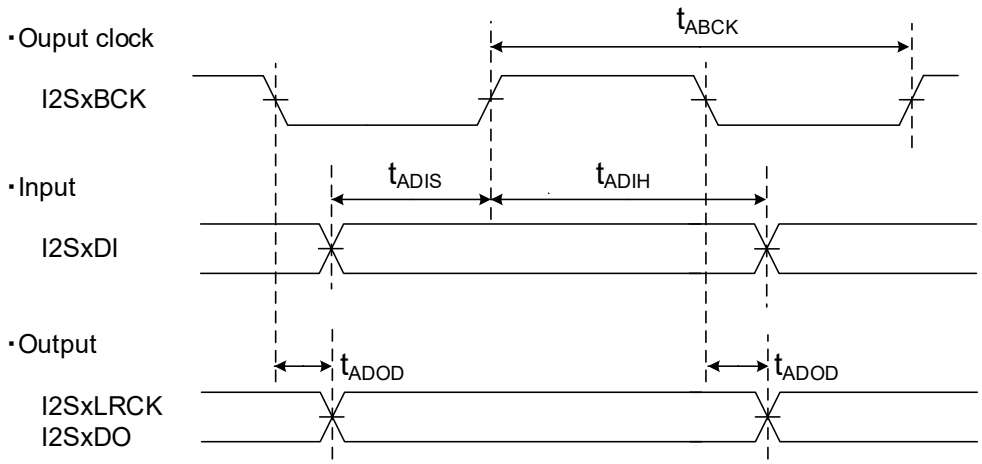
Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.10.7.2. AC Electrical Characteristics

(1) Master mode

Parameter	Symbol	Min	Max	Unit
Output Clock Period	t_{ABCK}	81.38 (Note)	-	ns
Input Data Setup Time	t_{ADIS}	25	-	
Input Data Hold Time	t_{ADIH}	10	-	
Output Delay Time	t_{ADOD}	-5	15	

Note: Max 12.288MHz



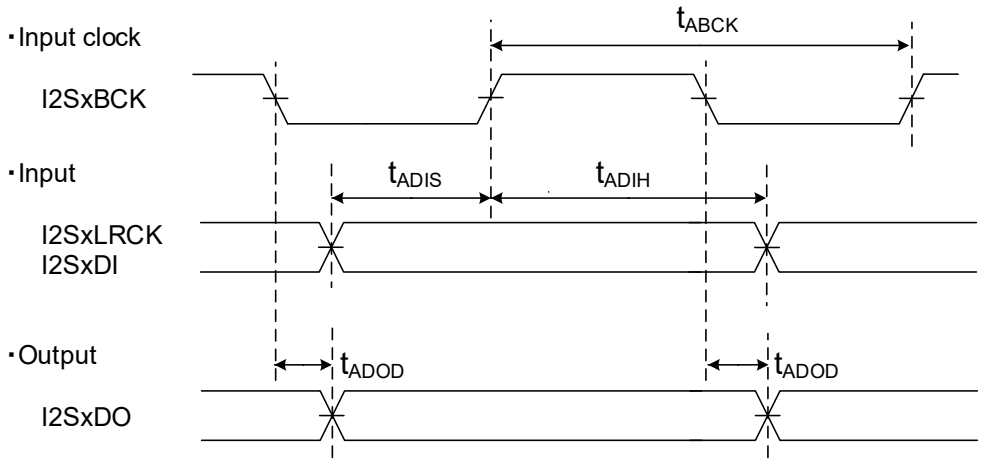
(Falling edge data output, rising edge input data sampling)

Figure 7.24 I²S Interface Master mode

(2) Slave mode

Parameter	Symbol	Min	Max	Unit
Output Clock Period	t_{ABCK}	81.38 (Note)	-	ns
Input Data Setup Time	t_{ADIS}	10	-	
Input Data Hold Time	t_{ADIH}	10	-	
Output Delay Time	t_{ADOD}	0	30	

Note: Max 12.288MHz



(Falling edge data output, rising edge input data sampling)

Figure 7.25 I²S Interface Slave mode

7.10.8. Synchronous serial interface (TSSI)

7.10.8.1. Conditions

The conditions for AC characteristics are as follows:

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C (fsysh ≤ 200MHz)
- Output level: High = 0.5×DVDD3, Low = 0.5×DVDD3
- Input level: High = 0.5×DVDD3, Low = 0.5×DVDD3
- Load capacity: CL = 30pF

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.10.8.2. AC Electrical Characteristics

(1) Master mode

Parameter	Symbol	Equation	Min	Max	Unit
TSSIxTCK/TSSIxRCK Output clock frequency	f_{CYC}	-	-	**10**	MHz
TSSIxTCK/TSSIxRCK Output clock period	t_{CYC}	$1/f_{CYC}$	100	-	ns
TSSIxTCK/TSSIxRCK Low level output pulse width	t_{WL}	$(t_{CYC}/2)-10$	40	-	
TSSIxTCK/TSSIxRCK High level output pulse width	t_{WH}	$(t_{CYC}/2)-10$	40	-	
TSSIxRXD Input setup time	t_{DSU}	0.5T – 25	25	-	
TSSIxRXD Input hold time	t_{DHD}	0.5T – 25	25	-	
TSSIxTXD Output delay time	t_{DDLY2}	0.5T – 25	-	25	
TSSIxTXD Output hold time	t_{DDLY1}	-(0.5T – 25)	-25	-	

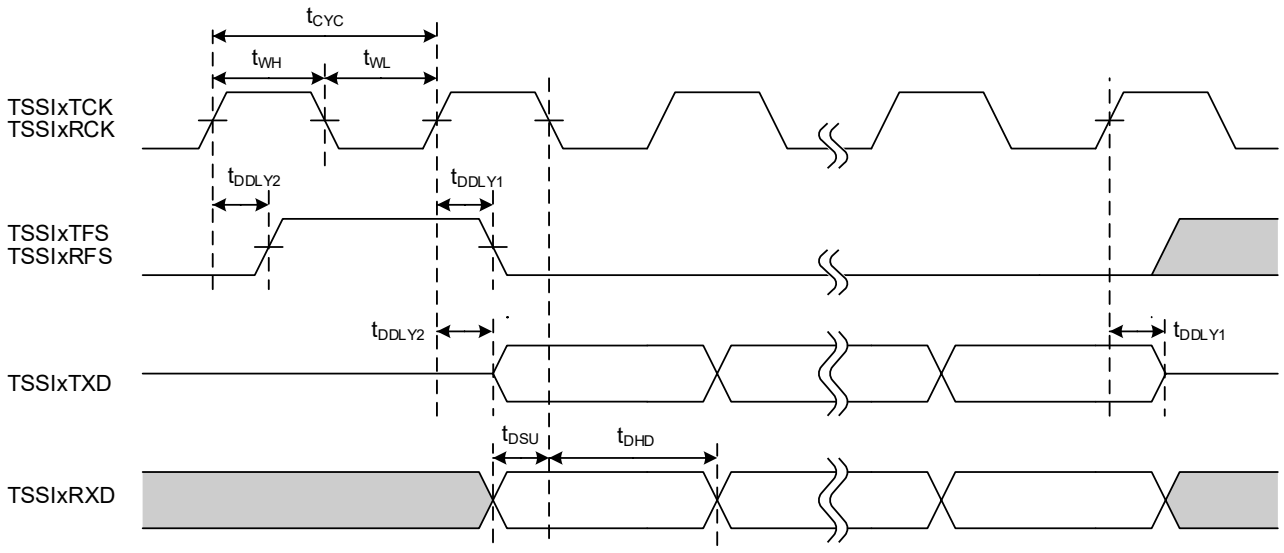


Figure 7.26 Master operation

(2) Slave mode

Parameter	Symbol	Equation	Min	Max	Unit
TSSIxTCK/TSSIxRCK Input clock frequency	f_{CYC}	-	-	**10**	MHz
TSSIxTCK/TSSIxRCK Input clock period	t_{CYC}	$1/f_{CYC}$	**100**	**-**	ns
TSSIxRXD/TSSIxTSF/TSSIxRSF Input setup time	t_{DSU}	0.5T – 25	25	-	
TSSIxRXD/TSSIxTSF/TSSIxRSF Input hold time	t_{DHD}	0.5T – 25	25	-	
TSSIxTXD Output delay time	t_{DDLY2}	0.5T – 25	-	25	
TSSIxTXD Output hold time	t_{DDLY1}	-(0.5T – 25)	-25	-	

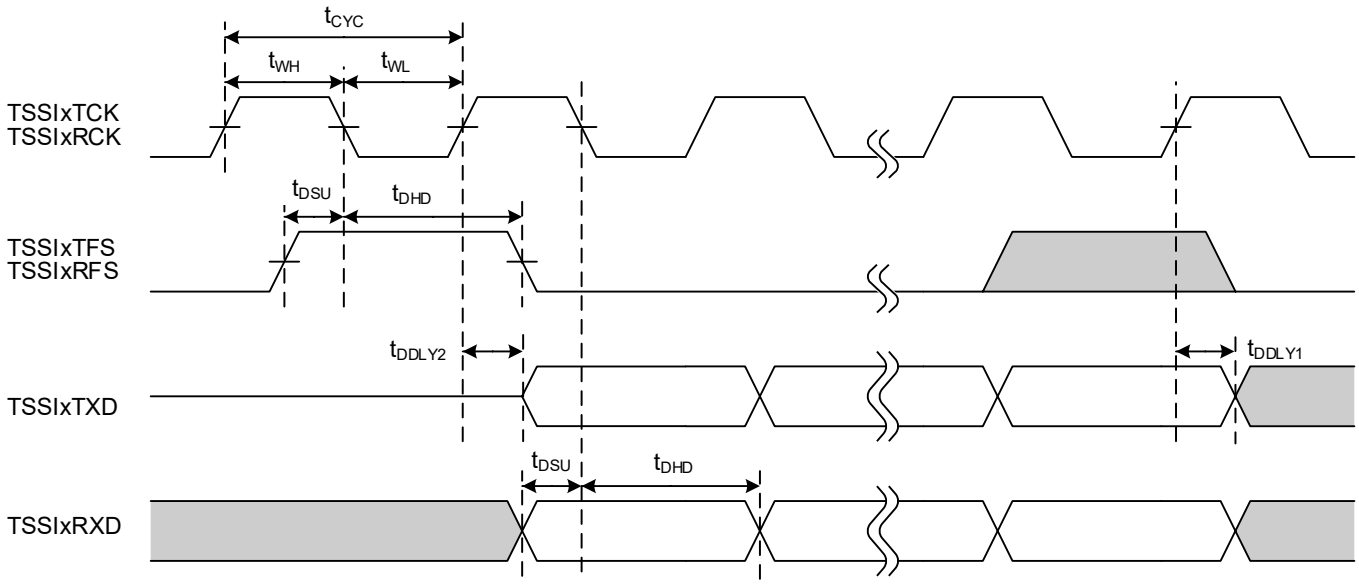


Figure 7.27 Slave operation

7.10.9. External Interrupt

7.10.9.1. Conditions

The conditions for AC characteristics are as follows:

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C (fsysh ≤ 200MHz)
- Input level: High = 0.75×DVDD3, Low = 0.25×DVDD3
- Load capacity: CL = 30pF

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.10.9.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

(1) NORMAL, IDLE mode

Parameter	Symbol	Equation		fsysh=200MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{INTAL1}	T + 100	-	105	-	ns
High level pulse width	t_{INTAH1}	T + 100	-	105	-	

(2) STOP1, STOP2 mode

Parameter	Symbol	Equation		fsysh=200MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{INTCL2}	500	-	500	-	ns
High level pulse width	t_{INTCH2}	500	-	500	-	

7.10.10. Trigger Input (TRGINx)

7.10.10.1. Conditions

The conditions for AC characteristics are as follows:

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C
- Input level: High = 0.75×DVDD3, Low = 0.25×DVDD3
- Load capacity: CL = 30pF

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.10.10.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

Parameter	Symbol	Equation		fsysm=100MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{ADL}	2T + 20	-	40	-	ns
High level pulse width	t_{ADH}	2T + 20	-	40	-	

7.10.11. Debug Communication

7.10.11.1. Conditions

The conditions for AC characteristics are as follows:

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C (fsys ≤ 200MHz)
- Output level: High = 0.8×DVDD3, Low = 0.2×DVDD3
- Input level: High = 0.75×DVDD3, Low = 0.25×DVDD3
- Load capacity: CL = 30pF

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.10.11.2. SWD Interface

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold time from the rising edge of CLK	t_{d1}	1	-	
Output data valid time from the rising edge of CLK	t_{d2}	-	35	
From input data valid time to the rising edge of CLK	t_{ds}	20	-	
Input data hold time from the rising edge of CLK	t_{dh}	15	-	

7.10.11.3. JTAG Interface

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold time from the falling edge of CLK	t_{d1}	0	-	
Output data valid time from the falling edge of CLK	t_{d2}	-	35	
From input data valid time to the rising edge of CLK	t_{ds}	20	-	
Input data hold time from the rising edge of CLK	t_{dh}	15	-	

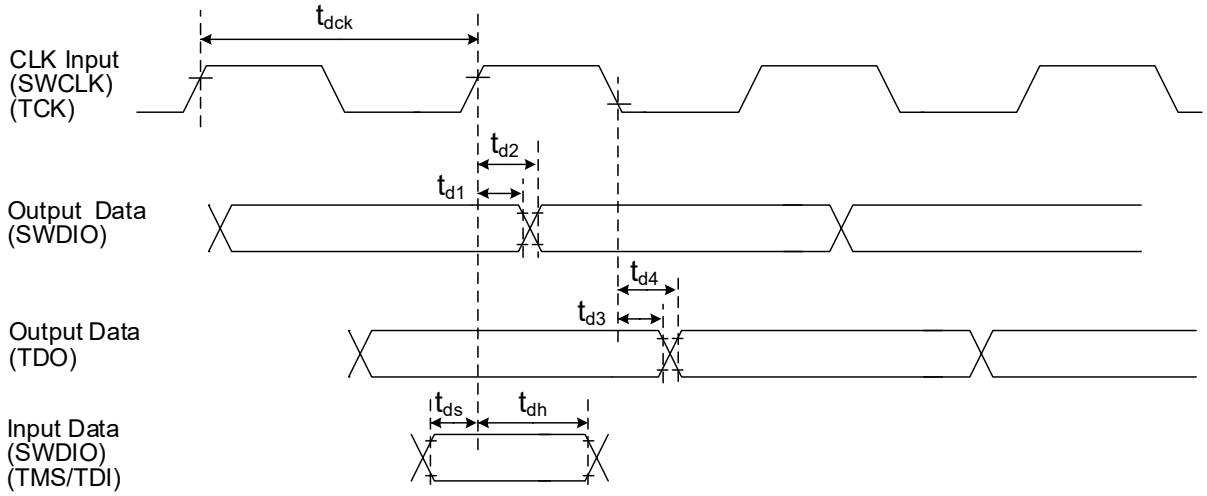


Figure 7.28 JTAG/SWD waveform

7.10.11.4. ETM Trace

Parameter	Symbol	Min	Max	Unit
TRACECLK cycle	t_{tclk}	20	-	ns
TRACEDATA valid time from rising edge of TRACECLK	t_{setupr}	2	-	
TRACEDATA hold time from the rising edge of TRACECLK	t_{holdr}	1	-	
TRACEDATA valid time from the falling edge of TRACECLK	t_{setupf}	2	-	
TRACEDATA hold time from the falling edge of TRACECLK	t_{holdf}	1	-	

Note: When fsys > 100MHz, the condition is DVDD3=3.3V, CL=10pF.

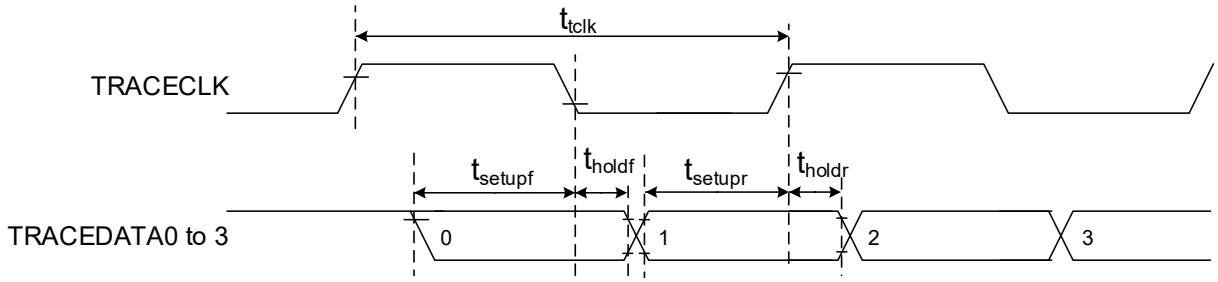


Figure 7.29 Trace signal waveform

7.10.11.5. Non Break Debug Interface (NBDIF)

Parameter	Symbol	Min	Max	Unit
NBDCLK cycle Time	t_{NDCYC}	80	-	ns
NBDCLK low level pulse width	t_{NDL}	35	-	
NBDDATA output delay time	t_{NDD}	-	t_{NDCYC} - 20	
NBDDATA output hold time	t_{NDHD}	5	-	
NBDDATA setup time	t_{NDS}	20	-	
NBDDATA hold time	t_{NDH}	5	-	
NBDSYNC setup time	t_{NDSYS}	20	-	
NBDSYNC output hold time	t_{NDSYH}	5	-	

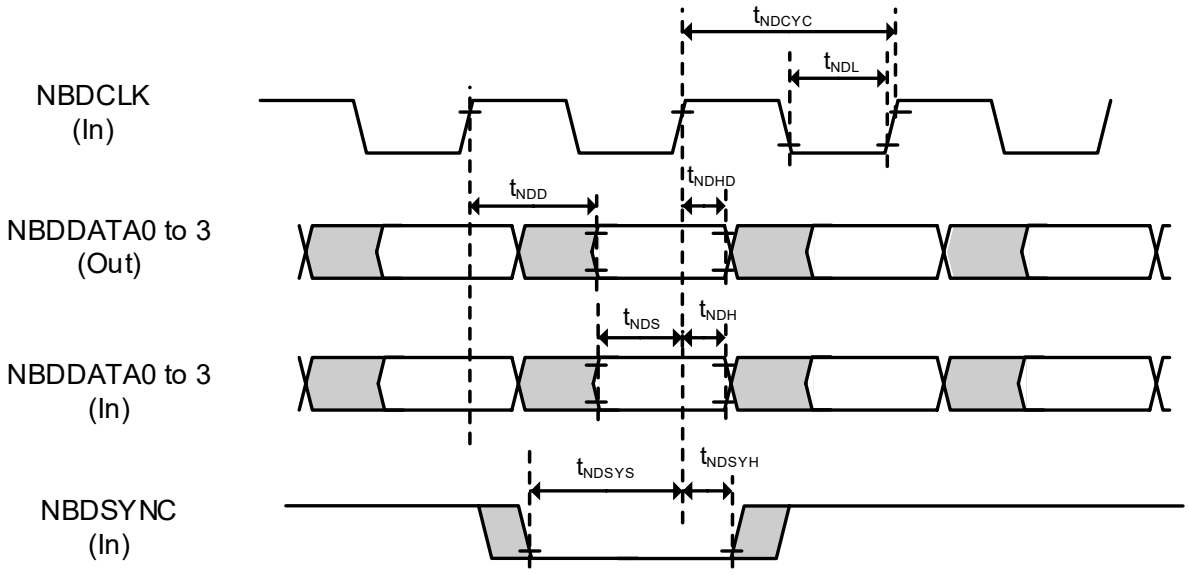


Figure 7.30 NBDIF waveform

7.10.11.6. Noise Filter Characteristics

Parameter	Condition	Min	Typ.	Max	Unit
Noise cancel width	-	15	30	60	ns

7.10.12. External Clock Input

7.10.12.1. Conditions

The conditions for AC characteristics are as follows:

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C
- Input level: High = 0.75×DVDD3, Low = 0.25×DVDD3
- Load capacity: CL = 30pF

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.10.12.2. AC Electrical Characteristics

(1) High speed clock input

Parameter	Symbol	Min	Typ.	Max	Unit
Clock frequency (f_{ehcin} = 1 / t_{ehcin})	f_{ehcin}	8	-	24	MHz
Clock duty	-	45	-	55	%
Clock rise time	t_r	-	-	10	ns
Clock fall time	t_f	-	-	10	ns

(2) Low speed clock input

Parameter	Symbol	Min	Typ.	Max	Unit
Clock frequency (f_{ehcin} = 1 / t_{ehcin})	f_{ehcin}	30	-	34	kHz
Clock duty	-	45	-	55	%
Clock rise time	t_r	-	-	100	ns
Clock fall time	t_f	-	-	100	ns

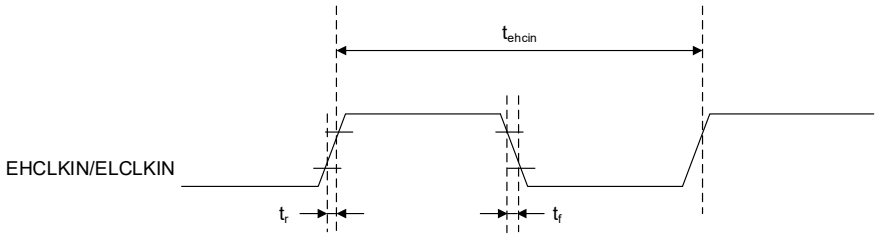


Figure 7.31 External clock input waveform

7.11. Flash Memory Characteristics

7.11.1. Code Flash

DVDD3=2.7V to 3.6V
Ta= -40 to 85°C

Parameter	Condition	Min	Typ.	Max	Unit
Endurance		-	-	100,000	cycles
Programming time	Word Program time	-	22.6	-	μs
Erase time	Page Erase time	1.1	-	4.2	ms
	Block Erase time	8.4	-	33.6	
	Area Erase time (Note2)	-	9.1	-	

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

Note2: No block with effective protection.

7.11.2. Data Flash

DVDD3=2.7V to 3.6V
Ta= -40 to 85°C

Parameter	Condition	Min	Typ.	Max	Unit
Endurance		-	-	100,000	cycles
Programming time		-	78	-	μs
Erase time	Page Erase time	1.1	-	4.2	ms
	Block Erase time	16.2	-	64.6	
	Area Erase time (Note2)	-	9.1	-	

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

Note2: No block with effective protection.

7.11.3. Chip Erase

Item	Products
Group A Product	TMPM4GRF20FG, TMPM4GRF20XBG, TMPM4GQF20FG, TMPM4GQF20XBG, TMPM4GNF20FG, TMPM4GRF15FG, TMPM4GRF15XBG, TMPM4GQF15FG, TMPM4GQF15XBG, TMPM4GNF15FG
Group B Product	TMPM4GRF10FG, TMPM4GRF10XBG, TMPM4GQF10FG, TMPM4GQF10XBG, TMPM4GNF10FG TMPM4GRFDFG, TMPM4GRFDXBG, TMPM4GQFDFG, TMPM4GQFDXBG, TMPM4GNFDFG

Note: For the newest status of each product, please contact your sales representative.

DVDD3=2.7V to 3.6V
Ta= -40 to 85°C

Parameter	Condition	Group A Product			Group B Product			Unit
		Min	Typ.	Max	Min	Typ.	Max	
Chip Erase time	Erasing of Code flash, Data flash, Protect bits (Code), Protect bits (Data), Security bits	30.6	—	39.8	21.5	—	30.7	ms

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

Note2: It does not include overhead and communication time between command executions.

Note3: When Chip Erase command executes, no block with effective protection.

7.12. Regulator

DVDD3=2.7V to 3.6V
Ta= -40 to 85°C

Parameter	Condition	Min	Typ.	Max	Unit
Capacitance of REGOUT1 capacitor		-	1.0	-	μF

7.13. Oscillation Circuit

7.13.1. Internal Oscillator

DVDD3=2.7V to 3.6V
Ta= -40 to 85°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{IHOSC1}		9.9	10	10.1	MHz
	f_{IHOSC2}		-	10	-	

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.13.2. External Oscillator

DVDD3=2.7V to 3.6V
Ta= -40 to 85°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{EHOSC}		8	-	24	MHz
	f_{ELOSC}		30	-	34	kHz

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

Note2: Please contact the oscillator vendor, regarding the matching data of the device and the oscillator.

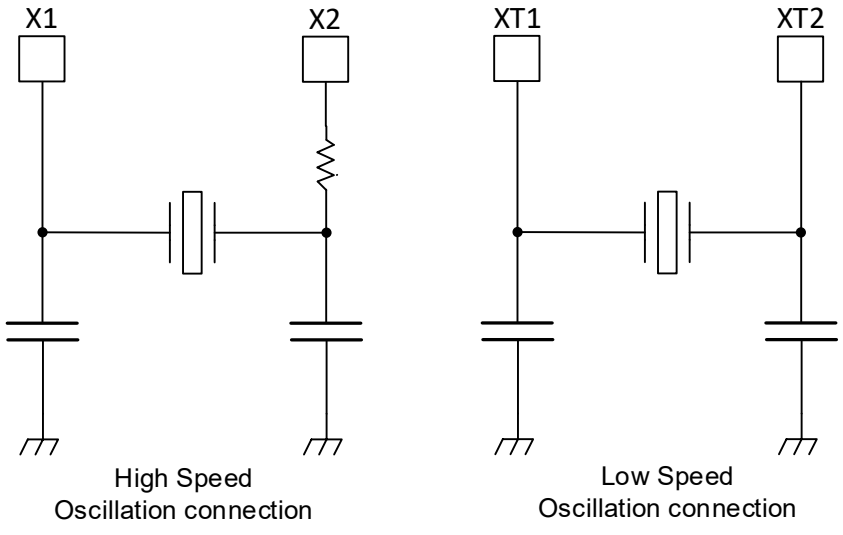


Figure 7.32 Oscillation circuit sample

To obtain a stable oscillation, load capacity and the position of the oscillator must be configured properly.

Since these factors are strongly affected by substrate patterns, please evaluate oscillation stability using the substrate you use.

This product has been evaluated by the oscillator vendor below. Please refer this information when selecting external parts.

7.13.3. Ceramic Resonator

This product has been evaluated by the ceramic resonator by Murata Manufacturing Co., Ltd.
Please refer to the Murata Website for details.

7.13.4. Crystal Unit

This product has been evaluated by the crystal unit by KYOCERA Corporation and Murata Manufacturing Co., Ltd.
Please refer to the KYOCERA and Murata Manufacturing Website for details..

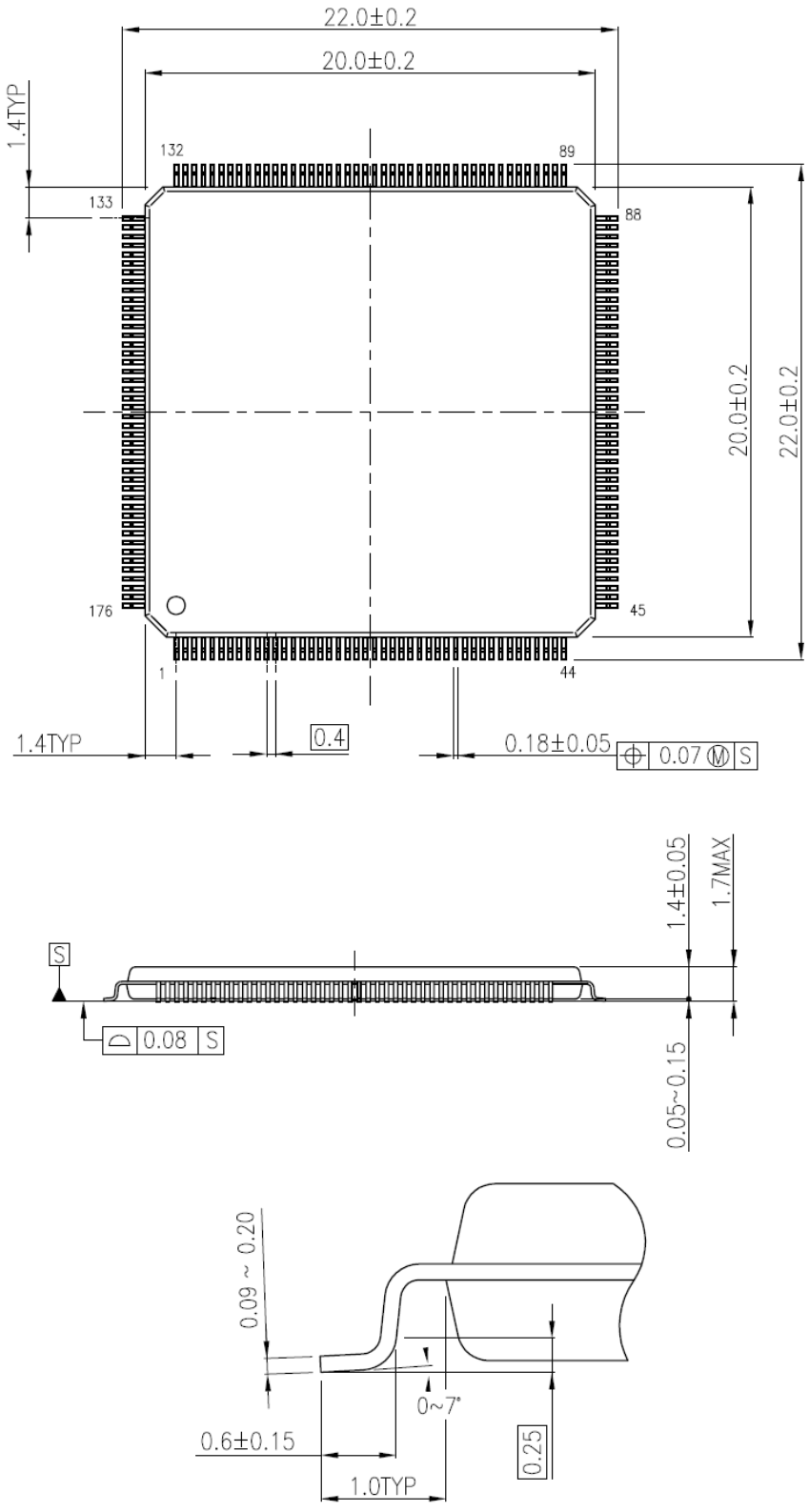
7.13.5. Precautions for designing printed circuit board

Be sure to design printed circuit board patterns that connect a crystal unit with other oscillation elements so that the length of such patterns become shortest possible to prevent deterioration of characteristics due to stray capacitances and wiring inductance. For multilayer circuit boards, it is important not to wire the ground and other signal patterns right beneath the oscillation circuit. For more information, please refer to the URL of the oscillator vendor.

8. Package Dimensions

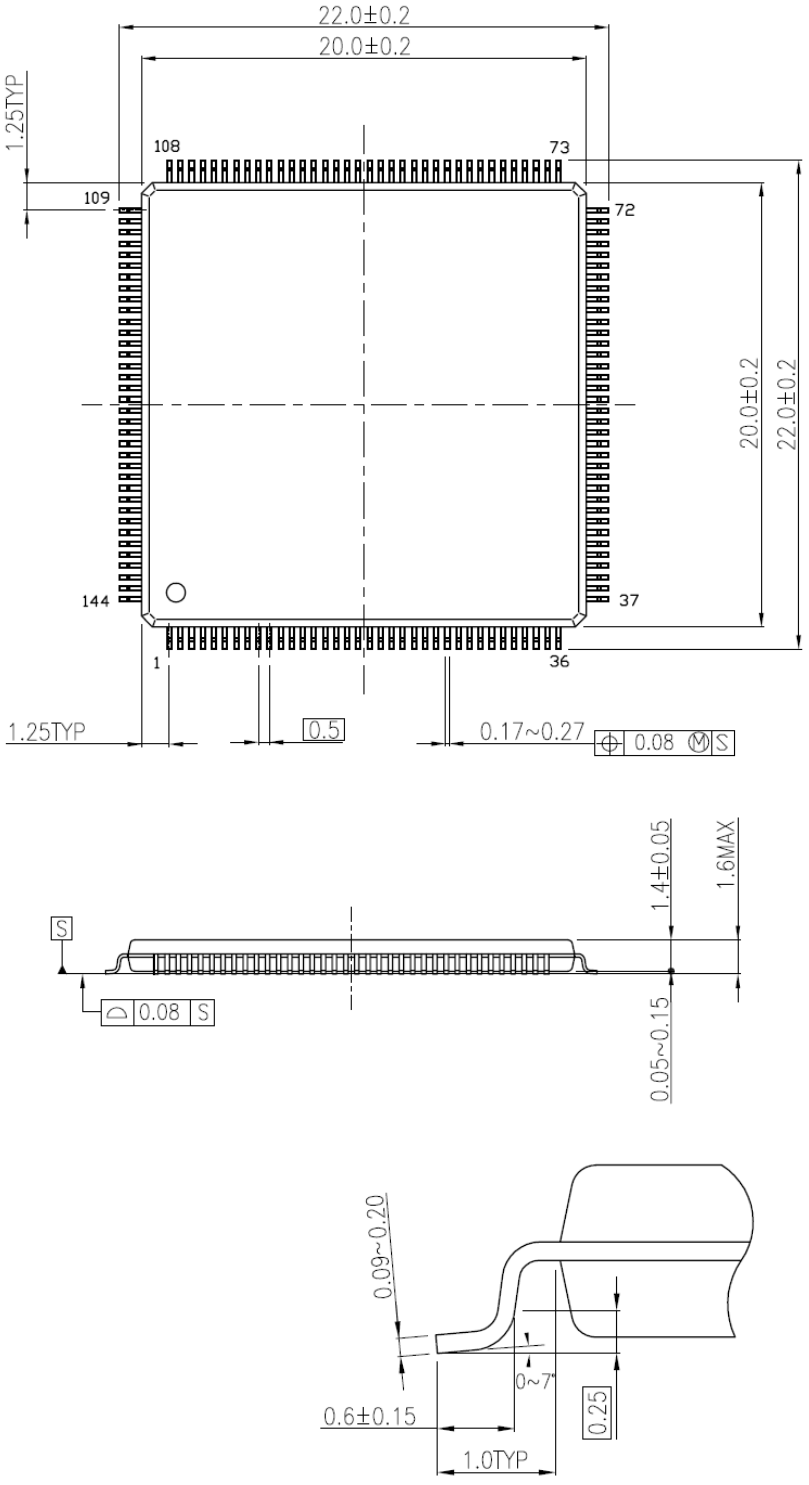
8.1. P-LQFP176-2020-0.40-002

Unit: mm



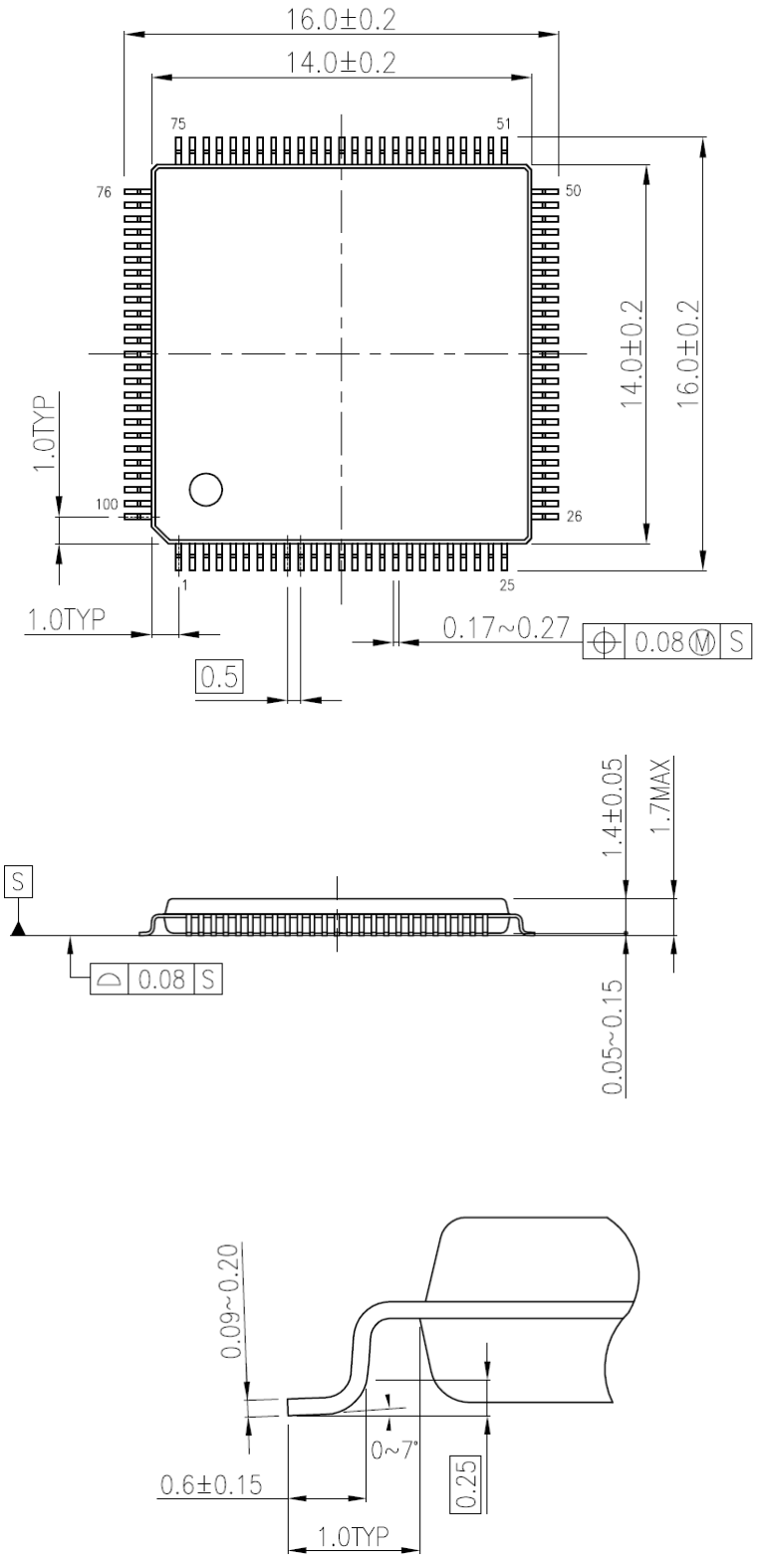
8.2. P-LQFP144-2020-0.50-002

Unit: mm



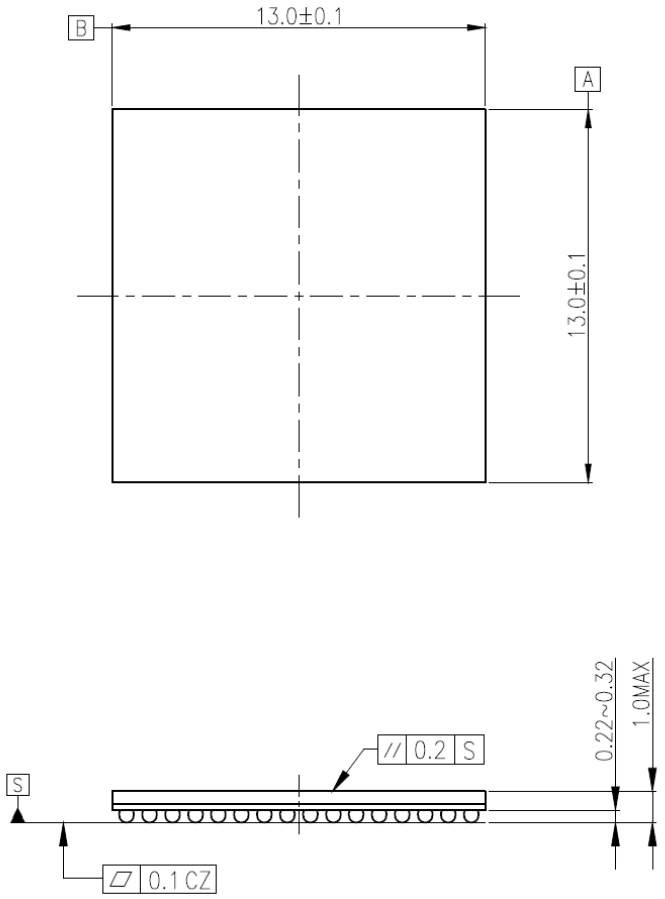
8.3. P-LQFP100-1414-0.50-002

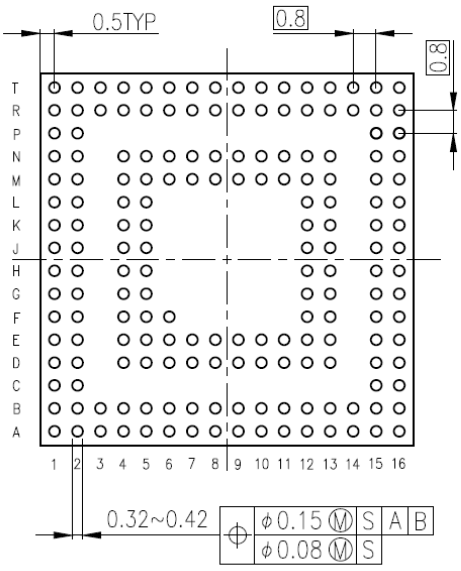
Unit: mm



8.4. P-VFBGA177-1313-0.80-001

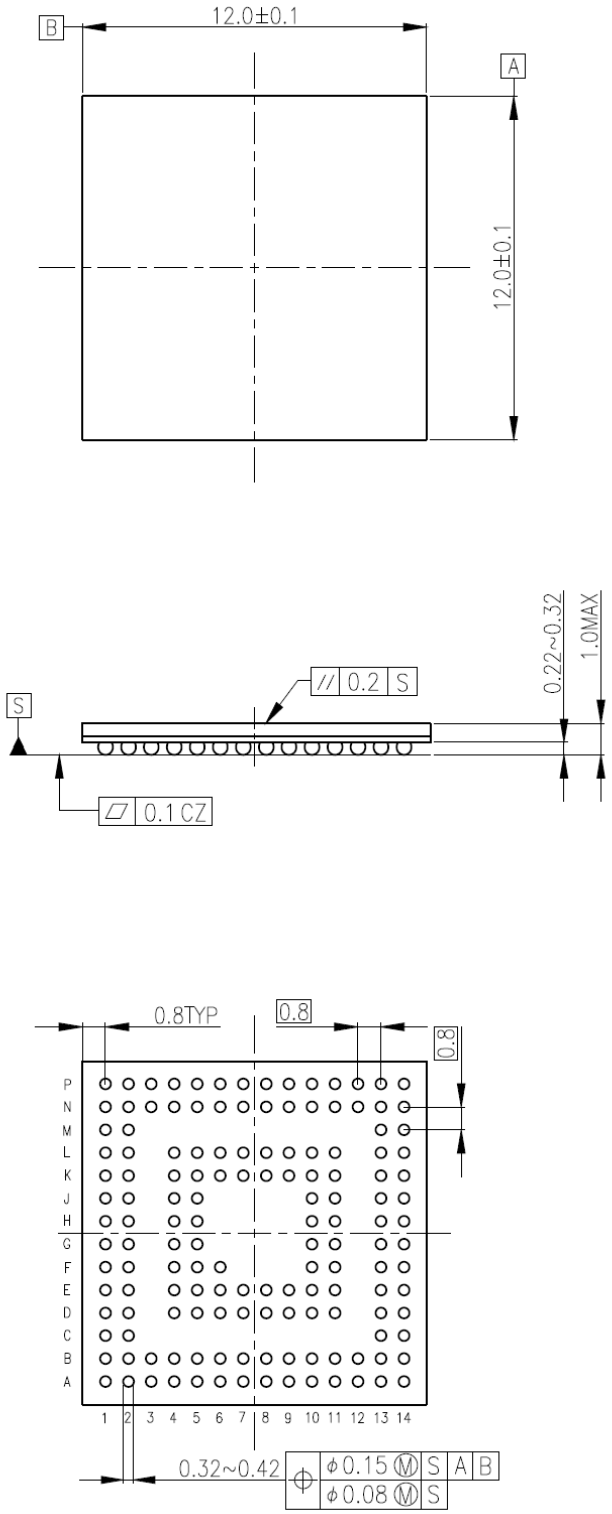
Unit: mm





8.5. P-VFBGA145-1212-0.80-001

Unit: mm



9. Precautions

This Page explains general precautions on the use of our MCUs.

Note that if there is a difference between the general precautions and the description in the body of the document, the description in the body of document has higher priority.

(1) The MCUs' operation at power-on

At power-on, internal state of the MCUs is unstable. Therefore, state of the pins is undefined until reset operation is started and valid.

When a reset is performed by an external reset pin, pins of the MCUs that use the reset pin are undefined until reset operation by the external pin is started and valid.

Also, when a reset is performed by the internal power-on reset, pins of the MCUs that use the internal power-on reset are undefined until power supply voltage reaches the voltage at which power-on reset operation is started and valid.

(2) Unused pins

Unused input/output ports of the MCUs are prohibited to use. The pins are high-impedance.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch- up may occur in the internal LSI due to induced voltage influenced from external noise.

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

(3) Clock oscillation stability

A reset state must be released after the clock oscillation becomes stable. If the clock is changed to another clock while the program is in progress, wait until the destination clock is stable.

10. Revision History

Table 10.1 Revision History

Revision	Date	Description
1.0	2021-06-30	- First Release

Appendix

List of All pins

Function A, B: These are the functions which become effective without setting up port function registers.
Function 1 to 8: These are the functions which become effective with setting up port function registers.

M4GR LQFP176	M4GQ LQFP144	M4GN LQFP100	M4GR BGA177	M4GQ BGA145	Pin Name	Function A	Function B	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Input / Output	PU/PD	OD	5VT / 3VT	SMT / CMOS	Under Reset	After Reset
1	1	-	B3	B3	PF5			ECS3_N								I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
2	2	1	B2	B2	PF6			EBELL_N								I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
3	3	2	B1	B1	PF7		INT05b	EBELH_N			TSPI2CSIN	TSPI2CS0				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
4	4	-	D4	D4	PC7		INT15a	EA23								I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
5	5	-	E4	E4	PC6		INT14a	EA22								I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
6	6	-	C2	C2	PC5			EA21		T32A10OUTB						I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
7	7	-	C1	C1	PC4			EA20		T32A10OUTA		T32A10OUTC				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
8	8	-	D2	D2	PC3			EA19		T32A08OUTB	I2S1LRCK					I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
9	9	-	D1	D1	PC2			EA18		T32A08OUTA	I2S1BCK	T32A08OUTC				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
10	10	-	F5	F5	PC1		INT13a	EA17		T32A08INB0	I2S1DI	T32A08INC1				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
11	11	-	F4	F4	PC0		INT12a	EA16		T32A08INA0	I2S1DO	T32A08INC0				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
12	12	3	A1	A1	DVDD3A											-	-	-	-	-	-	-
13	13	4	M1	K1	DVSSA											-	-	-	-	-	-	-
14	14	5	G5	G5	PB7		INT07a	EA15	T32A03INA1	T32A03INB0	I2S0DO	T32A03INC1				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
15	15	6	G4	G4	PB6		INT06a	EA14	T32A03INB1	T32A03INA0	I2S0DI	T32A03INC0				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
16	16	7	E2	E2	PB5			EA13		T32A03OUTB	I2S0BCK					I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
17	17	8	E1	E1	PB4			EA12		T32A03OUTA	I2S0LRCK	T32A03OUTC				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
18	18	9	F2	F2	PB3			EA11		T32A02OUTB						I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
19	19	10	F1	F1	PB2			EA10		T32A02OUTA		T32A02OUTC				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
20	20	11	G2	H5	PB1		INT05a	EA09	T32A02INA1	T32A02INB0		T32A02INC1	HDMAREQA			I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
21	21	12	G1	H4	PB0		INT04a	EA08	T32A02INB1	T32A02INA0	I2S0MCLK	T32A02INC0				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
22	22	13	H2	J5	PA7		INT03a	EA07	T32A01INA1	T32A01INB0		T32A01INC1	TSPI2CSIN	TSPI2CS0		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
23	23	14	H1	G2	PA6			EA06		T32A01OUTB			TSPI0CS3	TSPI2SCK		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
24	24	15	J2	G1	PA5			EA05		T32A01OUTA		T32A01OUTC	TSPI0CS2	TSPI2RXD		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
25	25	16	J1	H2	PA4			EA04	T32A01INB1	T32A01INA0		T32A01INC0	TSPI0CS1	TSPI2TXD		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
26	26	17	K2	H1	PA3			EA03	T32A00INA1	T32A00INB0		T32A00INC1	TSPI2CS1	TSPI0TXD		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
27	27	18	K1	J2	PA2			EA02		T32A00OUTB				TSPI0RXD		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
28	28	19	L2	J1	PA1			EA01		T32A00OUTA		T32A00OUTC		TSPI0SCK		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
29	29	20	L1	J4	PA0		INT02a	EA00	T32A00INB1	T32A00INA0		T32A00INC0	TSPI0CSIN	TSPI0CS0		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
30	30	21	M2	K2	PY4	BOOT_N		ISDCOUT			EEXBCLK					Output	PU/PD	YES	N/A	SMT	Hi-Z (Note1)	Hi-Z
31	31	22	H5	K4	PT3		INT00b	RTCOUT	T32A03OUTA	T32A03OUTC	RXIN0		TRGIN2			I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
32	32	-	R2	N2	DVDD3B											-	-	-	-	-	-	-
33	33	-	N2	L2	DVSSB											-	-	-	-	-	-	-
34	-	-	H4	-	PU0				T32A12OUTA	T32A12OUTC				UT4TXDA		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
35	-	-	J4	-	PU1				T32A12OUTB					UT4RXD		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
36	-	-	J5	-	PU2		INT06b		T32A12INA0	T32A12INC0			TSSI1TCK	UT4CTS_N		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
37	-	-	K4	-	PU3		INT07b		T32A12INB0	T32A12INC1			TSSI1TFS	UT4RTS_N		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
38	-	-	K5	-	PU4		INT08b		T32A13INB0	T32A13INC1			TSSI1TXD	UT3RTS_N		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
39	-	-	L5	-	PU5		INT09b		T32A13INA0	T32A13INC0			TSSI1RXD	UT3CTS_N		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
40	-	-	L4	-	PU6				T32A13OUTA	T32A13OUTC			TSSI1RFS	UT3RXD		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
41	-	-	M4	-	PU7				T32A13OUTB				TSSI1RCK	UT3TXDA		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
42	34	23	R1	N1	RESET_N											-	PU	-	-	SMT	-	-
43	35	24	N1	L1	PY3	XT2										Input	PU/PD	-	N/A	SMT	Hi-Z	Hi-Z
44	36	25	P1	M1	PY2	XT1/ ELCLKIN										Input	PU/PD	-	N/A	SMT	Hi-Z	Hi-Z
45	37	26	T2	P2	PY0	X1/ EHCLKIN										Input	PU/PD	-	N/A	SMT	Hi-Z	Hi-Z
46	38	27	T3	P3	PY1	X2										Input	PU/PD	-	N/A	SMT	Hi-Z	Hi-Z
47	39	28	T1	P1	MODE											-	PD	-	-	SMT	-	-
48	40	29	N5	L4	PD0			ED00/EAD00	T32A04INB1	T32A04INA0	TSPI4CS0	T32A04INC0	TSPI4CSIN	UO0		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
49	41	30	M6	L5	PD1			ED01/EAD01	T32A04INA1	T32A04INB0	TSPI4SCK	T32A04INC1		XO0		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
50	42	31	N6	K6	PD2			ED02/EAD02		T32A04OUTA	TSPI4RXD	T32A04OUTC		VO0	TSSI0TCK	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
51	43	32	M7	L6	PD3			ED03/EAD03		T32A04OUTB	TSPI4TXD			YO0	TSSI0TFS	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
52	44	33	N7	L7	PD4			ED04/EAD04		T32A05OUTA		T32A05OUTC	I2S0LRCK	WO0	TSSI0TXD	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
53	45	34	M8	K7	PD5			ED05/EAD05		T32A05OUTB			I2S0BCK	ZO0	TSSI0RXD	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
54	46	35	N8	K8	PD6			ED06/EAD06	T32A05INB1	T32A05INA0		T32A05INC0	I2S0DI	EMG0	TSSI0RFS	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
55	47	36	M9	L8	PD7			ED07/EAD07	T32A05INA1	T32A05INB0		T32A05INC1	I2S0DO	OVV0	TSSI0RCK	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
56	48	-	R3	N3	DVDD3C											-	-	-	-	-	-	-
57	49	-	P2	M2	DVSSC											-	-	-	-	-	-	-

M4GR LQFP176	M4GQ LQFP144	M4GN LQFP100	M4GR BGA177	M4GQ BGA145	Pin Name	Function A	Function B	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Input / Output	PU/PD	OD	5VT / 3VT	SMT / CMOS	Under Reset	After Reset
58	50	37	R4	N4	PE0			ED08/EAD08	T32A06INB1	T32A06OUTB	EA23	T32A06INA1		UT0RTS_N	EA15	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
59	51	38	R5	N5	PE1			ED09/EAD09		T32A06OUTA	EA22	T32A06OUTC		UT0CTS_N	EA14	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
60	52	39	T5	P5	PE2			ED10/EAD10		T32A06INA0	EA21	T32A06INC0		UT0RXD	EA13	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
61	53	40	T6	N6	PE3			ED11/EAD11		T32A06INB0	EA20	T32A06INC1		UT0TXDA	EA12	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
62	54	41	R6	P6	PE4			ED12/EAD12		T32A07INA0	EA19	T32A07INC0	I2S1DO	ISDAIN0	EA11	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
63	55	42	R7	P7	PE5			ED13/EAD13		T32A07INB0	EA18	T32A07INC1	I2S1DI	ISDAIN1	EA10	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
64	56	43	T7	N7	PE6			ED14/EAD14		T32A07OUTA	EA17	T32A07OUTC	I2S1BCK	ISDAIN2	EA09	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
65	57	44	T8	N8	PE7			ED15/EAD15	T32A07INB1	T32A07OUTB	EA16	T32A07INA1	I2S1LRCK	ISDAIN3	EA08	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
66	-	-	N9	-	PJ7							FUT1RXD	EI2C3SCL	I2C3SCL		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
67	-	-	R8	-	PJ6							FUT1TXD	EI2C3SDA	I2C3SDA		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
68	-	-	R9	-	PJ5				T32A03INB0	T32A03INC1		FUT0RXD				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
69	-	-	T9	-	PJ4				T32A03INA0	T32A03INC0		FUT0TXD				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
70	58	45	T10	P8	REGOUT1											-	-	-	-	-	-	-
71	59	46	M12	K10	DVDD3D											-	-	-	-	-	-	-
72	60	47	E12	E10	DVSSD											-	-	-	-	-	-	-
-	-	-	T16	P14	BSC											-	PD	-	-	SMT	-	-
73	61	-	R10	K9	PT5		INT02b		T32A03OUTB							I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
74	-	-	N10	-	PW3						TSPI8TXD	T32A01OUTB				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
75	-	-	M10	-	PW2						TSPI8RXD	T32A01OUTA		T32A01OUTC		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
76	-	-	N11	-	PW1						TSPI8SCK	T32A00OUTA		T32A00OUTC		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
77	-	-	M11	-	PW0						TSPI8CS0	T32A00OUTB	TSPI8CSIN			I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
78	62	-	R11	L9	PV7				T32A05OUTB		TSPI5CS0	OVV0	TSPI5CSIN	UT1RTS_N		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
79	63	-	T11	N9	PV6				T32A05OUTA	T32A05OUTC	TSPI5SCK	EMG0		UT1CTS_N		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
80	64	-	T12	P9	PV5			EI2C2SDA	T32A04OUTA	T32A04OUTC	TSPI5TXD	ZO0	I2C2SDA	UT1TXDA		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
81	65	-	R12	N10	PV4			EI2C2SCL	T32A04OUTB		TSPI5RXD	WO0	I2C2SCL	UT1RXD		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
82	66	-	T13	P10	PM7			EI2C4SCL	T32A07OUTB		I2C4SCL	FUT1IROUT	TSPI7TXD	FUT1TXD		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
83	67	-	R13	N11	PM6			EI2C4SDA	T32A07OUTA	T32A07OUTC	I2C4SDA	FUT1IRIN	TSPI7RXD	FUT1RXD		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
84	68	-	T14	P11	PM5				T32A06OUTA	T32A06OUTC			TSPI7SCK	FUT1RTS_N		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
85	69	-	N12	L10	PM4		INT15b		T32A06OUTB		TSPI7CSIN		TSPI7CS0	FUT1CTS_N		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
86	70	48	R14	N12	PH7			TRST_N		UT0CTS_N		UT0RTS_N				I/O	PU/PD	YES	N/A	SMT	PU (Note2)	PU (Note2)
87	71	49	R15	P12	PH6			TDO/SWV		UT0RTS_N		UT0CTS_N				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
88	72	50	T15	P13	PH5			TCK/SWCLK		UT0TXDA		UT0RXD				I/O	PU/PD	YES	N/A	SMT	PD (Note2)	PD (Note2)
89	73	51	R16	N14	PH4			TMS/SWDIO		UT0RXD		UT0TXDA				I/O	PU/PD	YES	N/A	SMT	PU (Note2)	PU (Note2)
90	74	52	P15	N13	PH3			TDI		UT1CTS_N	NBDSYNC	UT1RTS_N				I/O	PU/PD	YES	N/A	SMT	PU (Note2)	PU (Note2)
91	75	53	P16	M14	PH2			TRACEDATA3		UT1RTS_N	NBDDATA3	UT1CTS_N				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
92	76	54	N15	M13	PH1			TRACEDATA2		UT1TXDA	NBDDATA2	UT1RXD				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
93	77	55	N16	L11	PH0			TRACEDATA1		UT1RXD	NBDDATA1	UT1TXDA				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
94	78	56	M15	L13	PG7			TRACEDATA0			NBDDATA0	FUT0CTS_N				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
95	79	57	M16	L14	PG6			TRACECLK			NBDCLK	FUT0RTS_N	I2S1MCLK			I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
96	80	58	M13	K11	PG5				T32A02OUTA	T32A02OUTC	FUT0IRIN	FUT0RXD	EI2C2SCL	I2C2SCL		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
97	81	59	L12	K13	PG4				T32A02OUTB		FUT0IROUT	FUT0TXD	EI2C2SDA	I2C2SDA		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
98	-	-	N13	-	DVDD3E											-	-	-	-	-	-	-
99	-	-	D13	-	DVSSE											-	-	-	-	-	-	-
100	82	60	L16	K14	PL3				T32A02INB0	T32A02INC1		SMI0D7	TSPI3CS1	TSPI1TXD		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
101	83	61	L15	J13	PL2							SMI0D6		TSPI1RXD		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
102	84	62	K16	J14	PL1							SMI0D5		TSPI1SCK		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
103	85	63	L13	J11	PL0		INT01a		T32A02INA0	T32A02INC0		SMI0D4	TSPI1CSIN	TSPI1CS0		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
104	86	64	K12	J10	PK7		INT00a		T32A01INB0	T32A01INC1	TSPI3CS0		SMI0CS0_N	TSPI3CSIN		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
105	87	65	J16	H14	PK6			TSPI1CS3	T32A01INA0	T32A01INC0	TSPI3SCK		SMI0CLK			I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
106	88	66	K15	H13	PK5			TSPI1CS2			TSPI3RXD		SMI0D3			I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
107	89	67	J15	G14	PK4			TSPI1CS1			TSPI3TXD		SMI0D2			I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
108	90	68	K13	G13	PK3			ECS1_N					SMI0D1			I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
109	91	69	J13	F14	PK2			ECS0_N					SMI0D0			I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
110	92	70	J12	H11	PK1		INT11a	ISDBOUT	T32A00INB0	T32A00INC1	HDMAREQB	TSPI3CS0	TSPI3CSIN			I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
111	93	71	H12	H10	PK0		INT10a	ISDAOUT	T32A00INA0	T32A00INC0			SMI0CS1_N			I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
112	94	-	H13	G10	PV3				T32A09OUTB		ISDBIN3	YO0	UT3CTS_N	UT3RTS_N		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
113	95	-	G12	G11	PV2				T32A09OUTA	T32A09OUTC	ISDBIN2	VO0	UT3RTS_N	UT3CTS_N		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
114	96	-	G13	F11	PV1				T32A09INB0	T32A09INC1	ISDBIN1	XO0	UT3TXDA	UT3RXD		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
115	97	-	F12	F10	PV0				T32A09INA0	T32A09INC0	ISDBIN0	UO0	UT3RXD	UT3TXDA		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
116	98	-	F13	E11	PT4		INT01b				RXIN1					I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
117	-	-	H16	-	PW7					T32A10INA1		T32A11OUTB	ISDCIN3	T32A11INA0		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
118	-	-	H15	-	PW6							T32A11OUTA	ISDCIN2	T32A11OUTC		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
119	-	-	G16	-	PW5							T32A10OUTA	ISDCIN1	T32A10OUTC		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
120	-	-	G15	-	PW4					T32A11INA1		T32A10OUTB	ISDCIN0	T32A10INA0		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
121	99	-	E13	F13	PM3		INT14b		T32A11OUTB		TSPI6CSIN	UT4CTS_N	TSPI6CS0	UT4RTS_N		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
122	100	-	F16	E14	PM2				T32A11OUTA	T32A11OUTC		UT4RTS_N	TSPI6SCK	UT4CTS_N		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z

M4GR LQFP176	M4GQ LQFP144	M4GN LQFP100	M4GR BGA177	M4GQ BGA145	Pin Name	Function A	Function B	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Input / Output	PU/PD	OD	5VT / 3VT	SMT / CMOS	Under Reset	After Reset
123	101	-	F15	E13	PM1			EI2C3SCL			I2C3SCL	UT4TXDA	TSPI6RXD	UT4RXD		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
124	102	-	E16	D14	PM0			EI2C3SDA			I2C3SDA	UT4RXD	TSPI6TXD	UT4TXDA		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
125	-	-	E15	-	PL5		INT13b		T32A08OUTB							I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
126	-	-	D16	-	PL4		INT12b		T32A08OUTA	T32A08OUTC						I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
127	103	-	T4	P4	DVDD3F											-	-	-	-	-	-	-
128	104	-	A16	A14	DVSSF											-	-	-	-	-	-	-
129	105	72	D15	D13	PG0		INT08a	EALE		UT2RXD		UT2TXDA				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
130	106	73	C16	C14	PG1		INT09a	EWAIT_N		UT2TXDA		UT2RXD				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
131	107	74	C15	C13	PG2					UT2RTS_N	ALARM_N	UT2CTS_N	EI2C0SDA	I2C0SDA		I/O	PU/PD	YES	5VT	SMT	Hi-Z	Hi-Z
132	108	75	B16	B14	PG3					UT2CTS_N	TRGIN0	UT2RTS_N	EI2C0SCL	I2C0SCL		I/O	PU/PD	YES	5VT	SMT	Hi-Z	Hi-Z
133	109	76	B15	B13	PN0	AINA00										I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
134	110	77	A15	A13	PN1	AINA01										I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
135	111	78	B14	B12	PN2	AINA02										I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
136	112	79	A14	A12	PN3	AINA03										I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
137	113	80	B13	B11	PN4	AINA04										I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
138	114	81	A13	A11	PN5	AINA05										I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
139	115	82	B12	B10	PN6	AINA06										I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
140	116	83	A12	A10	PN7	AINA07										I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
141	117	84	D12	D11	PP0	AINA08			T32A04INA0	T32A04INC0		T32A04INB1				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
142	118	85	D11	D10	PP1	AINA09			T32A04INB0	T32A04INC1		T32A04INA1				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
143	119	86	B11	B9	PP2	AINA10			T32A05INA0	T32A05INC0		T32A05INB1				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
144	120	87	A11	A9	PP3	AINA11			T32A05INB0	T32A05INC1		T32A05INA1				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
145	121	88	E11	D9	PP4	AINA12			T32A06INA0	T32A06INC0		T32A06INB1				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
146	122	89	D10	E9	PP5	AINA13			T32A06INB0	T32A06INC1		T32A06INA1				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
147	123	90	B10	B8	PP6	AINA14	INT10b		T32A07INA0	T32A07INC0		T32A07INB1				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
148	124	91	A10	A8	PP7	AINA15	INT11b		T32A07INB0	T32A07INC1		T32A07INA1				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
149	125	-	E10	D8	PR0	AINA16			T32A08INA0	T32A08INC0						I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
150	126	-	D9	E8	PR1	AINA17			T32A08INB0	T32A08INC1						I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
151	127	-	B9	B7	PR2	AINA18			T32A09INA0	T32A09INC0						I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
152	128	-	A9	A7	PR3	AINA19			T32A09INB0	T32A09INC1						I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
153	129	-	A8	D7	PR4	AINA20			T32A10INA0	T32A10INC0						I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
154	130	-	B8	E7	PR5	AINA21			T32A10INB0	T32A10INC1						I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
155	131	-	E9	E6	PR6	AINA22			T32A11INA0	T32A11INC0						I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
156	132	-	D8	D6	PR7	AINA23			T32A11INB0	T32A11INC1						I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
157	133	92	A7	A6	AVDD3											-	-	-	-	-	-	-
158	134	93	B7	B6	AVSS											-	-	-	-	-	-	-
159	135	94	A6	A5	PT0	DAC0										I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
160	136	95	A5	A4	PT1	DAC1										I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
161	137	-	M5	K5	DVDD3G											-	-	-	-	-	-	-
162	138	-	F6	F6	DVSSG											-	-	-	-	-	-	-
163	-	-	E8	-	PL7			TRGIN1	T32A09OUTB							I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
164	-	-	E7	-	PL6		INT03b		T32A09OUTA	T32A09OUTC						I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
165	-	-	D7	-	PJ3					UT5CTS_N		UT5RTS_N	EI2C4SDA	I2C4SDA		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
166	-	-	D6	-	PJ2					UT5RTS_N		UT5CTS_N	EI2C4SCL	I2C4SCL		I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
167	-	-	B6	-	PJ1					UT5TXDA		UT5RXD				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
168	-	-	B5	-	PJ0					UT5RXD		UT5TXDA				I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
169	-	-	N4	-	DVDD3H											-	-	-	-	-	-	-
170	-	-	E5	-	DVSSH											-	-	-	-	-	-	-
171	139	96	E6	E5	PT2									CEC0		I/O	PU/PD	YES	3VT	SMT	Hi-Z	Hi-Z
172	140	97	D5	D5	PF0		INT04b	ERD_N								I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
173	141	98	A4	B5	PF1			EWR_N								I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
174	142	99	B4	B4	PF2								EI2C1SDA	I2C1SDA		I/O	PU/PD	YES	5VT	SMT	Hi-Z	Hi-Z
175	143	100	A3	A3	PF3								EI2C1SCL	I2C1SCL		I/O	PU/PD	YES	5VT	SMT	Hi-Z	Hi-Z
176	144	-	A2	A2	PF4			ECS2_N								I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z

Note1: The built-in pull-up is ON during the reset period by the reset terminal (RESET_N) and POR.

Note2: The Initial value of built-in Pull-up/Pull-down resistor is ON.

Note3: Some functions may not be available depending on the product. For details, refer to the Reference Manual "Product Individual Information".

Part Naming Conventions

TMP M4G R F 20 x FG

The identification of Toshiba microcontrollers

Core

Symbol	Core
M4	Arm Cortex-M4 processor with FPU
M3	Arm Cortex-M3
M0	Arm Cortex-M0

Product Group

Family	Group	Application
TXZ TXZ+	H	For General-purpose/Consumer electronic equipment
	K	For Motor/Inverter control industrial equipment(MCU+AMP/COMP)
	M	For Motor/Inverter control industrial equipment(MCU+AMP/COMP/CAN)
	G	For OA/Digital equipment/industrial equipment
	E	For Precision instruments control
	J	For FA/Inverter control industrial Robotics
	L	For Motor/Inverter control industrial equipment
	N	Sensor Hub/USB equipment
	U	For General purpose/Consume electronic equipment (Entry Series)
	V	

Pin Count

Symbol		Pin Count	Symbol		Pin Count
0	G	Under 32pin	8	Q	129pin to 144pin
1	H	33pin to 44pin	9	R	145pin to 176pin
2	J	45pin to 48pin	A	S	177pin to 200pin
3	K	49pin to 52pin	B	T	201pin to 224pin
4	L	53pin to 64pin	C	U	225pin to 250pin
5	M	65pin to 80pin	D	V	251pin to 300pin
6	N	81pin to 100pin			
7	P	101pin to 128pin			

Revision

Package

Symbol	Package
QG	Plastic shrink quad outline non-leaded package; dry-packed
UG.DUG, FG,DFG	Plastic quad flat package; dry-packed
MG,DMG	Plastic small-outline package; dry-packed
XBG	Plastic ball grid array; dry-packed

ROM Size

Symbol	Size[KB]
M	32
P	48
S	64
U	96
W	128
Y	256
Z	384
D	512
E	768
10	1,024
15	1,536
20	2,048
40	4,096
80	8,192

ROM Type

Symbol	Type
F	Flash
C	Mask

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