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May 2016

FSA7830
8-Channel Voltage MUX with Integrated Voltage Divider and OVP

Features

- Voltage Supply, 2.7 to 5.5 V
- Input Voltage Range, 0 to 5.4 V
- Up to 8-Channel Inputs
- Integrated 1/3, 2/3 Voltage Divider
- Integrated Over-Voltage Protection and Assertion
- Total Introduced Offset < ±10 mV
- I_{CC} < 100 µA, Ishutdown < 1 µA
- 1.8 V I^2C Interface, Addr<1:0> to Set Address for Multi Chip Solution
- 16-Ball, 0.4 mm Pitch, 1.56 mm ×1.56 mm, WLCSP Package

Applications

- Cell Phones
- Tablets

Description

The FSA7830 is an 8-Channel, low-power Voltage MUX.

It integrates 8 analog switches for input voltage selection, and voltage dividers to provide 1/3, 2/3 fraction of selected voltage. With another 3 analog switches, FSA7830 provides feasibility to choose 1/3, 2/3 or 1 times of selected voltage.

FSA7830 also contains output buffer to enhance driving capability. It features over-voltage protection to ensure output less than 2 V, interrupt will be alerted at the same time.

FSA7830 supports 1.8 V I2C interface to communicate with processor, and 2 address pins to provide multi-chip solution.

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FSA7830BUCX	GT	-40 to +85°C	16-Ball, 0.4 mm Pitch Wafer Level Chip Scale Package (WLCSP) Package (1.56 x 1.56 mm)

Typical Application

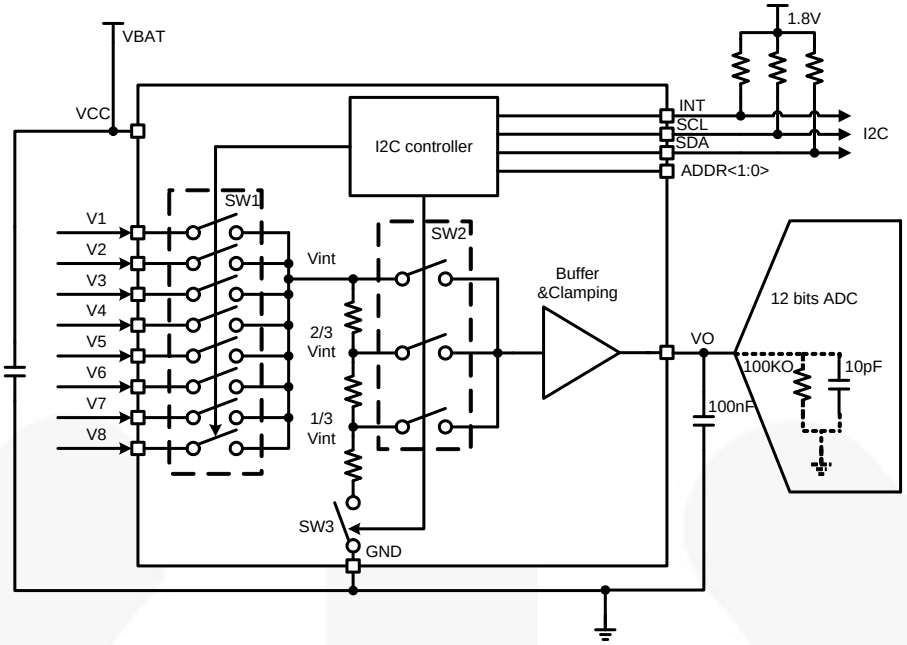


Figure 1. Application Diagram

Pin Configuration

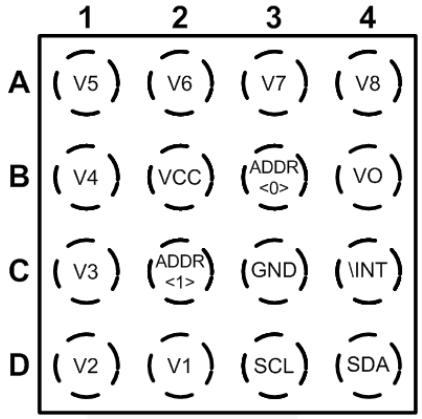


Figure 2. 16 Ball WLCSP Package(Top View)

Pin Definitions

Pin#	Name	Description
A1	V5	Input Port 5
A2	V6	Input Port 6
A3	V7	Input Port 7
A4	V8	Input Port 8
B1	V4	Input Port 4
B2	VCC	Voltage Supply
B3	ADDR<0>	Address Pin, Bit 0
B4	VO	Output Voltage
C1	V3	Input Port 3
C2	ADDR<1>	Address Pin, Bit 1
C3	GND	Ground
C4	\INT	I2C Interrupt
D1	V2	Input Port 2
D2	V1	Input Port 1
D3	SCL	I2C Clock
D4	SDA	I2C Data

I2C Specifications

Symbol	Parameter	Fast Mode		
		Min.	Max.	Unit
f_{SCL}	I2C_SCL Clock Frequency	0	400	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.6		µs
t_{LOW}	LOW Period of I2C_SCL Clock	1.3		µs
t_{HIGH}	HIGH Period of I2C_SCL Clock	0.6		µs
$t_{SU;STA}$	Set-up Time for Repeated START Condition	0.6		µs
$t_{HD;DAT}$	Data Hold Time	0	0.9	µs
$t_{SU;DAT}$	Data Set-up Time(1)	100		ns
t_r	Rise Time of I2C_SDA and I2C_SCL Signals(1)	20+0.1C_b	300	ns
t_f	Fall Time of I2C_SDA and I2C_SCL Signals(1)	20+0.1C_b	300	ns
$t_{SU;STO}$	Set-up Time for STOP Condition	0.6		µs
t_{BUF}	BUS-Free Time between STOP and START Conditions	1.3		µs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

Note:

1. A fast-mode I2C-bus device can be used in a standard-mode I2C-bus system, but the requirement $t_{SU;DAT} \geq$ 250 ns must be met. This is automatically the case if the device does not stretch the LOW period of the I2C_SCL signal. If such a device does stretch the LOW period of the I2C_SCL signal, it must output the next data bit to the I2C_SDA line $t_{r\_max} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the standard-mode I2C bus specification) before the I2C_SCL line is released.

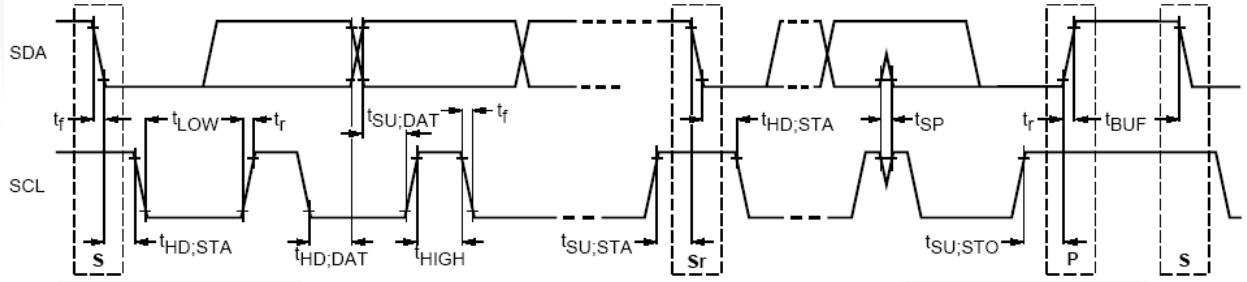


Figure 1. Definition of Timing for Full-Speed Mode Devices on the I2C Bus

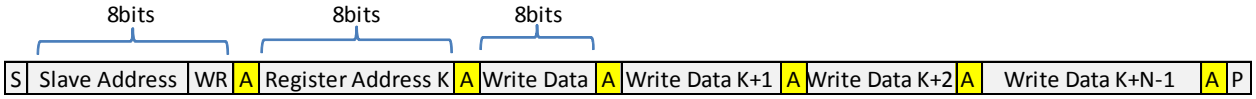
Table 1. I²C™ Slave Address

ADDR<1:0>	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	1	0	0	0	0	1	0	R/W
01	1	0	0	0	0	1	1	R/W
10	1	0	0	0	1	0	1	R/W
11	1	0	1	0	1	0	0	R/W

I2C Interface

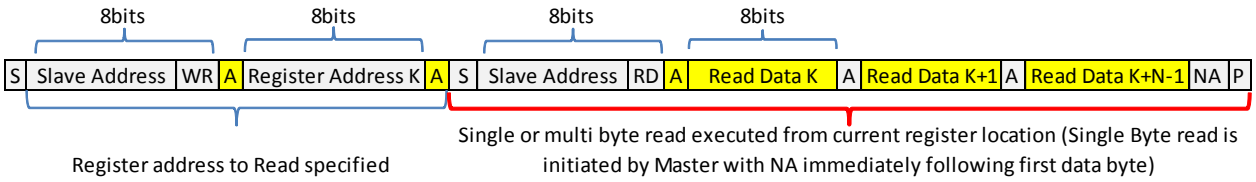
The FSA7830 includes a full I2C slave controller. The I2C slave fully complies with the I2C specification version 2.1 requirements. This block is designed for fast mode, 400 kHz, signals.

Examples of an I2C write and read sequence are shown in below Figure 3 and Figure 4 respectively.



Note: Single Byte read is initiated by Master with P immediately following first data byte

Figure 3. I2C Write Example



Note: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed

	From Master to Slave	**S**	Start Condition	**NA**	NOT Acknowledge (SDA High)	**RD**	Read =1
	From Slave to Master	**A**	Acknowledge (SDA Low)	**WR**	Write=0	**P**	Stop Condition

Figure 4. I2C Read Example

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	6	V
V1~8	Input Voltage		-0.5	6	V
I_{IK}	DC Input Diode Current		-50		mA
T_{STG}	Storage Temperature		-65	+150	°C
MSL	Moisture Sensitivity Level (JEDEC J-STD-020A)			1	Level
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins	2		kV
		I/O to GND	2		
		Power to GND	2		
	Charged Device Model, JEDEC: JESD22-C101		500		V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.7	5.5	V
V1~8	Input Voltage	0	5.4	V
V_{ADDR}	Address Pin Voltage	0	V_{CC}	V
$V_{SCL,SDA,\overline{INT}}$	I2C Bus Voltage Swing	0	1.8	V
T_A	Operating Temperature	-40	+85	°C

DC Electrical Characteristics

All typical value are for V_{CC}=3.7 V at T_A=25°C, with 100 KΩ and 100 nF+10 pF loading at VO, unless otherwise specified.

Symbol	Parameter	Condition	V_{CC} (V)	T_A=- 40°C to +85°C			Unit
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	I_{IN}=-18 mA				-0.7	V
V_{IHI2C}	High-Level Input Voltage		2.7 to 5.5	1.26			V
V_{ILI2C}	Low-Level Input Voltage		2.7 to 5.5			0.54	V
V_{HYSI2C}	Hysteresis of Schmitt Trigger Inputs		2.7 to 5.5	0.09			V
I_{I2C}	Input Current of SDA, SCL and \INT	Input Voltage 0.26 V to 2 V	2.7 to 5.5	-10		10	µA
I_{CCTI2C}	V_{CC} current when SDA or SCL is HIGH	Input Voltage 1.8 V	5.5			1	µA
V_{IHADDR}	High-Level Input Voltage		2.7 to 5.5	1.26			V
V_{ILADDR}	Low-Level Input Voltage		2.7 to 5.5			0.54	V
$V_{HYSADDR}$	Hysteresis of Schmitt Trigger Inputs		2.7 to 5.5	0.09			V
V_{OLSDA}	Low-Level Output Voltage of SDA Pin	4 mA Sink Current (Open-Drain)	2.7 to 5.5			0.36	V
V_{OLINTN}	Low-Level Output Voltage of \INT	4 mA Sink Current (Open-Drain)	2.7 to 5.5			0.36	V
R_{ON1}	Switch1 On Resistance		2.7 to 5.5		100	200	Ω
R_{ON2}	Switch2 On Resistance[2]		2.7 to 5.5		100	200	Ω
R_{VD}	Voltage Divider On Resistance[2]		2.7 to 5.5	1			MΩ
I_{CC}	Quiescent Supply Current	All blocks in Enable Mode	2.7 to 5.5			100	µA
I_{CCZ}	Disable Mode Leakage Current		2.7 to 5.5	-1		3.9	µA
$I_{LEAK,ON}$	Leakage Current of each channel from V1~8 to GND in Enable Mode					2	µA
$I_{LEAK,OFF}$	Leakage Current of each channel from V1~8 to GND in Disable Mode					1	µA
V_{OFFSET}	Offset Voltage introduced by FSA7830, referring to VO		2.7 to 5.5	-10		10	mV
V_{OVP}	Over-Voltage Protection Threshold (Low to High)	Register 06h set to ‘00’	2.7 to 5.5	1.87	2.00	2.15	V
$V_{OVP,HYS}$	Over-Voltage Assertion Hysteresis		2.7 to 5.5		50		mV
$V_{CLAMPING}$	Clamping Voltage on VO when OVP happens	Register 06h set to ‘00’	2.7 to 5.5	1.87	2.00	2.15	V
$V_{O,DYNAMIC}$	VO Dynamic Range	100 KΩ between VO to 0.9 V, output buffer has the ability to drive the target value with maximum 1% mismatch	2.7 to 5.5	0.5		2.1	V

Note:

2. Guaranteed by Design.

AC Electrical Characteristics

All typical value are for V_{CC}=4.2 V at T_A=25°C, with 100 KΩ and 100 nF+10 pF loading at VO, unless otherwise specified.

Symbol	Parameter	Condition	V_{CC} (V)	T_A=- 40°C to +85°C			Unit
				Min.	Typ.	Max.	
C_I	Input Capacitance on V1~8[3]	F=1 MHz	2.7 to 5.5			50	pF
$t_{SETTLING}$	VO Settling Time after each Switching[3]	R_S=50 Ω, C_O=100 nF+10 pF, R_O=100 KΩ, VO reaches 99% of target value	2.7 to 5.5			200	µs
$t_{LOADRESPONSE}$	VO Buffer Load Response, Settling Time of Load Change[3]	Loading on VO switches from 100 nF to C_O=100 nF+10 pF, R_O=100 K. VO reaches 99% of target value	2.7 to 5.5			150	ns
PSRR	Power Supply Rejection Ratio of VO from V_{CC}	Power supply noise, F=217 Hz, Vpp=50 mV, C_O=100 nF+10 pF, R_O=100 KΩ	2.7 to 5.5		70		dB
Xtalk	Cross Talk between V1~8	F=500 KHz, Vpp=50 mV, C_O=100 nF+10 pF, R_O=100 KΩ	2.7 to 5.5		80		dB

Note:

3. Guaranteed by characterization and not tested in production.

Application Information

Interrupt operation

The \INT pin is an active low, open drain output which indicates to the host processor that an interrupt has occurred in the FSA7830 which needs attention. The \INT pin is HIGH-Z by default after power-up or device reset.

The \INT pin stays HIGH-Z in preparation of future interrupts. When an interruptible event occurs, \INT is driven LOW and is HIGH-Z again when the processor clears the interrupt by reading the interrupt registers.

Subsequent to the initial power up or reset; if the processor writes a “1” to one of interrupt mask bits when the system is already powered up, the \INT pin stays HIGH-Z and ignores corresponding interrupt until the interrupt mask bit is cleared. If an event happens that would ordinarily cause an interrupt when the interrupt mask bit is set, the \INT pin goes LOW when the interrupt mask is cleared.

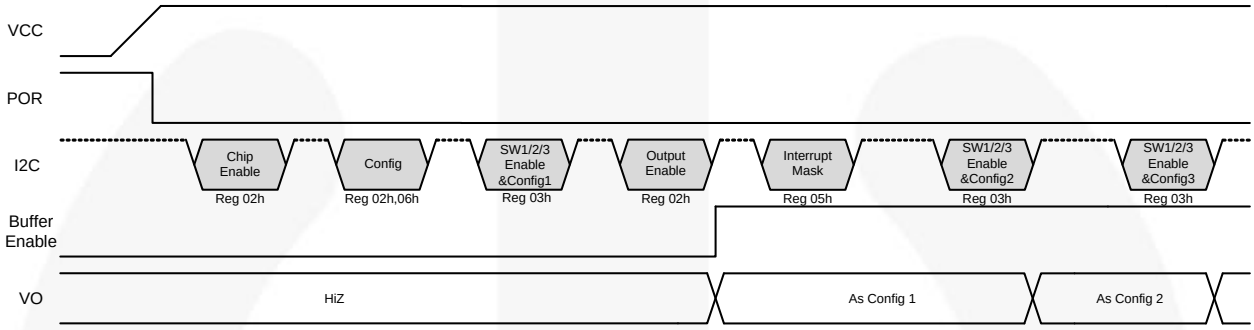


Figure 5. Typical Application Sequence

Buffer & Clamping Enable Truth Table

To prevent non-ideal waveforms on VO node, enable of Output Buffer and Clamping circuitry depends on status of multi-internal register values.

Table 2. Register Map

Registers					Buffer & Clamping Enable
Chip Enable	SW1 Enable	SW2 Enable	SW3 Enable	Output Enable	
0	x	x	x	x	0
1	0	x	x	x	0
1	x	0	x	x	0
1	1	1	x	0	0
1	1	1	x	1	1

Register Definitions

Table 3. Register Map

Address	Register Name	Type	Rst Val	Description
0x01	Device ID	RO	08	Device Version and Revision
0x02	Control	RW	00	Device Control
0x03	SWCTL	RW	00	Switch Status Control
0x04	INT	RO	00	Interrupt
0x05	INT_MASK	RW	80	Interrupt Mask
0x06	OVP	RW	00	OVP Threshold

Notes:
4. Do not use registers that are blank.
5. Values read from undefined register bits are not defined and invalid. Do not write to undefined registers.

Table 4. Register Device ID

Address: 01h

Reset Value: 0x0000_1000

Type: Read

Bits	Name	Size	Description
7:6	Vendor ID	2	Vendor ID
5:3	Version ID	3	Device Version ID
2:0	Revision ID	3	Revision History ID

Table 5. Control

Address: 02h

Reset Value: 0x0000_0000

Type: Read/Write

Bits	Name	Size	Description
7	Chip Enable	1	FSA7830 Enable/Shutdown **0: Shutdown (all other registers, including bits<6:0> of this register, reset to default value)** 1: Enable
6	Output Enable	1	Output Buffer Enable **0: Disable, VO maintains HiZ** 1: Enable
<5:4>	OVP action	2	Actions after OVP **00: Clamp output voltage to 2 V (based on register 06h)** 01: Pull VO to 0V 10: No Action
<3:0>	Reserved	4	Do Not Use

Table 6. SWCTL

Address: 03h
Reset Value: 0x0000_0000
Type: Read/Write

Bits	Name	Size	Description
7	SW1 Enable	1	Switch 1 Enable **0: All Switches Off** 1: One switch on, status based on <6:4>
<6:4>	SW1 Control	3	Switch 1 Control **000: V1 to Vint** 001: V2 to Vint 010: V3 to Vint 011: V4 to Vint 100: V5 to Vint 101: V6 to Vint 110: V7 to Vint 111: V8 to Vint
3	SW2 Enable	1	Switch 2 Enable **0: All Switches Off** 1: One switch on, status based on <2:1>
<2:1>	SW2 Control	2	Switch 2 Control **00: VO to Vint** 01: VO to 1/3Vint 10: VO to 2/3Vint 11: Reserved
0	SW3 Control	1	Switch 3 Control **0: SW3 OFF** 1: SW3 ON

Table 7. INT

Address: 04h
Reset Value: 0x0000_0000
Type: Read/Clear

Bits	Name	Size	Description
7	OVP	1	**0: OVP event has not occurred** 1: OVP event has occurred
<6:0>	Reserved	7	Do Not Use

Table 8. INT_MASK

Address: 05h
Reset Value: 0x1000_0000
Type: Read/Write

Bits	Name	Size	Description
7	OVP	1	0: Do not mask OVP interrupt **1: Mask OVP interrupt**
<6:0>	Reserved	7	Do Not Use

Table 9. OVP

Address: 06h

Reset Value: 0x0000_0000

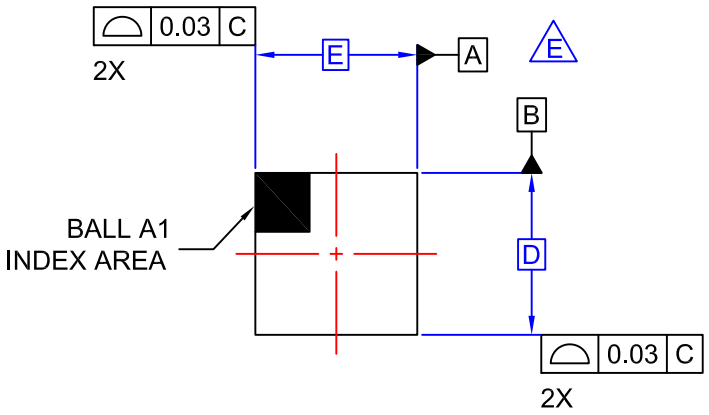
Type: Read/Write

Bits	Name	Size	Description
<7:3>	Reserved	5	Do Not Use
<2:0>	OVP Threshold	3	Over-voltage protection threshold **000: Default** 001: +50 mV 010: +100 mV 011: -250 mV 100: -50 mV 101: -100 mV 110: -150 mV 111: -200 mV

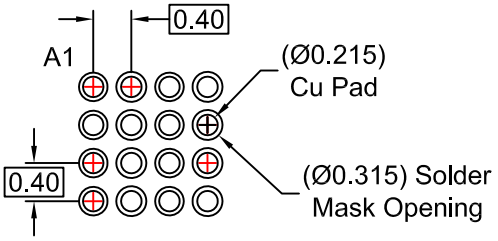
The table below pertains to the WLCSP package information on the following page.

Physical Dimensions

Product	D	E	X	Y
FSA7830BUCX	1.56 mm	1.56 mm	0.18 mm	0.18 mm



TOP VIEW



RECOMMENDED LAND PATTERN
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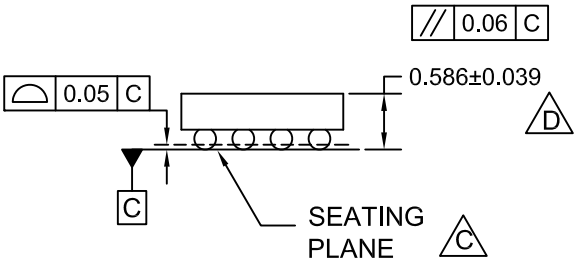
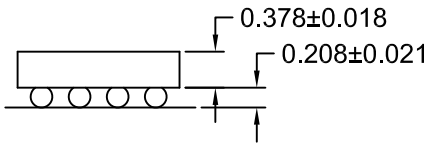
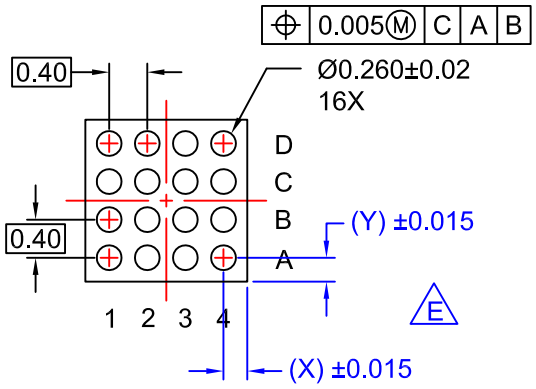




SIDE VIEWS



BOTTOM VIEW

NOTES

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

D. PACKAGE NOMINAL HEIGHT IS 586 ± 39 MICRONS (547-625 MICRONS).

E. FOR DIMENSIONS D,E,X, AND Y SEE PRODUCT DATASHEET.

F. DRAWING FILNAME: MKT-UC016AF revA

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