LM66100 Ideal Diode Evaluation Module

The LM66100EVM evaluation module (EVM) allows the user to control and connect power to the 6-pin, SC-70 package ideal diode. Parameters such as the on-resistance, rise time, and voltage drop can be easily and accurately evaluated.

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Trademarks

1 Introduction

1.1 Description

The LM66100EVM is a two-layer PCB containing two LM66100 ideal diode devices. The VIN and VOUT connections to the device and the PCB layout routing are capable of handling high continuous currents and provide a low-resistance pathway into and out of the device under test. Test point connections allow the EVM user to control the device with user-defined test conditions and make accurate R_{ON} measurements.

Table 1 lists a short description of the LM66100 ideal diode performance specifications; for additional details on performance, application notes, and the datasheet, see www.ti.com/idealdiode.

Table 1. LM66100 Rise Time, Output Current Rating, Enable and Output Discharge Characteristics

EVM	Device	Rise Time Typical (µs)	V_{IN} (V)	Maximum Continuous Current (A)	Enable (CE Pin)
PSIL052	LM66100	Fixed	1.5 to 5.5	1.5	IN > CE = ON IN < CE = OFF

1.2 Features

This EVM has the following features:

- Two LM66100 devices to evaluate OR-ing configurations
- V_{IN} input voltage range: 1.5 V to 5.5 V
- Access to the VIN, VOUT, CE, ST, and GND pins of the LM66100 ideal diode device
- Onboard C_{IN} and C_{OUT} capacitors
- 1.5-A maximum continuous current operation
- Jumpers to evaluate reverse current blocking, OR-ing, reverse polairty protection
- Battery holder

2 Electrical Performance

For detailed Electrical Characteristics of the LM66100 refer to the *LM66100 ± 6-V, Low IQ ideal diode with input polarity protection*.

3 Schematic

Figure 1 illustrates the LM66100EVM schematic.

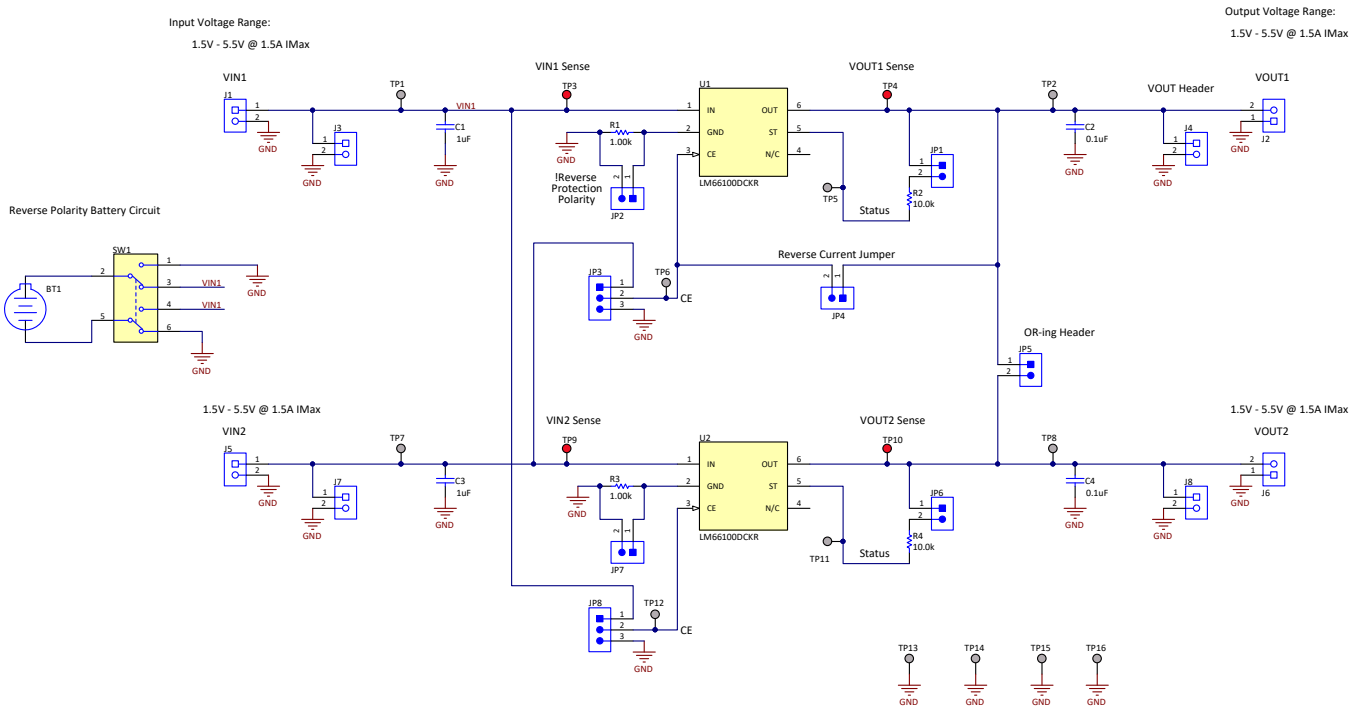

Figure 1. LM66100EVM Schematic

4 Layout

Figure 2 and Figure 3 show the PCB layout images.

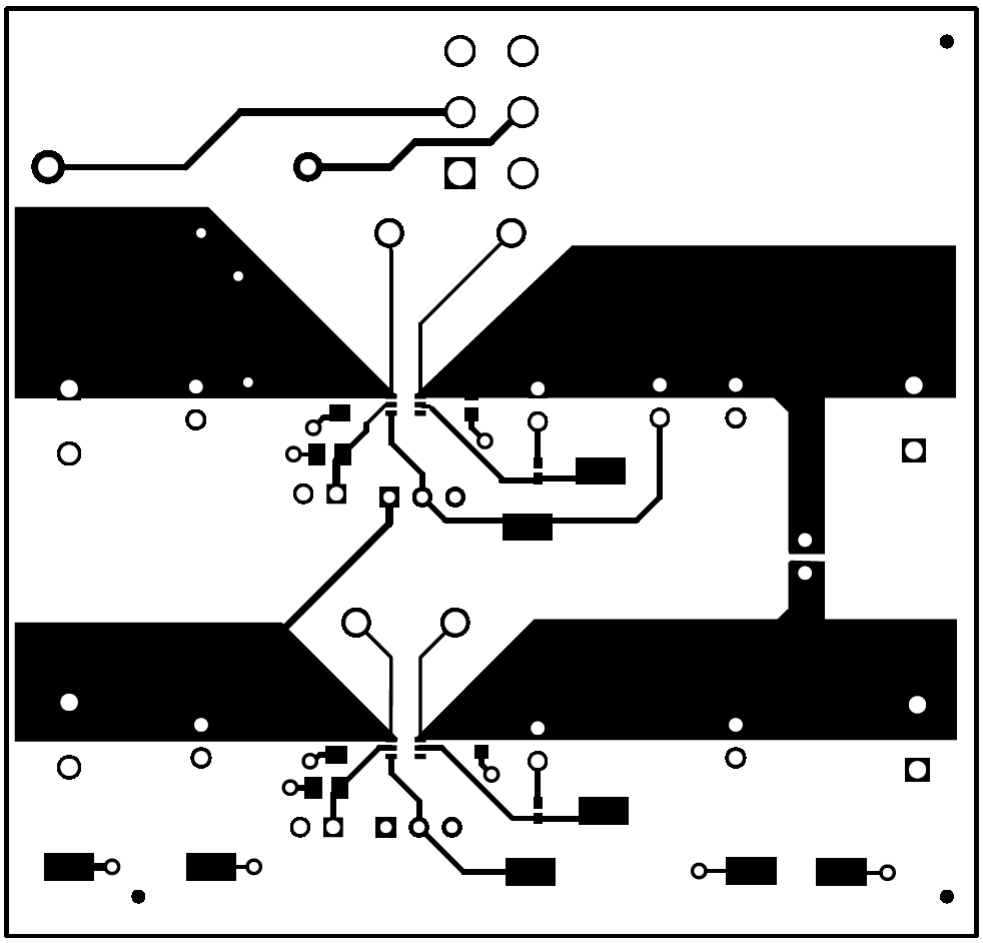

Figure 2. LM66100EVM Top Layout

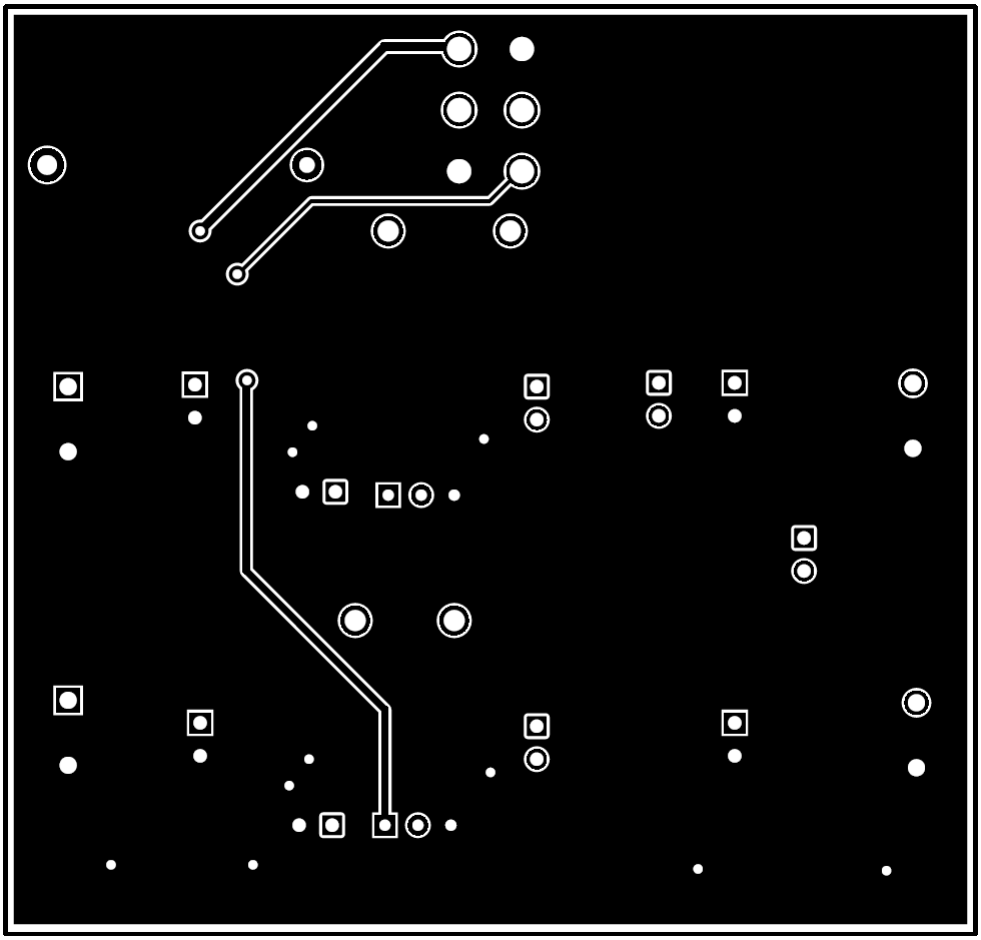

Figure 3. LM66100EVM Bottom Layout

4.1 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the EVM.

4.1.1 Input Connection- J1 (TP1), J5 (TP7)

This is the connection for the leads from the input source. Connect the positive lead to the + terminal (VIN) and the negative lead to the – terminal (GND). J1 and TP1 control VIN1, whereas J5 and TP7 control VIN2.

4.1.2 Output Connection- J2 (TP2), J6 (TP4)

This is the connection for the output of the EVM. Connect the positive lead to the + terminal (VOUT) and the negative lead to the – terminal (GND). J2 and TP2 control VOUT1, whereas J6 and TP8 control VOUT2.

4.1.3 CE- JP3 (TP6), JP8 (TP12)

This is the connector for the input comparator for the device. A shorting jumper can be installed on JP3 (VIN1) or JP8 (VIN2) in either the GND position or VINx position. An external enable source can be applied to the EVM by removing the shunt and connecting a signal to TP6 (VIN1) or TP12(VIN2). Refer to the data sheet for proper ON and OFF voltage level settings. A switching signal may also be used and connected at this point.

4.1.4 Status (ST)- JP1, JP6

During normal operation, a shorting jumper is placed on JP1 or JP6. This connects the ST pin to the VOUT pin of the device, enabling a Hi-Z signal when the chip is enabled. If the device is disabled, the pin acts as an open-drain output and is pulled low.

4.1.5 VINx Sense (TP3 and TP9), VOUTx Sense (TP4 and TP10)

These two connections are used when very accurate measurements of the input or output are required. Make R_{ON} measurements using these sense connections when measuring the voltage drop from VINx to VOUTx.

4.1.6 GND - (TP13, TP14, TP15, TP16)

These are connections to GND.

5 Operation of U1

Connect the VIN power supply to the J1 terminal (VIN). The input voltage range of the LM66100EVM is 1.5 V to 5.5 V.

External output loads can be applied to the switch by using the J2 terminal (VOUT). The LM66100EVM is rated for a maximum continuous current of 1.5 A. A shunt on JP1 must be installed for proper operation. When the voltage on the CE pin is lower than VIN1, the output of U1 is enabled.

6 Test Configurations

6.1 On-Resistance (R_{ON}) Test Setup

Figure 4 shows the typical setup for measuring on-resistance. The voltage drop across the switch is measured using the sense connections, and this can be divided by the load current to calculate the R_{ON} resistance.

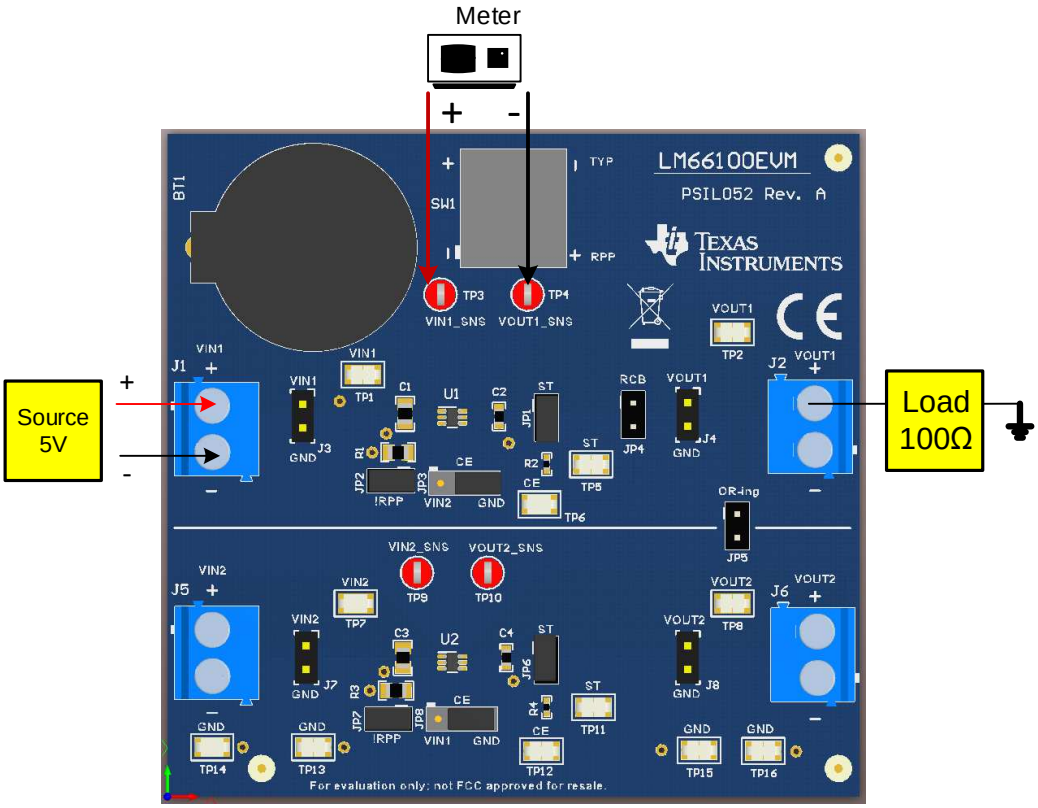

Figure 4. R_{ON} Test Setup

6.2 ORing Test Setup

Figure 5 shows the test setup for ORing between two LM66100. To enable ORing, connect jumpers JP3, JP8, and JP5. By connecting jumpers on the VINx connection on jumpers JP3 and JP8, the comparator pins will compare the voltages from the device's input voltage and the other channel's output voltage. For example, U1 will compare VIN1 voltage against VOUT2 on the CE pin. If VIN1 is higher, then the output will be enabled. Otherwise, the output will be VIN2.

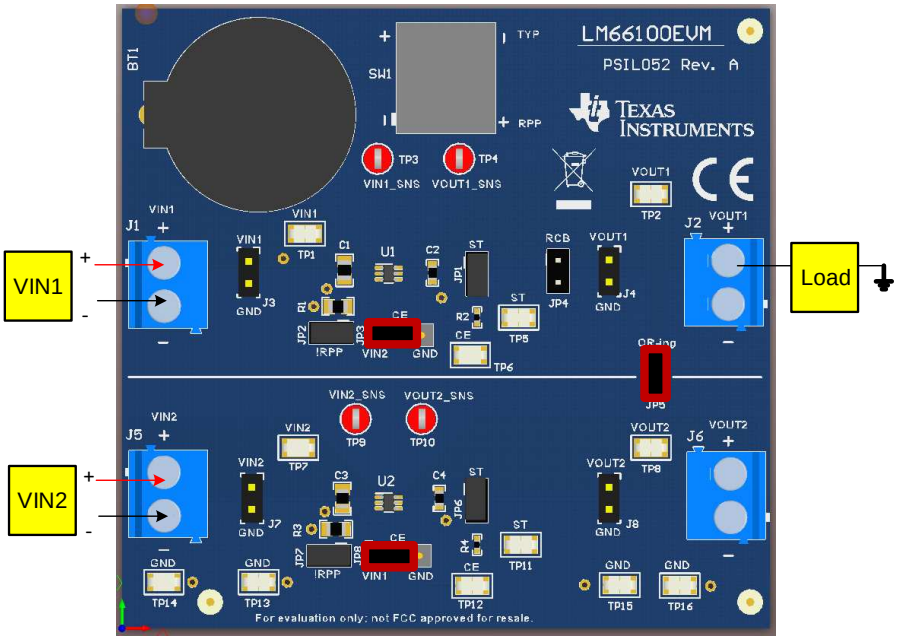

Figure 5. ORing Test Setup

6.3 Reverse Current Blocking Test Setup

Figure 6 shows the test setup for Reverse Current Blocking on U1. To enable RCB, connect jumper JP4. By connecting JP4, this allows the internal comparator to detect reverse current flow through IN1. If the output VOUT1 is forced above VIN1 by V_{OFF}, the channel will switch off.

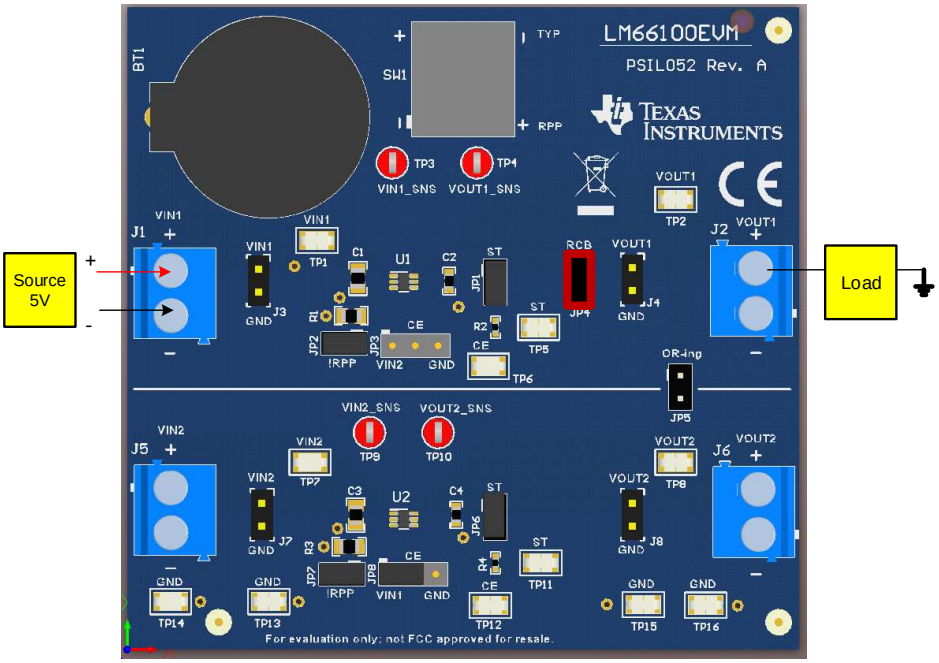

Figure 6. Reverse Current Blocking Test Setup

6.4 Reverse Polarity Protection Test Setup

Figure 7 shows the test setup for Reverse Polarity Protection on U1. For ORing applications that need RPP, remove jumpers JP2 and JP7 to enable a resistor that limits the current that passes through the device GND pin.

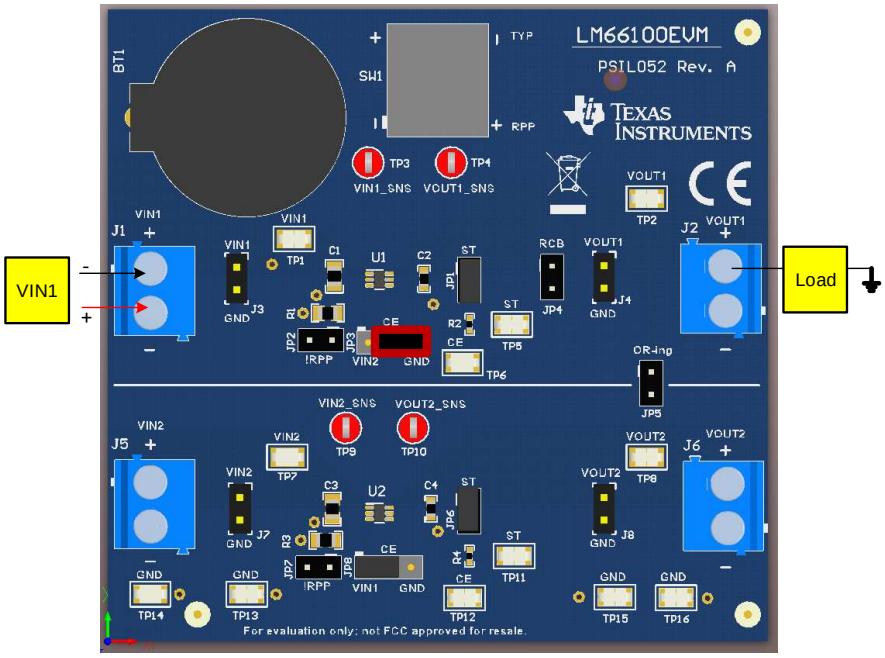

Figure 7. Reverse Polarity Protection Test Setup

7 Bill of Materials

Table 2 lists the LM66100EVM BOM.

Table 2. LM66100EVM Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		PSIL052	Any
BT1	1		Battery Holder, CR2032, Retainer clip, TH	CR2032 holder	BS-7	Memory Protection Devices
C1, C3	2	1 uF	CAP, CERM, 1 uF, 16 V, +/- 10%, X8R, 0805	0805	C2012X8R1C105K125AB	TDK
C2, C4	2	0.1 uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X5R, 0603	0603	06033D104KAT2A	AVX
J1, J2, J5, J6	4		Terminal Block, 5 mm, 2×1, Tin, TH	Terminal Block, 5 mm, 2x1, TH	691 101 710 002	Wurth Elektronik
J3, J4, J7, J8	4		Receptacle, 2.54 mm, 2×1, Gold, TH	Receptacle, 2.54 mm, 2x1, TH	SSQ-102-03-G-S	Samtec
JP1, JP2, JP4, JP5, JP6, JP7	6		Header, 100 mil, 2×1, Tin, TH	Header, 2 PIN, 100 mil, Tin	PEC02SAAN	Sullins Connector Solutions
JP3, JP8	2		Header, 100 mil, 3×1, TH	Header, 3×1, 100 mil, TH	800-10-003-10-001000	Mill-Max
R1, R3	2	1.00 k	RES, 1.00 k, 0.5%, 0.1 W, 0805	0805	RR1220P-102-D	Susumu Co Ltd
R2, R4	2	10.0 k	RES, 10.0 k, 1%, 0.063 W, 0402	0402	MCR01MRTF1002	Rohm
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6	6	1×2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
SW1	1		Switch, DPDT, On-On, 5 A, 120 VAC, 28 VDC, TH	12.7×11.43 mm	100DP1T1B1M2QEH	E-Switch
TP1, TP2, TP5, TP6, TP7, TP8, TP11, TP12, TP13, TP14, TP15, TP16	12		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
TP3, TP4, TP9, TP10	4		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
U1, U2	2		+/-6 V, Low IQ Ideal Diode with Input Polarity Protection, DCK0006A (SOT-SC70-6)	DCK0006A	LM66100DCKR	Texas Instruments
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A

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