

# 74ABT16245B

16-bit bus transceiver; 3-state

Rev. 6 — 14 July 2021

Product data sheet

## 1. General description

The 74ABT16245B is a 16-bit transceiver with 3-state outputs. The device can be used as two 8-bit transceivers or one 16-bit transceiver. The device features two output enables (1OE and 2OE) each controlling eight outputs, and two send/receive (1DIR and 2DIR) inputs for direction control. A HIGH on nOE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power down applications using I<sub>OFF</sub>. The I<sub>OFF</sub> circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

## 2. Features and benefits

- Supply voltage range from 4.5 to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- 16-bit bidirectional bus interface
- Multiple V<sub>CC</sub> and GND pins minimize switching noise
- Power-up 3-state
- 3-state buffers
- Output capability: +64 mA and -32 mA
- Live insertion/extraction permitted
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - CDM JESD22-C101C exceeds 1000 V
- Specified from -40 °C to 85 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT16245BDGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4. Functional diagram

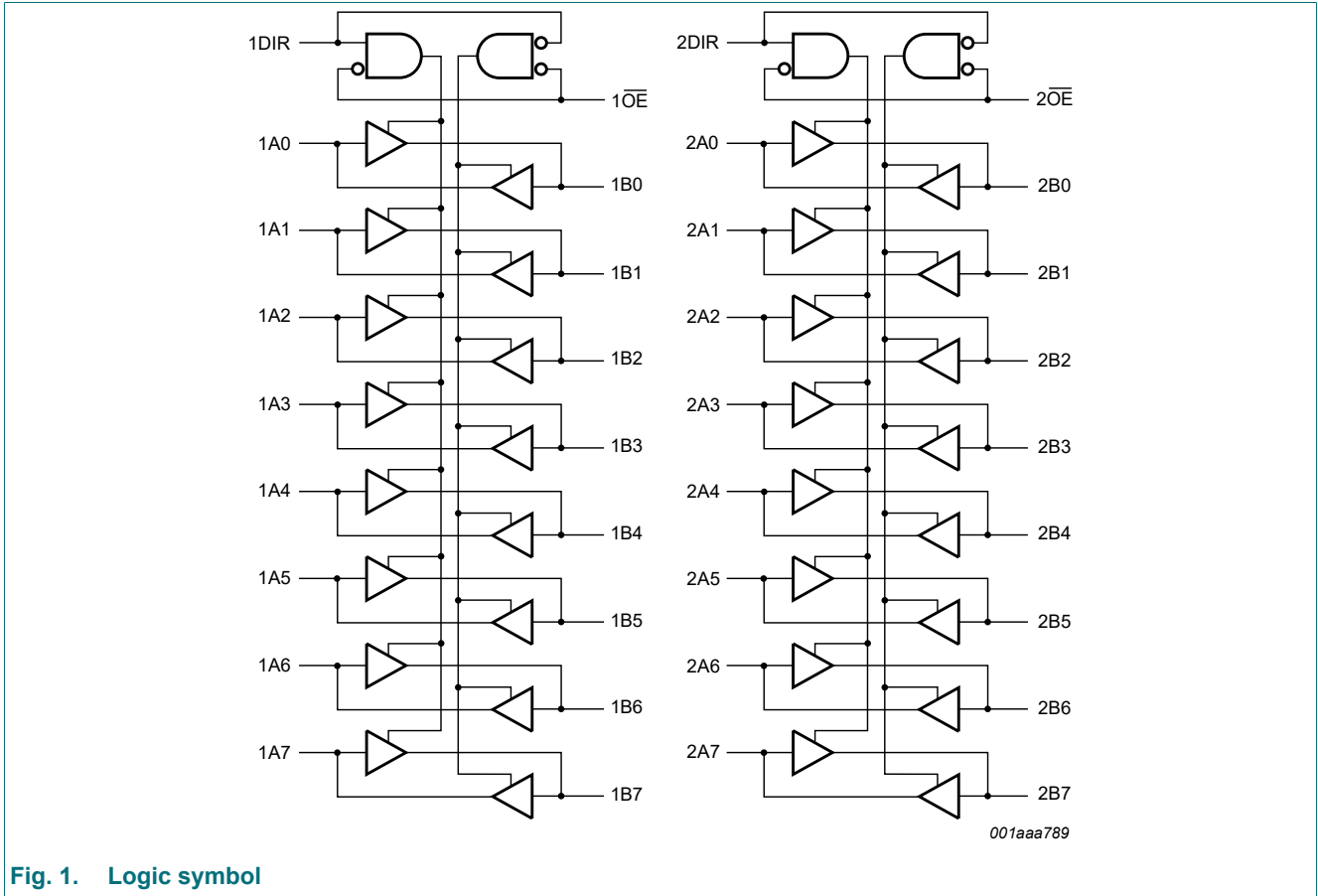


Fig. 1. Logic symbol

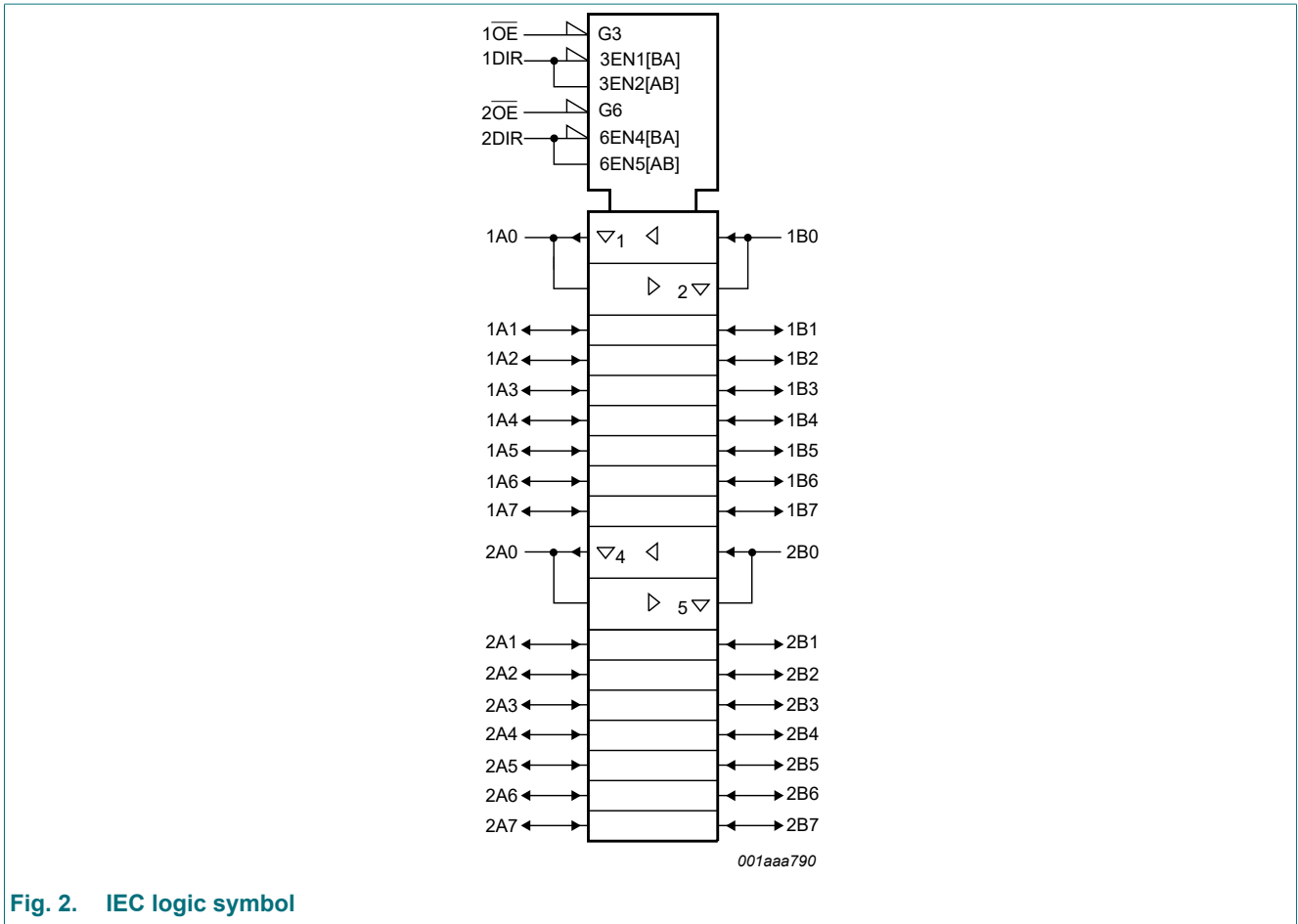
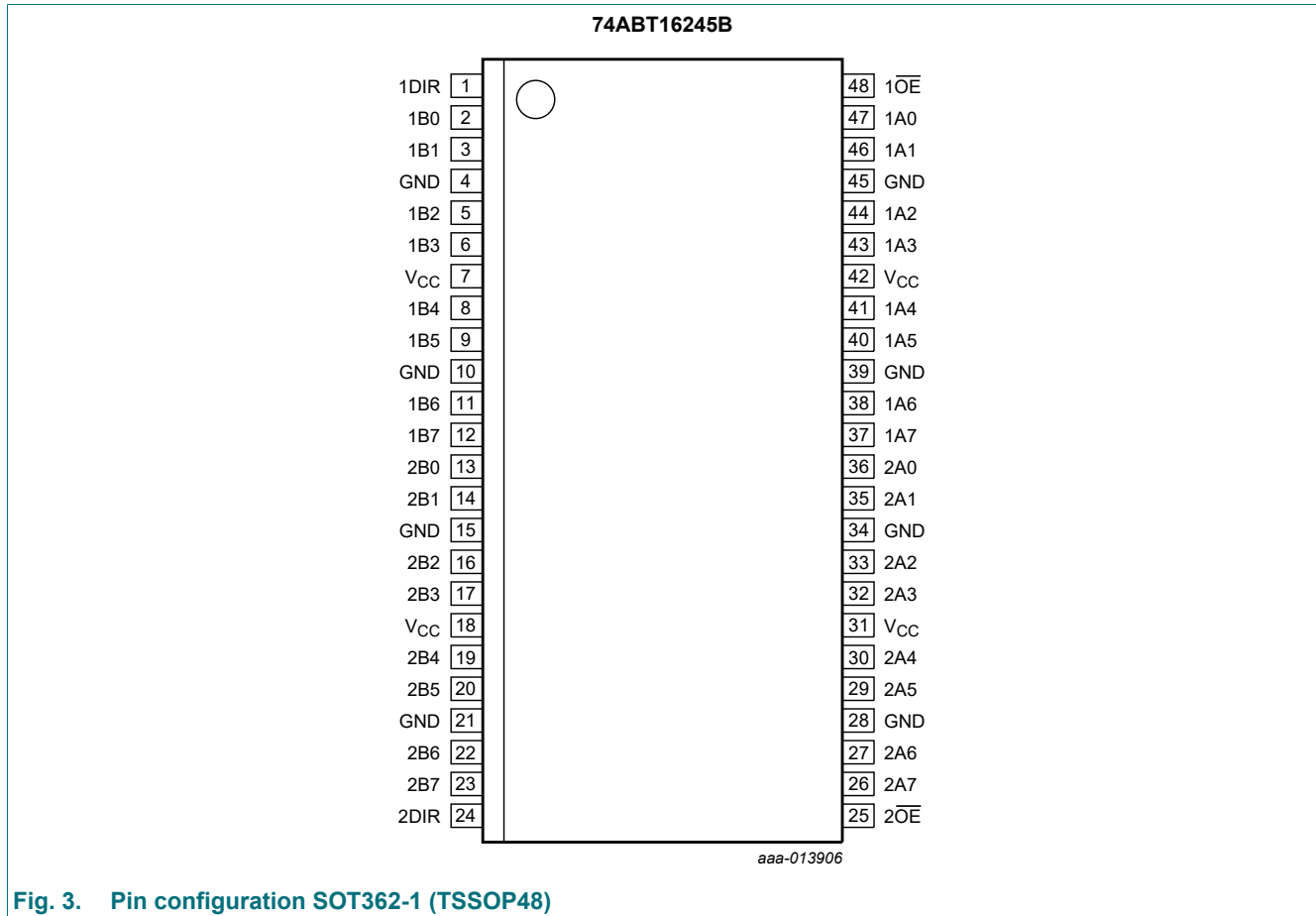


Fig. 2. IEC logic symbol

## 5. Pinning information

### 5.1. Pinning



**Fig. 3.** Pin configuration SOT362-1 (TSSOP48)

### 5.2. Pin description

**Table 2.** Pin description

Symbol	Pin	Description
1DIR, 2DIR	1, 24	direction control input
1B0 to 1B7	2, 3, 5, 6, 8, 9, 11, 12	data input/output
2B0 to 2B7	13, 14, 16, 17, 19, 20, 22, 23	data input/output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V <sub>CC</sub>	7, 18, 31, 42	supply voltage
1OE, 2OE	48, 25	output enable input (active LOW)
1A0 to 1A7	47, 46, 44, 43, 41, 40, 38, 37	data input/output
2A0 to 2A7	36, 35, 33, 32, 30, 29, 27, 26	data input/output

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.*

Inputs		Outputs	
nOE	nDIR	nAn	nBn
L	L	nAn = nBn	inputs
L	H	inputs	nBn = nAn
H	X	Z	Z

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage	[1]	-1.2	+7.0	V
V <sub>O</sub>	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+5.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-18	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
I <sub>O</sub>	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T <sub>j</sub>	junction temperature	[2]	-	150	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		4.5	5.5	V
V <sub>I</sub>	input voltage		0	V <sub>CC</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	V
V <sub>IL</sub>	LOW-level input voltage		-	0.8	V
I <sub>OH</sub>	HIGH-level output current		-32	-	mA
I <sub>OL</sub>	LOW-level output current		-	64	mA
Δt/ΔV	input transition rise and fall rate		-	10	ns/V
T <sub>amb</sub>	ambient temperature	in free air	-40	+85	°C

## 9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
$V_{IK}$	input clamping voltage	$V_{CC} = 4.5 \text{ V}$ ; $I_{IK} = -18 \text{ mA}$	-1.2	-0.9	-	-1.2	-	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IL}$ or $V_{IH}$						
		$V_{CC} = 4.5 \text{ V}$ ; $I_{OH} = -3 \text{ mA}$	2.5	2.9	-	2.5	-	V
		$V_{CC} = 5.0 \text{ V}$ ; $I_{OH} = -3 \text{ mA}$	3.0	3.4	-	3.0	-	V
		$V_{CC} = 4.5 \text{ V}$ ; $I_{OH} = -32 \text{ mA}$	2.0	2.4	-	2.0	-	V
$V_{OL}$	LOW-level output voltage	$V_{CC} = 4.5 \text{ V}$ ; $I_{OL} = 64 \text{ mA}$ ; $V_I = V_{IL}$ or $V_{IH}$	-	0.42	0.55	-	0.55	V
$I_I$	input leakage current	control pins; $V_{CC} = 5.5 \text{ V}$ ; $V_I = V_{CC}$ or GND	-	$\pm 0.01$	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_{CC} = 0 \text{ V}$ ; $V_I$ or $V_O \leq 4.5 \text{ V}$	-	$\pm 5.0$	$\pm 100$	-	$\pm 100$	$\mu\text{A}$
$I_{O(pu/pd)}$	power-up/ power-down output current	$V_{CC} = 2.0 \text{ V}$ ; $V_O = 0.5 \text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; [1] $n\text{OE} = \text{HIGH}$	-	$\pm 5.0$	$\pm 50$	-	$\pm 50$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_{CC} = 5.5 \text{ V}$ ; $V_I = V_{IL}$ or $V_{IH}$						
		output HIGH-state at $V_O = 5.5 \text{ V}$	-	0.1	10	-	10	$\mu\text{A}$
		output LOW-state at $V_O = 0 \text{ V}$	-	-0.1	-10	-	-10	$\mu\text{A}$
$I_{CEX}$	output high leakage current	HIGH-state; $V_O = 5.5 \text{ V}$ ; $V_{CC} = 5.5 \text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$	-	5.0	50	-	50	$\mu\text{A}$
$I_O$	output current	$V_{CC} = 5.5 \text{ V}$ ; $V_O = 2.5 \text{ V}$ [2]	-50	-92	-180	-50	-180	mA
$I_{CC}$	supply current	$V_{CC} = 5.5 \text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$						
		outputs HIGH-state	-	0.30	0.7	-	0.7	mA
		outputs LOW-state	-	10	19	-	19	mA
		outputs 3-state	-	0.30	0.7	-	0.7	mA
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 5.5 \text{ V}$ ; one data input at 3.4 V and other inputs at $V_{CC}$ or GND [3]						
		outputs enabled	-	400	700	-	700	$\mu\text{A}$
		outputs disabled	-	100	250	-	250	$\mu\text{A}$
		control pins; outputs disabled; one enable input at 3.4 V and other inputs at $V_{CC}$ or GND	-	400	700	-	700	$\mu\text{A}$
$C_I$	input capacitance	$V_I = 0 \text{ V}$ or $V_{CC}$	-	4	-	-	-	pF
$C_{I/O}$	input/output capacitance	outputs disabled; $V_O = 0 \text{ V}$ or $V_{CC}$	-	7	-	-	-	pF

[1] This parameter is valid for any  $V_{CC}$  between 0 V and 2.1 V, with a transition time of up to 10 ms.

From  $V_{CC} = 2.1 \text{ V}$  to  $V_{CC} = 5 \text{ V} \pm 10 \%$ , a transition time of up to 100  $\mu\text{s}$  is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

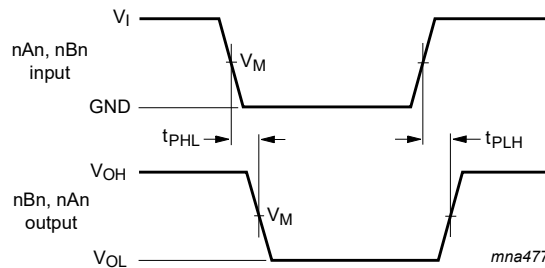
## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

$GND = 0\text{ V}$ . For test circuit, see Fig. 6.

Symbol	Parameter	Conditions	25 °C; $V_{CC} = 5.0\text{ V}$			-40 °C to +85 °C; $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$		Unit
			Min	Typ	Max	Min	Max	
$t_{PLH}$	LOW to HIGH propagation delay	nAn to nBn; see Fig. 4	1.0	2.0	3.2	1.0	3.5	ns
$t_{PHL}$	HIGH to LOW propagation delay	nAn to nBn; see Fig. 4	1.0	2.3	3.5	1.0	4.0	ns
$t_{PZH}$	OFF-state to HIGH propagation delay	$\overline{nOE}$ to nAn or nBn; see Fig. 5	1.0	3.0	4.4	1.0	5.1	ns
$t_{PZL}$	OFF-state to LOW propagation delay	$\overline{nOE}$ to nAn or nBn; see Fig. 5	1.7	4.0	5.2	1.7	6.1	ns
$t_{PHZ}$	HIGH to OFF-state propagation delay	$\overline{nOE}$ to nAn or nBn; see Fig. 5	1.7	3.5	4.9	1.7	5.4	ns
$t_{PLZ}$	LOW to OFF-state propagation delay	$\overline{nOE}$ to nAn or nBn; see Fig. 5	1.5	3.2	4.4	1.5	5.0	ns

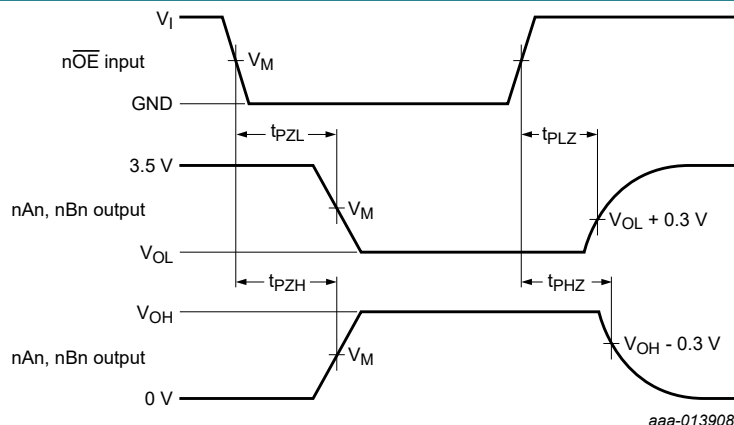
### 10.1. Waveforms and test circuit



$V_M = 1.5\text{ V}$

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 4. Input (nAn) to output (nBn) propagation delay times**



$V_M = 1.5\text{ V}$

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 5. 3-state output enable and disable times**

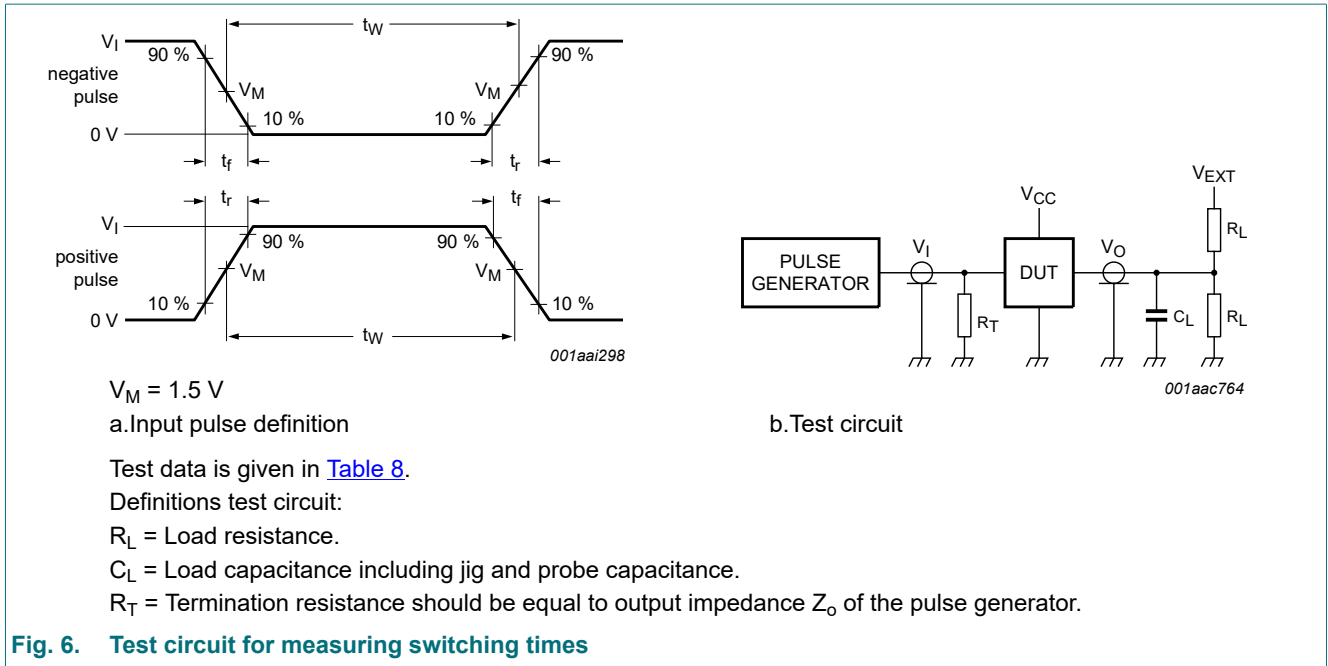


Table 8. Test data

Input				Load		$V_{EXT}$		
$V_I$	$f_i$	$t_w$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
3.0 V	1 MHz	500 ns	2.5 ns	50 pF	500 $\Omega$	open	7.0 V	open



11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

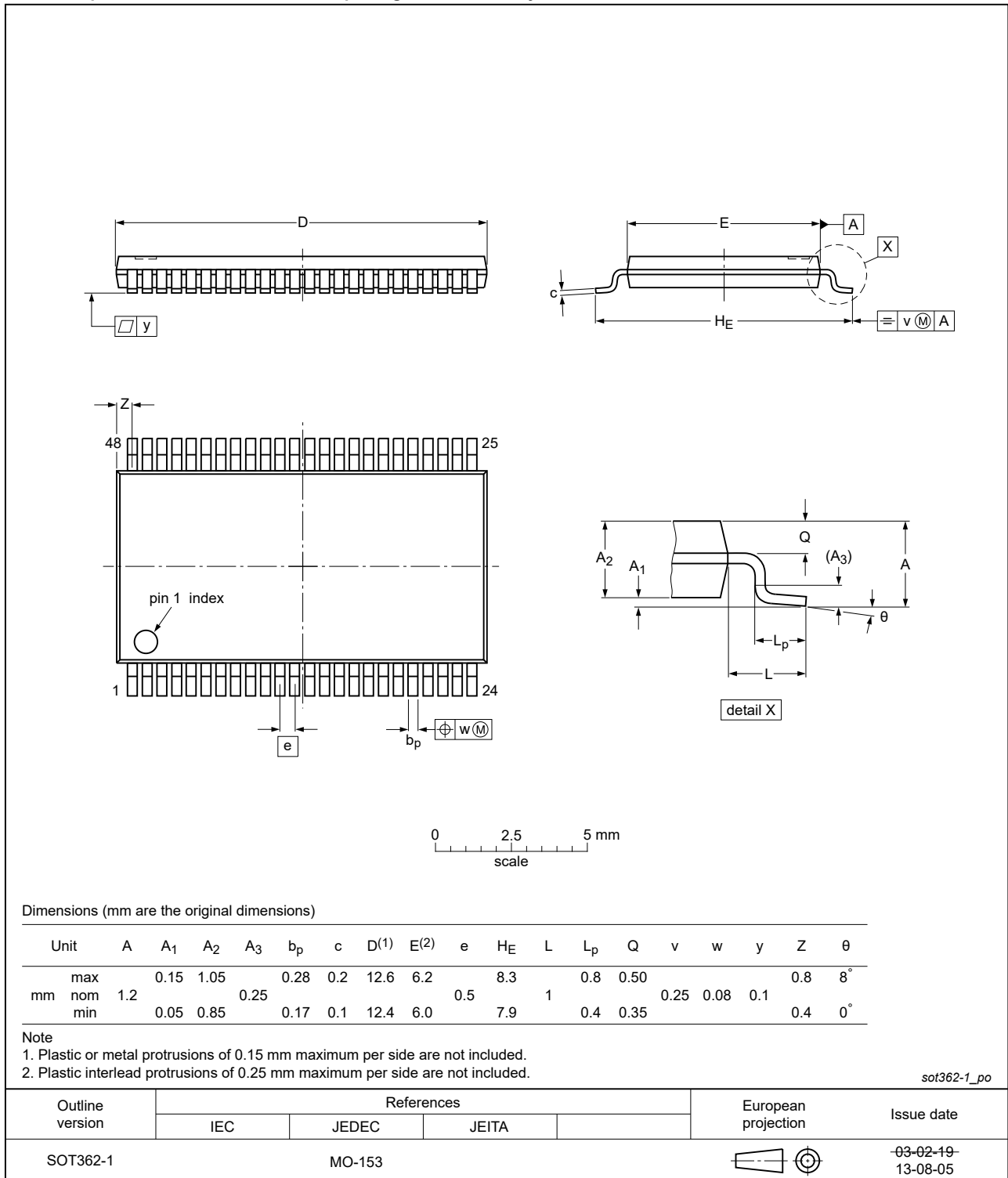


Fig. 7. Package outline SOT362-1 (TSSOP48)

## 12. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT16245B v.6	20210714	Product data sheet	-	74ABT16245B v.5
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li>• Type number 74ABT16245BDL (SOT370-1/SSOP48) removed.</li> </ul>			
74ABT16245B v.5	20170410	Product data sheet	-	74ABT16245B v.4
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74ABT16245B v.4	20140819	Product data sheet	-	74ABT_H16245B v.3
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Type number 74ABTH16245BDL removed.</li> </ul>			
74ABT_H16245B v.3	20021213	Product data sheet	-	74ABT_H16245B v.2
74ABT_H16245B v.2	19980225	Product data sheet	-	74ABT_H16245B v.1
74ABT_H16245B v.1	19961120	Product data sheet	-	-

## 14. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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