Features

- ESD protection for four high-speed I/O channels
- Provide transient protection for each line to
  IEC 61000-4-2 (ESD) ±15kV (air), ±12kV (contact)
  IEC 61000-4-5 (Lightning) 6.5A (8/20μs)
- **For low operating voltage of 3.3V and below**
- **Ultra-low capacitance:0.2pF typical**
- **Fast turn-on and ultra-low clamping voltage**
- Array of ESD rated diodes with internal equivalent TVS (Transient Voltage Suppression) diode
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- **HDMI 1.3, 1.4, 2.0, and 2.1 version**
- **DisplayPort 1.1, 1.2, and 1.3 version**
- USB3.0 and USB3.1 interfaces
- USB Type-C interface
- SATA and eSATA interfaces
- Handheld portable applications

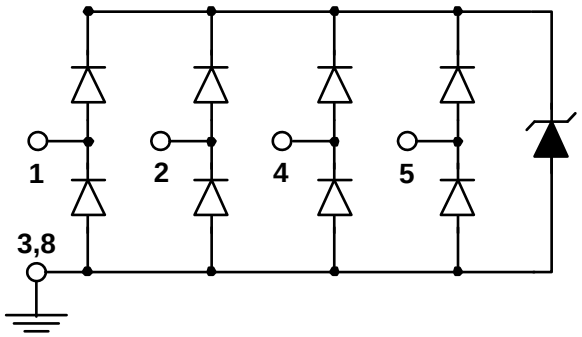
Description

AZ1123-04F is a design which includes ESD rated diode arrays to protect high-speed data interfaces. The AZ1123-04F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage damage caused by Electrostatic Discharging (ESD), Lightning, and Cable Discharge Event (CDE).

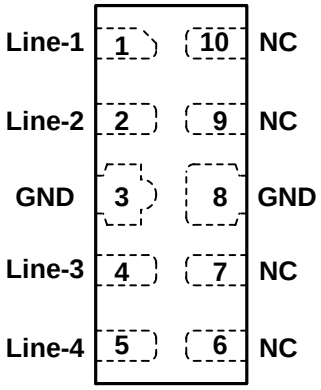
AZ1123-04F is a unique design which includes ESD rated, ultra-low capacitance steering diodes and unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the internal ESD line or to ground line. The internal unique design of clamping cell prevents over-voltage on the internal ESD line and on the I/O line, which is protecting any downstream components.

AZ1123-04F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



DFN2510P10E (Top View)

Specifications

Absolute Maximum Ratings (T_A= 25°C, unless otherwise specified)			
Parameter	**Symbol**	**Rating**	**Unit**
Peak Pulse Current (t_p = 8/20μs)	I_{PP}	6.5	A
Operating Voltage (I/O pin-GND)	V_{DC}	3.6	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD-1} V_{ESD-2}	±15 ±12	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C

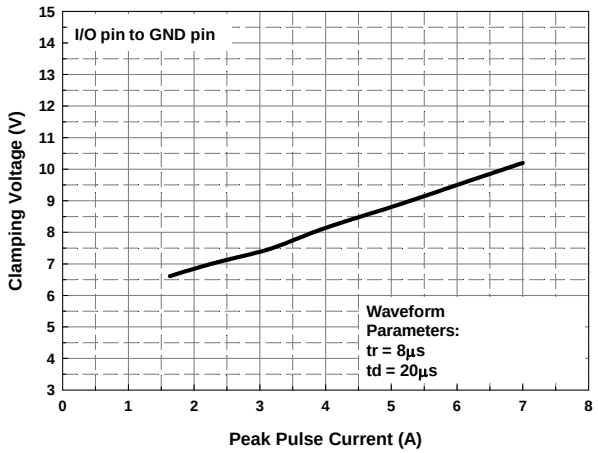
Electrical Characteristics						
Parameter	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Reverse Stand-Off Voltage	V_{RWM}	Pin-1,-2,-4,-5 to pin-3,-8, T = 25°C.			3.3	V
Channel Leakage Current	$I_{CH-Leak}$	$V_{Pin-1,-2,-4,-5}$ = 3.3V, $V_{Pin-3,-8}$ = 0V, T = 25°C.			1	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, pin-1,-2,-4,-5 to pin-3,-8, T = 25°C.	5		7.5	V
Forward Voltage	V_F	I_F = 40mA, pin-3,-8 to pin-1,-2,-4,-5, T = 25°C.		1	1.5	V
Surge Clamping Voltage	$V_{CL-surge}$	I_{PP} = 5A, T = 25°C, any I/O pin to GND.		9		V
ESD Clamping Voltage (Note 1)	V_{CL-ESD}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), contact mode, T = 25°C, any I/O pin to GND.		10		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0~+8kV, T = 25°C, contact mode, any I/O pin to GND.		0.3		Ω
Channel Input Capacitance	C_{IN}	$V_{pin-3,-8}$ = 0V, V_{IN} = 1.65V, f = 1MHz, T = 25°C, any I/O pin to GND.		0.2	0.3	pF
Channel to Channel Input Capacitance	$C_{I/O-to-I/O}$	$V_{pin-3,-8}$ = 0V, V_{IN} = 1.65V, f = 1MHz, T = 25°C, between I/O pins.		0.05	0.1	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

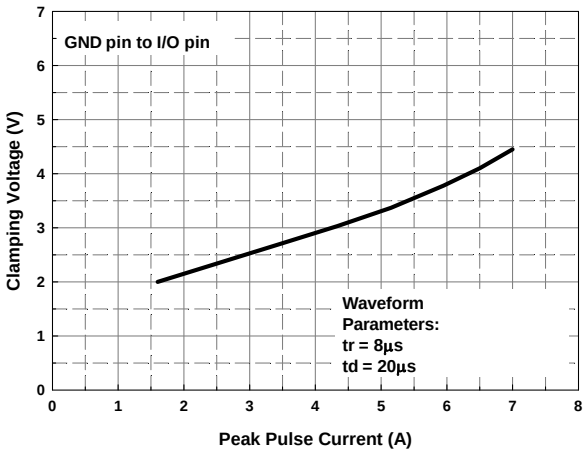
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics

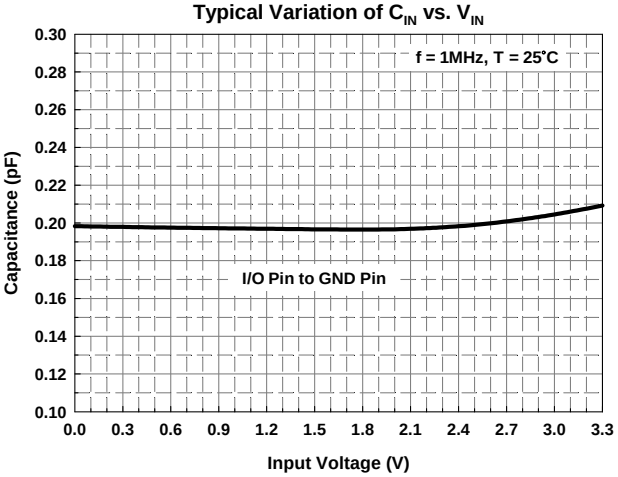
Reverse Clamping Voltage vs. Peak Pulse Current



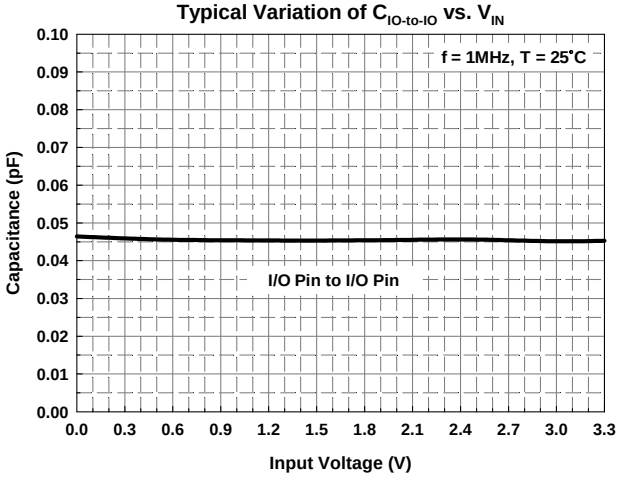
Forward Clamping Voltage vs. Peak Pulse Current



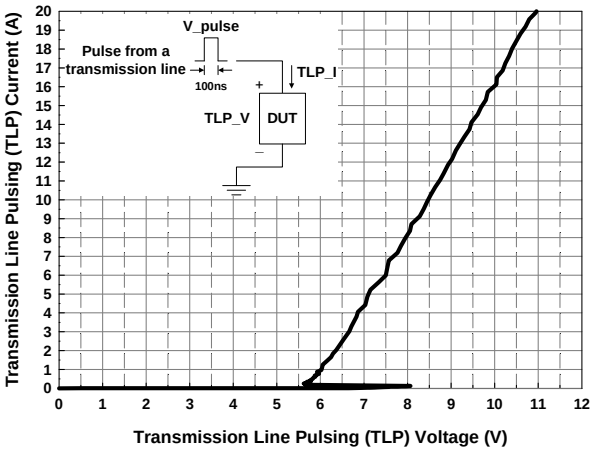
Typical Variation of C_{IN} vs. V_{IN}



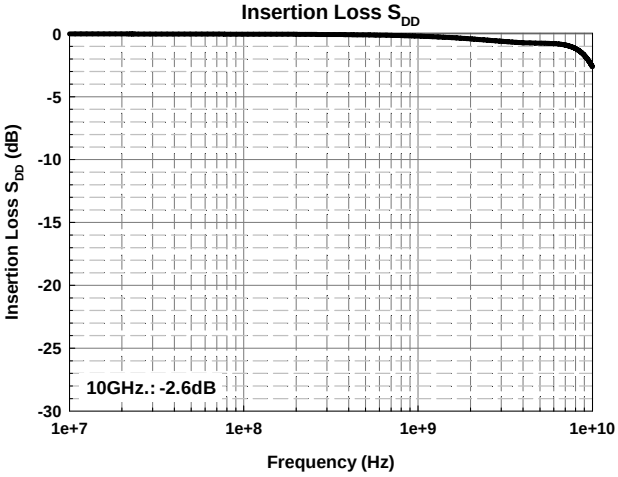
Typical Variation of $C_{IO\text{-}to\text{-}IO}$ vs. V_{IN}



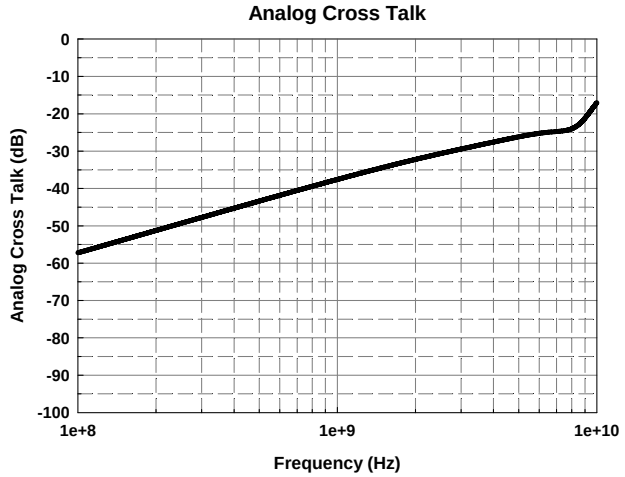
Transmission Line Pulsing (TLP) Measurement



Insertion Loss S_{DD}



Typical Characteristics



Application Information

The AZ1123-04F is designed to protect four data lines from transient over-voltage (such as ESD stress pulse). The device connection of AZ1123-04F is shown in the Fig. 1. In Fig. 1, the four protected data lines are connected to the ESD protection pins (pin1, pin2, pin4, and pin5) of AZ1123-04F. The ground pins (pin3 and pin8) of AZ1123-04F are the negative reference pins. These pins should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should be kept as short as possible.

AZ1123-04F can provide ESD protection for four I/O signal lines simultaneously. If the number of I/O signal lines is less than four, the unused I/O pins can be simply left as NC pins.

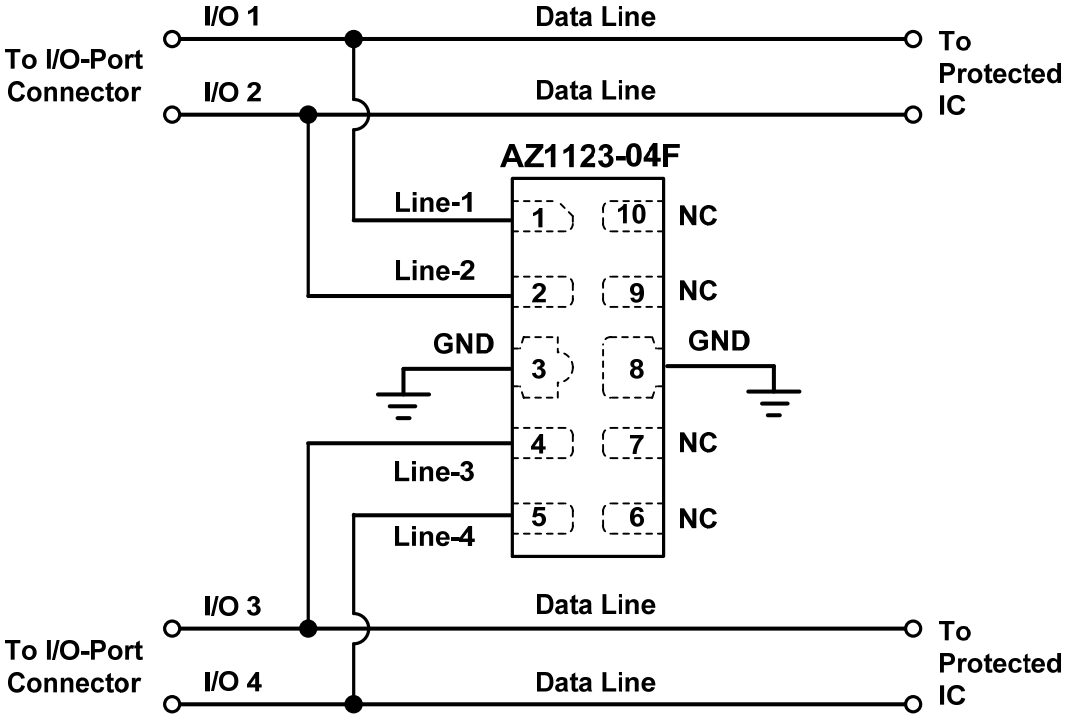


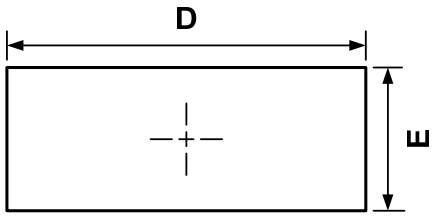
Fig. 1 Data lines connection of AZ1123-04F.

Mechanical Details

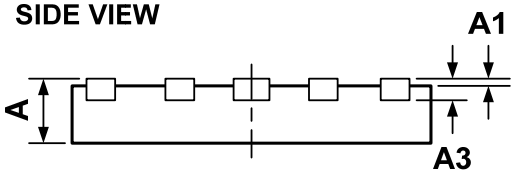
DFN2510P10E

Package Diagrams and Package Dimensions

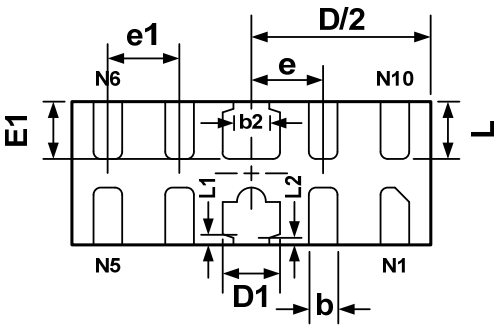
TOP VIEW



SIDE VIEW

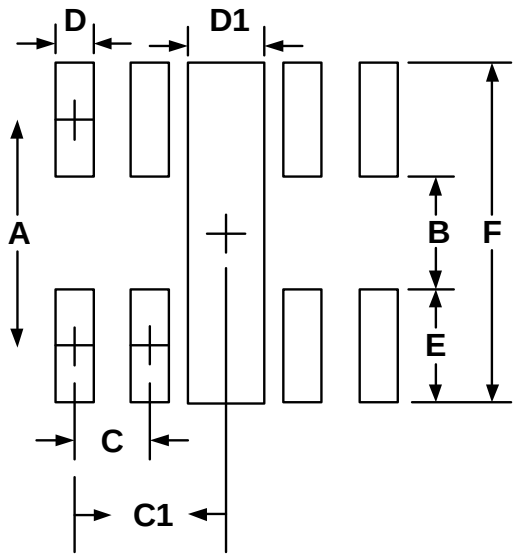


BOTTOM VIEW



SYMBOL	MILLIMETERS	
	MIN.	MAX.
A	0.400	0.550
A1	-	0.050
A3	0.152REF	
D	2.450	2.550
E	0.950	1.050
D1	0.350	0.450
E1	0.350	0.450
b	0.150	0.250
e	0.500 BSC	
e1	0.500 BSC	
L1	0.075 REF	
L2	0.050 REF	
b2	0.200	0.300
L	0.350	0.450

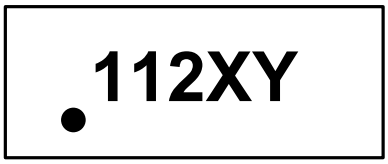
Land Layout



Dimensions		
Index	**Millimeter**	**Inches**
A	0.875	0.034
B	0.20	0.008
C	0.50	0.02
C1	1.00	0.039
D	0.25	0.01
D1	0.4	0.016
E	0.675	0.027
F	1.55	0.061

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

Marking Code



112 = Device Code
X = Date Code
Y= Control Code

Part Number	Marking Code
AZ1123-04F.R7G (Green Part)	112XY

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ1123-04F.R7G	Green	T/R	7 inch	3,000/reel	4 reels=12,000/box	6 boxes=72,000/carton

Revision History

Revision	Modification Description
Revision 2021/06/11	Formal Release.