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**TEXAS INSTRUMENTS**

**TPS7B4255**
SBVS441 – DECEMBER 2022

# TPS7B4255 70-mA, 40-V, Voltage-Tracking LDO With Voltage-Buffering Capability

## 1 Features

- Wide input operating voltage range (3 V to 40 V):
  - Absolute maximum input range: –40 V to +45 V
- Wide output voltage range: 2 V to 30 V
- Very-tight, output-tracking tolerance: 5 mV (max)
- Low dropout voltage: 500 mV (max) at 70 mA
- Reverse polarity protection
- Reverse current protection
- Combined reference and enable input
- Low quiescent current at light loads (100-µA load):
  - 50 µA (max)
- Wide ESR range:
  - Stable with 1-µF to 200-µF ceramic output capacitor, 1-mΩ to 3-Ω ESR
- Overtemperature protection
- Output short-circuit protection to ground and supply
- Junction temperature: –40°C to +150°C, $T_J$
- Available in 5-pin SOT-23 DBV package
- Buffers signals up to 1 kHz (see the *Signal-Buffering LDO* section)

## 2 Applications

- Condition monitoring sensors
- Motion detectors (PIR, uWave, and so forth)
- Wired controls
- Telemetry and RTUs
- Robot sensing modules

## 3 Description

The TPS7B4255 is a low-dropout (LDO) voltage-tracking regulator, with high tracking accuracy and excellent load and line transient response. The device is available in a 5-pin, SOT-23 (DBV) package. The TPS7B4255 is designed to supply off-board sensors in industrial applications such as condition monitoring sensor systems. The device provides integrated protection features such as reverse polarity, output short to supply and ground, current limit, and thermal shutdown to protect against the high risk of cable failures in an off-board power system. The device is designed to survive a 45-V (absolute maximum) input voltage during extreme transient events.
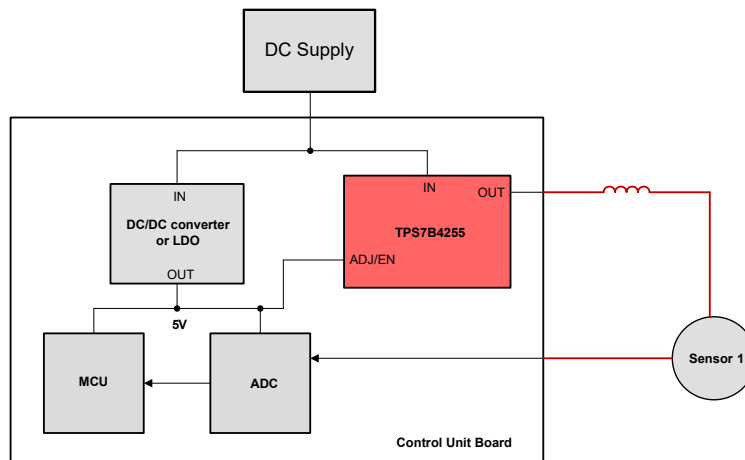
A reference voltage applied at the ADJ/EN pin is effectively tracked with high accuracy for loads up to 70 mA. The high tracking accuracy provides accurate power supply to off-board modules and enables better accuracy when making measurements using ratiometric sensors.

By setting the ADJ/EN input pin low, the TPS7B4255 switches to standby mode and reduces the quiescent current to the minimum value.

**Package Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS7B4255 | DBV (SOT-23, 5) | 2.90 mm × 1.60 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



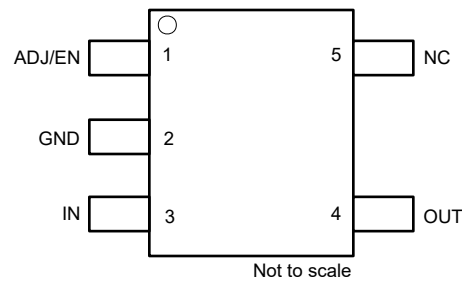**Typical Application**

# Table of Contents

# 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| December 2022 | * | Initial Release |

# 5 Pin Configuration and Functions



**Figure 5-1. DBV Package, 5-Pin SOT-23 (Top View)**

**Table 5-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| ADJ/EN | 1 | I | ADJ/EN pin. Connect the reference voltage to this pin. This pin connects to the error amplifier internally. A low signal below $V_{IL}$ disables the device and a high signal above $V_{IH}$ enables the device. Connect the voltage reference directly or with a voltage divider for lower output voltages. To compensate for line influences, place a capacitor close to this pin. |
| GND | 2 | — | Ground pin. |
| NC | 5 | — | This pin is not internally connected. Connect this pin to GND for improved thermal performance. |
| IN | 3 | I | Input power-supply voltage pin. This pin is the device supply. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to GND as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the input of the device as possible to compensate for line influences. |
| OUT | 4 | O | Regulated output voltage pin. A capacitor is required from OUT to GND for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to GND; see the *Recommended Operating Conditions* table. Place the output capacitor as close to output of the device as possible. |

# 6 Specifications
## 6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)[1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Unregulated input voltage | -40 | 45 | V |
| $V_{OUT}$ | Regulated output voltage | −5 | 45 | V |
| $V_{ADJ/EN}$ | Adjustable input and enable input voltage | -0.3 | 45 | V |
| $V_{IN} - V_{OUT}$ | Input output voltage difference | -40 | 40 | V |
| $T_J$ | Operating junction temperature | −40 | 150 | °C |
| $T_{stg}$ | Storage temperature | −65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect the device reliability, functionality, performance, and shorten the device lifetime.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] — All pins | ±500 | |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] — Corner pins | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Unregulated input voltage | 3 |  | 40 | V |
| $V_{OUT}$ | Regulated output voltage | 2 |  | 30 | V |
| $I_{OUT}$ | Output current | 0 |  | 70 | mA |
| $C_{IN}$ | Input capacitor[1] | 0 | 1 |  | µF |
| $C_{OUT}$ | Output capacitor[2] | 1 |  | 200 | µF |
| ESR | Output capacitor ESR requirements | 0.001 |  | 3 | Ω |
| $T_J$ | Operating junction temperature | −40 |  | 150 | °C |

(1)     For robust EMI performance the minimum input capacitance is 500 nF.
(2)     Effective output capacitance of 500 nF minimum required for stability.

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TPS7B4255 | UNIT |
|---|---|---|---|
| | | DBV (SOT-23)[2] | |
| | | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 176.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 75.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 44.4 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 17.9 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 44.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1)     For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2)     Evaluated using JEDEC standard (2s2p).

## 6.5 Electrical Characteristics

specified at $T_J$ = –40°C to +150°C, $V_{IN}$ = 13.5 V, $I_{OUT}$ = 100 µA, $C_{OUT}$ = 1 µF, 1 mΩ < $C_{OUT}$ ESR < 2 Ω, $C_{IN}$ = 1 µF, and $V_{ADJ}$ = 5 V (unless otherwise noted), typical values are at $T_J$ = 25°C

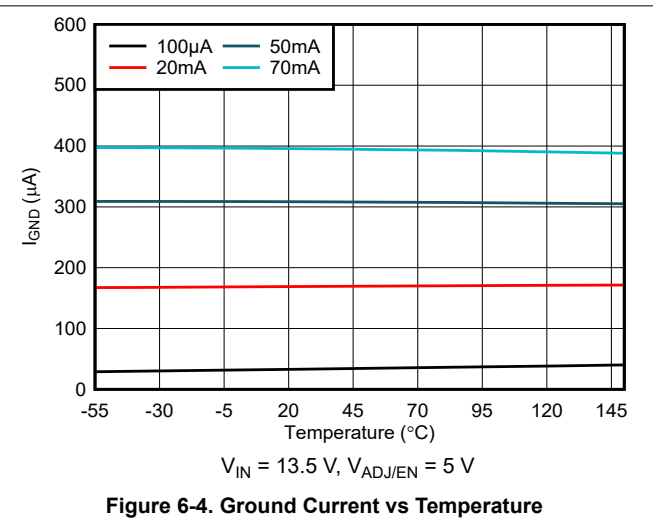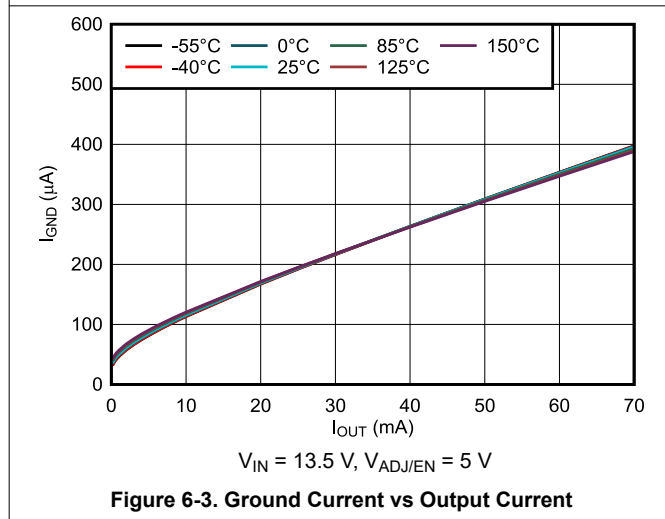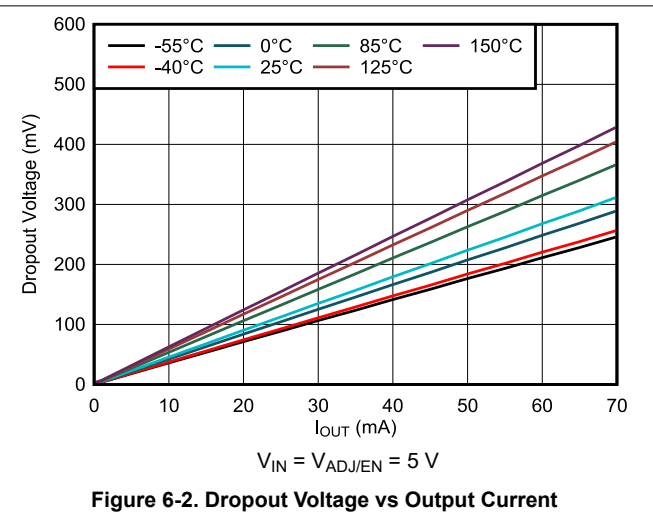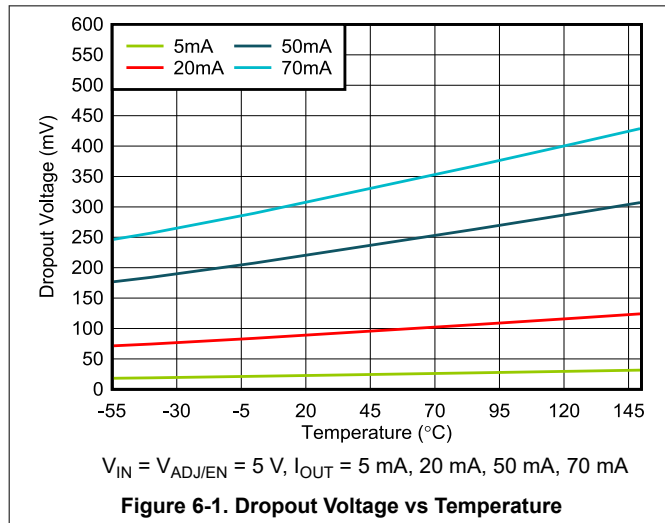| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\Delta V_{OUT}$ | Output voltage tracking accuracy | $V_{IN}$ = $V_{OUT}$ + 600 mV to 40 V, $I_{OUT}$ = 100 µA to 70 mA | –5 | | 5 | mV |
| $\Delta V_{OUT(\Delta VIN)}$ | Line regulation | $V_{IN}$ = $V_{OUT}$ + 600 mV to 40 V | | | 0.5 | mV |
| $\Delta V_{OUT(\Delta IOUT)}$ | Load regulation | $V_{IN}$ = $V_{OUT}$ + 600 mV, $I_{OUT}$ = 100 µA to 70 mA [(1)] | | | 0.5 | mV |
| $I_Q$ | Quiescent current | $V_{IN}$ = 5.6 V to 40 V, $I_{OUT}$ = 100 µA, $T_J$ = 25°C | | 34 | 40 | µA |
| | | $V_{IN}$ = 5.6 V to 40 V, $I_{OUT}$ = 100 µA, -40°C < $T_J$ < 85°C | | | 45 | |
| | | $V_{IN}$ = 5.6 V to 40 V, $I_{OUT}$ = 100 µA | | | 50 | |
| $I_{GND}$ | Ground current | $V_{IN}$ = 5.6 V to 40 V, $I_{OUT}$ = 70 mA, $T_J$ = 25°C | | | 470 | |
| | | $V_{IN}$ = 5.6 V to 40 V, $I_{OUT}$ = 70 mA | | | 550 | |
| $V_{DO}$ | Dropout voltage | $I_{OUT}$ = 70 mA, $V_{ADJ}$ ≥ 3.3 V, $V_{IN}$ = $V_{ADJ}$ | | | 470 | mV |
| | | $I_{OUT}$ = 50 mA, $V_{ADJ}$ ≥ 4 V, $V_{IN}$ = $V_{ADJ}$ | | | 330 | |
| $I_{SHUTDOWN}$ | Shutdown supply current ($I_{GND}$) | $V_{ADJ/EN}$ = 0 V | | | 3 | µA |
| $I_{ADJ/EN}$ | ADJ/EN pin current | | | | 0.25 | |
| $V_{UVLO(RISING)}$ | Rising input supply UVLO | $V_{IN}$ rising | 2.6 | 2.7 | 2.81 | V |
| $V_{UVLO(FALLING)}$ | Falling input supply UVLO | $V_{IN}$ falling | 2.3 | 2.4 | 2.5 | |
| $V_{UVLO(HYST)}$ | $V_{UVLO(IN)}$ hysteresis | | | 300 | | mV |
| $V_{IL}$ | Adjustable and enable logic input low level | | | | 1 | V |
| $V_{IH}$ | Adjustable and enable logic input high level | | 1.65 | | | |
| $I_{CL}$ | Output current limit | $V_{IN}$ = $V_{OUT}$ + 1 V, $V_{OUT}$ short to 90% x $V_{ADJ}$ | 75 | 100 | 130 | mA |
| PSRR | Power-supply ripple rejection | $V_{IN}$ - $V_{OUT}$ = 1 V, Frequency = 100 Hz, $I_{OUT}$ = 70 mA | | 80 | | dB |
| $V_n$ | Output noise voltage | $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 1 mA, a 5 µ$V_{RMS}$ reference is used for this measurement | | 150 | | µ$V_{RMS}$ |
| $I_R$ | Reverse current at $V_{IN}$ | $V_{IN}$ = 0 V, $V_{OUT}$ = 20 V, $V_{ADJ}$ = 5 V | -0.25 | | 0.25 | µA |
| $I_{RN1}$ | Reverse current at negative $V_{IN}$ | $V_{IN}$ = -20 V, $V_{OUT}$ = 20 V, $V_{ADJ}$ = 5 V | -0.5 | | 0.5 | |
| $I_{RN2}$ | Reverse current at negative $V_{IN}$ | $V_{IN}$ = -20 V, $V_{OUT}$ = 0 V, $V_{ADJ}$ = 5 V | -0.5 | | 0.5 | |
| $T_J$ | Junction temperature | | –40 | | 150 | °C |
| $T_{SD(SHUTDOWN)}$ | Junction shutdown temperature | | | 175 | | °C |
| $T_{SD(HYST)}$ | Hysteresis of thermal shutdown | | | 15 | | °C |

(1)     Power dissipation is limited to 2 W for device production testing purposes. The power dissipation can be higher during normal operation. Please see the thermal dissipation section for more information on how much power the device can dissipate while maintaining a junction temperature below 150°C.

## Timing Characteristics

specified at $V_{IN}$ = 13.5 V, $I_{OUT}$ = 100 µA, $C_{OUT}$ = 1 µF, $C_{IN}$ = 1 µF, and $V_{ADJ}$ = 5 V (unless otherwise noted), typical values are at $T_J$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Timing Characteristics** | | | | | | |
| tstartup | Startup time | Time from EN high to $V_{OUT}$ = 95% × $V_{ADJ}$ | | 255 | | µs |

## 6.6 Typical Characteristics



$V_{IN} = V_{ADJ/EN} = 5$ V, $I_{OUT} = 5$ mA, 20 mA, 50 mA, 70 mA

**Figure 6-1. Dropout Voltage vs Temperature**



$V_{IN} = V_{ADJ/EN} = 5$ V

**Figure 6-2. Dropout Voltage vs Output Current**



$V_{IN} = 13.5$ V, $V_{ADJ/EN} = 5$ V

**Figure 6-3. Ground Current vs Output Current**



$V_{IN} = 13.5$ V, $V_{ADJ/EN} = 5$ V

**Figure 6-4. Ground Current vs Temperature**



$V_{IN} = 13.5$ V, $V_{ADJ/EN} = 5$ V

**Figure 6-5. Current Limit vs Temperature**



$V_{IN} = 13.5$ V, $V_{ADJ/EN} = 5$ V
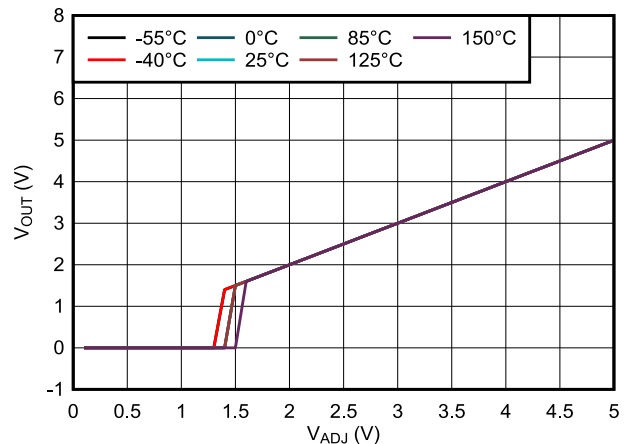
**Figure 6-6. Tracking Error vs Temperature**
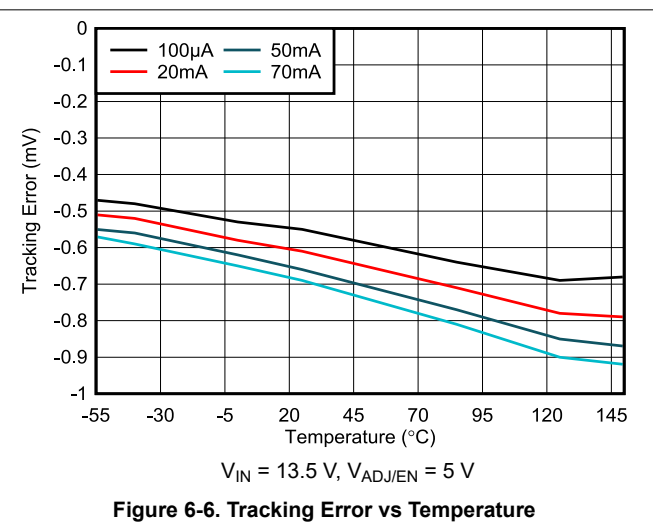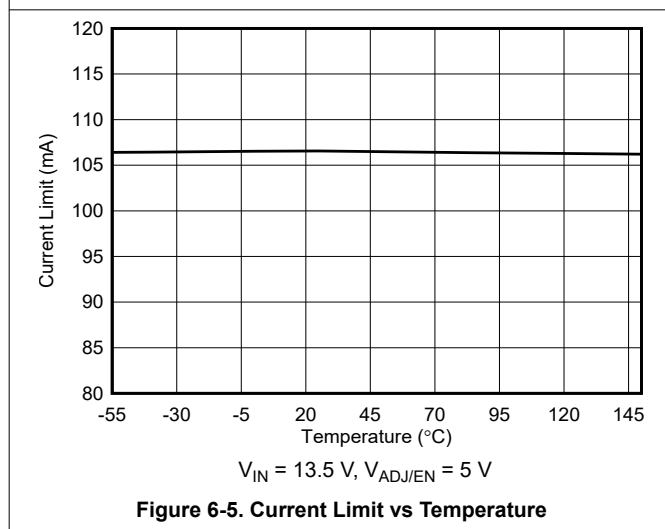
## 6.6 Typical Characteristics (continued)
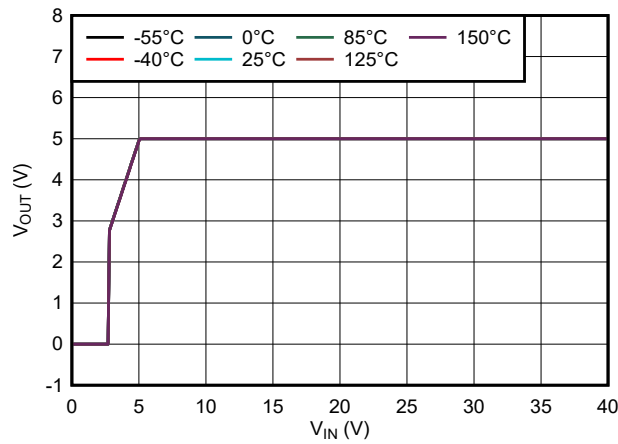


$V_{ADJ/EN}$ = 5 V, $I_{OUT}$ = 10 mA

**Figure 6-7. Output Voltage vs Input Voltage**



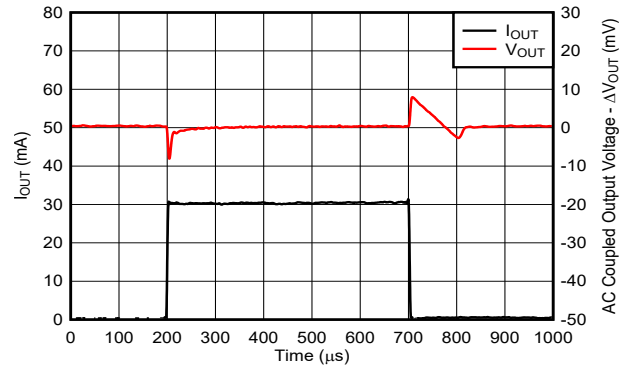$V_{IN}$ = 13.5 V, $I_{OUT}$ = 10 mA

**Figure 6-8. Output Voltage vs Adjustable Voltage**
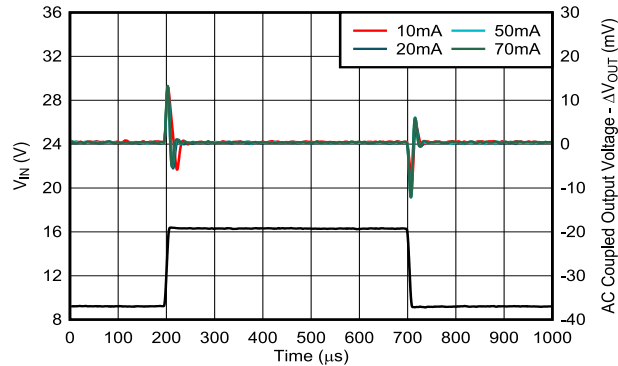


$V_{ADJ/EN}$ = 5 V, $C_{OUT}$ = 10 µF, $V_{IN}$ = 9 V to 16 V

**Figure 6-9. Line Transient**



$V_{IN}$ = 13.5 V, $V_{ADJ/EN}$ = 5 V, $C_{OUT}$ = 10 µF, $I_{OUT}$ = 1 mA to 30 mA

**Figure 6-10. Load Transient**
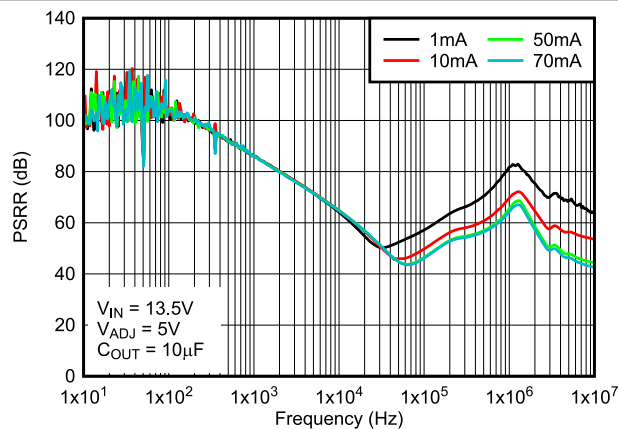


$V_{IN}$ = 13.5 V, $C_{OUT}$ = 10 µF, $I_{OUT}$ = 1 mA, 10 mA, 50 mA, 70 mA, $V_{ADJ/EN}$ = 5 V

**Figure 6-11. Power-Supply Rejection Ratio vs Frequency**
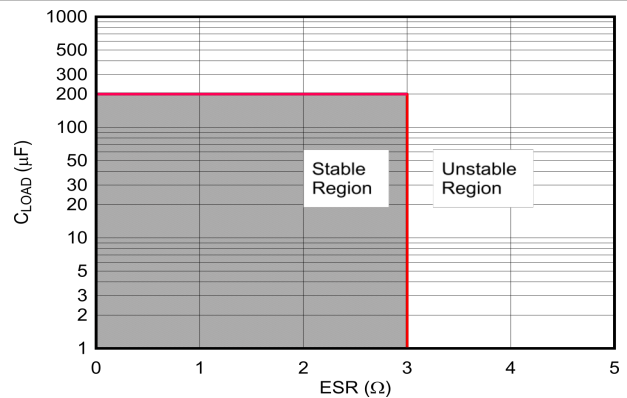


**Figure 6-12. Load Capacitance vs ESR Stability**

Product Folder Links: *TPS7B4255*

# 7 Detailed Description

## 7.1 Overview

The TPS7B4255 is an integrated, low-dropout (LDO) voltage tracker with ultra-low tracking tolerance. Because of the high risk of cable shorts when powering sensors off-board, multiple protection features are built into the LDO including short to battery, short to GND, and reverse current protection.

This device features thermal shutdown protection, brick-wall current limiting, undervoltage lockout (UVLO), and reverse current protection.
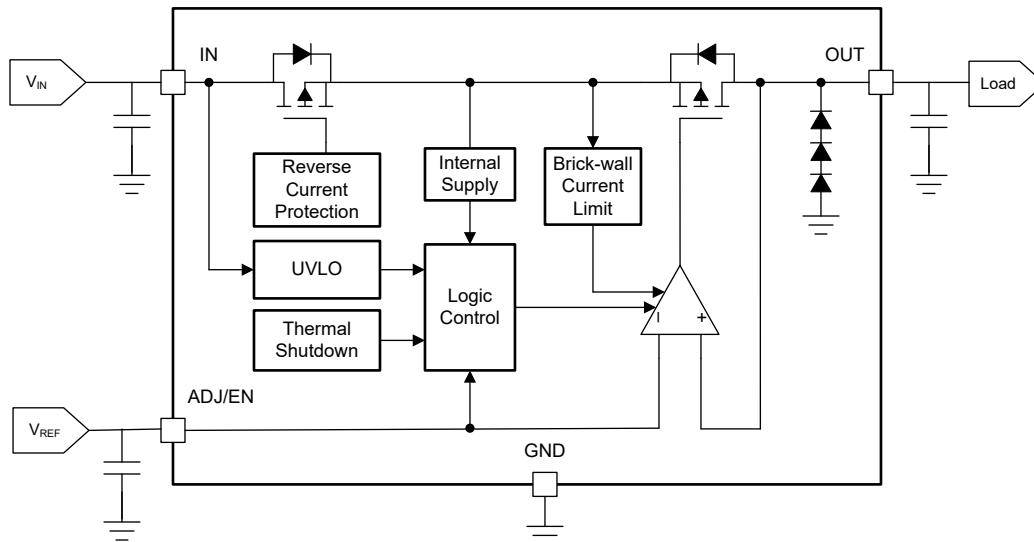
## 7.2 Functional Block Diagram



**Figure 7-1. Functional Block Diagram**

## 7.3 Feature Description

### 7.3.1 Regulated Output ($V_{OUT}$)

This device is a tracking LDO; thus, the output voltage is determined by the voltage provided to the ADJ/EN pin, provided that $V_{IN}$ is greater than $V_{IH}$. When the voltage at the ADJ/EN pin exceeds the required voltage to enable the LDO ($V_{IH}$), the output begins to rise to the voltage on the ADJ/EN pin. The output rises linearly as determined by the load, the output capacitor, and the current limit. When the voltage reaches the level on the ADJ/EN pin, the output voltage remains within 5 mV from the voltage set on the ADJ/EN pin over all specified operating conditions.

### 7.3.2 Undervoltage Lockout

The device has an internally fixed undervoltage lockout threshold. Undervoltage lockout activates when the input voltage on $V_{IN}$ drops below the undervoltage lockout (UVLO) level (see the $V_{UVLO(FALLING)}$ parameter in the *Electrical Characteristics* table). This activation makes sure the regulator is not latched into an unknown state during a low input supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up in the standard power-up sequence when the input voltage recovers to the required level (see the $V_{UVLO(RISING)}$ parameter in the *Electrical Characteristics* table).

### 7.3.3 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 175°C, which allows the device to cool. When the junction temperature cools to approximately 160°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle off and on until the excessive power dissipation condition is removed. This cycling limits the dissipation of the regulator, thus protecting the regulator from damage as a result of overheating.

The internal protection circuitry of the TPS7B4255 is designed to protect against overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the TPS7B4255 into thermal shutdown degrades device reliability.

### 7.3.4 Current Limit

The device has an internal current limit circuit to protect the device during overcurrent or shorting conditions. The current limit circuit, as shown in Figure 7-2, is a brick-wall scheme. When the device is in current limit, the device sources $I_{CL}$ and the output voltage is not regulated. In this scenario, the output voltage depends on the load impedance.

During a current limit event, the potential for high power dissipation exists because of the elevated current level and the increased input-to-output differential voltage ($V_{IN} - V_{OUT}$). If the device heats enough, the device can enter thermal shutdown. If the current-limit condition is not removed when the device turns back on after cooling, the device can enter thermal shutdown again and continue this cycle until the current limit condition is removed. The device survives this fault, but repeatedly operating in this mode degrades long-term reliability.
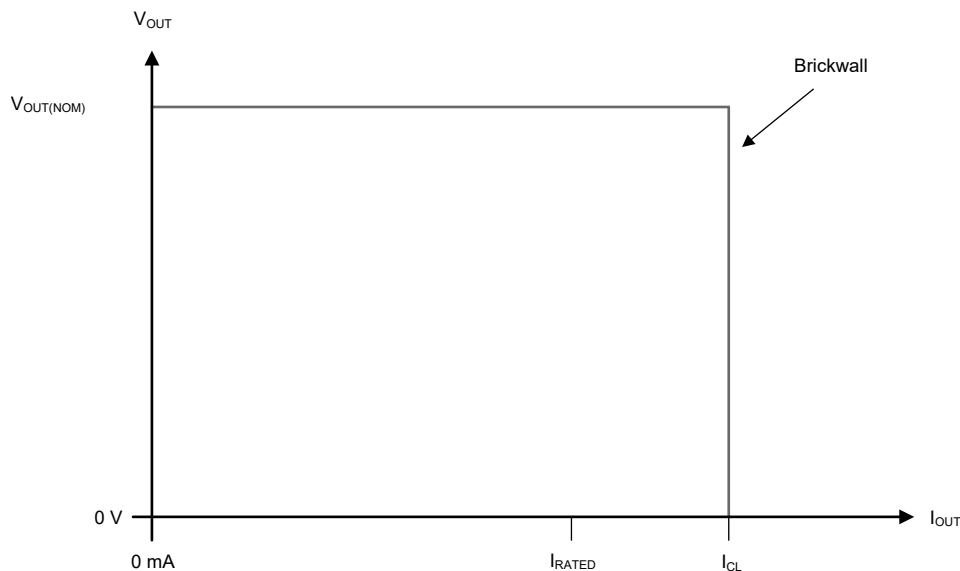


**Figure 7-2. Current Limit: Brick-Wall Scheme**

### 7.3.5 V<sub>OUT</sub> Short to Battery

When the output is shorted to the supply (as shown in Figure 7-3), the TPS7B4255 survives and no damage occurs to the device. As shown in Figure 7-4, a short to the supply can also occur when the device is powered by an isolated supply at a lower voltage. In this example, the TPS7B4255 supply input voltage is set at 7 V when a short to the main supply (14 V typical) occurs on $V_{OUT}$, which typically runs at 5 V. The device survives without damage, and continuous reverse current that flows out through $V_{IN}$ is less than 5 µA.
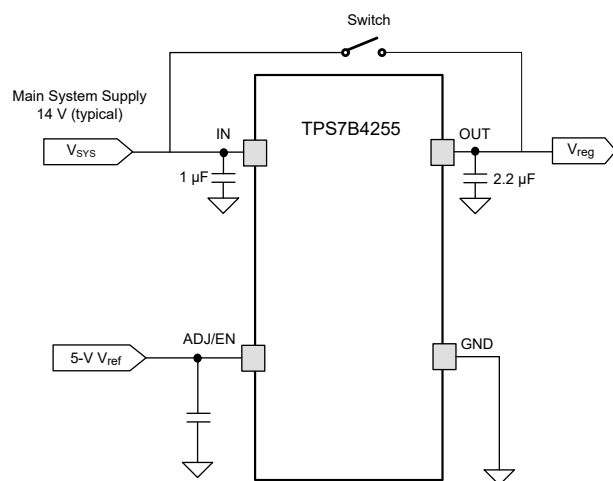


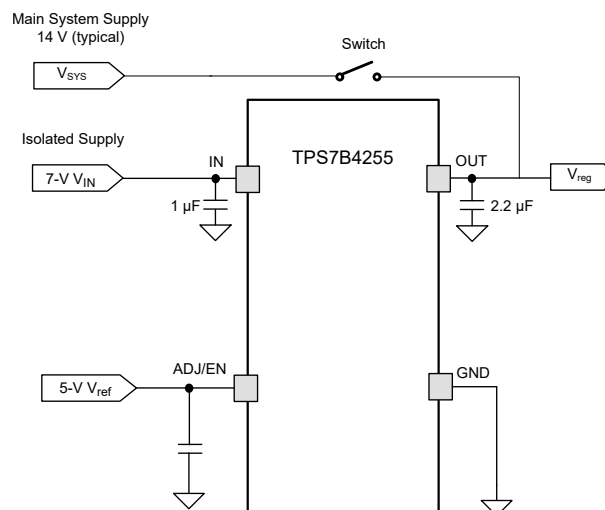**Figure 7-3. Output Voltage Short to Supply**



**Figure 7-4. Output Voltage Higher Than the Input**

### 7.3.6 Tracking Regulator With an Enable Circuit

Pulling the reference voltage below 0.7 V disables the device, and the device enters a sleep state where the device draws 3 µA (max) from the power supply. In a typical application, the reference voltage is generally sourced from another LDO voltage rail. A scenario where the device must be disabled without a shutdown of the reference voltage can occur; the device can be configured as shown in Figure 7-5 in this case. The TPS7B84-Q1 is a 150-mA LDO with ultra-low quiescent current that is used as a reference voltage to the TPS7B4255 and also as a power supply to the ADC. The operational status of the device is controlled by a microcontroller (MCU) input or output.
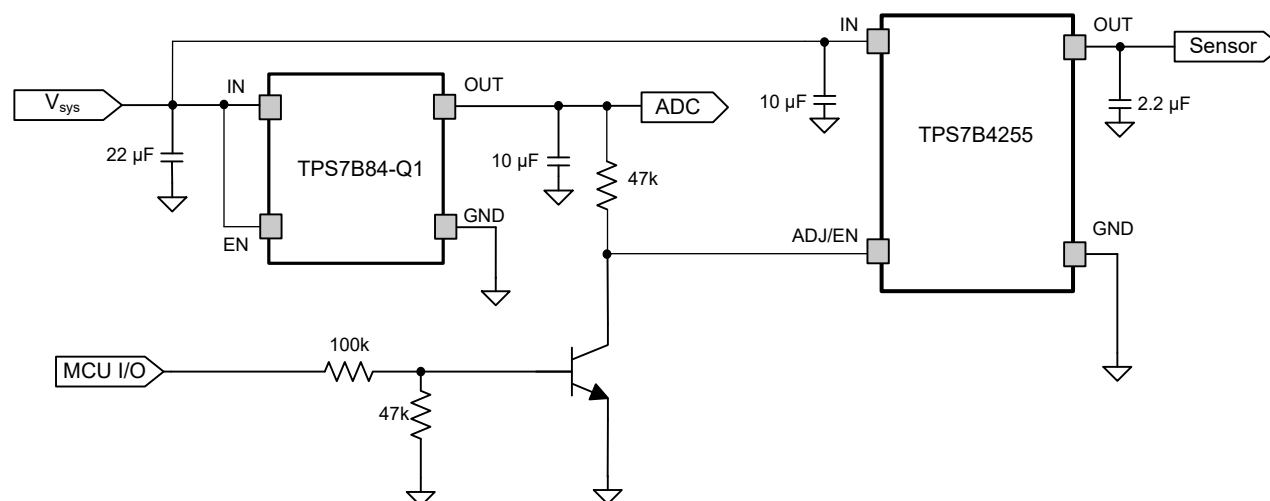


**Figure 7-5. Tracking an LDO With an Enable Circuit**

## 7.4 Device Functional Modes

The device operates with input voltages above 3 V to ensure proper operation. The device turns on when $V_{IN}$ is greater than $V_{UVLO(RISING)}$ and $V_{ADJ/EN}$ is greater than $V_{IH}$, and operates correctly as long as the input voltage stays above 3 V.

### 7.4.1 Operation With $V_{IN}$ < 3 V

For voltages below 3 V and above $V_{UVLO(FALLING)}$, the LDO continues to operate but certain circuits can possibly not have the proper headroom to operate within specification. When the input voltage drops below $V_{UVLO(FALLING)}$ the device shuts off again.

### 7.4.2 Operation With ADJ/EN Control

The ADJ/EN pin operates as both the reference and the enable pin to the LDO. When the input voltage is greater than $V_{UVLO(RISING)}$ and $V_{ADJ/EN}$ is greater than $V_{IH}$, the LDO is enabled and functional. When in this mode, the LDO tracks the voltage at the ADJ/EN pin because this pin functions as the reference to the control loop in the error amplifier. When $V_{IN}$ is greater than $V_{UVLO(RISING)}$ and $V_{ADJ/EN}$ is lower than $V_{IL}$, the LDO is disabled and is in a lower power mode.

# 8 Application and Implementation

> **Note**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

Depending on the end-application, different values of external components can be used. An application can require a larger output capacitor during fast load steps to prevent a reset from occurring. Use a low ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

### 8.1.1 Dropout Voltage

Dropout voltage ($V_{DO}$) is defined as the input voltage minus the output voltage ($V_{IN} - V_{OUT}$) when the pass transistor is fully on. This condition arises when the input voltage falls to the point where the error amplifier must drive the pass device all the way to the rail and has no remaining headroom for the control loop to operate. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage follows, minus the dropout voltage ($V_{DO}$).

In dropout mode, the output is no longer regulated, and transient performance is severely degraded. The device loses PSRR, and load transients can cause large output voltage deviation.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated output current ($I_{RATED}$, see the *Recommended Operating Conditions* table), the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

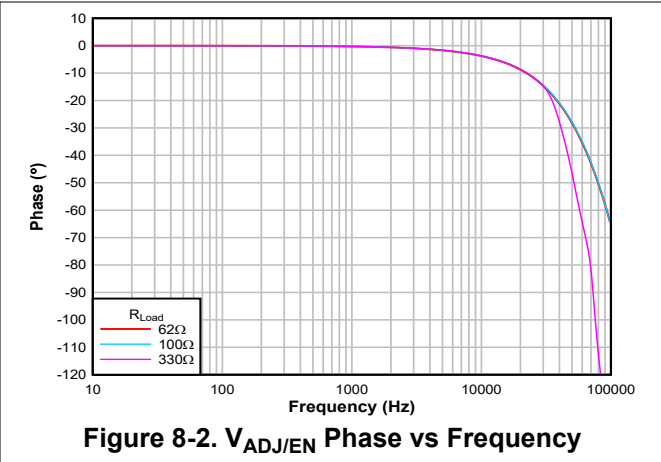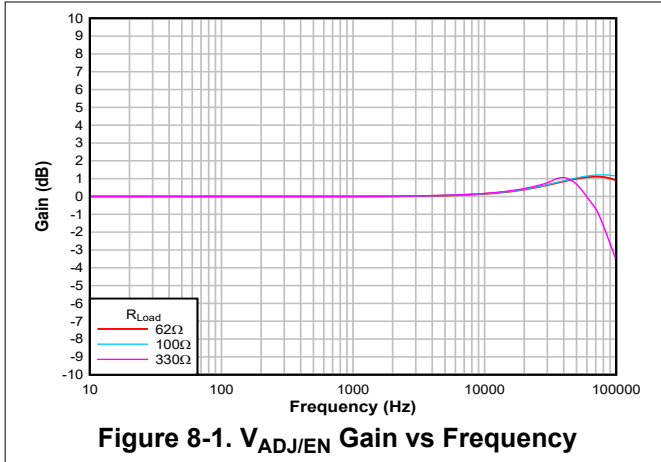$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}}$$

(1)

### 8.1.2 Reverse Current

The TPS7B4255 incorporates reverse current protection that prevents damage from a reverse polarity (that is, when $V_{OUT}$ is higher than $V_{IN}$). During a reverse polarity event, where the $V_{IN}$ and $V_{OUT}$ absolute maximum ratings are not violated and $V_{OUT} - V_{IN}$ is less than 40 V, no damage occurs and less than 5 µA flows out of $V_{IN}$. The reverse current comparator typically responds to a reverse voltage condition and limits the reverse current in 1 µs.

### 8.1.3 Signal-Buffering LDO

The TPS7B4255 can be used as a signal buffer up to frequencies of 1 kHz. The output tracks the signal in the ADJ/EN pin if $V_{ADJ/EN}$(min) is greater than $V_{IH}$. A phase change begins at approximately 2 kHz, causing distortion in the output signal. At frequencies higher than 2 kHz, the signal gets attenuated and distorted further.

Low-dropout regulators (LDOs) cannot sink current into the output, so for the signal-buffering circuit to operate correctly, the device must be loaded. The buffering LDO is limited by the current capability of the device, so use the minimum output capacitor (1 µF) to avoid high AC current.

Figure 8-1 and Figure 8-2 depict the gain and phase, respectively, for the buffering LDO with resistive loads of 62 Ω, 100 Ω, and 330 Ω, and $C_{OUT}$ = 1 µF.

Figure 8-1. $V_{ADJ/EN}$ Gain vs Frequency



Figure 8-2. $V_{ADJ/EN}$ Phase vs Frequency

## 8.2 Typical Application

Figure 8-3 shows a typical application circuit for the TPS7B4255.
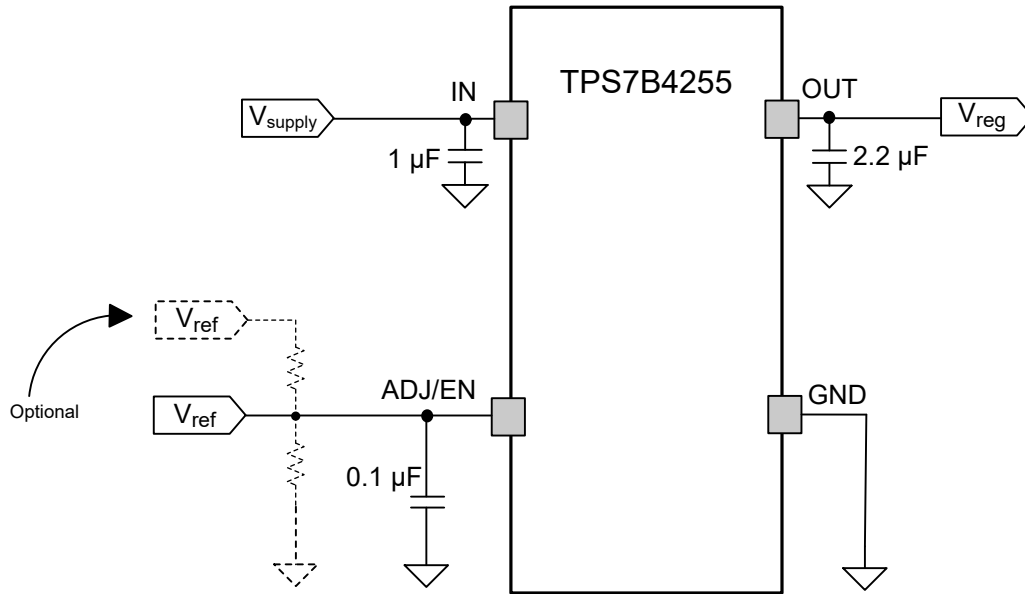


Figure 8-3. Typical Application Schematic

### 8.2.1 Design Requirements

Use the parameters listed in Table 8-1 for this design example.

**Table 8-1. Design Parameters**

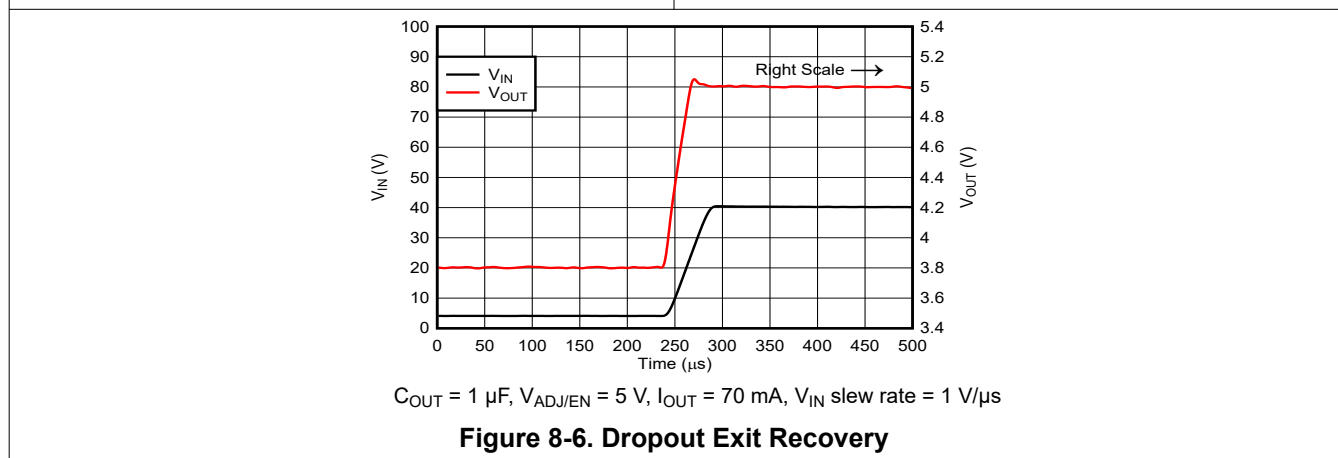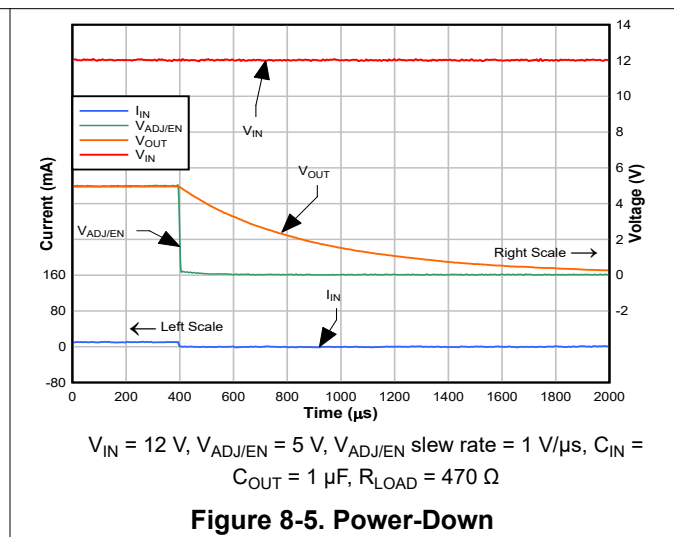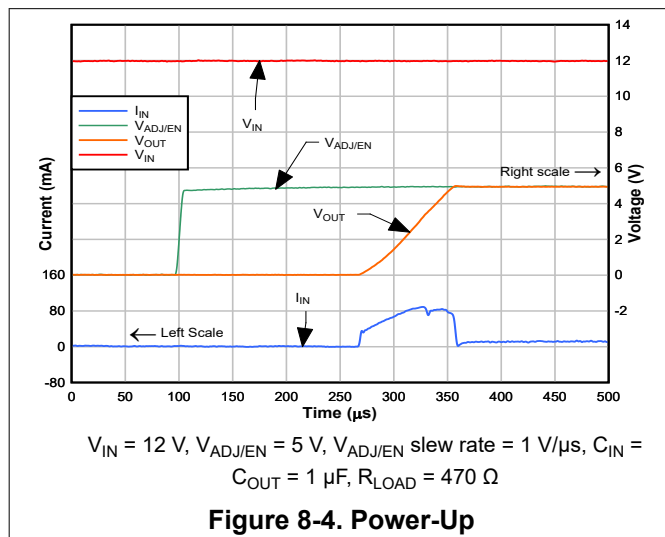| DESIGN PARAMETER | EXAMPLE VALUES |
|---|---|
| Input voltage | 3 V to 40 V |
| ADJ/EN reference voltage | 2 V to 30 V |
| Output voltage | 2 V to 30 V |
| Output current rating | 70 mA |
| Output capacitor range | 1 µF to 200 µF |
| Output capacitor ESR range | 1 mΩ to 3 Ω |

Product Folder Links: *TPS7B4255*

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Input and Output Capacitor Selection

The TPS7B4255 requires an output capacitor of at least 1 µF (500 nF or larger capacitance) for stability and an equivalent series resistance (ESR) between 0.001 Ω and 3 Ω. Without the output capacitor, the regulator oscillates. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitor is 200 µF.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND, connected close to the device pins. Some input supplies have a high impedance; thus, placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast rise-time load transients are anticipated, or if the device is located several inches from the input power source.

### 8.2.3 Application Curves



$V_{IN}$ = 12 V, $V_{ADJ/EN}$ = 5 V, $V_{ADJ/EN}$ slew rate = 1 V/µs, $C_{IN}$ = $C_{OUT}$ = 1 µF, $R_{LOAD}$ = 470 Ω

**Figure 8-4. Power-Up**



$V_{IN}$ = 12 V, $V_{ADJ/EN}$ = 5 V, $V_{ADJ/EN}$ slew rate = 1 V/µs, $C_{IN}$ = $C_{OUT}$ = 1 µF, $R_{LOAD}$ = 470 Ω

**Figure 8-5. Power-Down**



$C_{OUT}$ = 1 µF, $V_{ADJ/EN}$ = 5 V, $I_{OUT}$ = 70 mA, $V_{IN}$ slew rate = 1 V/µs

**Figure 8-6. Dropout Exit Recovery**

Product Folder Links: *TPS7B4255*

## 8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 3 V to 40 V. If the input supply is located more than a few inches from the TPS7B4255, add an electrolytic capacitor with a value of 10 µF and a ceramic bypass capacitor at the input.

## 8.4 Layout

### 8.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. The use of vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. TI also recommends a ground reference plane either embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similarly to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

#### 8.4.1.1 Package Mounting

Solder-pad footprint recommendations for the TPS7B4255 are available at the end of this document and at www.ti.com.

#### 8.4.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for $V_{IN}$ and $V_{OUT}$, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close as possible to the device and on the same side of the printed circuit board (PCB) as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. Using vias and long traces is strongly discouraged because of the negative impact on system performance. Vias and long traces can also cause instability.

If possible, and to make sure that the maximum performance is as denoted in this product data sheet, use the same layout pattern used for the TPS7B4255 evaluation board, available at www.ti.com.

#### 8.4.1.3 Power Dissipation and Thermal Considerations

Equation 2 calculates the device power dissipation.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_Q \times V_{IN} \tag{2}$$

where:

- $P_D$ = Continuous power dissipation
- $I_{OUT}$ = Output current
- $V_{IN}$ = Input voltage
- $V_{OUT}$ = Output voltage
- $I_Q$ = Quiescent current

Because $I_Q$ is much less than $I_{OUT}$, the term $I_Q \times V_{IN}$ in Equation 2 can be ignored.

Calculate the junction temperature ($T_J$) with Equation 3 for a device under operation at a given ambient air temperature ($T_A$).

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{3}$$

where:

- $R_{\theta JA}$ = Junction-to-junction-ambient air thermal impedance

Equation 4 calculates a rise in junction temperature because of power dissipation.

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D) \tag{4}$$

The maximum ambient air temperature ($T_{AMAX}$) at which the device can operate can be calculated with Equation 5 for a given maximum junction temperature ($T_{JMAX}$).

$$T_{AMAX} = T_{JMAX} - (R_{\theta JA} \times P_D) \tag{5}$$

### 8.4.1.4 Thermal Performance Versus Copper Area

The most used thermal resistance parameter $R_{\theta JA}$ is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard (Figure 8-7), PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.
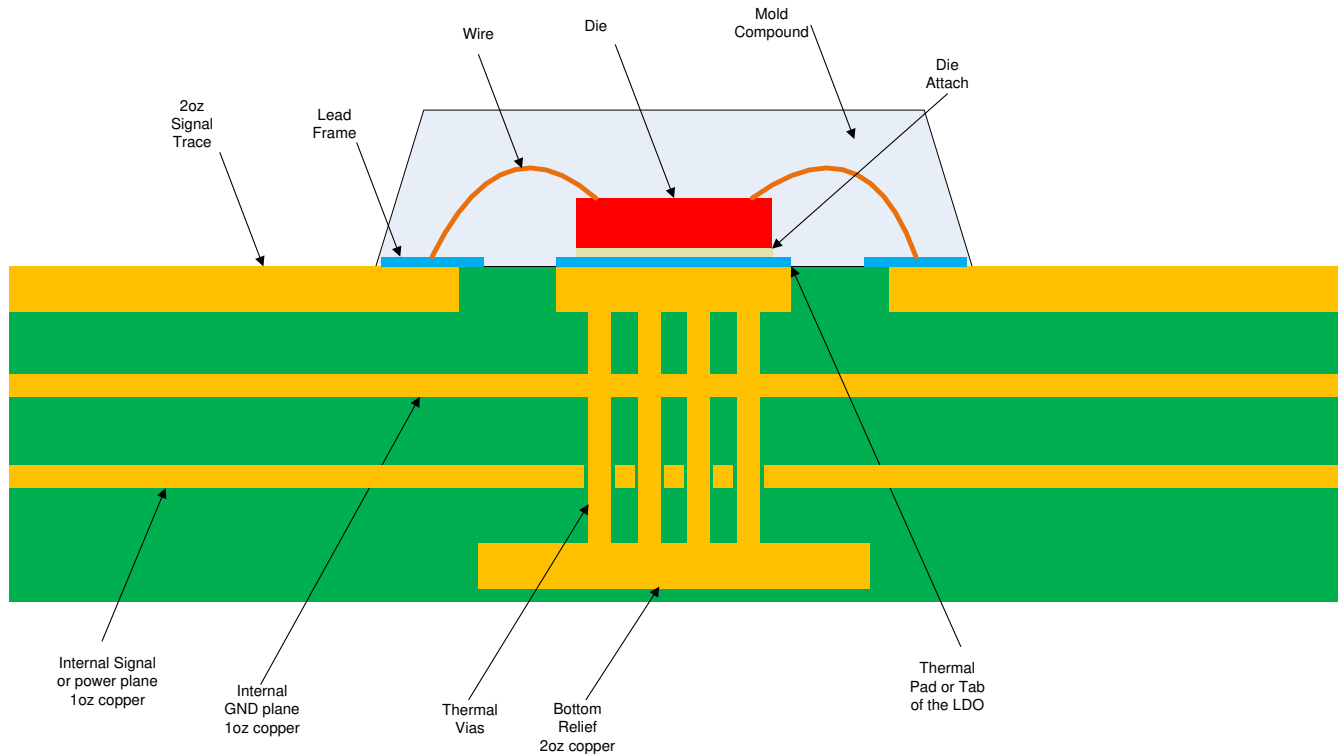


**Figure 8-7. JEDEC Standard 2s2p PCB**

Figure 8-8 and Figure 8-9 illustrate the functions of $R_{\theta JA}$ and $\psi_{JB}$ versus copper area and thickness. These plots are generated with a 101.6-mm × 101.6-mm × 1.6-mm PCB of two and four layers. For the 4-layer board, inner planes use 1-oz copper thickness. Outer layers are simulated with both 1-oz and 2-oz copper thickness. A 4 x 5 (DBV package) array of thermal vias with a 300-μm drill diameter and 25-μm copper plating is located as close as practical to the GND pin of the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. Each of the layers has a copper plane of equal area.

As illustrated in Figure 8-9, $\psi_{JB}$ increases with increasing connecting copper area. The reason for this increase is that the board temperature is measured at the copper near the GND pin, and because the GND pin is fused to the die pad, more heat escapes through the GND pin when more copper is connected to the pad, and thus

the temperature at this point is higher. Consequently the $\psi_{JB}$ increases. This increase does not imply that heat sinking for the device is reduced when more connecting copper is added. Increasing connecting copper area always increases board-level heat sinking for the device. Furthermore, the boards used for Figure 8-9 have vias connecting to internal copper planes. Therefore, $\psi_{JB}$ is much higher than what is specified in the *Thermal Information* table, which uses the high-K board layout specified in JESD51-7 that has no thermal vias.
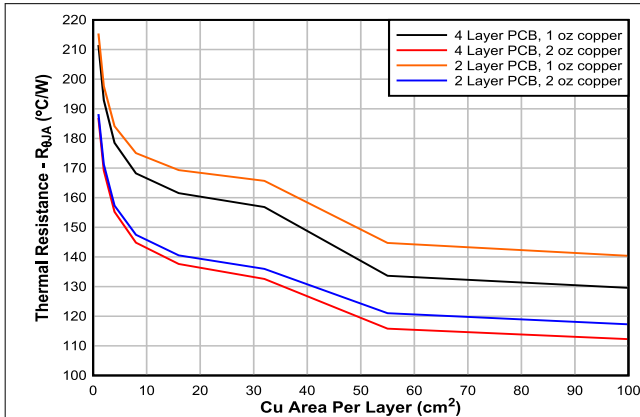


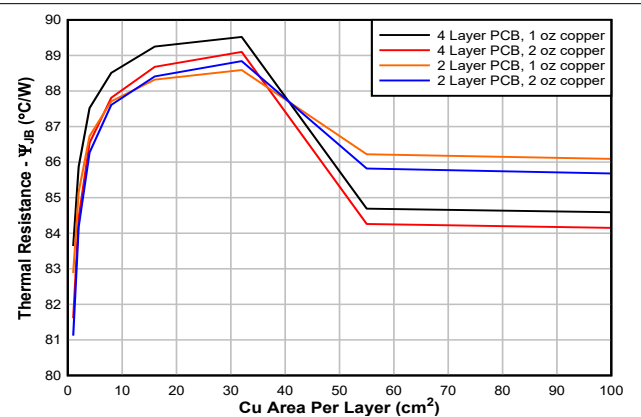Figure 8-8. $R_{\theta JA}$ vs Copper Area (DBV Package)



Figure 8-9. $\psi_{JB}$ vs Copper Area (DBV Package)
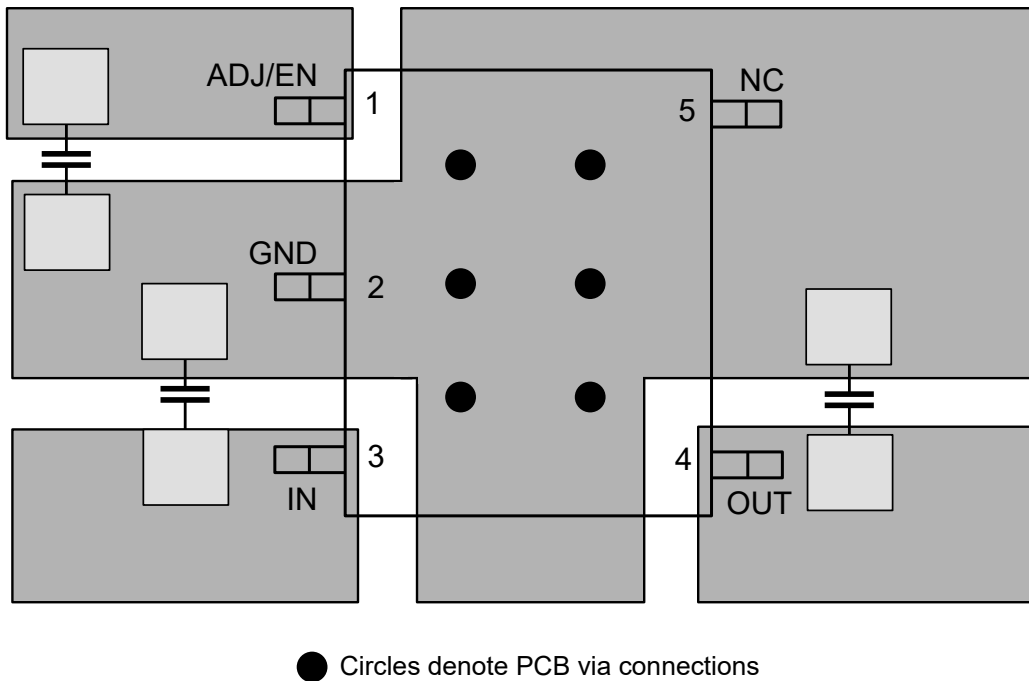
### 8.4.2 Layout Example



● Circles denote PCB via connections

**Figure 8-10. DBV Package Layout Example**

# 9 Device and Documentation Support

## 9.1 Device Support

### 9.1.1 Device Nomenclature

#### Table 9-1. Device Nomenclature[1]

| PRODUCT | $V_{OUT}$ |
|---|---|
| TPS7B4255**yyyR** | **yyy** is the package designator.<br>**R** is the packaging quantity. |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

### 9.1.2 Development Support

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

TI Glossary          This glossary lists and explains terms, acronyms, and definitions.

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *TPS7B4255*

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7B4255DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2W4F | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS7B4255 :**

● Automotive : TPS7B4255-Q1

NOTE: Qualified Version Definitions:

   ● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**



Reel Diameter

Reel Width (W1)

**TAPE DIMENSIONS**



Cavity

| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Sprocket Holes

| Q1 | Q2 |
| Q3 | Q4 |

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7B4255DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS7B4255DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |

PIN 1
INDEX AREA

3.0
2.6

1.75
1.45

B

A

2X 0.95

1.9

1

2

3

5

4

(0.1)

(0.15)

3.05
2.75

1.9

5X 0.5
0.3

⊕ 0.2 Ⓜ C A B

NOTE 5

C

◁ 0.1 C

1.45
0.90

(1.1)

0.15
0.00 TYP

0.25

GAGE PLANE

8°
0° TYP

0.6
0.3 TYP

SEATING PLANE

0.22
0.08 TYP
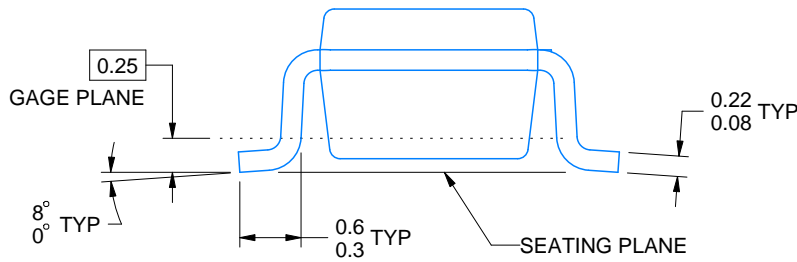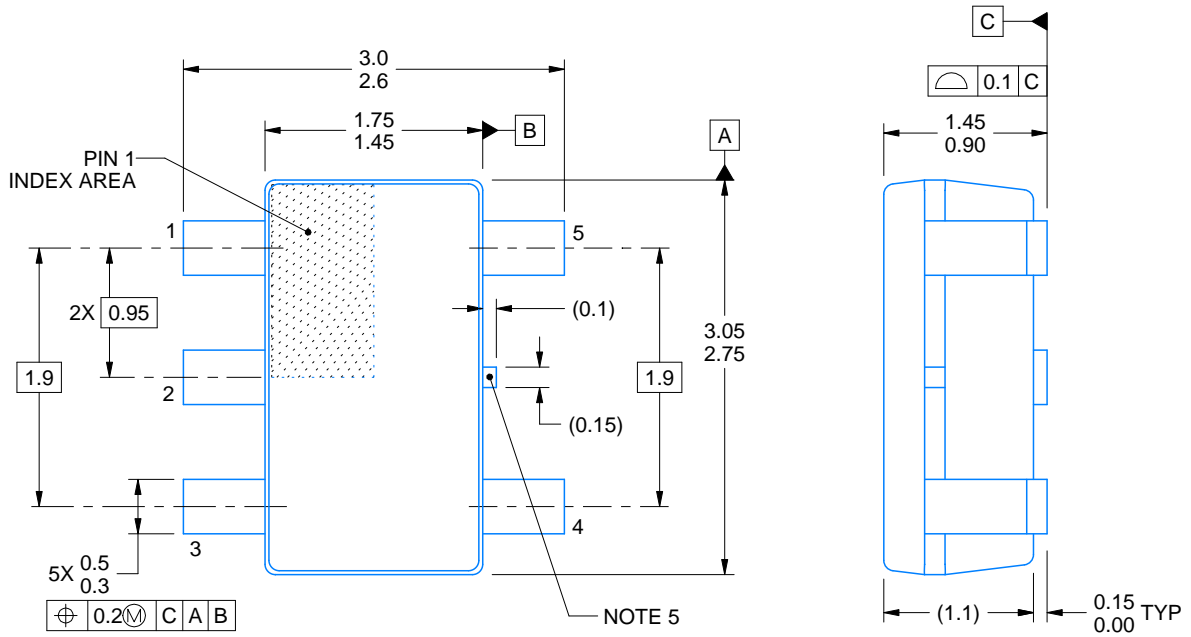
4214839/G   03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.
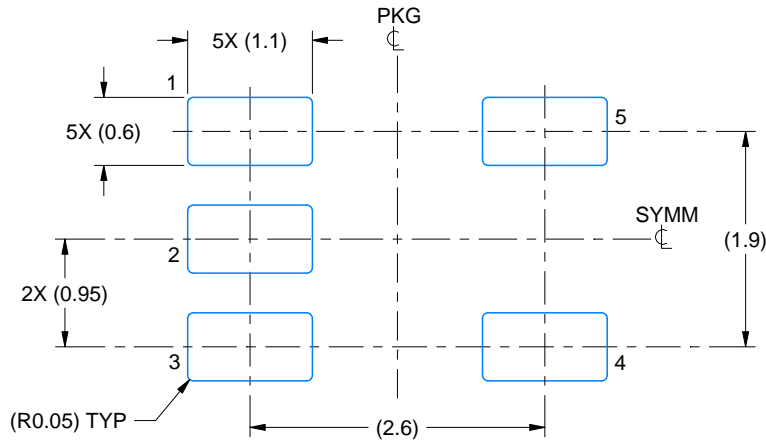
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

5X (1.1)

PKG

1

5X (0.6)

5

2

SYMM

(1.9)

2X (0.95)

3

4

(R0.05) TYP

(2.6)

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/G   03/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PKG

5X (1.1)

1

5X (0.6)

5

SYMM

2

(1.9)

2X(0.95)

3

4

(R0.05) TYP

(2.6)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/G   03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# IMPORTANT NOTICE AND DISCLAIMER