VC-709

HCSL, LVDS, LVPECL Crystal Oscillator Data Sheet

Description

Vectron's VC-709 Crystal Oscillator is a quartz stabilized, differential output oscillator, operating off a 2.5 or 3.3 volt supply in a hermetically sealed 5x7 ceramic package.

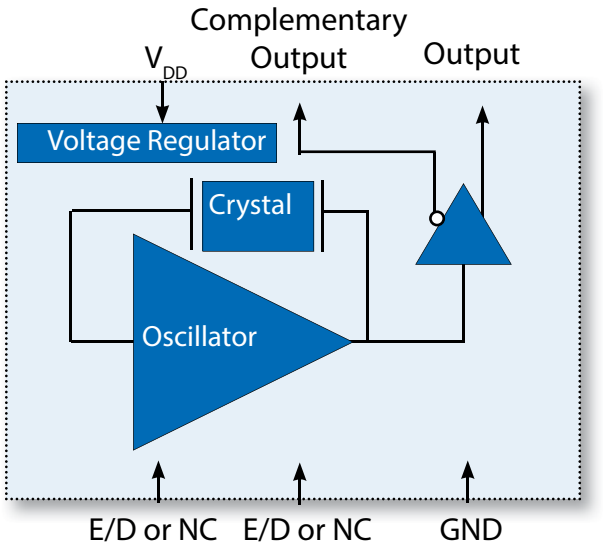
Features

- Ultra Low Jitter Performance, 3rd OT or Fundamental Crystal Design
- 13.500-220.0000MHz Output Frequencies
- Low Power
- 400ps max Rise and Fall Time
- Excellent Power Supply Rejection Ratio
- Enable/Disable
- 3.3 or 2.5V operation
- -10/70°C or -40/85°C Operation
- Hermetically Sealed 5x7 Ceramic Package
- Product is compliant to RoHS directive and fully compatible with lead free assembly

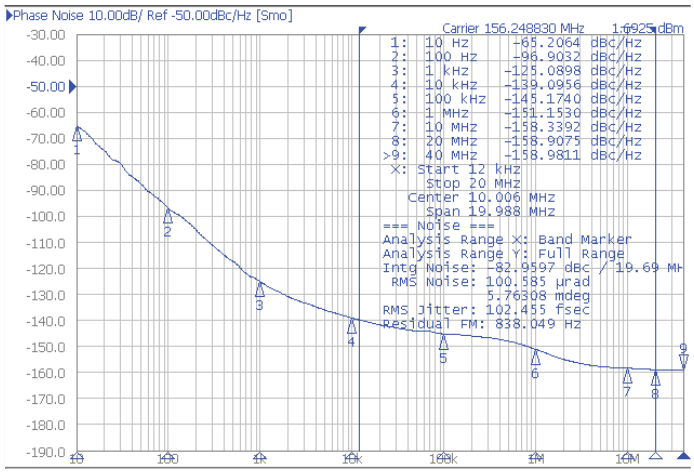
Applications

- PCI Express
- Ethernet, GbE, Synchronous Ethernet
- Fiber Channel
- Enterprise Servers
- Telecom
- Clock source for A/D's, D/A's
- Driving FPGA's
- Test and Measurement
- PON
- Medical
- COTS

Block Diagram



Phase Noise



Performance Specifications

Table 1. Electrical Performance, LVPECL Option					
Parameter	Symbol	Min	Typical	Maximum	Units
Voltage[1]	V_{DD}	3.135 2.375	3.3 2.5	3.465 2.625	V V
Current[2], 3.3V 2.5V	I_{DD}			45 42	mA
Frequency					
Nominal Frequency : 3.3V Supply 2.5V Supply	f_N	13.5 125.0		220.000 220.00	MHz
Stability[3] (Ordering Option)		±20, ±25, ±50 or ±100			ppm
Outputs					
Output Logic Levels[2] Output Logic High Output Logic Low	 V_{OH} V_{OL}	 V_{DD}-1.025 V_{DD}-1.810		 V_{DD}-0.880 V_{DD}-1.650	 V V
Output Rise and Fall Time[2]	t_R/t_F			400	ps
Load		50 ohms into V_{DD}-2.0V			
Duty Cycle[4]		45		55	%
Jitter[5], 156.250MHz 12kHz-50MHz 12kHz -20MHz 10kHz-1MHz	ϕJ			 200 150 100	 fs fs fs
Period Jitter[6], 156.250MHz, RMS P/P Cycle-Cycle[6] RMS P/P Random Jitter[7] Deterministic Jitter[7]	ϕJ		 1.1 10.5 1.9 17.7 2.2 0	 2.2 21.0 3.8 35.4 4.4	 ps ps ps ps ps ps
Enable/Disable					
Outputs Enabled[8] Outputs Disabled	V_{IH} V_{IL}	0.7*V_{DD}		 0.3*V_{DD}	V V
Disable Time	t_D			200	ns
Enable/Disable Leakage Current				±200	uA
Start-Up Time	t_{SU}			10	ms
Operating Temp. (Ordering Option)	T_{OP}	-10/70 or -40/85			°C
Package Size		5.0 x 7.0 x 1.5			mm

1. The VC-709 power supply pin should be filtered, eg, a 10uf, 0.1uf and 0.01uf capacitor.
2. Figure 1 defines the test circuit and Figure 2 defines these parameters.
3. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
4. Duty Cycle is defined as the On/Time Period.
5. Measured using an Agilent E5052.
6. Measured using a LeCroy Wavemaster 8600A, 90K samples
7. Measured using a Wavecrest SIA3300C, 90K samples.
8. Outputs will be Enabled if Enable/Disable is left open.

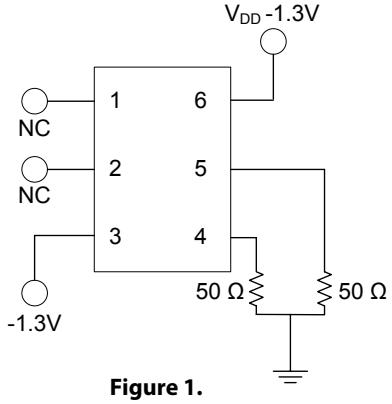


Figure 1.

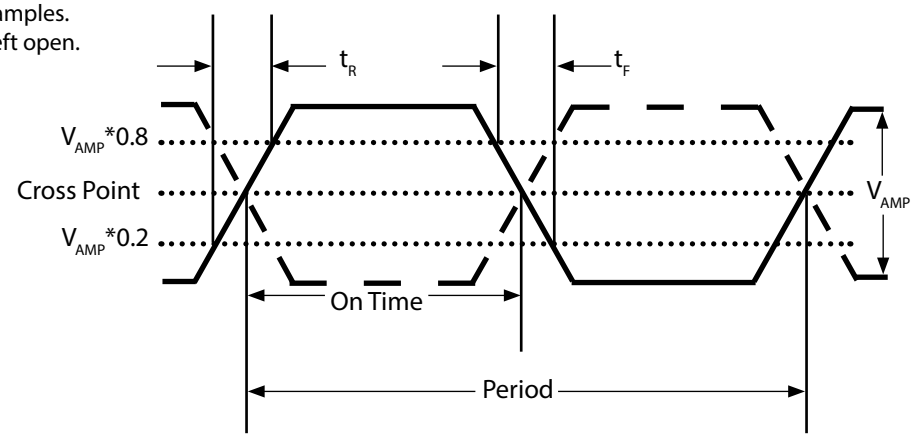


Figure 2.

Performance Specifications

Table 2. Electrical Performance, LVDS Option

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	3.135 2.375	3.3 2.5	3.465 2.625	V V
Current[2], 3.3V 2.5V	I_{DD}			17 14	mA
Frequency					
Nominal Frequency	f_N	13.5		220.000	MHz
Stability[3] (Ordering Option)		±20, ±25, ±50 or ±100			ppm
Outputs					
Output Logic Levels[2] Output Logic High Output Logic Low	 V_{OH} V_{OL}	 0.9	 1.43 1.10	 1.6	 V V
Output Amplitude		250	350	450	mV
Differential Output Error				50	mV
Offset Voltage		1.125	1.25	1.375	V
Offset Voltage Error				50	mV
Output Leakage Current, Outputs Disabled				10	uA
Output Rise and Fall Time[3]	t_R/t_F			400	ps
Load		100 ohms differential			
Duty Cycle[4]		45		55	%
Jitter[5], 156.250MHz 12kHz - 50MHz 12kHz - 20MHz 10kHz - 1MHz	ϕJ			 200 150 100	 fs fs fs
Period Jitter[6], 156.250MHz RMS P/P Cycle-Cycle Jitter[6] RMS P/P Random Jitter[7] Deterministic Jitter[7]	ϕJ		 1.1 10.5 1.9 17.7 2.2 0	 2.2 21.0 3.8 35.4 4.4	 ps ps ps ps ps ps
Enable/Disable					
Outputs Enabled[8] Outputs Disabled	V_{IH} V_{IL}	0.7*V_{DD}		 0.3*V_{DD}	V V
Disable Time	t_D			200	ns
Enable/Disable Leakage Current	$I_{E/D}$			±200	uA
Start-Up Time	t_{SU}			10	ms
Operating Temp. (Ordering Option)	T_{OP}	-10/70 or -40/85			°C
Package Size		5.0 x 7.0 x 1.5			mm

1. The VC-709 power supply pin should be filtered, eg, a 10uf, 0.1uf and 0.01uf capacitor.
2. Figure 2 defines these parameters and Figure 3 defines the test circuit.
3. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
4. Duty Cycle is defined as the On/Time Period.
5. Measured using an Agilent E5052.
6. Measured using a LeCroy Wavemaster 8600A, 90K samples.
7. Measured using a Wavecrest SIA3300C, 90K samples.
8. Outputs will be Enabled if Enable/Disable is left open.

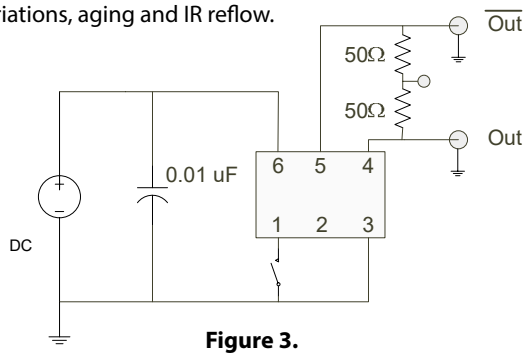


Figure 3.

Performance Specifications

Table 3. Electrical Performance, HCSL Output

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	2.375 3.165	2.5 3.3	2.625 3.465	V V
Current[2]	I_{DD}			39	mA
Frequency					
Nominal Frequency	f_N	13.5		170	MHz
Stability[3] (Ordering Options)		±25, ±50 or ±100			ppm
Outputs					
Output High, 3.3V Output High, 2.5V	V_{OH}	600 580		850 850	mV mV
Output Low	V_{OL}	-150		150	mV
Output Logic Swing, 3.3V Output Logic Swing, 2.5V	V_{OPP}	0.65 0.60			V V
Output Rise and Fall Time[3]	t_R/t_F			500	ps
Load		50 ohms to ground			
Duty Cycle[4]		45		55	%
Jitter[5] (12 kHz - 20 MHz) 100.000MHz	ϕJ			300	fs
Period Jitter[6], 100.000MHz RMS P/P Cycle-Cycle Jitter[6] RMS P/P Random Jitter[7] Deterministic Jitter[7]	ϕJ		 1.0 9.7 1.8 18.3 2.2 0	 2.0 19.4 3.6 36.6 4.4	 ps ps ps ps ps ps
Enable/Disable					
Outputs Enabled[8] Outputs Disabled	V_{IH} V_{IL}	0.7*V_{DD}		 0.3*V_{DD}	V V
Disable Time	t_D			200	ns
Enable/Disable Leakage Current	$I_{E/D}$			±200	uA
Start-Up Time	t_{SU}			10	ms
Operating Temp. (Ordering Option)	T_{OP}	-10/70 or -40/85			°C
Package Size		5.0 x 7.0 x 1.5			mm

1. The VC-709 power supply pin should be filtered, e.g., a 10uf, 0.1uf and 0.01uf capacitor.
2. Figure 4 defines the test circuit and Figure 5 defines these parameters.
3. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
4. Duty Cycle is defined as the On Time/Period.
5. Measured using an Agilent E5052.
6. Measured using a LeCroy Wavemaster 8600A, 90K samples.
7. Measured using a Wavecrest SIA3300C, 90K samples.
8. Outputs will be Enabled if the Enable/Disable pad is left open.

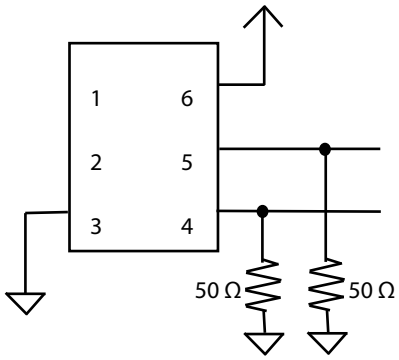


Figure 4.

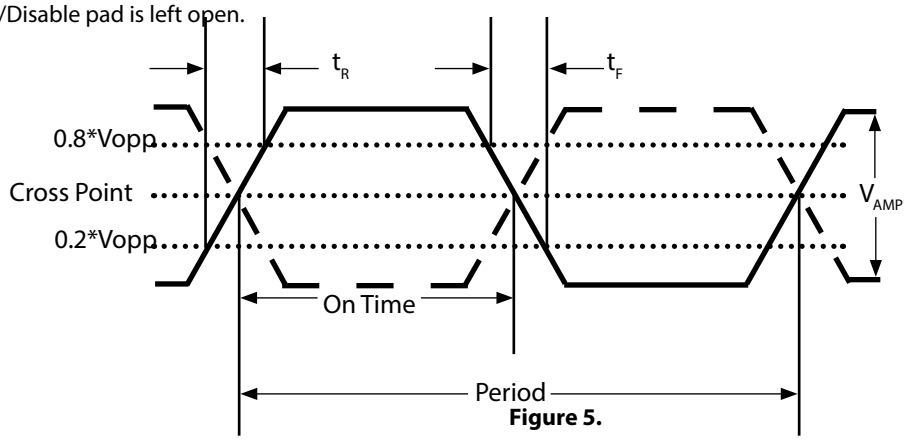


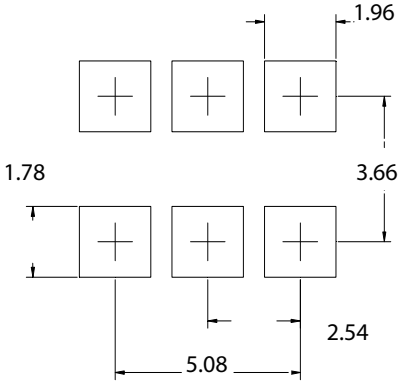
Figure 5.

Package and Pinout

Table 4. Pinout

Pin #	Symbol	Function
1	E/D or NC	Enable/Disable or No Connection
2	E/D or NC	Enable/Disable or No Connection
3	GND	Electrical and Lid Ground
4	f_O	Output Frequency
5	Cf_O	Complementary Output Frequency
6	V_{DD}	Supply Voltage

Marking Information
XXXMXX - Frequency (Example: 100M00)
YY - Year of Manufacture
WW - Week of the Year
C - Manufacturing Location
● - Pin 1 Indicator



Dimensions are in mm

Figure 6. Pad Layout

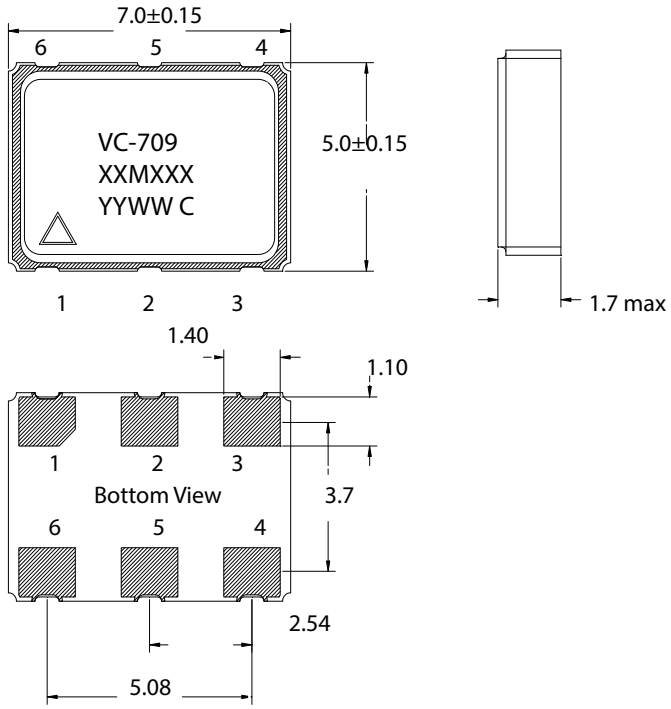


Figure 7. Package Outline Drawing

HCSL Application Diagrams

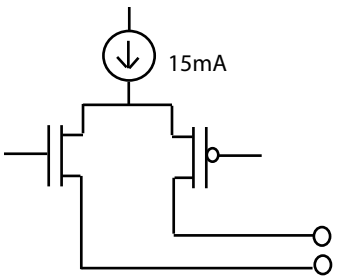


Figure 8.
Standard HCSL Output Configuration

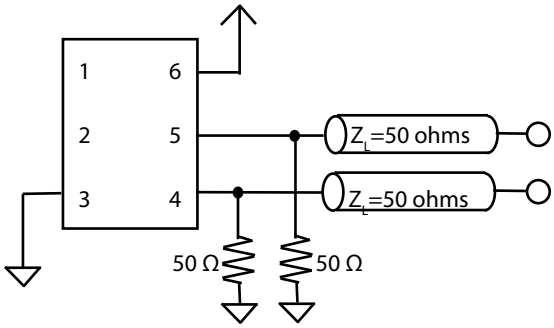


Figure 9.
Single Resistor Termination Scheme

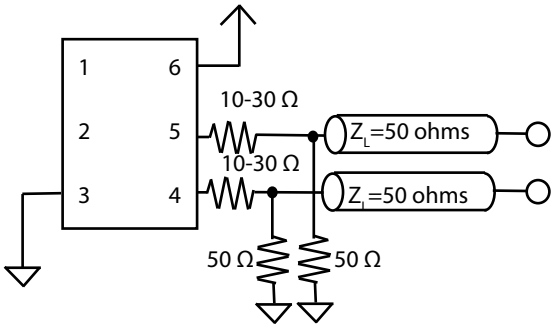


Figure 10.
In some cases a 10-30 ohm series resistor is used to help reduce overshoot.

The VC-709 incorporates a standard High Speed Current Logic, HCSL ,output scheme which is a 15mA current source switched between Out and Complementary Out. Being un-terminated drains, as shown in Figure 8, they require external 50 ohm resistors to ground as shown in Figure 9. HCSL is a high impedance output with quick switching times, in can be advantageous to use a 10 to 30 ohm series resistor as shown in Figure 10, to help reduce overshoot/ringing.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

LVPECL Application Diagrams

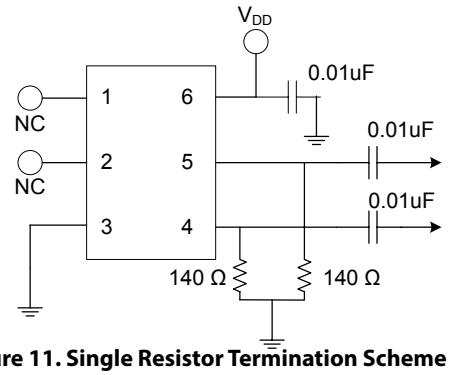


Figure 11. Single Resistor Termination Scheme
Resistor values are typically 140 ohms for 3.3V operation and 84 ohms for 2.5V operation.

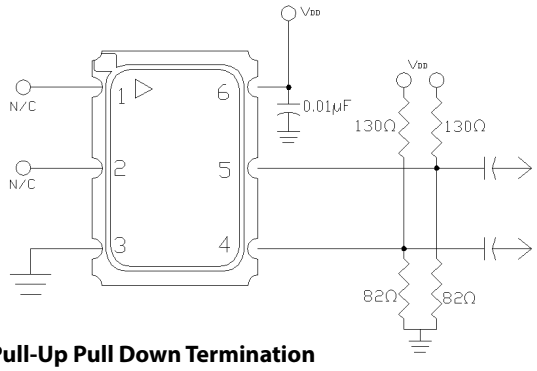


Figure 12. Pull-Up Pull Down Termination
Resistor values shown are typical for 3.3 V opertaion. For 2.5V operation, the resistor to ground is 62 ohms and the resistor to supply is 250 ohms

The VC-709 incorporates a standard PECL output scheme, which are un-terminated FET drains. There are numerous application notes on terminating and interfacing PECL logic and the two most common methods are a single resistor to ground, Figure 11, or for best 50 ohm matching a pull-up/pull-down scheme as shown in Figure 12 should be used. AC coupling capacitors are optional, depending on the application and the input logic requirements of the next stage.
One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

LVDS Application Diagrams

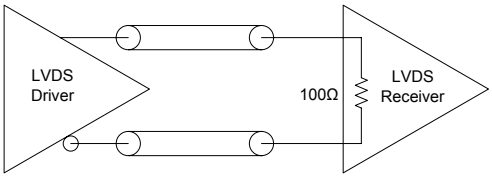


Figure 13. LVDS to LVDS Connection, Internal 100ohm Resistor
Some LVDS structures have an internal 100 ohm resistor on the input and do not need additional components. AC blocking capacitors can be used if the DC levels are incompatible.

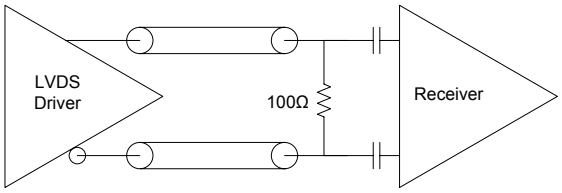


Figure 14. LVDS to LVDS Connection
Some input structures may not have an internal 100 ohm resistor on the input and will need an external 100ohm resistor for impedance matching. Also, the input may have an internal DC bias which may not be compatible with LVDS levels, AC blocking capacitors can be used.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

Environmental and IR Compliance

Table 5. Environmental Compliance

Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002
Mechanical Vibration	MIL-STD-883 Method 2007
Temperature Cycle	MIL-STD-883 Method 1010
Solderability	MIL-STD-883 Method 2003
Fine and Gross Leak	MIL-STD-883 Method 1014
Resistance to Solvents	MIL-STD-202 Method 215
Moisture Sensitivity Level	MSL1
Contact Pads	Gold (0.3-1.0um) over Nickel
ThetaJC (bottom of case)	31 °C/W
Wieght	167 mg

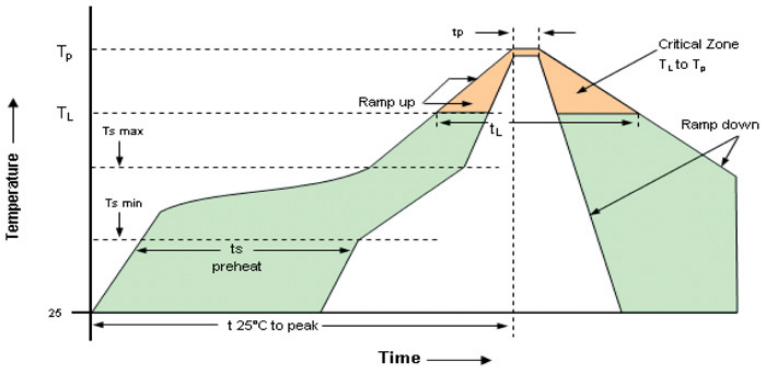
IR Compliance

Suggested IR Profile

Devices are built using lead free epoxy and can be subjected to standard lead free IR reflow conditions shown in Table 6. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220C.

Table 6. Reflow Profile		
Parameter	Symbol	Value
PreHeat Time	ts	200 sec Max
Ramp Up	R_{UP}	3°C/sec Max
Time above 217°C	tL	150 sec Max
Time to Peak Temperature	tAMB-P	480 sec Max
Time at 260°C	tP	30 sec Max
Time at 240°C	tP2	60 sec Max
Ramp down	R_{DN}	6°C/sec Max

Solderprofile:



Maximum Ratings, Tape & Reel

Absolute Maximum Ratings and Handling Precautions

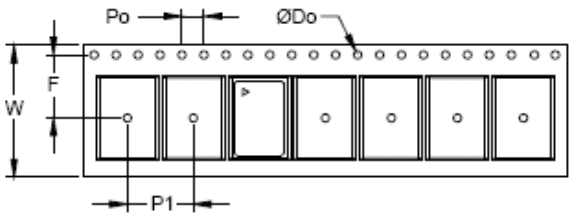
Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied or any other excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

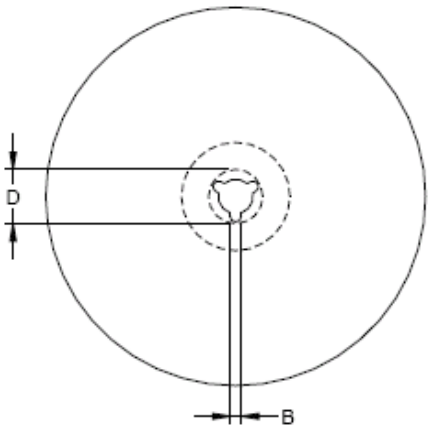
Although ESD protection circuitry has been designed into the VC-709, proper precautions should be taken when handling and mounting, VI employs a Human Body Model and Charged Device Model for ESD susceptibility testing and design evaluation.
ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM a standard resistance of 1.5kOhms and capacitance of 100pF is widely used and therefor can be used for comparison purposes.

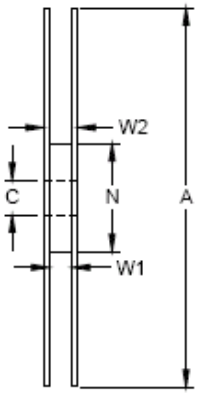
Table 7. Maximum Ratings		
Parameter		Unit
Storage Temperature	-55 to 125	°C
Junction Temperature	150	C
Supply Voltage	-0.5 to 5.0	V
Enable Disable Voltage	-0.5 to V_{DD}+0.5	V
ESD, Human Body Model	1500	V
ESD, Charged Device Model	1500	V

Table 8. Tape and Reel Information

Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
16	7.5	1.5	4	8	180	2	13	21	50	17	21	250







Ordering Information

VC-709- E C E - K A A N - xxxMxxxxxx

Product
XO

Package
5x7

Voltage Options
E: +3.3 Vdc ±5%
H: +2.5 Vdc ±5%

Output
H: HCSL
C: LVPECL
D: LVDS

Temp Range
W: -10/70°C
E: -40/85°C

Stability
F: ±25ppm
K: ±50ppm
S: ±100ppm

Enable/Disable Logic
A: Output is Enabled with a Logic High or open, Output is Disabled with a Logic Low

Enable/Disable Pin
A: Pin 1 (Pin 2 = No Connection)
B: Pin 2 (Pin 1 = No Connection)

Other (Future Use)
N: Standard

Frequency in MHz

Example: VC-709-ECE-KAAN-156M250000

±20ppm Options

VC-709-107-frequency= LVPECL, +3.3V, ±20ppm over -10/70°C, E/D on Pin1
VC-709-109-frequency= LVDS, +3.3V, ±20ppm over -10/70°C, E/D on Pin1
VC-709-110-frequency= LVPECL, +2.5V, ±20ppm over -10/70°C, E/D on Pin1
VC-709-111-frequency= LVDS, +2.5V, ±20ppm over -10/70°C, E/D on Pin1
VC-709-119-frequency= LVPECL, +3.3V, ±20ppm over -40/85°C, E/D on Pin1
VC-709-120-frequency= LVPECL, +2.5V, ±20ppm over -40/85°C, E/D on Pin1
VC-709-121-frequency= LVDS, +3.3V, ±20ppm over -40/85°C, E/D on Pin1
VC-709-122-frequency= LVDS, +2.5V, ±20ppm over -40/85°C, E/D on Pin1

PCI Express Ordering Information

VC-709- PCIE2 - 100M000000*

Product
XO

Package
5x7

Frequency in MHz

Options
Supply =2.25-3.63V
Output = HCSL
Stability = ±50 ppm over -40/85°C
Enable/Disable on Pin 1

*Parts compliant to PCIe Generation 1 and 2 Specifications

* Add **_SNPBDIP** for tin lead solder dip
Example: VC-709-ECE-KAAN-156M250000_SNPBDIP

Revision History

Revision Date	Approved	Description
Sep 05, 2014	VN	VC-709 Product Initial Release.
Dec 12, 2014	VN	Added min and max values for LVDS output amplitude.
Apr 27, 2016	VN	Updated LVDS 100MHz noise information and added maximum jitter numbers.
Aug 10, 2018	FB	Update logo and contact information, add SNPBDIP ordering option, marking detials, thetaJC and wieght

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