BLC9H10XS-500A

Power LDMOS transistor

Rev. 2 — 13 July 2018

AMPLEON

Product data sheet

1. Product profile

1.1 General description

500 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 617 MHz to 960 MHz.

Table 1. Typical performance 650 MHz

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit. V_{DS} = 48 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 1.0 V; unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	617 to 746	48	49.3	19.3	53	–29 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

Table 2. Typical performance 800 MHz

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty test circuit. V_{DS} = 48 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.5 V; unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	791 to 821	48	49.3	18.6	52	–36 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

Table 3. Typical performance 960 MHz

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit. V_{DS} = 48 V; I_{Dq} = 280 mA (main); $V_{GS(amp)peak}$ = 0.4 V; unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	925 to 960	48	49.3	17.4	51	–31.1 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability

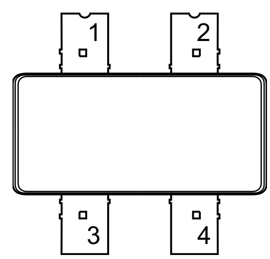
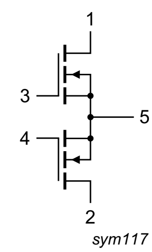
- Internal integrated wideband input matching for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 617 MHz to 960 MHz frequency range

2. Pinning information

Table 4. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 5. Ordering information

Type number	Package		
	Name	Description	Version
BLC9H10XS-500A	-	air cavity plastic earless flanged package; 4 leads	SOT1273-1

4. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	105	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–6	+11	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	operating [1]	–40	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 48 V; I_{Dq} = 500 mA; $V_{GS(peak)}$ = 0.65 V; T_{case} = 80 °C		
		P_L = 81 W	0.346	K/W
		P_L = 100 W	0.327	K/W

6. Characteristics

Table 8. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.5 mA	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 150 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 48 V; I_D = 500 mA	1.57	2.07	2.57	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	24.3	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 7.5 A	-	10	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 5.25 A	-	154	203	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.2 mA	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 220 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 48 V; I_D = 800 mA	1.57	2.07	2.57	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	34.4	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 11 A	-	14.57	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 7.7 A	-	113	142	mΩ

Table 9. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 - 64 DPCH; f_1 = 793.5 MHz; f_2 = 818.5 MHz; RF performance at V_{DS} = 48 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.5 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 791 MHz to 821 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 81 W	17.8	18.9	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 81 W	-	−21	−15	dB
η_D	drain efficiency	$P_{L(AV)}$ = 81 W	48	52	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 81 W	-	−35	−28	dBc

Table 10. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 - 64 DPCH; f = 818.5 MHz; RF performance at V_{DS} = 48 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.5 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 791 MHz to 821 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = 115 W	6.7	7.3	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)}$ = 115W	527	573	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC9H10XS-500A is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 52 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.5 V; f = 806 MHz; P_L = 200 W (5 dB OBO); pulsed CW (t_p = 100 μs; δ = 10 %).

7.2 Impedance information

Table 11. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 600 mA (main); V_{DS} = 50 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	P_L [2] (W)	η_D [2] (%)	G_p [2] (dB)
Maximum power load					
600	5.8 – j1.8	2.6 + j0.4	360.7	69.0	19.0
698	3.7 – j2.3	2.0 + j0.2	347.3	65.0	19.4
746	3.4 – j3.2	2.0 + j0.2	361.1	69.0	19.6
769	3.4 – j3.7	1.9 + j0.3	358.3	70.5	19.5
800	3.5 – j4.3	2.0 – j0.3	352.1	64.0	19.1
820	3.5 – j4.3	2.0 – j0.1	349.2	66.0	19.0
869	3.6 – j4.7	2.0 + j0.0	347.3	67.0	18.8
880	4.4 – j5.8	2.0 + j0.0	335.5	69.5	19.1
925	5.2 – j6.5	2.0 – j0.7	329.7	60.9	17.9
942	6.1 – j6.9	2.0 – j0.7	337.1	62.8	17.9
960	6.7 – j6.9	2.0 – j0.7	338.1	63.4	17.8
Maximum drain efficiency load					
600	5.5 – j1.4	2.3 + j2.7	224.5	80.6	21.6
698	3.6 – j2.2	2.2 + j1.6	270.9	76.6	21.4
746	3.2 – j3.1	1.8 + j2.2	202.8	78.9	22.4
769	3.3 – j3.5	2.1 + j1.6	249.6	77.9	21.6
800	3.3 – j4.0	1.6 + j1.4	240.2	77.3	22.0
820	3.2 – j4.1	1.4 + j1.9	182.7	78.4	22.5
869	3.5 – j4.5	1.7 + j1.4	246.3	77.6	21.1
880	4.2 – j5.6	1.7 + j1.4	213.8	76.3	21.4
925	4.9 – j6.1	1.2 + j1.2	186.7	74.6	21.4
942	5.7 – j6.4	1.2 + j1.2	177.3	77.4	21.8
960	6.5 – j6.6	1.4 + j0.7	247.8	77.2	20.5

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 12. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 880 mA (peak); V_{DS} = 50 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
600	3.7 – j1.9	1.4 + j0.0	512.9	64.7	17.6
698	2.8 – j2.3	1.4 – j0.5	497.5	64.5	18.3
720	2.7 – j2.6	1.4 – j0.5	442.3	61.5	18.3
769	2.8 – j3.1	1.4 – j0.5	478.2	63.9	17.9
800	2.9 – j3.4	1.4 – j0.5	482.6	65.6	18.6
820	3.1 – j3.6	1.4 – j0.6	486.4	66.7	18.3
869	3.6 – j4.0	1.4 – j0.6	469.9	68.0	18.5
880	3.8 – j4.0	1.4 – j0.6	464.2	67.9	18.5
925	4.6 – j4.0	1.2 – j1.2	450.7	57.4	17.2
942	4.8 – j3.8	1.2 – j1.2	458.8	59.2	17.3
960	5.1 – j3.5	1.1 – j1.2	461.6	61.1	17.4
Maximum drain efficiency load					
600	3.6 – j1.8	2.0 + j0.8	439.2	77.5	19.4
698	2.6 – j2.3	2.1 + j0.9	343.6	75.5	20.9
720	2.6 – j2.5	1.4 + j0.7	304.0	73.2	20.8
769	2.7 – j3.0	1.4 + j0.7	326.5	75.2	20.5
800	2.7 – j3.2	1.4 + j0.7	307.0	74.9	21.6
820	2.9 – j3.4	1.4 + j0.7	303.3	74.9	21.0
869	3.3 – j3.6	0.9 + j0.5	233.1	74.1	21.5
880	3.6 – j3.9	1.4 + j0.0	373.8	72.8	20.0
925	4.2 – j3.6	0.9 + j0.0	306.8	74.0	20.7
942	4.4 – j3.4	0.9 + j0.0	291.4	74.7	20.9
960	4.4 – j3.1	0.9 + j0.0	268.5	74.1	21.2

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

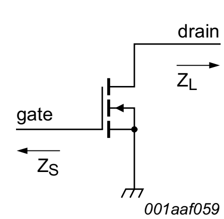


Fig 1. Definition of transistor impedance

7.3 Recommended impedances for Doherty design

Table 13. Typical impedance of main at 1 : 1 load

Measured load-pull data of main device; I_{Dq} = 600 mA (main); V_{DS} = 50 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	$P_{L(3dB)}$ (dBm)	η_D [2] (%)	G_p [2] (dB)
600	5.8 – j1.8	2.6 + j0.8	55.5	38	22.4
698	3.7 – j2.3	2.2 + j0.8	55.3	37.8	23.1
746	3.4 – j3.2	2.1 + j0.8	55.3	39.4	23.5
769	3.4 – j3.7	2.1 + j0.8	55.2	40.2	23.3
800	3.5 – j4.3	2.1 + j0.5	55.2	39.5	23.6
820	3.5 – j4.3	2.1 + j0.5	55.2	37.2	22.6
869	3.6 – j4.7	1.6 + j0.4	55.1	39.6	22.8
880	4.4 – j5.8	1.6 + j0.4	55.0	39.4	22.9
925	5.2 – j6.5	1.7 + j0.2	55.0	38.5	22.6
942	6.1 – j6.9	1.7 + j0.2	55.1	38.7	22.8
960	6.7 – j6.9	1.7 + j0.1	55.2	38.3	22.5

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 81 W.

Table 14. Typical impedance of main device at 1 : 2.5 load

Measured load-pull data of main device; I_{Dq} = 600 mA (main); V_{DS} = 50 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	$P_{L(3dB)}$ (dBm)	η_D [2] (%)	G_p [2] (dB)
600	5.5 – j1.4	2.5 + j3.4	52.4	59.1	25.1
698	3.6 – j2.2	2.1 + j3.0	52.1	59.2	25.9
746	3.2 – j3.1	1.9 + j2.8	52.0	60.4	25.8
769	3.3 – j3.5	1.9 + j2.8	51.9	60.6	25.6
800	3.3 – j4.0	1.9 + j2.4	52.2	59.1	25.5
820	3.2 – j4.1	1.5 + j2.1	52.2	54.8	25.2
869	3.5 – j4.5	1.2 + j1.7	52.2	57.6	25.2
880	4.2 – j5.6	1.2 + j1.7	52.1	57.4	25.3
925	4.9 – j5.9	1.3 + j1.5	52.2	56.2	25.2
942	5.7 – j6.4	1.1 + j1.4	52.1	58.4	25.4
960	6.5 – j6.6	1.1 + j1.2	52.2	56.5	25.0

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 81 W.

Table 15. Typical impedance of peak device at 1 : 1 load

Measured load-pull data of peak device; I_{Dq} = 880 mA (peak); V_{DS} = 50 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	$P_{L(3dB)}$	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(dBm)	(%)	(dB)
600	3.67 – j1.8	1.9 + j0.5	57.1	35.8	22.9
698	2.77 – j2.5	1.4 + j0.2	56.7	32.7	22.8
720	2.78 – j3.1	1.4 + j0.2	56.8	32.5	22.4
746	2.83 – j3.3	1.4 + j0.2	56.7	31.4	22.2
769	2.9 – j3.5	1.4 + j0.2	56.8	33.4	22.3
800	3.03 – j3.7	1.3 + j0.0	56.6	32.4	22.8
820	3.23 – j3.7	1.2 + j0.0	56.5	32.7	22.9
869	3.84 – j4.0	1.2 – j0.2	56.4	32.8	22.8
880	3.99 – j4.0	1.2 – j0.2	56.3	33.2	22.9
925	4.67 – j3.6	1.2 – j0.4	56.3	32.5	22.5
942	4.89 – j3.4	1.1 – j0.5	56.4	32.1	22.3
960	5.18 – j3.0	1.0 – j0.6	56.3	31.6	22.4

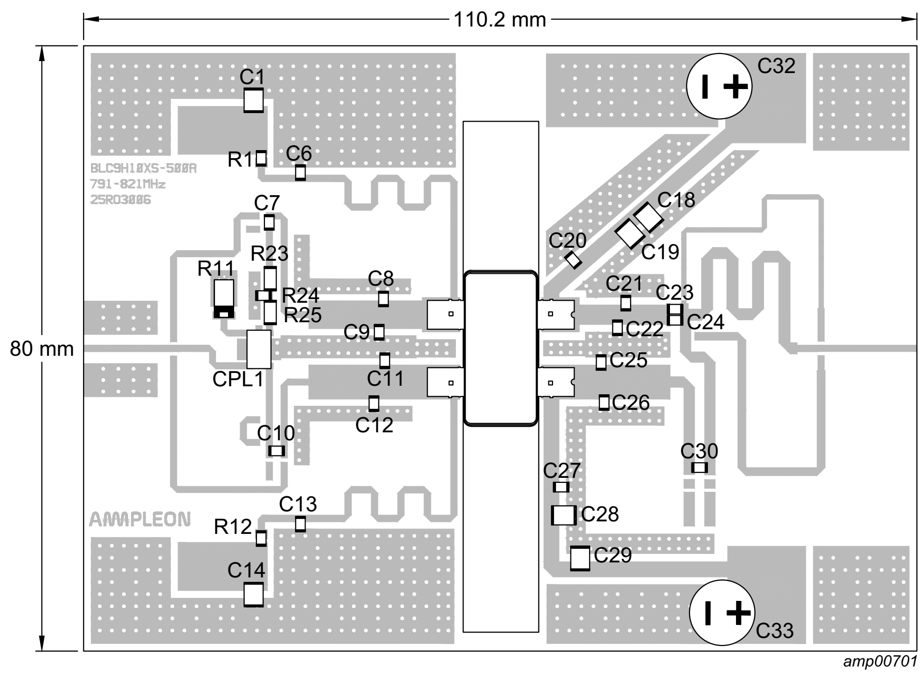
[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 81 W.

Table 16. Off-state impedances of peak device

f	Z_{off}
(MHz)	(Ω)
600	0.13 – j5.56
698	0.14 – j4.29
720	0.14 – j4.03
769	0.13 – j3.56
800	0.12 – j3.28
820	0.11 – j3.09
869	0.11 – j2.69
880	0.11 – j2.63
894	0.11 – j2.53
925	0.10 – j2.30
942	0.10 – j2.21
960	0.10 – j2.09

7.4 Test circuit



Printed-Circuit Board (PCB): RO3006: ε_r = 6.15; thickness = 0.635 mm; thickness copper plating = 35 μm. See Table 17 for a list of components.

Fig 2. Component layout

Table 17. List of components

See Figure 2 for component layout.

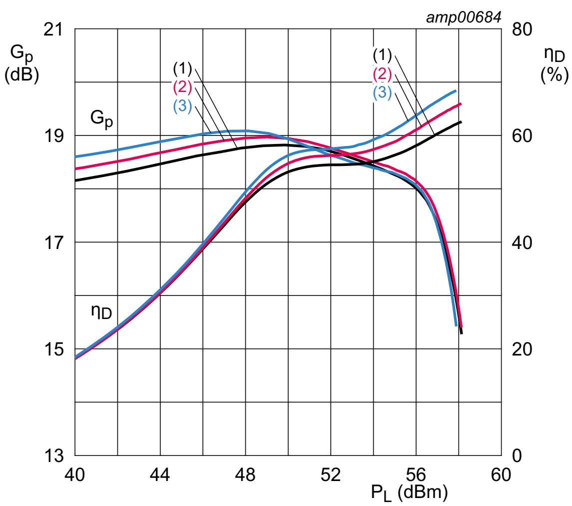
Component	Description	Value	Remarks
C1,C14	multilayer ceramic chip capacitor	4.7 μF, 50 V	Murata: SMD 1210, GRM32ER71H475KA88L
C6, C7, C10, C13, C27,C30	multilayer ceramic chip capacitor	68 pF	Murata: Hi-Q SMD 0805
C8, C9	multilayer ceramic chip capacitor	3.9 pF	Murata: Hi-Q SMD 0805
C11, C12	multilayer ceramic chip capacitor	5.6 pF	Murata: Hi-Q SMD 0805
C18, C19, C28, C29	multilayer ceramic chip capacitor	4.7 μF, 100 V	Murata: SMD 1210, GRM42-256X7S475K100H530
C20	multilayer ceramic chip capacitor	39 pF	Murata: Hi-Q SMD 0805
C21, C22	multilayer ceramic chip capacitor	8.2 pF	Murata: Hi-Q SMD 0805
C23, C24	multilayer ceramic chip capacitor	10 pF	Murata: Hi-Q SMD 0805
C25	multilayer ceramic chip capacitor	12 pF	Murata: Hi-Q SMD 0805
C26	multilayer ceramic chip capacitor	10 pF	Murata: Hi-Q SMD 0805
C32, C33	electrolytic capacitor	470 μF, 63 V	
R1, R12	resistor	4.7 Ω, 1 %	SMD 0805
R11	surface mount termination	50 Ω, 16 W	Anaren: C16A50Z4

Table 17. List of components *...continued*
See Figure 2 for component layout.

Component	Description	Value	Remarks
R23, R25	resistor	5.1 Ω, 1 %	SMD 1206
R24	resistor	240 Ω, 1 %	SMD 0805
CPL1	hybrid coupler	2 dB; 90°	Anaren: Xinger III, X3C07F1-02S

7.5 Graphical data

7.5.1 Pulsed CW



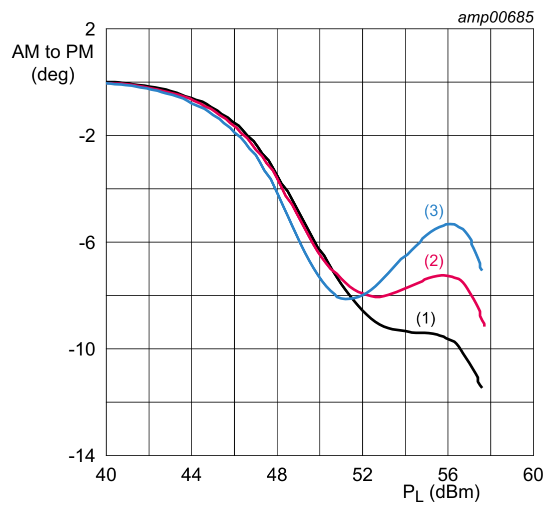
V_{DS} = 48 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.5 V;
t_p = 100 μs; δ = 10 %.

(1) f = 791 MHz

(2) f = 806 MHz

(3) f = 821 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 48 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.5 V;
t_p = 100 μs; δ = 10 %.

(1) f = 791 MHz

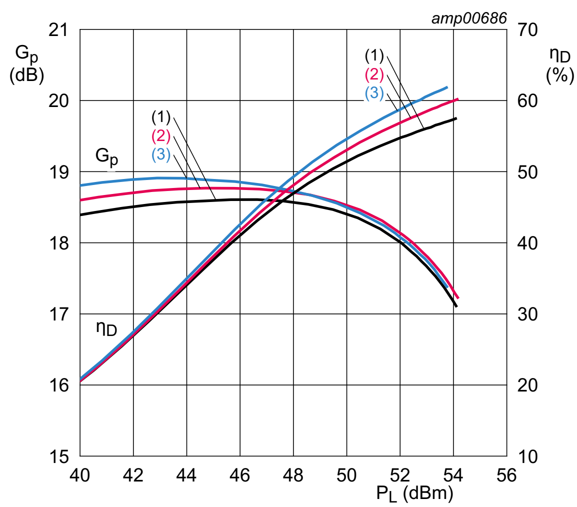
(2) f = 806 MHz

(3) f = 821 MHz

Fig 4. Normalized AM to PM as a function of output power; typical values

7.5.2 1-Carrier W-CDMA

PAR = 9.6 dB per carrier at 0.01 % probability on CCDF; 3GPP test model 1 with 64 DPCH (100 % clipping).



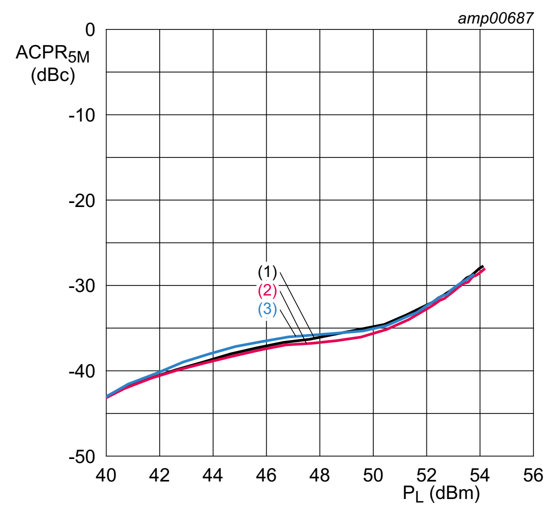
V_{DS} = 48 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 791 MHz

(2) f = 806 MHz

(3) f = 821 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



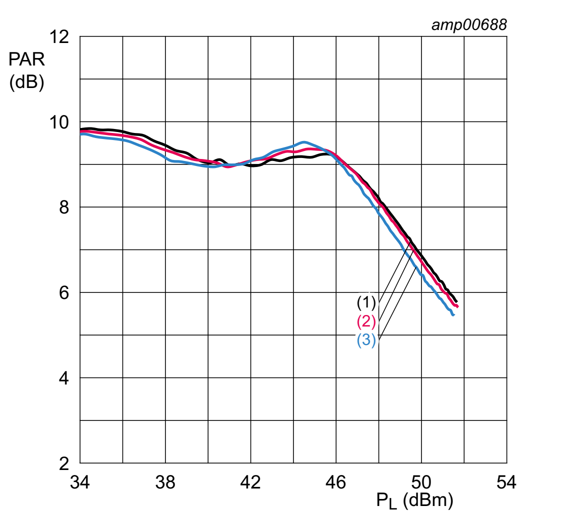
V_{DS} = 48 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 791 MHz

(2) f = 806 MHz

(3) f = 821 MHz

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



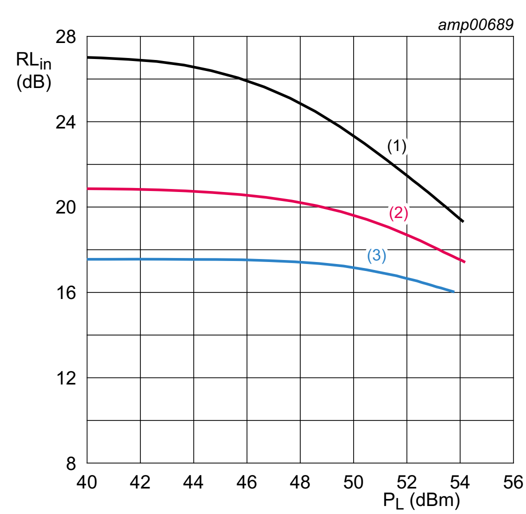
V_{DS} = 48 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 791 MHz

(2) f = 806 MHz

(3) f = 821 MHz

Fig 7. Peak-to-average power ratio as a function of output power; typical values



V_{DS} = 48 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.5 V.

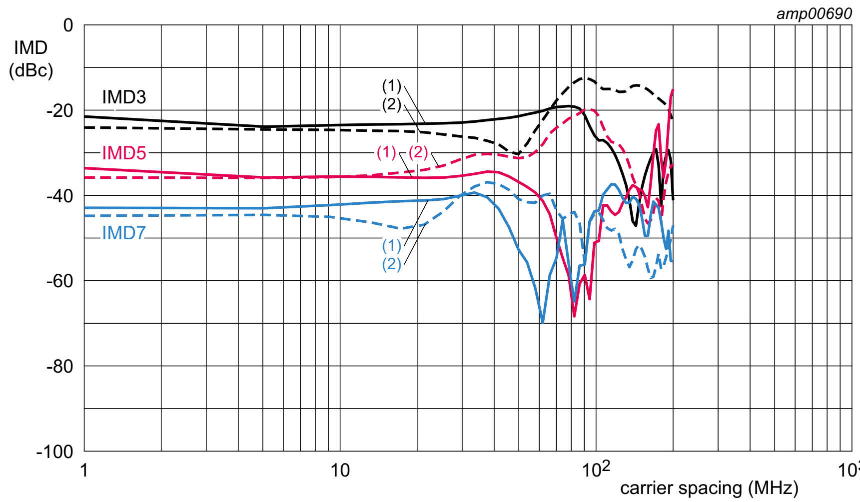
(1) f = 791 MHz

(2) f = 806 MHz

(3) f = 821 MHz

Fig 8. Input return loss as a function of output power; typical values

7.5.3 2-Tone VBW



V_{DS} = 48 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.5 V; f_c = 806 MHz.

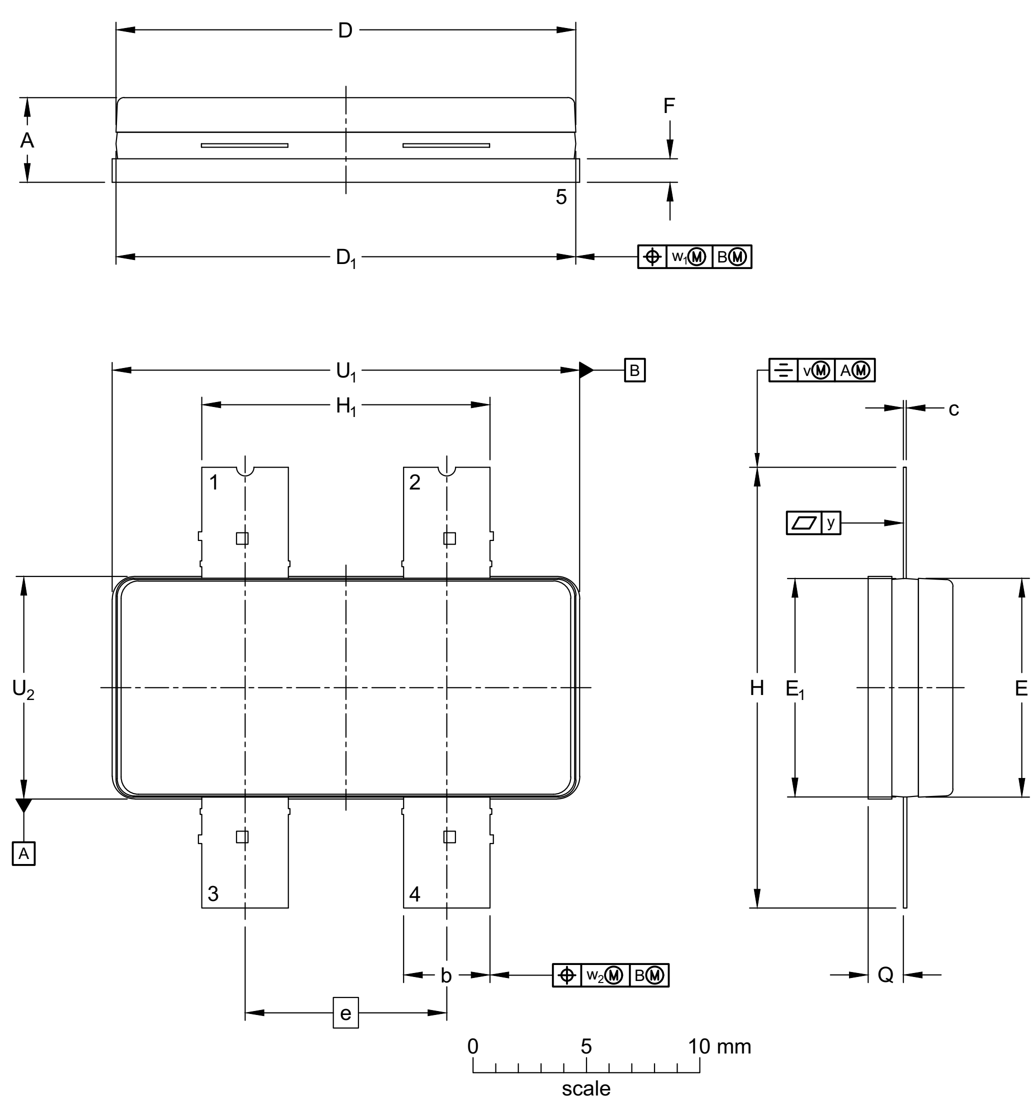
(1) IMD low

(2) IMD high

Fig 9. VBW capability in Doherty demo board

8. Package outline

Air cavity plastic earless flanged package; 4 leads — SOT1273-1



Dimensions

Unit		A	b	c	D	D_1	E	E_1	e	F	H	H_1	$Q^{(1)}$	U_1	U_2	v	w_1	w_2	y
mm	max	4.01	3.91	0.18	20.42	20.37	9.80	9.75		1.14	19.53	12.83	1.68	20.70	9.91	0.50	0.50	0.50	0.10
	nom								8.89										
	min	3.40	3.71	0.13	20.12	20.17	9.50	9.55		0.94	19.33	12.57	1.45	20.50	9.70				

Note:
1. Dimension Q is measured at 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1273-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1273-1						17-01-12

Fig 10. Package outline SOT1273-1

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 18. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of ≥ 1000 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 19. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
OBO	Output Back Off
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9H10XS-500A v.2	20180713	Product data sheet	-	BLC9H10XS-500A v.1
Modifications	• Table 9 on page 4: changed description • Table 10 on page 4: changed description • Section 7.3 on page 7: corrected heading of fourth column			
BLC9H10XS-500A v.1	20180702	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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For more information, please visit: **http://www.ampleon.com**

For sales office addresses, please visit: **http://www.ampleon.com/sales**

14. Contents

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