Data Sheet | December 1998 | File Number 4106.2

Triple 8-Bit, 50 MSPS, Video A/D Converter with Clamp Function

The HI2303 is a highly integrated 8-bit, 3-channel analog-to-digital converter that is designed for component (like RGB) digitizing applications. The internal DC Restore (video clamp) function and voltage reference simplifies system design and saves board space. The HI2303 can digitize RGB, YUV, YIQ and any other analog component color signals used in video systems. The variety of sub-sampling modes is compatible with RGB, YUV and YIQ color systems where 4:4:4, 4:2:2 and 4:1:1 data reduction is needed. The 2-step architecture boasts, low power operation, and excellent video performance.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI2303JCQ	-40 to 85	80 Ld MQFP	Q80.14x20-S
HI2303EVAL	25	Evaluation Kit	

Features

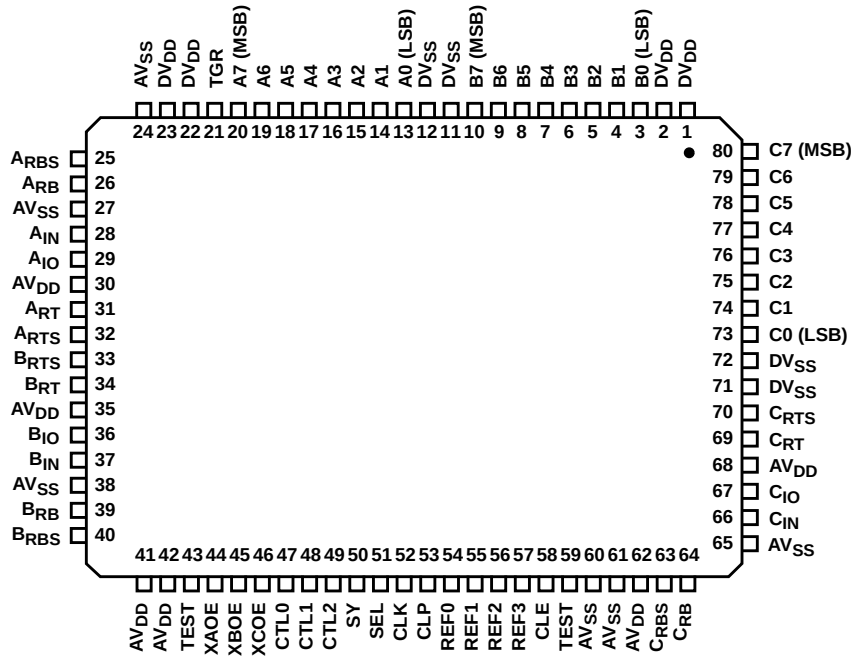
- Resolution 8-Bit 1/2 LSB (DL)
- Low Power Consumption (at 50 MSPS Typ) (Reference Current Excluded) 500mW
- Synchronizing Digital Clamp Function
- Clamp ON/OFF Function
- Reference Voltage Self-Bias Circuit
- Input CMOS/TTL Compatible
- Three-State TTL Compatible Output
- Single 5V Power Supply or Dual 5V or 3.3V Power Supplies
- Low Input Capacitance. 15pF
- Different Digital Output Multiplex Format
  - 4:4:4
  - 4:2:2
  - 4:1:1
- Direct Replacement for Sony CXD2303

Applications

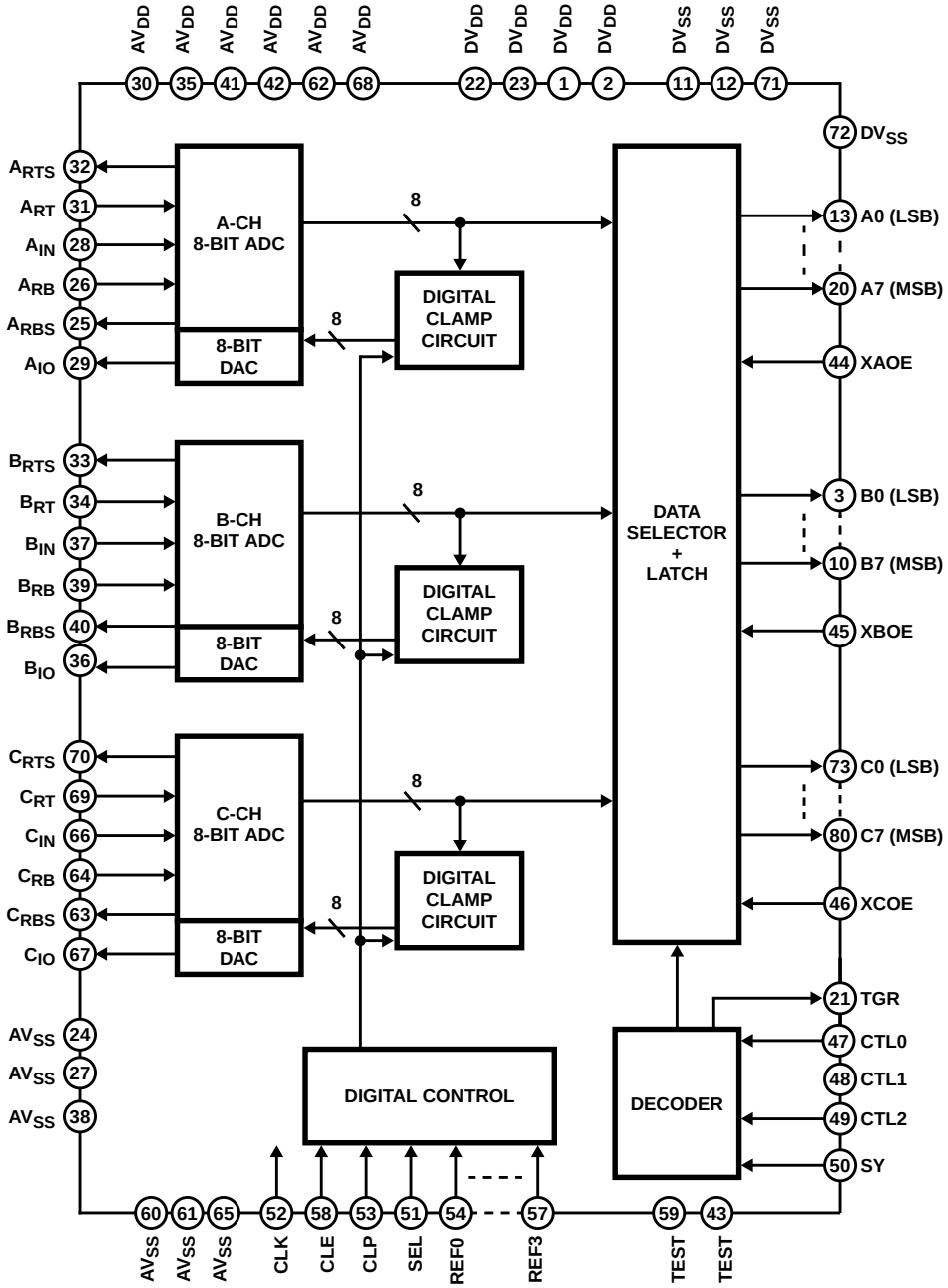
- Video Digitizing (Composite and Y-C)
- LCD Projectors
- LCD Panels
- RGB Graphics Processing

Pinout

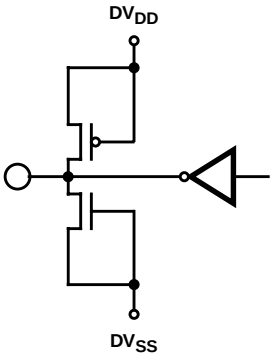
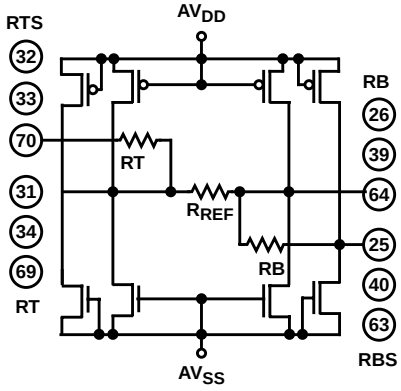
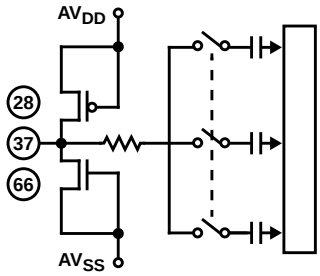
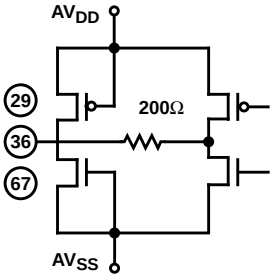
HI2303 (MQFP)
TOP VIEW



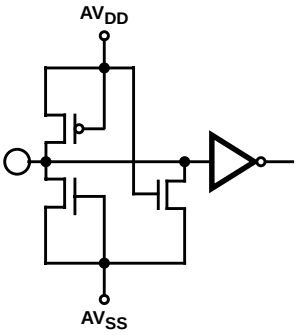
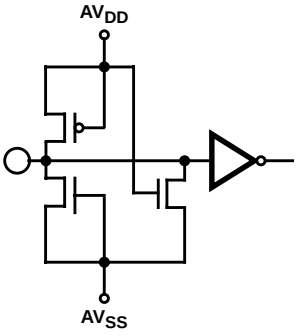
Functional Block Diagram



Pin Description

PIN NO.	SYMBOL		EQUIVALENT CIRCUIT	DESCRIPTION
1, 2, 22, 23	DV_{DD}	-		Digital Power Supply. +5V or +3.3V.
13 to 20 3 to 10 73 to 80	A0 to A7 B0 to B7 C0 to C7	O		Digital output. A0 (LSB) to A7 (MSB) B0 (LSB) to B7 (MSB) C0 (LSB) to C7 (MSB).
21	TGR	O		Trigger Output
11, 12, 71, 72	DV_{SS}	-		Digital Ground.
24, 27, 38, 60, 61, 65	AV_{SS}	-		Analog Ground.
25 40 63	ARBS BRBS CRBS	-		Shorting the RBS pins to AVSS generates voltage of approximately 0.6V at the ARB, BRB and CRB pins.
26 39 64	ARB BRB CRB	-		Reference Voltage (Bottom).
31 34 69	ART BRT CRT	-		Reference Voltage (Top).
32 33 70	ARTS BRTS CRTS	-		Shorting the RTS pins to AV_{DD} generates voltage of about 2.5V at the ART, BRT and CRT pins.
28 37 66	AIN BIN CIN	I		Analog Input.
29 36 67	AIO BIO CIO	O		Analog Output. These pins are the D/A converter outputs which comprise the digital clamp circuit.

Pin Description (Continued)

PIN NO.	SYMBOL		EQUIVALENT CIRCUIT	DESCRIPTION
30, 35, 41, 42, 62, 68	AV_{DD}			Analog +5V Power Supply.
43 59	TEST	I		Normally open. Pull-down resistors are incorporated.
44 45 46	XAOE XBOE XCOE	I		Output Enable Input. When these pins are Low, data is output from the digital output pins. When these pins are High, the digital output pins are High impedance. The A, B and C Channels can be controlled separately. Also, these pins are not synchronized with the clock signal. Pull-down resistors are incorporated.
47 48 49	CTL0 CTL1 CLT2	I		Determines the digital output mode. See the Mode tables and Timing Charts. Pull-down resistors are incorporated.
50	SY	I		Controls the digital output mode switching timing. The mode is switched by detecting the transition point where this pin changes from Low to High. See the Mode Tables and Timing Charts for details. A pull-down resister is incorporated.
51	SEL	I		Controls the CLP signal polarity. When this pin is Low, CLP is High active. When this pin is High, CLP is Low active. This pin has a built-in pull-down resistor.
52	CLK	I		Clock Input. A pull-down resistor is incorporated.
53	CLP	I		Clamp Pulse Input. The polarity can be set to either High or Low by setting SEL. This pin has a built-in pull-down resistor.
54 55 56 57	REF0 REF1 REF2 REF3	I		Determines the clamp circuit reference data. See the mode tables for the set data. These pins are not synchronized with the clock input signal. Pull-down resistors are incorporated.
58	CLE	I		Clamp Enable. When this pin is Low the clamp circuit does not operate. When this pin is High, the clamp circuit operates. A pull-down resistor is incorporated.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (AV_{DD}, DV_{DD}) 7V
Input Voltage (V_{IN}, All Pins) . . . . . V_{DD} +0.5V to V_{SS} -0.5V
Output Voltage (V_D, Digital) . . . . . V_{DD} +0.5V to V_{SS} -0.5V

Operating Conditions

Supply Voltage:
AV_{DD}, AV_{SS} . . . . . 4.75V to 5.25V
DV_{DD}, DV_{SS} . . . . . 3.0V to 5.5V
$|DV_{SS}, AV_{SS}|$ . . . . . 0mV to 100mV
Reference Input Voltage:
V_{ARB}, V_{BRB}, V_{CRB} . . . . . 0V or More
V_{ART}, V_{BRT}, V_{CRT} . . . . . 2.7V or Less
Analog Input:
A_{IN}, B_{IN}, C_{IN} . . . . . $1.7V_{P-P}$ or More
Clock Pulse Width:
t_{PW1}, t_{PW0} . . . . . 9ns (Min) to 1.1ms (Max)
Ambient Temperature (TOPR) . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
MQFP Package	88

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range (T_{STG}) . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications f_C = 50 MSPS, AV_{DD} = 5V, DV_{DD} = 3.0V to 5.0V, V_{RB} = 0.5V, V_{RT} = 2.5V, $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG CHARACTERISTICS DV_{DD} = 3V to 5.5V							
Conversion Rate	f_C	AV_{DD} = 4.75V to 5.25V, $T_A = -20^oC$ to 75^oC, V_{IN} = 0.5V to 2.5V, f_{IN} = 1kHz Triangular Wave		0.5	-	50	MSPS
Analog Input Band (-1dB)	BW	Envelope	-1dB	-	60	-	MHz
		R_{IN} = 33Ω	-3dB	-	100	-	MHz
Differential Non-Linearity Error	E_D	End Point		-	±0.3	±0.5	LSB
Integral Non-Linearity Error	E_L			-	±0.7	±1.5	LSB
Offset Voltage (Note 2)	E_{OT}	Potential Difference to A_{RT}, B_{RT}, C_{RT}		-50	-	-10	mV
	E_{OB}	Potential Difference to A_{RB}, B_{RB}, C_{RB}		0	-	40	mV
Differential Gain Error	DG	NTSC 40 IRE Mod Ramp, f_C = 14.3 MSPS		-	3	-	%
Differential Phase Error	DP			-	1.5	-	Deg
Cross Talk	CT	f_{IN} = 1MHz Sinewave		-	52	-	dB
Clamp Offset Voltage	E_{OC}	V_{IN} = DC, C_{IN} = 10µF, t_{PCW} = 2.75µs, f_{CLK} = 14.3MHz, f_{CLP} = 15.75kHz	Ref Data = 00010000	-	-	±1	LSB
			Ref Data = 10000000	-	-	±1	LSB
Signal To Noise Ratio	SNR	f_{IN} = 150kHz		-	43	-	dB
		f_{IN} = 500kHz		-	42	-	dB
		f_{IN} = 1MHz		-	42	-	dB
		f_{IN} = 3MHz		-	41	-	dB
		f_{IN} = 10MHz		-	38	-	dB
		f_{IN} = 20MHz		-	35	-	dB

Electrical Specifications

f_C = 50 MSPS, AV_{DD} = 5V, DV_{DD} = 3.0V to 5.0V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Spurious Free Dynamic Range		SFDR	f_{IN} = 150kHz		-	59	-	dB
			f_{IN} = 500kHz		-	59	-	dB
			f_{IN} = 1MHz		-	55	-	dB
			f_{IN} = 3MHz		-	49	-	dB
			f_{IN} = 10MHz		-	44	-	dB
			f_{IN} = 20MHz		-	41	-	dB
DC CHARACTERISTICS DV_{DD} = 5V or 3.3V								
Supply Current	Both	$I_{AD} + I_{DD}$	NTSC Ramp Wave Input CLE = High f_{CLP} = 15.75kHz	DV_{DD} = 5V	-	80	100	mA
	Analog	I_{AD}		D_{VDD} = 3.3V	-	70	90	mA
	Digital	I_{DD}			-	5	10	mA
	Both	$I_{AD} + I_{DD}$	NTSC Ramp Wave Input CLE = Low	D_{VDD} = 5V	-	70	90	mA
	Analog	I_{AD}		D_{VDD} = 3.3V	-	60	80	mA
	Digital	I_{DD}			-	5	10	mA
Reference Current		I_{REF}	For Every Channel		4.1	5.4	7.7	mA
Reference Resistance (V_{RT} to V_{RB})		R_{REF}	For Every Channel		260	370	480	Ω
Self Bias		V_{RB}	Short AV_{SS} and A_{RBS}, B_{RBS}, C_{RBS}		0.50	0.54	0.58	V
		$V_{RT} - V_{RB}$	Short AV_{DD} and A_{RTS}, B_{RTS}, C_{RTS}		1.8	1.92	2.04	V
Analog Input Resistance		R_{IN}	V_{IN}	f_{CLK} = 50MHz	-	13	-	kΩ
				f_{CLK} = 35MHz	-	16	-	kΩ
				f_{CLK} = 20MHz	-	30	-	kΩ
Input Capacitance		C_{A11}	A_{IN}, B_{IN}, C_{IN}, V_{IN} = 1.5V + 0.07V_{RMS}		-	15	-	pF
		C_{A12}	A_{RTS}, A_{RT}, A_{RB}, A_{RBS}, B_{RTS}, B_{RT}, B_{RB}, B_{RBS}, C_{RTS}, C_{RT}, C_{RB}, C_{RBS}		-	-	9	pF
		C_{DIN}	Digital Input Pin		-	-	9	pF
Output Capacitance		C_{AO}	A_{IO}, B_{IO}, C_{IO}		-	-	11	pF
		C_{DO}	Digital Output Pin		-	-	11	pF
Digital Input Voltage		V_{IH}	AV_{DD} = 4.75V to 5.25V, DV_{DD} = 3V to 5.5V		2.2	-	-	V
		V_{IL}			-	-	0.8	V
Digital Input Current		I_{IH}	V_I = 0V to AV_{DD}		-40	-	240	µA
		I_{IL}			-40	-	240	µA
Digital Output Current		I_{OH}	X_{OE} = 0V DV_{DD} = 5V	V_{OH} = DV_{DD} - 0.8V	-	-	-2	mA
		I_{OL}		V_{OL} = 0.4V	4	-	-	mA
		I_{OH}	X_{OE} = 0V DV_{DD} = 3.3V	V_{OH} = DV_{DD} - 0.8V	-	-	-1.2	mA
		I_{OL}		V_{OL} = 0.4V	2.4	-	-	mA
		I_{OZH}	X_{OE} = 3V DV_{DD} = 3V to 5.5V	V_{OH} = DV_{DD}	-40	-	40	mA
		I_{OZL}		V_{OL} = 0V	-40	-	40	mA

Electrical Specifications f_C = 50 MSPS, AV_{DD} = 5V, DV_{DD} = 3.0V to 5.0V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Digital Output Voltage	V_{OH}	X_{OE} = 0V, DV_{DD} = 5V	I_{OH} = -2mA	DV_{DD} -0.8	-	-	V
	V_{OL}		I_{OL} = 4mA	-	-	0.4	V
	V_{OH}	X_{OE} = 0V, DV_{DD} = 3.3V	I_{OH} = -1.2mA	DV_{DD} -0.8	-	-	V
	V_{OL}		I_{OL} = -2.4mA	-	-	0.4	V

NOTES:

2. The offset voltage E_{OB} is a potential difference between A_{RB}, B_{RB}, C_{RB} and a point of position where the voltage drops equivalent to $^1/_2$ LSB of the voltage when the output data changes from “00000000” to “00000001”. E_{OR} is a potential difference between A_{RT}, B_{RT}, C_{RT} and a potential of point where the voltage rises equivalent to $^1/_2$ LSB of the voltage when the output data changes from “11111111” to “11111110”.

3. Full scale input ratio = $\left| \frac{(2V + E_{OT} - E_{OB}) \text{ of each channel}}{\text{Average of } (2V + E_{OT} - E_{OB}) \text{ of each channel}} - 1 \right| x100(\%)$.

Timing f_C = 50 MSPS, AV_{DD} = 5V, DV_{DD} = 5V or 3.3V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output Data Delay	t_{PLH}	C_L = 15pF, XOE = 0V	DV_{DD} = 5V	4.5	8.5	11	ns
	t_{PHL}			4.5	7.4	11	ns
	t_{PLH}		DV_{DD} = 3.3V	3.8	10	13.8	ns
	t_{PHL}			3.8	6.7	13.8	ns
Three-State Output Enable Time	t_{PZH}	R_L = 1kΩ, CL = 15pF, XOE = 0V → 3V	DV_{DD} = 5V	4.2	7.1	11.3	ns
	t_{PZL}			4.2	8.0	11.3	ns
	t_{PZH}		DV_{DD} = 3.3V	3.5	8.4	12.8	ns
	t_{PZL}			3.5	7.2	12.8	ns
Three-State Output Disable Time	t_{PHZ}	R_L = 1kΩ, C_L = 15pF, XOE = 0V → 3V	DV_{DD} = 5V	3.6	6.8	9.5	ns
	t_{PLZ}			3.6	6.3	9.5	ns
	t_{PHZ}		DV_{DD} = 3.3V	2.9	6.8	10.5	ns
	t_{PLZ}			2.9	6.0	10.5	ns
Sampling Delay	t_{SD}			-	-3	-	ns
Set-up Time	t_S			3.5	-	-	ns
Hold Time	t_H			4.5	-	-	ns
Pulse Width	CLP			2.0	-	-	Cycles
Pulse Width	SY			1	-	-	Cycles

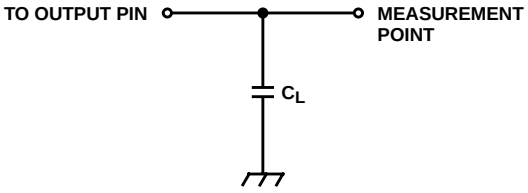
Digital Output

The following table shows the relationship between analog input voltage and digital output code.

TABLE 1. I/O CORRESPONDENCE

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE MSB LSB
V_{ART}, V_{BRT}, V_{CRT}	0	1 1 1 1 1 1 1 1
	127	1 0 0 0 0 0 0 0
	128	0 1 1 1 1 1 1 1
V_{ARB}, V_{BRB}, V_{CRB}	255	0 0 0 0 0 0 0 0

Test Circuits



NOTE: C_L includes capacitance of probes.

FIGURE 1. OUTPUT DATA DELAY MEASUREMENT CIRCUIT

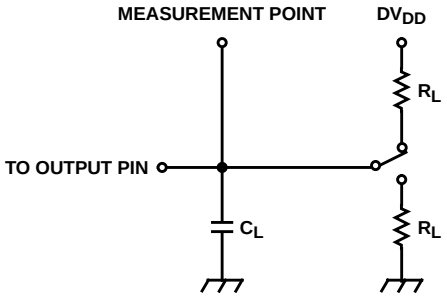


FIGURE 2. THREE-STATE MEASUREMENT CIRCUIT

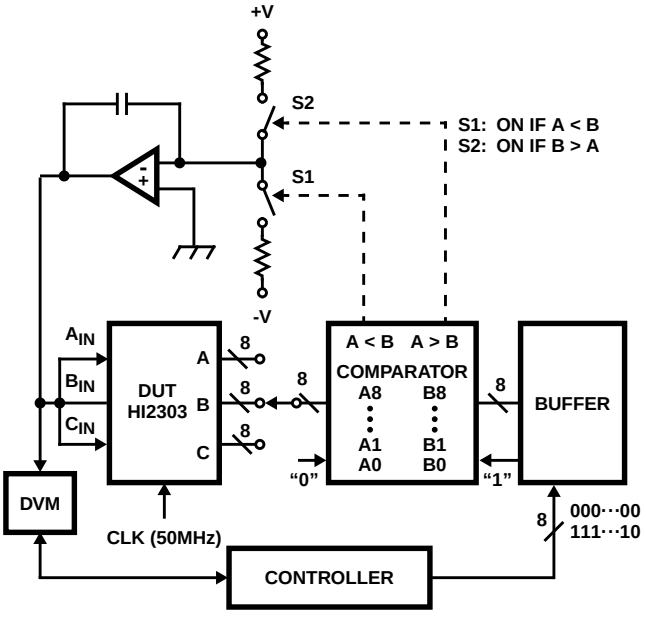


FIGURE 3. INTEGRAL NON-LINEARITY ERROR, DIFFERENTIAL NON-LINEARITY ERROR AND OFFSET VOLTAGE TEST CIRCUIT

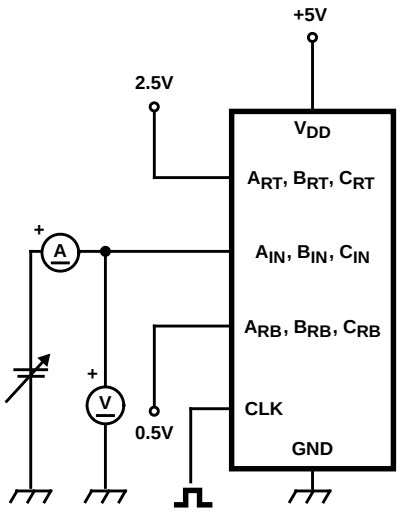


FIGURE 4. ANALOG INPUT RESISTANCE TEST CIRCUIT

Test Circuits (Continued)

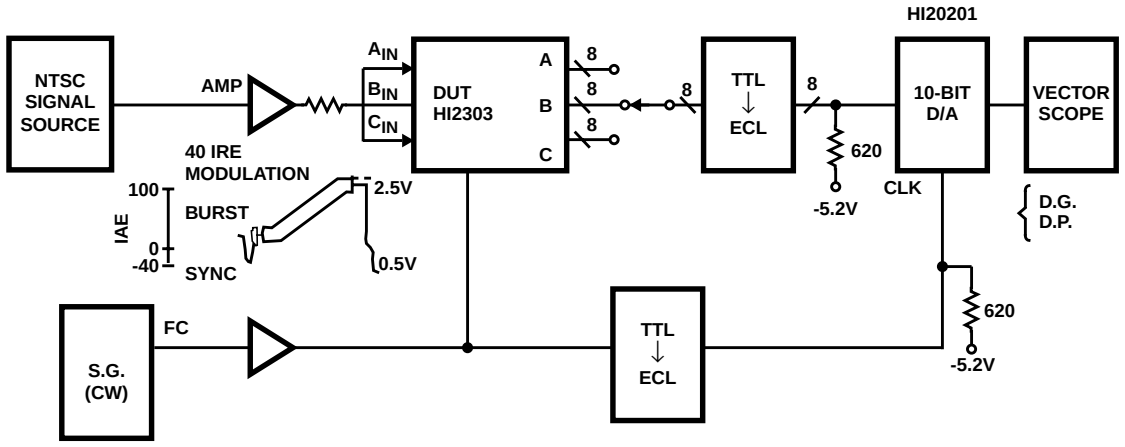


FIGURE 5. DIFFERENTIAL GAIN AND PHASE ERROR vs TEST CIRCUIT

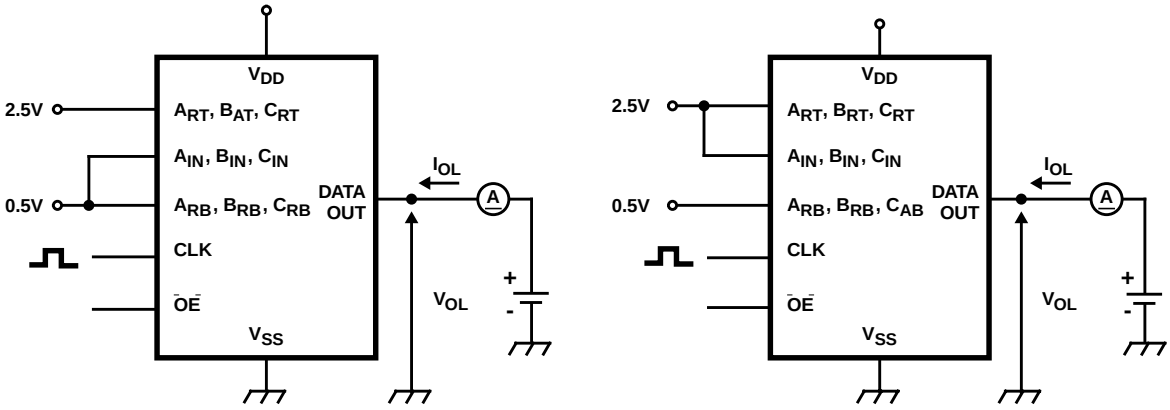


FIGURE 6. DIGITAL OUTPUT TEST CIRCUIT

Description of Operation

Digital Output Format

The HI2303 supports eight different output formats as detailed in Table 2. For clarity, these formats are labeled mode 0 to 7. The modes are selected via three control pins labeled CTL0, CTL1 and CTL2.

The converter has a latency of five clock cycles which places a constraint on the users ability to change the mode on the fly without corrupting the data within the converter. Please refer to Figure 10. The SY pin is used to control mode changes. This is achieved by using the SY as a reset/latch signal. The Mode is reset when the SY is asserted low. When SY transitions from low to high the control pins are latched internally and mode is changed per timing diagram latency.

TABLE 2. SETTING VALUES AND OUTPUT FORMATS

SETTING			OUTPUT	
CTL2	CTL1	CTLO	MODE	FORMAT
L	L	L	0	4:4:4
L	L	H	1	4:2:2 ($8F_S$)
L	H	L	2	4:2:2 (D2)
L	H	H	3	4:2:2 (Special)
H	L	L	4	4:1:1
H	L	H	5	4:1:1 (Special)
H	H	L	6	Simple Boundary, Scan 1
H	H	H	7	Simple Boundary, Scan 2

Timing Diagrams

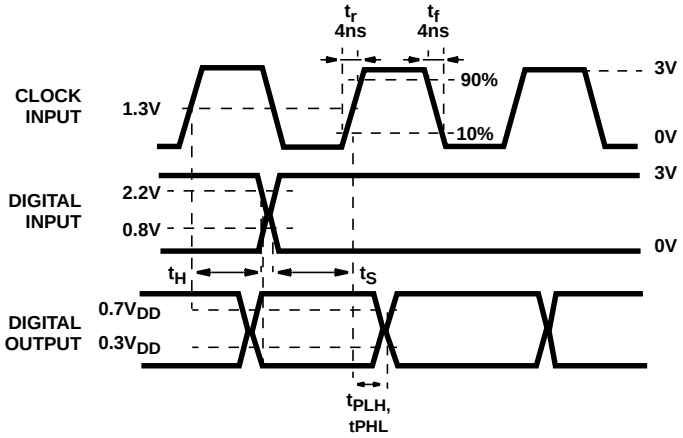


FIGURE 7.

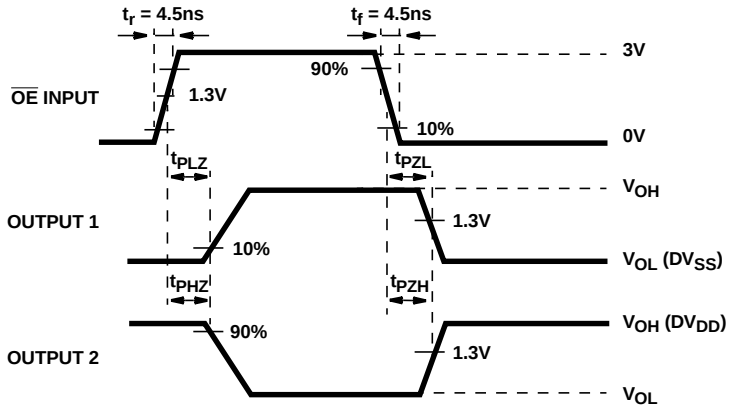


FIGURE 8. TIMING CHART I-2

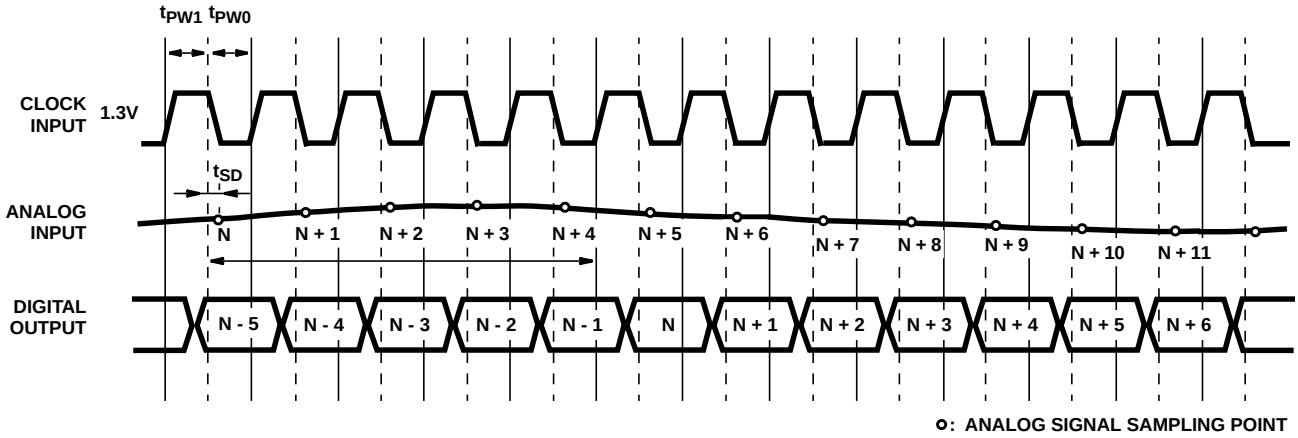


FIGURE 9.

Timing Diagrams (Continued)

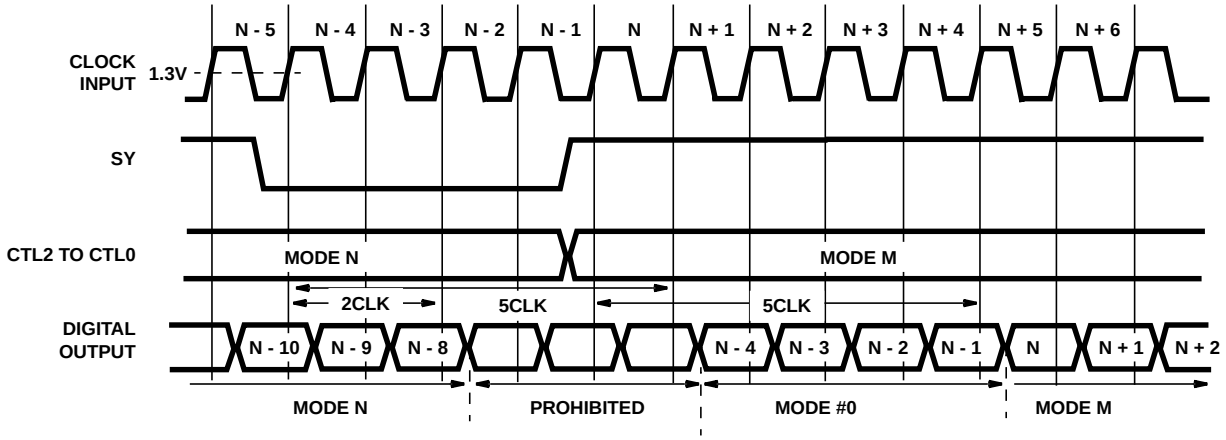
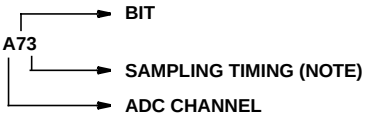


FIGURE 10.

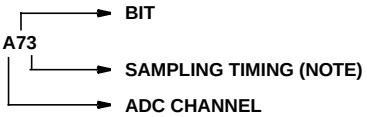
Mode #0 4:4:4



ADC CHANNEL	OUTPUT	DATA							
A	A7	A70	A71	A72	A73	A74	A75	A76	A77
	A6	A60	A61	A62	A63	A64	A65	A66	A67
	A5	A50	A51	A52	A53	A54	A55	A56	A57
	A4	A40	A41	A42	A43	A44	A45	A46	A47
	A3	A30	A31	A32	A33	A34	A35	A36	A37
	A2	A20	A21	A22	A23	A24	A25	A26	A27
	A1	A10	A11	A12	A13	A14	A15	A16	A17
	A0	A00	A01	A02	A03	A04	A05	A06	A07
B	B7	B70	B71	B72	B73	B74	B75	B76	B77
	B6	B60	B61	B62	B63	B64	B65	B66	B67
	B5	B50	B51	B52	B53	B54	B55	B56	B57
	B4	B40	B41	B42	B43	B44	B45	B46	B47
	B3	B30	B31	B32	B33	B34	B35	B36	B37
	B2	B20	B21	B22	B23	B24	B25	B26	B27
	B1	B10	B11	B12	B13	B14	B15	B16	B17
	B0	B00	B01	B02	B03	B04	B05	B06	B07
C	C7	C70	C71	C72	C73	C74	C75	C76	C77
	C6	C60	C61	C62	C63	C64	C65	C66	C67
	C5	C50	C51	C52	C53	C54	C55	C56	C57
	C4	C40	C41	C42	C43	C44	C45	C46	C47
	C3	C30	C31	C32	C33	C34	C35	C36	C37
	C2	C20	C21	C22	C23	C24	C25	C26	C27
	C1	C10	C11	C12	C13	C14	C15	C16	C17
	C0	C00	C01	C02	C03	C04	C05	C06	C07
TGR		Low	→						

NOTE: See Figure 9.

Mode #2 4:2:2 (D2)

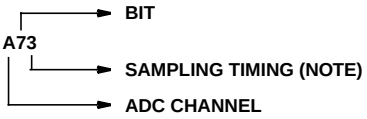


ADC CHANNEL	OUTPUT	DATA							
A	A7	A70	A71	A72	A73	A74	A75	A76	A77
	A6	A60	A61	A62	A63	A64	A65	A66	A67
	A5	A50	A51	A52	A53	A54	A55	A56	A57
	A4	A40	A41	A42	A43	A44	A45	A46	A47
	A3	A30	A31	A32	A33	A34	A35	A36	A37
	A2	A20	A21	A22	A23	A24	A25	A26	A27
	A1	A10	A11	A12	A13	A14	A15	A16	A17
	A0	A00	A01	A02	A03	A04	A05	A06	A07
B	B7	B70	C70	B72	C72	B74	C74	B76	C76
	B6	B60	C60	B62	C62	B64	C64	B66	C66
	B5	B50	C50	B52	C52	B54	C54	B56	C56
	B4	B40	C40	B42	C42	B44	C44	B46	C46
	B3	B30	C30	B32	C32	B34	C34	B36	C36
	B2	B20	C20	B22	C22	B24	C24	B26	C26
	B1	B10	C10	B12	C12	B14	C14	B16	C16
	B0	B00	C00	B02	C02	B04	C05	B06	C06
C	C7	HiZ	→						
	C6	HiZ	→						
	C5	HiZ	→						
	C4	HiZ	→						
	C3	HiZ	→						
	C2	HiZ	→						
	C1	HiZ	→						
	C0	HiZ	→						
TGR		HIGH	LOW	HIGH	LOW	HIGH	LOW	HIGH	LOW

HiZ: High Impedance

NOTE: See Figure 9.

Mode #3 4:2:2 (Special)

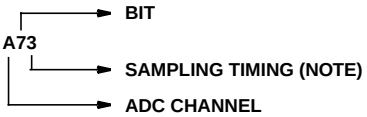


ADC CHANNEL	OUTPUT	DATA							
A	A7	A70	A71	A72	A73	A74	A75	A76	A77
	A6	A60	A61	A62	A63	A64	A65	A66	A67
	A5	A50	A51	A52	A53	A54	A55	A56	A57
	A4	A40	A41	A42	A43	A44	A45	A46	A47
	A3	A30	A31	A32	A33	A34	A35	A36	A37
	A2	A20	A21	A22	A23	A24	A25	A26	A27
	A1	A10	A11	A12	A13	A14	A15	A16	A17
	A0	A00	A01	A02	A03	A04	A05	A06	A07
B	B7	B70	C71	B72	C73	B74	C75	B76	C77
	B6	B60	C61	B62	C63	B64	C65	B66	C67
	B5	B50	C51	B52	C53	B54	C55	B56	C57
	B4	B40	C41	B42	C43	B44	C45	B46	C47
	B3	B30	C31	B32	C33	B34	C35	B36	C37
	B2	B20	C21	B22	C23	B24	C25	B26	C27
	B1	B10	C11	B12	C13	B14	C15	B16	C17
	B0	B00	C01	B02	C03	B04	C05	B06	C07
C	C7	HiZ	→						
	C6	HiZ	→						
	C5	HiZ	→						
	C4	HiZ	→						
	C3	HiZ	→						
	C2	HiZ	→						
	C1	HiZ	→						
	C0	HiZ	→						
TGR		HIGH	LOW	HIGH	LOW	HIGH	LOW	HIGH	LOW

HiZ: High Impedance

NOTE: See Figure 9.

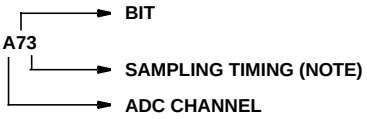
Mode #1 4:2:2 ($8F_S$)



ADC CHANNEL	OUTPUT	DATA							
A	A7	A70	A70	A72	A72	A74	A74	A76	A76
	A6	A60	A60	A62	A62	A64	A64	A66	A66
	A5	A50	A50	A52	A52	A54	A54	A56	A56
	A4	A40	A40	A42	A42	A44	A44	A46	A46
	A3	A30	A30	A32	A32	A34	A34	A36	A36
	A2	A20	A20	A22	A22	A24	A24	A26	A26
	A1	A10	A10	A12	A12	A14	A14	A16	A16
	A0	A00	A00	A02	A02	A04	A04	A06	A06
B	B7	B70	B70	C70	C70	B74	B74	C74	C74
	B6	B60	B60	C60	C60	B64	B64	C64	C64
	B5	B50	B50	C50	C50	B54	B54	C54	C54
	B4	B40	B40	C40	C40	B44	B44	C44	C44
	B3	B30	B30	C30	C30	B34	B34	C34	C34
	B2	B20	B20	C20	C20	B24	B24	C24	C24
	B1	B10	B10	C10	C10	B14	B14	C14	C14
	B0	B00	B00	C00	C00	B04	B04	C04	C04
C	C7	B70	A70	C70	A72	B74	A74	C74	A76
	C6	B60	A60	C60	A62	B64	A64	C64	A66
	C5	B50	A50	C50	A52	B54	A54	C54	A56
	C4	B40	A40	C40	A42	B44	A44	C44	A46
	C3	B30	A30	C30	A32	B34	A34	C34	A36
	C2	B20	A20	C20	A22	B24	A24	C24	A26
	C1	B10	A10	C10	A12	B14	A14	C14	A16
	C0	B00	A00	C00	A02	B04	A04	C04	A06
TGR		HIGH	LOW	→		HIGH	LOW	→	

NOTE: See Figure 9.

Mode #4 4:1:1

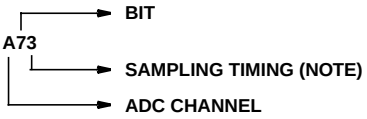


ADC CHANNEL	OUTPUT	DATA							
A	A7	A70	A71	A72	A73	A74	A75	A76	A77
	A6	A60	A61	A62	A63	A64	A65	A66	A67
	A5	A50	A51	A52	A53	A54	A55	A56	A57
	A4	A40	A41	A42	A43	A44	A45	A46	A47
	A3	A30	A31	A32	A33	A34	A35	A36	A37
	A2	A20	A21	A22	A23	A24	A25	A26	A27
	A1	A10	A11	A12	A13	A14	A15	A16	A17
	A0	A00	A01	A02	A03	A04	A05	A06	A07
B	B7	B70	B60	B30	B10	B74	B54	B34	B14
	B6	B60	B40	B20	B00	B64	B44	B24	B04
	B5	C10	C50	C30	C10	C74	C54	C34	C14
	B4	C60	C40	C20	C00	C64	C44	C24	C04
	B3	HiZ	→						
	B2	HiZ	→						
	B1	HiZ	→						
	B0	HiZ	→						
C	C7	HiZ	→						
	C6	HiZ	→						
	C5	HiZ	→						
	C4	HiZ	→						
	C3	HiZ	→						
	C2	HiZ	→						
	C1	HiZ	→						
	C0	HiZ	→						
TGR		HIGH	LOW	→		HIGH	LOW	→	

HiZ: High Impedance

NOTE: See Figure 9.

Mode #5 4:1:1 (Special)



ADC CHANNEL	OUTPUT	DATA							
A	A7	A70	A71	A72	A73	A74	A75	A76	A77
	A6	A60	A61	A62	A63	A64	A65	A66	A67
	A5	A50	A51	A52	A53	A54	A55	A56	A57
	A4	A40	A41	A42	A43	A44	A45	A46	A47
	A3	A30	A31	A32	A33	A34	A35	A36	A37
	A2	A20	A21	A22	A23	A24	A25	A26	A27
	A1	A10	A11	A12	A13	A14	A15	A16	A17
	A0	A00	A01	A02	A03	A04	A05	A06	A07
B	B7	B30	B70	C32	C72	B34	B74	C36	C76
	B6	B20	B60	C22	C62	B24	B64	C26	C66
	B5	B10	B50	C12	C52	B14	B54	C16	C56
	B4	B00	B40	C02	C42	B04	B44	C06	C46
	B3	HiZ	→						
	B2	HiZ	→						
	B1	HiZ	→						
	B0	HiZ	→						
C	C7	HiZ	→						
	C6	HiZ	→						
	C5	HiZ	→						
	C4	HiZ	→						
	C3	HiZ	→						
	C2	HiZ	→						
	C1	HiZ	→						
	C0	HiZ	→						
TGR		HIGH	LOW	→		HIGH	LOW	→	

HiZ: High Impedance

NOTE: See Figure 9.

Mode #6, #7 - Simple Boundary Scan 1 and Scan 2

The HI2303 has a simple boundary scan function.

TABLE 3. SIMPLE BOUNDARY SCAN

BITS			OUTPUT DATA	
			MODE #6	MODE #7
A7	B7	C7	H	L
A6	B6	C6	L	H
A5	B5	C5	H	L
A4	B4	C4	L	H
A3	B3	C3	H	L
A2	B2	C2	L	H
A1	B1	C1	H	L
A0	B0	C0	L	H

NOTE: CLK and SY must be set.

Clamp Function

The following two points should be noted when using the digital clamp circuit.

- The clamp pulse must be supplied externally.
- The clamp circuit is not designed for V cycle clamping.

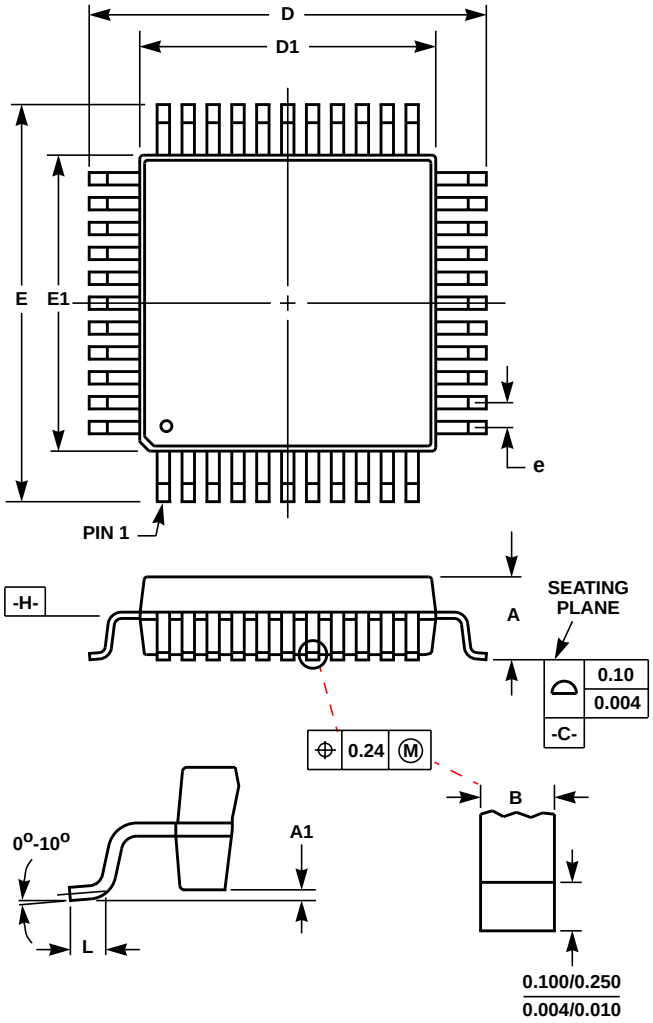
16 different reference levels can be selected for the digital clamp circuit through a combination of the REF0, REF1, REF2 and REF3 inputs as shown in the table below. Note that the REF0, REF1, REF2 and REF3 input signals are fetched asynchronously with the clock input signal.

$$A_{IN(pedestal)} = V_{RB} + (\text{Binary Code} * \text{LSB}) + E_{OB}$$

TABLE 4. SETTING VALUES AND REFERENCE LEVEL

SETTING				REFERENCE LEVEL				
					CHANNEL A		CHANNELS B AND C	
REF3	REF2	REF1	REF0	MODE	DECIMAL	BINARY	DECIMAL	BINARY
L	L	L	L	0	16	00010000	128	10000000
L	L	L	H	1	32	00100000	128	10000000
L	L	H	L	2	48	00110000	128	10000000
L	L	H	H	3	64	01000000	128	10000000
L	H	L	L	4	1	00000001	1	00000001
L	H	L	H	5	16	00010000	16	00010000
L	H	H	L	6	32	00100000	32	00100000
L	H	H	H	7	48	00110000	48	00110000
H	L	L	L	8	239	11101111	127	01111111
H	L	L	H	9	223	11011111	127	01111111
H	L	H	L	A	207	11001111	127	01111111
H	L	H	H	B	191	10111111	127	01111111
H	H	L	L	C	254	11111110	254	11111110
H	H	L	H	D	239	11101111	239	11101111
H	H	H	L	E	223	11011111	223	11011111
H	H	H	H	F	207	11001111	207	11001111

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q80.14x20-S

80 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.103	0.122	2.60	3.10	-
A1	0.002	0.011	0.05	0.30	-
B	0.010	0.019	0.25	0.50	5
D	0.926	0.956	23.50	24.30	2
D1	0.784	0.803	19.90	20.40	3, 4
E	0.689	0.720	17.50	18.30	2
E1	0.548	0.566	13.90	14.40	3, 4
L	0.024	0.039	0.60	1.00	-
N	80		80		6
e	0.032 BSC		0.80 BSC		-
ND	24		24		-
NE	16		16		-

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NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. “N” is the number of terminal positions.

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