

## SFP-10GB-DW-C-40-E-C

MSA and TAA Compliant 10GBase-DWDM 50GHz SFP+ Transceiver (SMF, Tunable, 80km, LC, DOM)

### Features:

- SFF-8432 and SFF-8472 Compliance
- Duplex LC Connector
- Single-mode Fiber
- Commercial Temperature 0 to 70 Celsius
- Hot Pluggable
- Metal with Lower EMI
- Excellent ESD Protection
- RoHS Compliant and Lead Free



### Applications:

- 10G Ethernet

### Product Description

This MSA Compliant SFP+ transceiver provides 10GBase-DWDM throughput up to 80km over single-mode fiber (SMF) using a tunable wavelength via an LC connector. It is built to MSA standards and is uniquely serialized and data-traffic and application tested to ensure that they will integrate into your network seamlessly. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

ProLabs's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."



## Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883E Method 3015.4
- ESD to the LC Receptacle: compatible with IEC 61000-4-3
- EMI/EMC compatible with FCC Part 15 Subpart B Rules, EN55022:2010
- Laser Eye Safety compatible with FDA 21CFR, EN60950-1& EN (IEC) 60825-1,2
- RoHS compliant with EU RoHS 2.0 directive 2015/863/EU

## Tunable SFP+ Channel Number and Wavelength

Channel No.	Frequency (THz)	Center Wavelength (nm)	Channel No	Frequency (THz)	Center Wavelength (nm)
1	191.35	1566.72	49	193.75	1547.32
2	191.40	1566.31	50	193.80	1546.92
3	191.45	1565.90	51	193.85	1546.52
4	191.50	1565.50	52	193.90	1546.12
5	191.55	1565.09	53	193.95	1545.72
6	191.60	1564.68	54	194.00	1545.32
7	191.65	1564.27	55	194.05	1544.92
8	191.70	1563.86	56	194.10	1544.53
9	191.75	1563.45	57	194.15	1544.13
10	191.80	1563.05	58	194.20	1543.73
11	191.85	1562.64	59	194.25	1543.33
12	191.90	1562.23	60	194.30	1542.94
13	191.95	1561.83	61	194.35	1542.54
14	192.00	1561.42	62	194.40	1542.14
15	192.05	1561.01	63	194.45	1541.75
16	192.10	1560.61	64	194.50	1541.35
17	192.15	1560.20	65	194.55	1540.95
18	192.20	1559.79	66	194.60	1540.56
19	192.25	1559.39	67	194.65	1540.16
20	192.30	1558.98	68	194.70	1539.77
21	192.35	1558.58	69	194.75	1539.37
22	192.40	1558.17	70	194.80	1538.98
23	192.45	1557.77	71	194.85	1538.58
24	192.50	1557.36	72	194.90	1538.19
25	192.55	1556.96	73	194.95	1537.79
26	192.60	1556.56	74	195.00	1537.40
27	192.65	1556.15	75	195.05	1537.00
28	192.70	1555.75	76	195.10	1536.61
29	192.75	1555.34	77	195.15	1536.22
30	192.80	1554.94	78	195.20	1535.82
31	192.85	1554.54	79	195.25	1535.43
32	192.90	1554.13	80	195.30	1535.04
33	192.95	1553.73	81	195.35	1534.64
34	193.00	1553.33	82	195.40	1534.25
35	193.05	1552.93	83	195.45	1533.86
36	193.10	1552.52	84	195.50	1533.47
37	193.15	1552.12	85	195.55	1533.07

38	193.20	1551.72	86	195.60	1532.68
39	193.25	1551.32	87	195.65	1532.29
40	193.30	1550.92	88	195.70	1531.90
41	193.35	1550.52	89	195.75	1531.51
42	193.40	1550.12	90	195.80	1531.12
43	193.45	1549.72	91	195.85	1530.72
44	193.50	1549.32	92	195.90	1530.33
45	193.55	1548.91	93	195.95	1529.94
46	193.60	1548.52	94	196.00	1529.55
47	193.65	1548.11	95	196.05	1529.16
48	193.70	1547.72	96	196.10	1528.77

### Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Maximum Supply Voltage	VccT	0	+3.6	V	+3.3V
Optical Receiver Input	PIMAX		+5	dBm	Average
Operating Case Temperature	Tc	0	70	°C	
Storage Temperature	TSTR	-40	85	°C	
ESD SFI pins	ESD1		1	kV	HBM
ESD except for SFI pins	ESD2		2	kV	HBM

### Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	Vcc	3.135	3.300	3.465	V	+3.3V
Supply Current	Icc3			0.54	A	Note 1
Power Consumption	PDS			1.7	W	Note 2
Low Speed Control Pin Logic Levels						
Host Vcc Range	Host_Vcc	3.14		3.47	V	with ± 5% variation
TX_Fault, RX_LOS	VOL	0.0		0.4	V	Note 3
	VOH	Vcc-0.5		Vcc+0.3	V	Note 3
TX_Disable	VIL	-0.3		0.8	V	Pulled up with 10k ohms to VccT in the module
	VIH	2.0		VccT +0.3	V	

#### Notes:

1. < 0.64 A Tc<25degC
2. <2.0 W Tc<25degC
3. Rpullup (Rp) is the pull up resistor. Active bus termination may be used by the host in place of a pullup resistor. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module. Measures at the Host side of the connector

## Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
<b>Transmitter</b>						
Data Rate		9.95		11.3	Gbps	NRZ
Frequency range		191.35		196.10	THz	50GHz grid, 96 channels
Frequency accuracy		-2.5		+2.5	GHz	EOL
Optical transmit power	Po	-1.0		+3.0	dBm	EOL
Shuttered output power				-35	dBm	
Optical power stability	$\Delta P_o$	-1.0		+1.0	dB	All channels, SOL
Side mode suppression	SMSR	35			dB	$\pm 2.5$ nm, modulated
Spectral width	$\Delta\lambda$		0.3	0.5	nm	-20dB, modulated
Extinction ratio	ER	9.0			dB	Filtered, 10.709Gb/s
Eye diagram compliance		GR-253, ITU-T G.691				
Mask margin		10			%	
Tuning speed				10	s	warmed-up, from any CH to any other CH
<b>Receiver</b>						
Data Rate		9.95		11.3	Gbps	NRZ
Input operating wavelength		1525		1575	nm	
Minimum Receiver Sensitivity (Back to Back)	P <sub>rmin</sub>			-24	dBm	10.709Gb/s, 1E-12, OSNR>35dB
Minimum receiver sensitivity (-300~+1400ps/nm)	P <sub>rmin</sub>	0		-21	dBm	
Maximum input power (overload)	P <sub>ro</sub>	-7			dBm	
Receiver Reflectance	RL			-27	dB	
LOS Assert				-27	dBm	Note 1
LOS De-Assert				-25	dBm	Note 1
LOS Hysteresis		0.5		4.0	dB	Note 1
LOS Assert Time				100	us	
LOS De-Assert Time				100	us	

### Notes:

1.



## SFP+ 2 Wire Interface Timing Requirements

Parameter	Symbol	Min	Max	Unit	Conditions
Clock Frequency	fSCL	100	400	kHz	
Clock Pulse Width Low	t <sub>LOW</sub>	1.3		μs	
Clock Pulse Width High	t <sub>HIGH</sub>	0.6		μs	
Time bus free before new transaction can start	t <sub>BUF</sub>	20		μs	Between STOP and START
START Hold time	t <sub>HD,STA</sub>	0.6		μs	
START Set-Up time	t <sub>SU,STA</sub>	0.6		μs	
Data in Hold time	t <sub>HD,DAT</sub>	0		μs	
Data in Set-Up time	t <sub>SU,DAT</sub>	0.1		μs	
Input Rise time (100 kHz)	t <sub>R,100</sub>		1000	ns	Note 1
Input Rise time (400 kHz)	t <sub>R,400</sub>		300	ns	Note 1
Input Fall time (100 kHz)	t <sub>F,100</sub>		300	ns	Note 1
Input Fall time (400 kHz)	t <sub>F,400</sub>		300	ns	Note 1
STOP Set-Up time	t <sub>SU,STO</sub>	0.6		μs	
Serial Interface Clock Holdoff "Clock Stretching"	T <sub>clock_hold</sub>		500	μs	Maximum time the SFP+ may hold the SCL line low before continuing R or W operation
Complete Single or Sequential Write	t <sub>WR</sub>		40	ms	Complete (up to) 8 Byte Write
Endurance (Write Cycles)		10 k		Cycles	@ Max Operating Temperature

### Notes:

1. From (VIL, MAX -0.15) to (VIH, MIN +0.15)



## SFP+ Timing Requirements

Parameter	Symbol	Min	Max	Unit	Conditions
<b>Tx_Disable assert time</b>	t_off		100	μs	Rising edge of TX_Disable to fall of output signal below 10% of nominal.
<b>TX_Disable negate time</b>	T_on		2	ms	Falling edge of TX Disable to rise output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
<b>Time to initialize 2-wire interface</b>	t_2w_start_up		300	ms	From power on or hot plug after the supply meeting
<b>Time to initialize cooled module and time to power up a cooled module to Power Level II</b>	t_start_up_cooled		90	sec	From power supplies meeting or hot plug, or Tx disable negated during power up or Tx_Fault recovery, until cooled power level II part during fault recovery is fully operational. Also, from stop bit-low-to-high SDA transition enabling Power Level II until cooled module is fully operational.
<b>Tx_Fault assert for cooled module</b>	Tx_fault_on_cooled		1	ms	From occurrence of fault to assertion of TX_Fault
<b>Tx_Fault Reset</b>	t_reset	10		μs	Time TX_disable must be held high to reset TX_Fault
<b>RX_LOS assert delay</b>	t_los_on		100	μs	From occurrence of loss of signal to assertion of RX_LOS
<b>Rx_LOS negate delay</b>	t_los_off		100	μs	From occurrence of presence of signal to negation of RX_LOS.
<b>Maximum Current Ramp on Power Supply</b>					
<b>Icc instantaneous peak current</b>			600	mA	Note 1,2
<b>Icc sustained peak current</b>			500	mA	Note 1,2

### Notes:

1. The maximum currents are the allowed currents for each power supply VccT or VccR, therefore the total module peak currents can be twice this value. The instantaneous peak current is allowed to exceed to specified maximum current capacity of the connector contact for a short period.
2. Not to exceed the sustained peak limit for the more than 50 μs; may exceed this limit for shorter durations.

## Pin Descriptions

Pin	Logic	Symbol	Power Sequence Order	Name/Descriptions	Ref.
1		VeeT	1	Module Transmitter Ground	1
2	LVTTTL-O	TX_Fault	3	Module Transmitter Fault	2
3	LVTTTL-I	TX_Disable	3	Transmitter Disable; Turn off laser output	3
4	LVTTTL-I/O	SDA	3	2-Wire Serial Interface Data Line	
5	LVTTTL-I/O	SCL	3	2-Wire Serial Interface Clock	
6		Mod_Abs	3	Module Absent, connected to VeeT or VeeR in the module	4
7	LVTTTL-I	RS0	3	NA. 30kohm pull down inside the module	
8	LVTTTL-O	RX_LOS	3	Receiver Loss of Signal Indicator	2
9	LVTTTL-I	RS1	3	NA. 30kohm pull down inside the module	
10		VeeR	1	Module Receiver Ground	1
11		VeeR	1	Module Receiver Ground	1
12	CML-O	RD-	3	Receiver Inverted Data Output(SFI)	
13	CML-O	RD+	3	Receiver Non-Inverted Data Output(SFI)	
14		VeeR	1	Module Receiver Ground	1
15		VccR	2	Module Receiver 3.3V Supply	5
16		VccT	2	Module Transmitter 3.3V Supply	5
17		VeeT	1	Module Transmitter Ground	1
18	CML-I	TD+	3	Transmitter Non-Inverted Data Output(SFI)	
19	CML-I	TD-	3	Transmitter Inverted Data Output(SFI)	
20		VeeT	1	Module Transmitter Ground	1

### Notes:

1. The module signal ground pins, VeeR and VeeT, are isolated from the module case.
2. This pin is an open drain output pin and shall be pulled up with a 4.7k-10kohms to Host\_Vcc on the host board. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module VccT/R + 0.5V.
3. This pin is an input pin with 10kohms pull up to VccT in the module.
4. This pin shall be pulled up with 4.7k-10kohms to Host\_Vcc on the host board.
5. VccT and VccR are tied together inside the module.



Pin-out of connector Block on Host board

### Recommended Circuit Schematic





### Mechanical Specifications

Small Form Factor Pluggable (SFP) transceivers are compatible with the dimensions defined by the SFP Multi-Sourcing Agreement (MSA).



### EEPROM Information

EEPROM memory map specific data field description is as below:



## **About ProLabs**

Our experience comes as standard; for over 15 years ProLabs has delivered optical connectivity solutions that give our customers freedom and choice through our ability to provide seamless interoperability. At the heart of our company is the ability to provide state-of-the-art optical transport and connectivity solutions that are compatible with over 90 optical switching and transport platforms.

## **Complete Portfolio of Network Solutions**

ProLabs is focused on innovations in optical transport and connectivity. The combination of our knowledge of optics and networking equipment enables ProLabs to be your single source for optical transport and connectivity solutions from 100Mb to 400G while providing innovative solutions that increase network efficiency. We provide the optical connectivity expertise that is compatible with and enhances your switching and transport equipment.

## **Trusted Partner**

Customer service is our number one value. ProLabs has invested in people, labs and manufacturing capacity to ensure that you get immediate answers to your questions and compatible product when needed. With Engineering and Manufacturing offices in the U.K. and U.S. augmented by field offices throughout the U.S., U.K. and Asia, ProLabs is able to be our customers best advocate 24 hours a day.

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