Evaluating the ADRF5141 Silicon, Transmit and Receive Switch with Limiter, 6 GHz to 12 GHz

FEATURES

- Full featured evaluation board for the ADRF5141
- Simple connection to the test equipment
- Thru line for calibration

EQUIPMENT NEEDED

- DC power supplies
- Network analyzer

GENERAL DESCRIPTION

The ADRF5141 is a transmit and receive switch with limiter manufactured in the silicon process.

This user guide describes the ADRF5141-EVALZ evaluation board, designed to simply evaluate the features and performance of the ADRF5141. The ADRF5141 is pin compatible with the ADRF5144. A photograph of the evaluation board is shown in Figure 1.

The ADRF5141 data sheet provides full specifications for the ADRF5141. Consult the ADRF5141 data sheet in conjunction with this user guide when using the ADRF5141-EVALZ.

EVALUATION BOARD PHOTOGRAPH

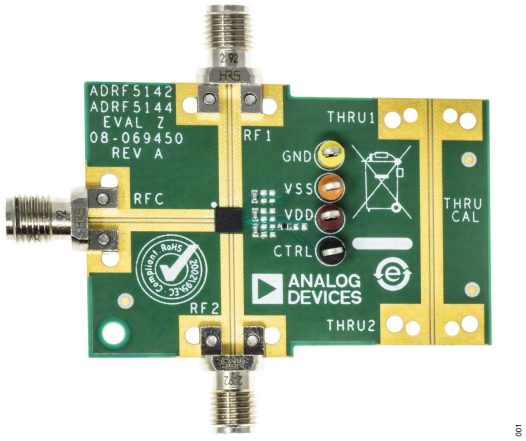

Figure 1. Evaluation Board Photograph

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REVISION HISTORY

10/2022—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

The ADRF5141-EVALZ is a connectorized board, assembled with the ADRF5141 and its application circuitry. All components are placed on the primary side of ADRF5141-EVALZ. An assembly drawing for the ADRF5141-EVALZ is shown in Figure 7, and an evaluation board schematic is shown in Figure 6.

BOARD LAYOUT

The ADRF5141-EVALZ is designed using RF circuit design techniques on an 8-layer printed circuit board (PCB). The PCB stack-up is shown in Figure 2.

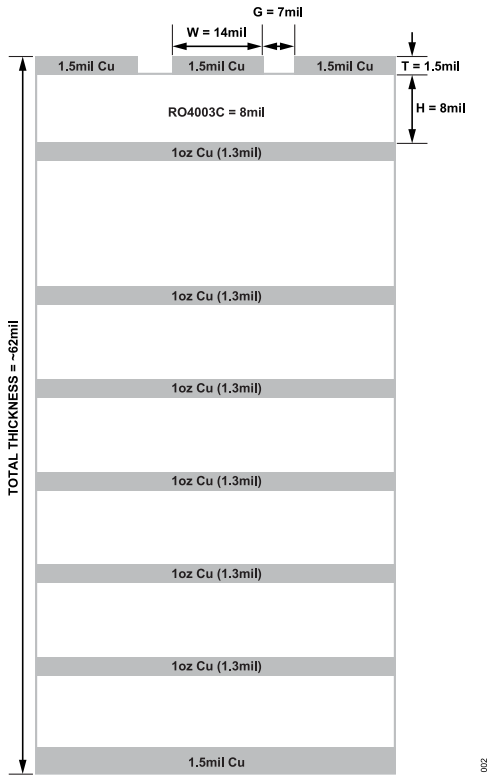

Figure 2. Evaluation Board Stack-Up

The outer copper layers are 1.5 mil thick and the inner layers are 1.3 mil thick.

The top dielectric material is 8 mil Rogers 4003C, which provides 50 Ω controlled impedance and optimizes the high-frequency performance. All RF traces are routed on the top layer, and the second layer is used as the ground plane for RF transmission lines. The remaining six layers are also ground planes filled with FR4 material to manage the thermal rise during high-power operations, and are supported with dense and filled vias to the PCB bottom for thermal relief. The overall board thickness is approximately 62 mil for mechanical strength.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 14 mil and ground spacing of 7 mil to have a characteristic impedance of 50 Ω. Ground via fences are arranged on both sides of a CPWG to improve isolation between nearby RF lines and other signal lines.

The exposed ground pad of the ADRF5141, which is soldered on the PCB ground pad, is the main thermal conduit for heat dissipation. The PCB ground pad is densely populated with filled, through vias to provide the lowest possible thermal resistance path from the top to the bottom of the PCB. The connections from the package ground leads to ground are kept as short as possible.

POWER-SUPPLY AND CONTROL INPUTS

The ADRF5141-EVALZ has two power-supply inputs, one control input, and a ground, as shown in Table 1. The DC test points are populated on VDD, VSS, CTRL, and GND. A 3.3 V supply is connected to the DC test points on VDD, and a −3.3 V supply is connected to the DC test points on VSS. Ground reference can be connected to GND. Connect the control input (CTRL) to 3.3 V or 0 V. The typical total current consumption for the ADRF5141 is 380 µA.

The VDD supply pin of the ADRF5141 is decoupled with 100 pF and 1000 pF capacitors, while the VSS supply pin and the CTRL control pin are decoupled with a 100 pF capacitor.

Table 1. Power-Supply and Control Inputs

Test Points	Description
VDD	Positive supply voltage
VSS	Negative supply voltage
CTRL	Control Input
GND	Ground

EVALUATION BOARD HARDWARE

RF INPUTS AND OUTPUTS

The ADRF5141-EVALZ has five edge-mounted, 2.92 mm connectors for the RF inputs and outputs, as shown in Table 2.

Table 2. RF Inputs and Outputs

2.92 mm Connectors	Description
RFC	Antenna port
RF1	Transmit port
RF2	Receive port
THRU1	Thru line input and output
THRU2	Thru line input and output

The through calibration line, connecting the THRU1 and THRU2 RF connectors, calibrates out the board loss effects from the measurements of the ADRF5141-EVALZ to determine the device performance at the pins of the IC. Figure 3 and Figure 4 show the typical board loss for the ADRF5141-EVALZ at room temperature, as well as the embedded and de-embedded insertion loss for the ADRF5141.

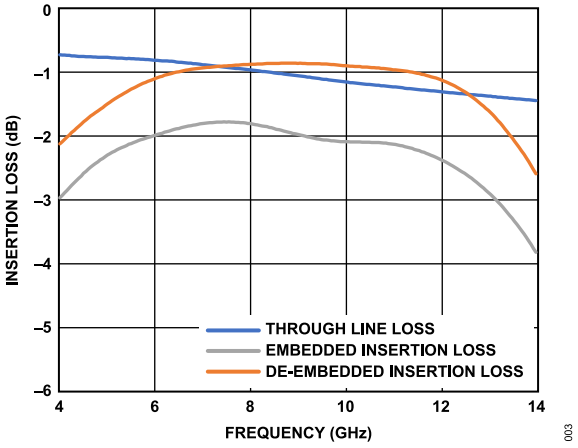

Figure 3. Insertion Loss vs. Frequency for TX

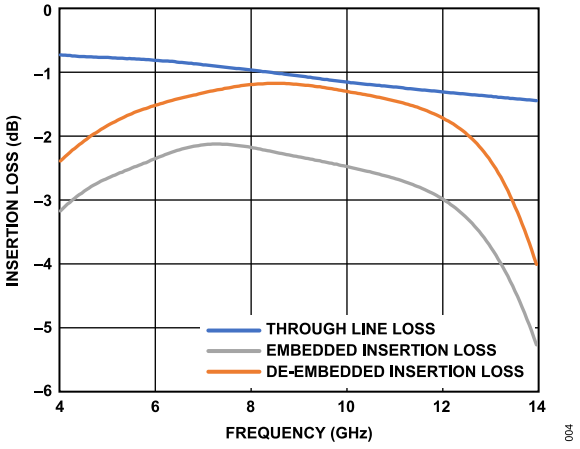

Figure 4. Insertion Loss vs. Frequency for RX

TEST PROCEDURE

BIASING SEQUENCE

To bias up the ADRF5141-EVALZ, perform the following steps:

1. Ground the GND test point.
2. Bias up the VDD test point.
3. Bias up the VSS test point.
4. Bias up the CTRL test point.
5. Apply an RF input signal.

The ADRF5141-EVALZ is shipped fully assembled and tested. Figure 5 provides a basic test setup diagram to evaluate the s-parameters using a network analyzer. Perform the following steps to complete the test setup and verify the operation of the ADRF5141-EVALZ:

1. Connect the GND test point to the ground terminal of the power supply.
2. Connect the VDD test point to the voltage-output terminal of the 3.3 V supply.
3. Connect the VSS test point to the voltage-output terminal of the −3.3 V supply.
4. Connect the CTRL test point to the voltage-output terminal of the 3.3 V supply. The ADRF5141 can be configured in different modes by connecting the CTRL test point to 3.3 V or 0 V, as shown in Table 3.
5. Connect a calibrated network analyzer to the RFC, RF1, and RF2 2.92 mm connectors. If the network analyzer port count is not enough, terminate the unused RF ports with 50 Ω. Sweep the frequency from 4 GHz to 14 GHz and set the power to –10 dBm.

Additional test equipment is needed to fully evaluate the device functions and performance.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is also recommended.

For power compression and power handling evaluations, use a 2-channel power meter and a signal generator. A high enough power amplifier is also recommended at the input. Test accessories, such as couplers and attenuators, must have enough power handling.

The ADRF5141-EVALZ comes with a support plate attached to the bottom side. To ensure maximum heat dissipation and to reduce thermal rise on the board during high-power evaluations, this support plate must be attached to a heatsink using thermal grease.

Note that the measurements performed at the 2.92 mm connectors of the ADRF5141-EVALZ include the losses of the 2.9 2mm connectors and the PCB. The thru line must be measured to calibrate out the effects on the ADRF5141-EVALZ. The thru line is the summation of an RF input line and an RF output line that are connected to the device and equal in length.

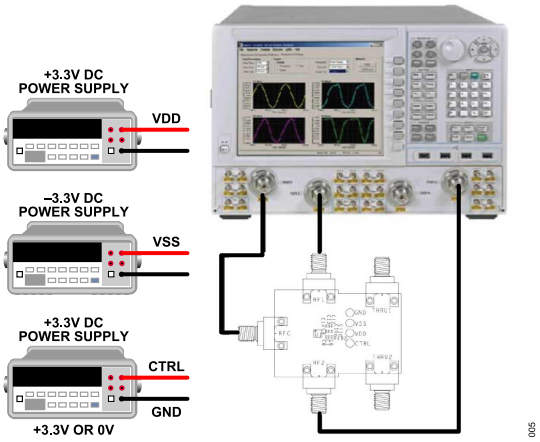

Figure 5. Test Setup Diagram

Table 3. Control Voltage Truth Table

Digital Control Input	RF Paths	
CTRL	**TX to ANT**	**ANT to RX**
Low	Insertion loss (on)	Isolation (off)
High	Isolation (off)	Insertion loss (on)

EVALUATION BOARD SCHEMATIC AND ASSEMBLY DIAGRAM

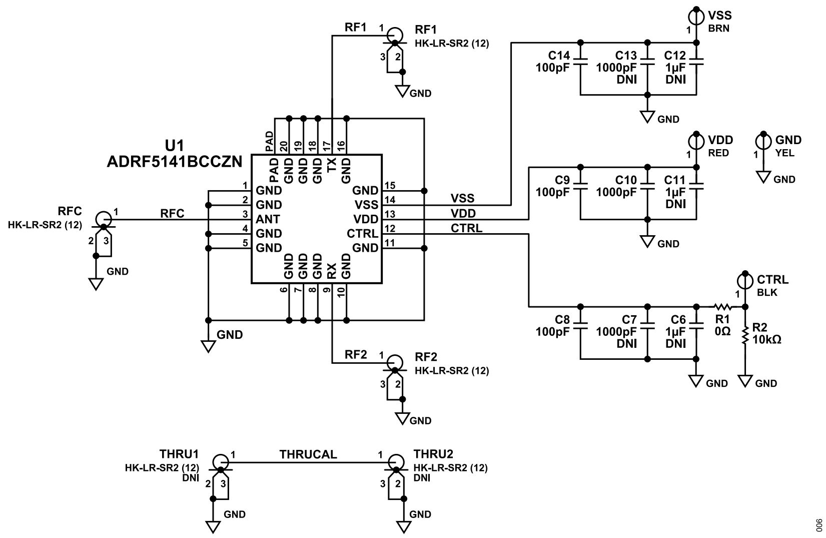

Figure 6. ADRF5141-EVALZ Evaluation Board Schematic

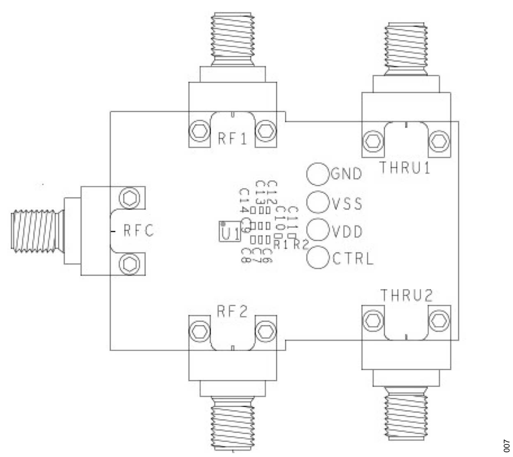

Figure 7. ADRF5141-EVALZ Evaluation Board Assembly Diagram

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. Bill of Materials for ADRF5141-EVALZ

Quantity	Reference Designator	Description	Manufacturer	Part Number
3	C8, C9, C14	Capacitors, 100 pF, 50 V, C0402 package	Murata	GCM1555C1H101JA16D
1	C10	Capacitor, 1000 pF, 25 V, C0402 package	TDK	CGJ2B2X7R1E102K050BA
2	C7, C13	Capacitor, 1000 pF, 25 V, C0402 package (do not insert, DNI)	TDK	CGJ2B2X7R1E102K050BA
3	C6, C11, C12	Capacitor, 1 µF, 16 V, C0402 package (DNI)	TDK	CGB2A1JB1C105M033BC
1	R1	Resistor, 0 Ω, 0.1 W, 0402 package	Panasonic	ERJ-2GE0R00X
1	R2	Resistor, 10 kΩ, 0.1 W, 0402 package	Panasonic	ERJ-2RKF1002X
5	RFC, RF1, RF2, THRU1, and THRU2	Edge-mount 2.92 mm connectors	Hirose Electric CO.	HK-LR-SR2(12)
4	GND, CTRL, VDD, and VSS	Surface-mount test points	Components Corporation	TP104-01
1	U1	Silicon, transmit and receive switch with limiter, 6 GHz to 12 GHz	Analog Devices	ADRF5141BCCZN
1	PCB	ADRF5141-EVALZ	Analog Devices	BR-069450

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.