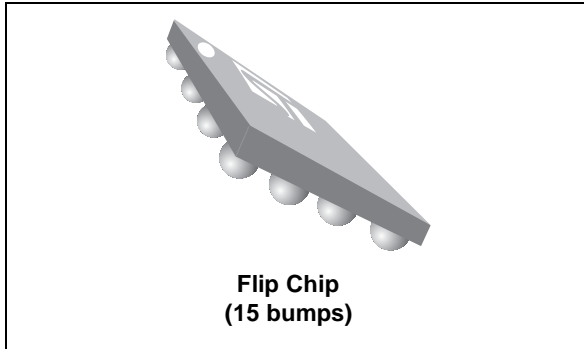


6-line low capacitance IPAD™ for micro-SD card with EMI filtering and ESD protection

Datasheet – production data



Features

- EMI low-pass filter
- ESD protection ± 8 kV (IEC 61000-4-2)
- Integrated pull up resistors to prevent bus floating when no card is connected
- 208 MHz clock frequency compatible with SDR104 mode (SD3.0)
- Lead-free package

Benefits

- Low power consumption
- Easy layout thanks to smart pin-out configuration
- Very low PCB space consumption
- High reliability offered by monolithic integration
- Reduction of parasitic elements thanks to CSP integration

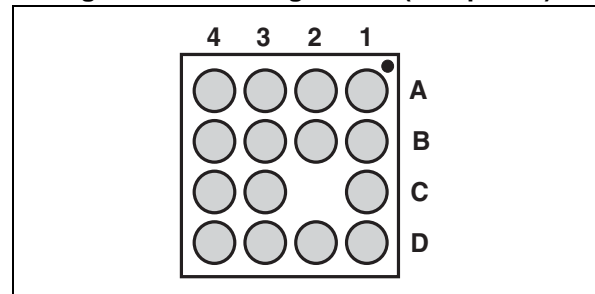
Complies with the following standards:

- IEC 61000-4-2 level 4:
 - ± 15 kV (air discharge)
 - ± 8 kV (contact discharge)

Description

The EMIF06-USD04F3 is a highly integrated device based on IPAD technology offering two functions: ESD protection to comply with IEC standard, and EMI filtering to reject mobile phone frequencies.

Figure 1. Pin configuration (bump side)



TM: IPAD is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Value	Unit		
V_{PP}	ESD discharge IEC 61000-4-2, level 4 (on pins Vcc, SDclk, SDcmd, SDdat0, SDdat1, SDdat2, SDdat3 Air discharge, external pins Contact discharge, external pins	15 8	kV		
	ESD discharge IEC 61000-4-2, level 1 (on pins dat0, dat1, clk, cmd, dat3, dat2) Air discharge, internal pins Contact discharge, internal pins	2 2			
	T_j	Maximum junction temperature		125	$^{\circ}\text{C}$
	T_{op}	Operating temperature range		- 30 to + 85	$^{\circ}\text{C}$
	T_{stg}	Storage temperature range		- 55 to + 150	$^{\circ}\text{C}$

Figure 2. EMIF06-USD04F3 Schematic

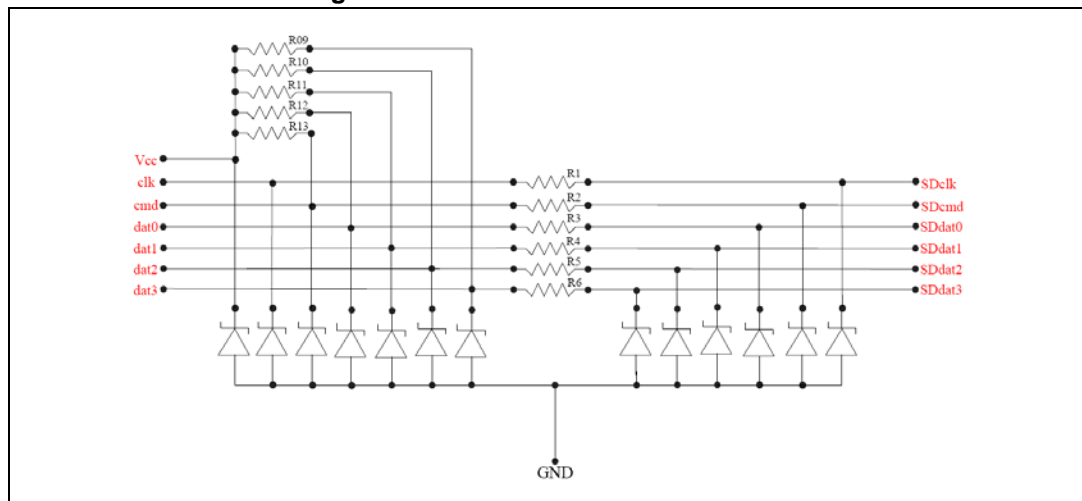


Table 2. Pin configuration

Pin	Signal	Pin	Signal
A1	dat0	C1	Cmd
A2	dat1		
A3	SDdat1	C3	GND
A4	SDdat0	C4	SDcmd
B1	clk	D1	dat3
B2	V_{cc}	D2	dat2
B3	GND	D3	SDdat2
B4	SDclk	D4	SDdat3

Table 3. Electrical characteristics (values, $T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	Breakdown voltage	$I_R = 1\text{ mA}$	14		20	V
I_{RM}	Leakage current at V_{RM}	$V_{RM} = 3\text{ V}$			100	nA
R1, R2, R3, R4, R5, R6	Serial resistance	Tolerance $\pm 10\%$, matching $\pm 2\%$		40		Ω
R9, R10, R11, R12	Pull-up resistance	Tolerance $\pm 10\%$, matching $\pm 2\%$		50		k Ω
R13	Pull-up resistance on cmd	Tolerance $\pm 10\%$		15		k Ω
C_{line}	Data line capacitance	$V = 0\text{ V}$, $F = 10\text{ MHz}$, $V_{OSC} = 30\text{ mV}$		10	12	pF
		$V = 1.8\text{ V}$, $F = 10\text{ MHz}$, $V_{OSC} = 30\text{ mV}$		7.5	10	
		$V = 2.9\text{ V}$, $F = 10\text{ MHz}$, $V_{OSC} = 30\text{ mV}$			9	

Figure 3. Electrical characteristics (definitions)

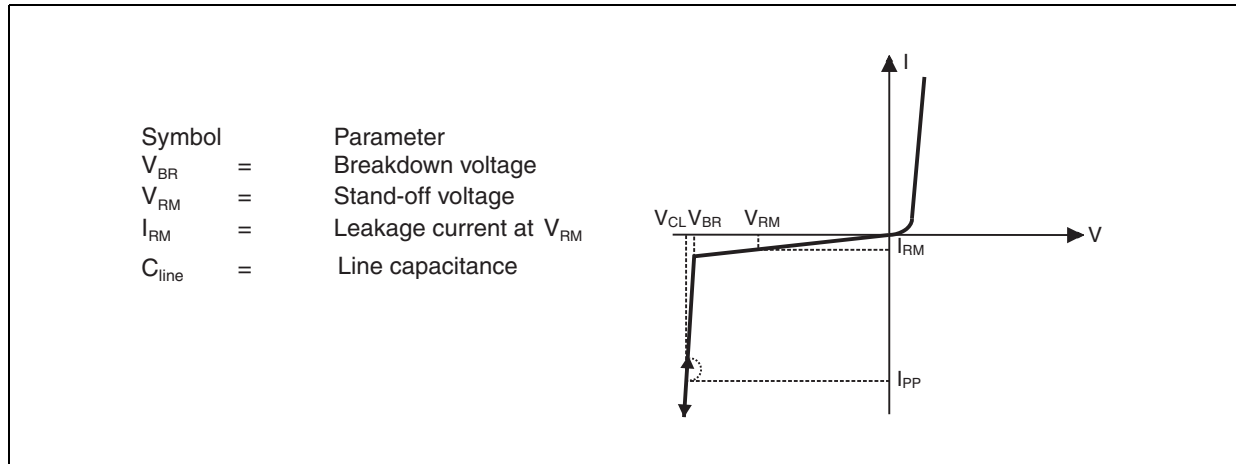


Figure 4. Attenuation versus frequency

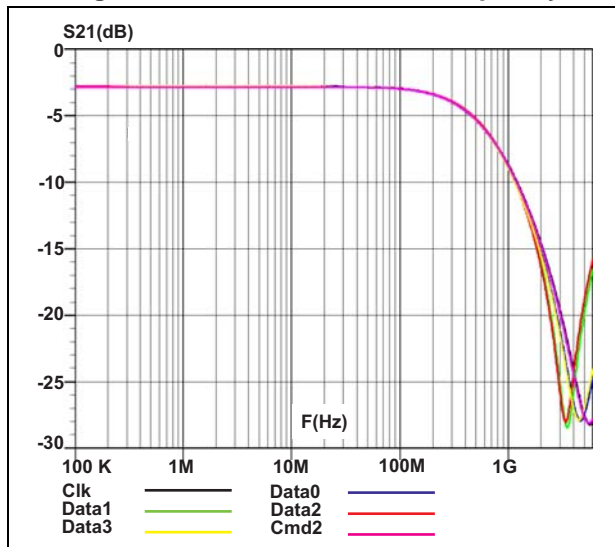


Figure 5. Analog crosstalk versus frequency

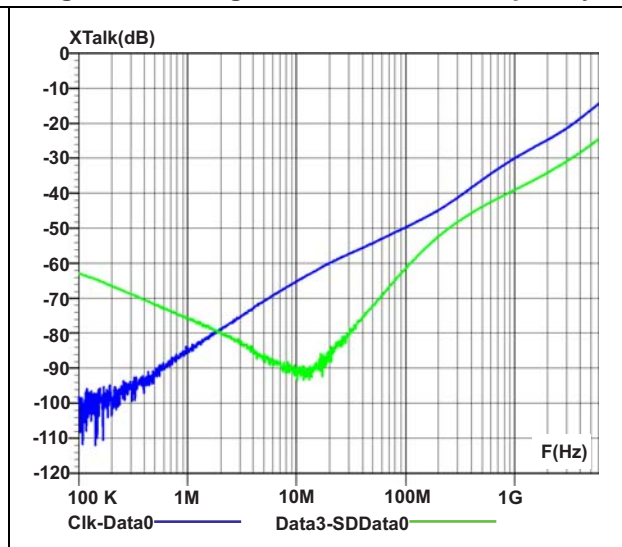


Figure 6. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

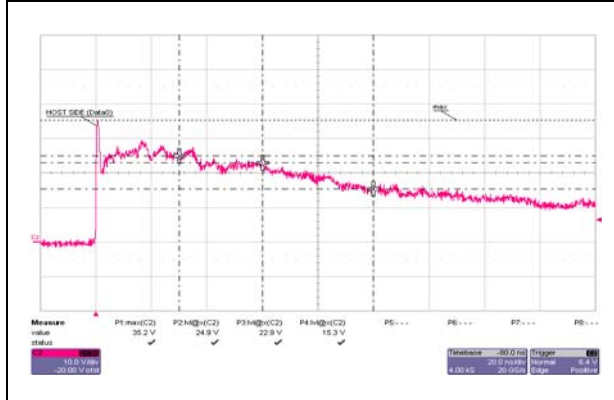


Figure 7. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

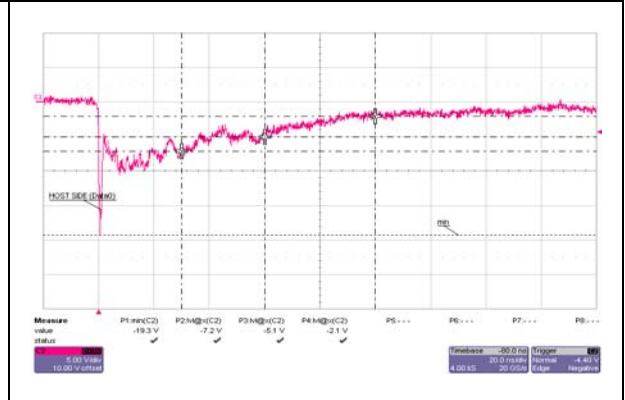
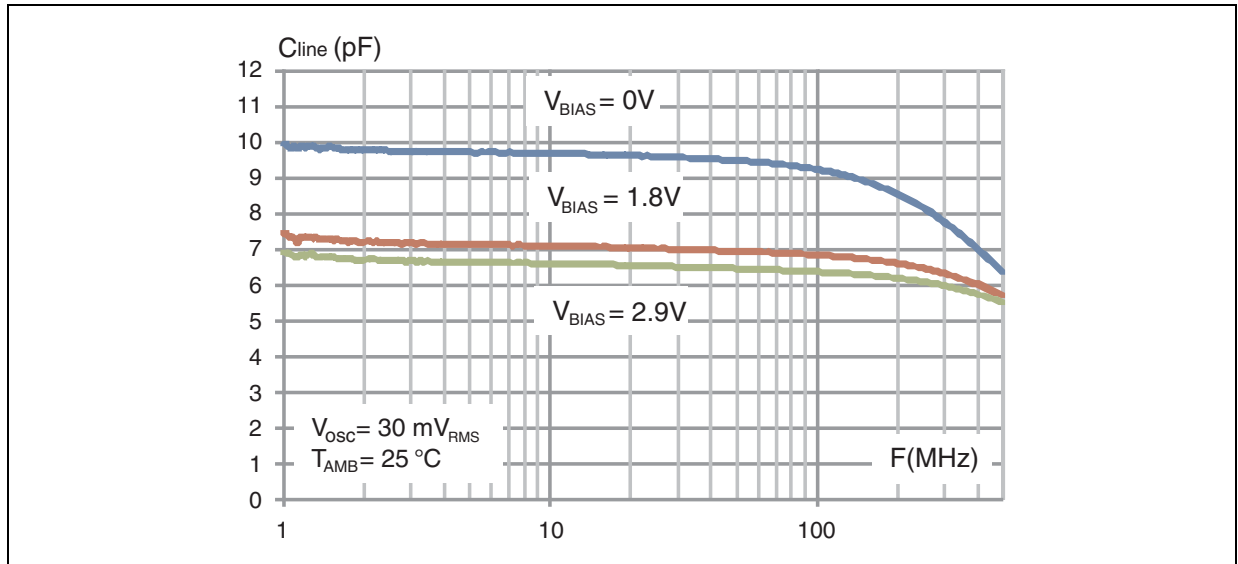


Figure 8. Line capacitance versus frequency and bias voltage (typical values)



2 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 9. Package dimensions

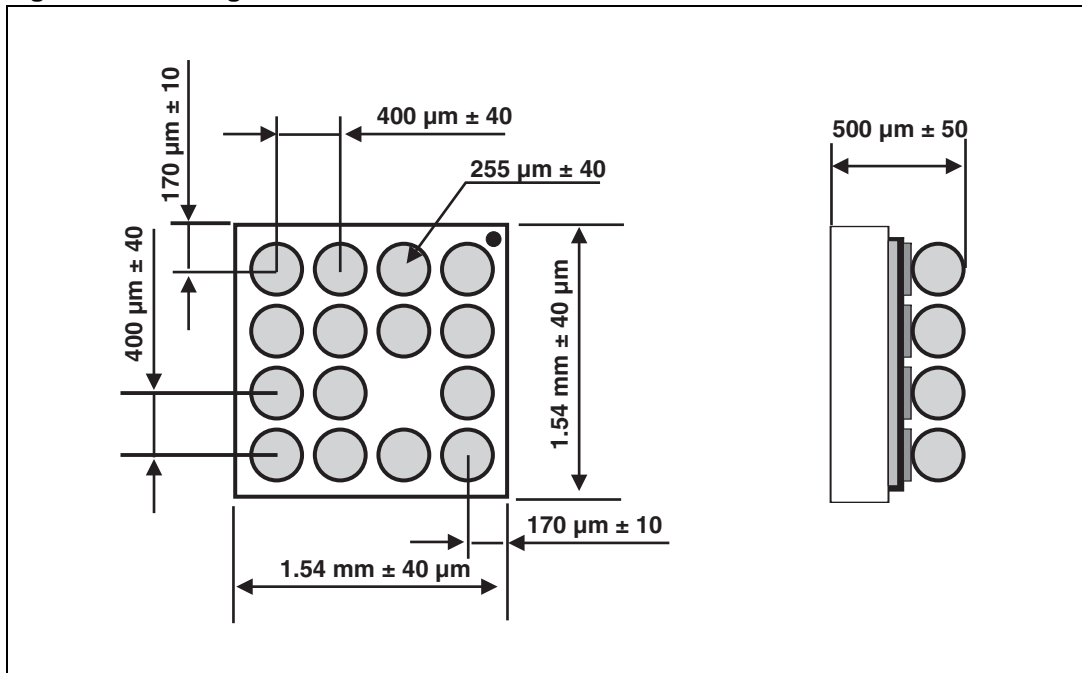


Figure 10. Footprint

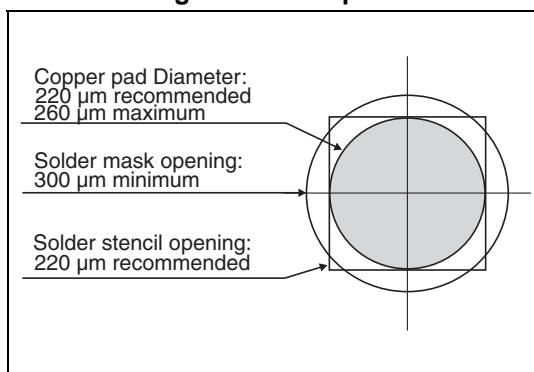


Figure 11. Marking

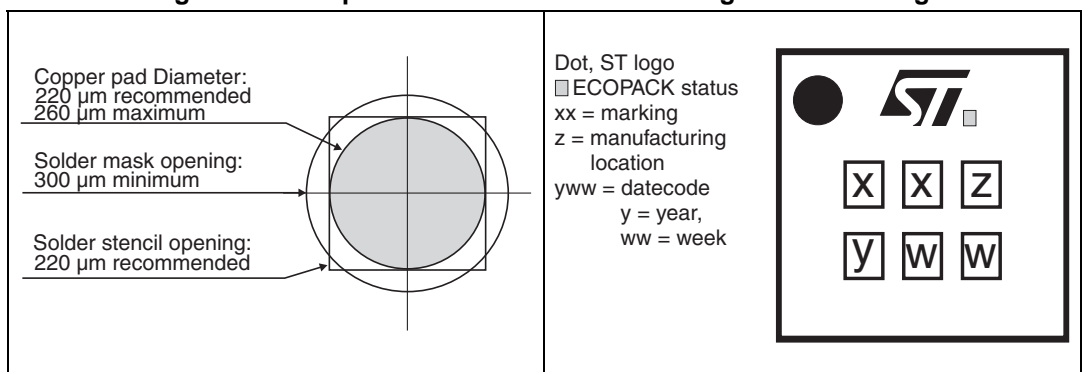
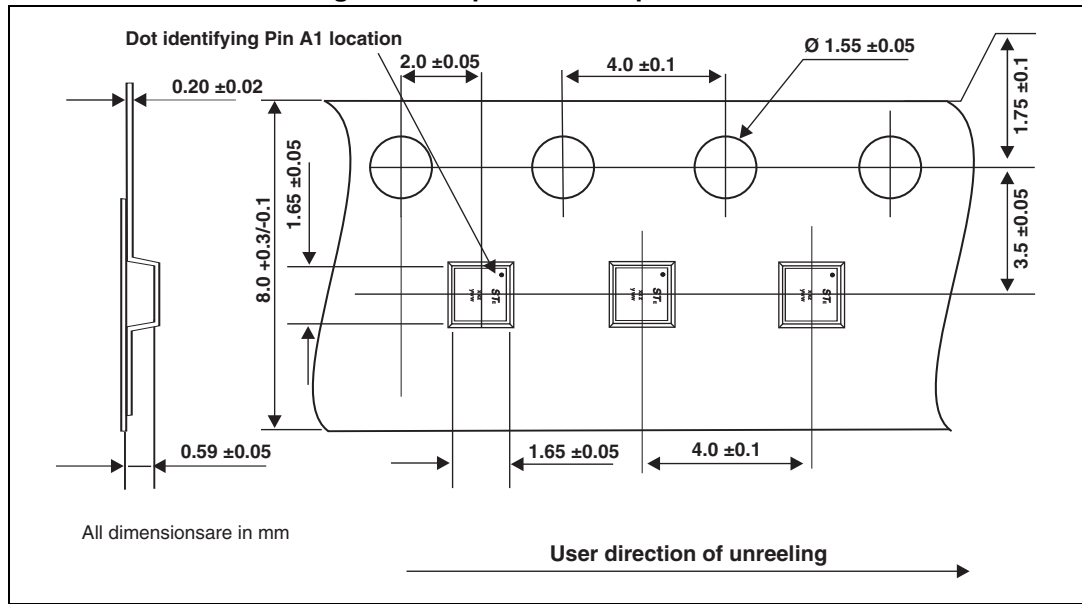


Figure 12. Tape and reel specification



3 Ordering information

Figure 13. Ordering information scheme

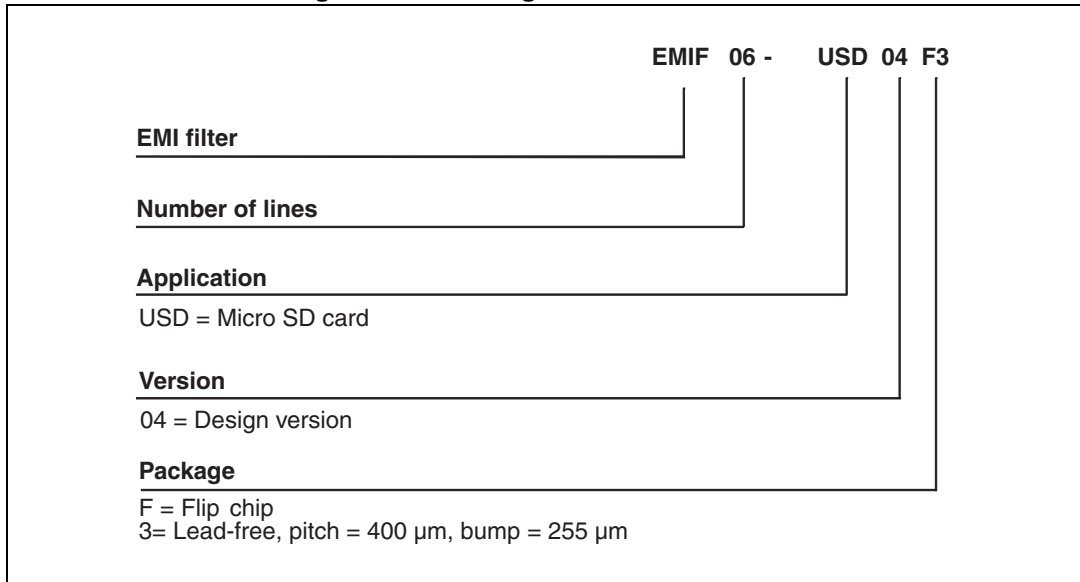


Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF06-USD04F3	JZ	Flip Chip	2.6 mg	5000	Tape and reel 7"

Note: More information is available in the STmicroelectronics Application notes:
 AN2348: "Flip Chip: Package description and recommendations for use"
 AN1751: "EMI Filters: Recommendations and measurements"

4 Revision history

Table 5. Document revision history

Date	Revision	Changes
09-May-2012	1	First issue.
27-Jun-2012	2	Added tolerances in Figure 12 .
30-Jun-2014	3	Updated Figure 4 , Figure 5 and breakdown voltage value in Table 3 .

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